

INTEGRATED CIRCUITS

D A T A B O O K

MARCH 1985

**INTEGRATED
CIRCUITS
DATA BOOK**

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SILICONIX

INTEGRATED CIRCUITS

INTRODUCTION

Siliconix, founded in 1962, is a worldwide corporation with headquarters in Santa Clara, California and wholly owned manufacturing facilities located in Swansea, Wales (UK), Taiwan, Hong Kong and a partnership sales operation in Japan.

Markets served by Siliconix range from the most demanding military QPL 38510 applications to traditional industrial, computer, instrumentation and selected consumer applications.

The products detailed in this data book represent a broad selection of state-of-the-art IC's manufactured by Siliconix for applications ranging from the simplest analog switch to very complex functions including complete analog data acquisition systems, computer interface semicustom circuits (gate arrays) and telephone dialers with on-chip RAM.

Siliconix is a world leader in CMOS and D/CMOS IC processing technology and is constantly striving to maintain that leadership with ongoing process and product developments that will provide even more advanced new circuit designs in the future.

Our emphasis in providing top quality parts to you, our customer, is enhanced by our strong market position in the hi-rel 38510 QPL products offered to military customers.

We solicit your comments, suggestions and ideas for new analog or digital IC products you'd like us at Siliconix to consider manufacturing.

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About This Edition of the Siliconix Integrated Circuit Data Book

This Catalog includes Application Notes that previously appeared in the Analog Switch Applications Handbook.

NEW PRODUCT DATA SHEETS APPEARING FOR THE FIRST TIME

D469	SD5400/SD5401/SD5402
DF820	Si520
DG221	Si7250
DG308A	Si7660
DG526/DG527	Si7661
PWM25/PWM27	Si8021/Si8020
SD5000/SD5001/SD5002	Si8601

PRELIMINARY PRODUCT INFORMATION INCLUDED IN THIS CATALOG

DG271	Si7135
DG5140-DG5145	Si8602
DG5240-DG5245	Si8901
DG568/DG569	Si9100
PWM125	Si9551/Si9552
Si25HC04	Si9553/Si9554

DATA SHEETS NO LONGER INCLUDED IN THIS CATALOG

D123 ²	DG508-DG509 ³
DF328 ¹	G115 ²
DG151/DG153 ²	G116 ²
DG152/DG154 ²	G117 ²
DG161/DG163 ²	G122 ²
DG162/DG164 ²	G123 ²
DG200 ³	Si1525 ³
DG201 ³	Si1527 ³
DG281-DG290 ¹	Si2525 ³
DG300-DG307 ³	Si2527 ³
DG308 ³	Si3525 ³
DG381-DG390 ³	Si3527 ³
DG506/DG507 ³	

NEW/DISCONTINUED PRODUCT CROSS REFERENCE

Old Product	Replacement
DG200	DG200A
DG201	DG201A
DG300-DG307	DG300A-DG307A
DG308	DG308A
DG381-DG390	DG381A-DG390A
DG506/DG507	DG506A/DG507A
DG508/DG509	DG508A/DG509A
Si1525	PWM25 (A Suffix)
Si1527	PWM27 (A Suffix)
Si2525	PWM25 (B Suffix)
Si2527	PWM27 (B Suffix)
Si3525	PWM25 (C Suffix)
Si3527	PWM27 (C Suffix)

NOTES:

1. Obsolete product.
2. Contact Factory on availability.
3. Replaced by improved version. See New/Discontinued Product CROSS REFERENCE.

INTEGRATED CIRCUIT CROSS REFERENCE GUIDE

EQUIVALENT PART:

Suggestions are based on the similarity of mechanical and electrical characteristics, as reported in the manufacturer's published data. Interchangeability is not guaranteed. Before selecting a device as a substitute, compare the specifications.

SIMILAR FUNCTION:

Suggestions are based on the similarity of electrical characteristics, as reported in the manufacturer's published data. Interchangeability is not guaranteed, as these parts usually have different pin configurations. Before selecting a device as a substitute, compare the specifications.

Company	Part Number	Siliconix Equivalent Part	Siliconix Similar Function	Function
AMD	AM2504	Si25HC04		12-bit SAR
Analog Devices	AD7501		DG508A	8 × CMOS Analog MUX
	AD7502		DG509A	4 × CMOS Diff Analog MUX
	AD7503		DG508A	8 × CMOS Analog MUX
	AD7506	DG506A		16 × CMOS Analog MUX
	AD7507	DG507A		8 × CMOS Diff Analog MUX
	AD7510DI		DG201A	4 × SPST CMOS Analog Switch
	AD7511DI		DG201A	4 × SPST CMOS Analog Switch
	AD7512DI		DG303	2 × SPDT CMOS Analog Switch
	AD7590		DG221	4 × SPST CMOS Analog Switch w/Latches
	AD7591		DG221	4 × SPST CMOS Analog Switch w/Latches
	AD7592		DG221	2 × SPDT CMOS Analog Switch w/Latches
	ADG200	DG200A		2 × SPST CMOS Analog Switch
	ADG201	DG201A		4 × SPST Virtual Gnd Analog Switch
Cherry	CS-1525	PWM25(A Suffix)		Pulse Width Modulator
	CS-1527	PWM27(A Suffix)		Pulse Width Modulator
	CS-2525	PWM25(B Suffix)		Pulse Width Modulator
	CS-2527	PWM27(B Suffix)		Pulse Width Modulator
	CS-3525	PWM25(C Suffix)		Pulse Width Modulator
	CS-3527	PWM27(C Suffix)		Pulse Width Modulator
EXAR	XR1525A	PWM25(A Suffix)		Pulse Width Modulator
	XR1527A	PWM27(A Suffix)		Pulse Width Modulator
	XR2525A	PWM25(B Suffix)		Pulse Width Modulator
	XR2527A	PWM27(B Suffix)		Pulse Width Modulator
	XR3525A	PWM25(C Suffix)		Pulse Width Modulator
	XR3527A	PWM27(C Suffix)		Pulse Width Modulator
General Instruments	AY5-9151		DF320	CMOS Loop Disconnect Dialer
Harris	HI-1800		DG184, DG302A, DG308A	2 × DPST CMOS Analog Switch
	HI-1800A		DG185, DG302A, DG306A	2 × DPST CMOS Analog Switch
	HI-1818		DG508A	8 × CMOS Analog MUX

IC CROSS REFERENCE GUIDE

Company	Part Number	Siliconix Equivalent Part	Siliconix Similar Function	Function
Harris (Cont.)	HI-1818A		DG508A	8 × CMOS Analog MUX
	HI-1828		DG509A	4 × CMOS Diff Analog MUX
	HI-1828A		DG509A	4 × CMOS Diff Analog MUX
	HI-200	DG200A		2 × SPST CMOS Analog Switch
	HI-201	DG201A		4 × SPST CMOS Analog Switch
	HI-201HS	DG271		4 × SPST High Speed
	HI-300	DG300A		2 × SPST CMOS Analog Switch
	HI-301	DG301A		1 × SPDT CMOS Analog Switch
	HI-302	DG302A		2 × DPST CMOS Analog Switch
	HI-303	DG303A		2 × SPDT CMOS Analog Switch
	HI-304	DG304A		2 × SPST CMOS Analog Switch
	HI-305	DG305A		1 × SPDT CMOS Analog Switch
	HI-306	DG306A		2 × DPST CMOS Analog Switch
	HI-307	DG307A		2 × SPDT CMOS Analog Switch
	HI-381	DG381A		2 × SPST CMOS Analog Switch
	HI-384	DG384A		2 × DPST CMOS Analog Switch
	HI-387	DG387A		1 × SPDT CMOS Analog Switch
	HI-390	DG390A		2 × SPDT CMOS Analog Switch
	HI-5040	DG5040		SPST CMOS Analog Switch
	HI-5041	DG5041		2 × SPST CMOS Analog Switch
	HI-5042	DG5042		SPDT CMOS Analog Switch
	HI-5043	DG5043		2 × SPDT CMOS Analog Switch
	HI-5044	DG5044		DPST CMOS Analog Switch
	HI-5045	DG5045		2 × DPST CMOS Analog Switch
	HI-5046		DG191, DG303A, DG307A	DPDT CMOS Analog Switch
	HI-5046A		DG190, DG303A, DG307A	DPDT CMOS Analog Switch
	HI-5047		DG185, DG302A, DG306A	4PST CMOS Analog Switch
	HI-5047A		DG184, DG302A, DG306A	4PST CMOS Analog Switch
	HI-5048		DG181, DG300A, DG304A	2 × SPST CMOS Analog Switch
	HI-5049	DG184		2 × DPST CMOS Analog Switch
	HI-5050		DG187, DG287, DG301A, DG305A	SPDT CMOS Analog Switch
	HI-5051	DG190		2 × SPDT CMOS Analog Switch
	HI-506	DG506A		16 × CMOS Analog MUX
	HI-506A	DG506A		16 × CMOS Analog MUX
	HI-506L	DG526		16 × CMOS Analog MUX w/Latches
	HI-507	DG507A		8 × CMOS Diff Analog MUX
	HI-507A	DG507A		8 × CMOS Diff Analog MUX
	HI-507L	DG527		8 × CMOS Diff Analog MUX w/Latches
	HI-508	DG508A		8 × CMOS Analog MUX
	HI-508A	DG508A		8 × CMOS Analog MUX
	HI-508L	DG528		8 × CMOS Analog MUX
	HI-509	DG509A		4 × CMOS Diff Analog MUX w/Latches
	HI-509A	DG509A		4 × CMOS Diff Analog MUX w/Latches
	HI-509L	DG529		4 × CMOS Diff Analog MUX w/Latches
	HS-1000		DG506A	16 × JFET Analog MUX
Intersil	D123	D123		6 × FET Driver
	D125	D125		6 × FET Driver

IC CROSS REFERENCE GUIDE

Company	Part Number	Siliconix Equivalent Part	Siliconix Similar Function	Function
Intersil (Cont.)	D129	D129		4 × CMOS Diff Driver w/Decode
	DG118		DG172	4 × SPST MOSFET Analog Switch
	DG123	DG123		5 × SPST MOSFET Analog Switch
	DG125	DG125		5 × SPST MOSFET Analog Switch
	DG126	DG126		2 × DPST JFET Analog Switch
	DG129	DG129		2 × DPST JFET Analog Switch
	DG139	DG139		DPDT Diff JFET Analog Switch
	DG140	DG140		2 × DPST JFET Analog Switch
	DG141	DG141		2 × SPST JFET Analog Switch
	DG142	DG142		DPDT Diff JFET Analog Switch
	DG143	DG143		SPDT Diff JFET Analog Switch
	DG144	DG144		SPDT Diff JFET Analog Switch
	DG145	DG145		DPDT Diff JFET Analog Switch
	DG146	DG146		SPDT Diff JFET Analog Switch
	DG180	DG180		2 × SPST JFET Analog Switch
	DG181	DG181, DG381A		2 × SPST JFET Analog Switch
	DG182	DG182		2 × SPST JFET Analog Switch
	DG183	DG183		2 × SPST JFET Analog Switch
	DG184	DG184, DG384A		2 × DPST JFET Analog Switch
	DG185	DG185		2 × DPST JFET Analog Switch
	DG186	DG186		2 × DPST JFET Analog Switch
	DG187	DG187, DG387A		SPDT JFET Analog Switch
	DG188	DG188		SPDT JFET Analog Switch
	DG189	DG189		2 × SPDT JFET Analog Switch
	DG190	DG190, DG390A		2 × SPDT JFET Analog Switch
	DG191	DG191		2 × SPDT JFET Analog Switch
	DG200	DG200A		2 × SPDT JFET Analog Switch
	DG201	DG201A		2 × SPDT JFET Analog Switch
	DS0026		D469	Dual MOSFET Driver
	G118	G118		6 × MOS FET Switch
	G119	G119		3 × Diff MOSFET Switch
	ICL2504	SI25HC04		12-bit SAR
	ICL7135	SI7135		4 1/2 Digit BCD A/D Converter
	ICL7660	SI7660	SI7661	Voltage Inverter/Converter
	ICL7662	SI7661		Voltage Inverter/Converter
	ICL8023		L144	Triple Low Power Op Amp
	IH200	DG200A		2 × SPST CMOS Analog Switch
	IH201	DG201A		4 × SPST CMOS Analog Switch
	IH202	DG202		4 × SPST CMOS Analog Switch
	IH5040	DG5040		SPST CMOS Analog Switch
	IH5041	DG5041		2 × SPST CMOS Analog Switch
	IH5042	DG5042		SPDT CMOS Analog Switch
	IH5043	DG5043		2 × SPDT CMOS Analog Switch
	IH5044	DG5044		DPST CMOS Analog Switch
	IH5045	DG5045		2 × DPST CMOS Analog Switch
	IH5046		DG191, DG303A, DG307A	DPDT CMOS Analog Switch
	IH5047		DG185, DG302A, DG306A	4PST CMOS Analog Switch
	IH5048		DG181, DG300A, DG304A, DG5041	2 × SPST CMOS Analog Switch
	IH5048		DG181, DG300, DG304A	2 × SPST CMOS Analog Switch
	IH5049		DG5045, DG306	2 × SPST CMOS Analog Switch

IC CROSS REFERENCE GUIDE

Company	Part Number	Siliconix Equivalent Part	Siliconix Similar Function	Function
Intersil (Cont.)	IH5050	DG187		SPDT CMOS Analog Switch
	IH5051	DG5043		2 × SPDT CMOS Analog Switch
	IH5052	DG211		Quad SPST CMOS Analog Switch
	IH5053	DG212		Quad SPST CMOS Analog Switch
	IH5140	DG5140		SPST CMOS Analog Switch
	IH5141	DG5141		2 × SPST CMOS Analog Switch
	IH5142	DG5142		SPDT CMOS Analog Switch
	IH5143	DG5143		2 × SPDT CMOS Analog Switch
	IH5144	DG5144		DPST CMOS Analog Switch
	IH5145	DG5145		2 × DPST CMOS Analog Switch
	IH6108	DG508A		8 × CMOS Analog MUX
	IH6116	DG506A		16 × CMOS Analog MUX
	IH6208	DG509A		4 × Diff Analog MUX
	IH6216	DG507A		8 × Diff Analog MUX
Linear Technology	LTC1044	Si7660	Si7661	Voltage Inverter/Converter
Micro Power	MP200DI	DG200A		2 × SPST CMOS Analog Switch
	MP201DI	DG201A		4 × SPST CMOS Analog Switch
	MP7501		DG501, DG508A	8 × CMOS Analog MUX
	MP7503		DG501, DG508A	8 × CMOS Analog MUX
	MP7506	DG506A		16 × CMOS Analog MUX
	MP7507	DG507A		Dual 8 × CMOS Analog MUX
	MP7508DI	DG508A		8 × CMOS Analog MUX
	MP7509DI	DG509A		Dual 4 × CMOS Analog MUX
	MP7622	Si8021/Si8020		12-bit CMOS Multiplying DAC
Mitel	MT4320	DF320		CMOS Loop Disconnect Dialer
	MT4322	DF322		CMOS Loop Disconnect Dialer
Motorola	MC1150L		DG501	8 × CMOS Analog MUX
	MC14016		DG201A	4 × SPST CMOS Analog Switch
	MC14051		DG508A	8 × CMOS Analog MUX
	MC14052		DG509A	4 × Diff CMOS Analog MUX
	MC14086		DG201A	4 × SPST CMOS Analog Switch
	MC14529		DG508A, DG509A	8 × CMOS Analog MUX
	MM4504		G118	6 × CMOS Analog Switch
	MM5393		DF320	CMOS Loop Disconnect Dialer
	MM5504		G118	6 × CMOS Analog Switch
National	AH0014		DG303A, DG307A	DPDT MOS Analog Switch
	AH0015		DG172, DG201A	4 × SPST CMOS Analog Switch
	AH0019		DG184, DG302A, DG306A	2 × DPST CMOS Analog Switch
	AH0126	DG126		2 × DPST JFET Analog Switch
	AH0129	DG129		2 × DPST JFET Analog Switch
	AH0133	DG133		2 × SPST JFET Analog Switch
	AH0134	DG134		2 × SPST JFET Analog Switch
	AH0139	DG139		DPDT Diff JFET Analog Switch
	AH0140	DG140		2 × DPST JFET Analog Switch
	AH0141	DG141		2 × SPST JFET Analog Switch
	AH0142	DG142		2 × DPST JFET Analog Switch

IC CROSS REFERENCE GUIDE

Company	Part Number	Siliconix Equivalent Part	Siliconix Similar Function	Function
National (Cont.)	AH0143	DG143		2 × SPST JFET Analog Switch
	AH0144	DG144		SPDT Diff JFET Analog Switch
	AH0145	DG145		DPDT 2 × Diff JFET Analog Switch
	AH0146	DG146		SPDT Diff JFET Analog Switch
	AH2114		DG181, DG184	DPST JFET Analog Switch
	AH5009		DG172	4 × SPST Virtual Gnd Analog Switch
	AH5010		DG172	4 × SPST Virtual Gnd Analog Switch
	AH5011		DG201A	4 × SPST Virtual Gnd Analog Switch
	AH5012		DG201A	4 × SPST Virtual Gnd Analog Switch
	AH5013		DG172(3/4)	3 × SPST Virtual Gnd Analog Switch
	AH5014		DG172(3/4)	3 × SPST Virtual Gnd Analog Switch
	AH5015		DG201A(3/4)	3 × SPST Virtual Gnd Analog Switch
	AH5016		DG201A(3/4)	3 × SPST Virtual Gnd Analog Switch
	AM181		DG181	SPST BIFET Switch
	AM182		DG182	SPST BIFET Switch
	AM184		DG184	2 × DPST BIFET Switch
	AM185		DG185	2 × DPST BIFET Switch
	AM187		DG187	SPDT BIFET Switch
	AM188		DG188	SPDT BIFET Switch
	AM190		DG190	2 × SPDT BIFET Switch
	AM191		DG191	2 × SPDT BIFET Switch
	AM2009		G118	6 × MOS Analog Switch
	LF11331		DG201A, DG211, DG308A	4 × SPST JFET Analog Switch
	LF11332		DG201A, DG211, DG308A	4 × SPST JFET Analog Switch
	LF11333		DG201A, DG211, DG308A	4 × SPST JFET Analog Switch
	LF12331		DG201A, DG211, DG308A	4 × SPST JFET Analog Switch
	LF12332		DG201A, DG211, DG308A	4 × SPST JFET Analog Switch
	LF12333		DG201A, DG211, DG308A	4 × SPST JFET Analog Switch
	LF13331		DG201A, DG211, DG308A	4 × SPST JFET Analog Switch
	LF13332		DG201A, DG211, DG308A	4 × SPST JFET Analog Switch
	LF13333		DG201A, DG211, DG308A	4 × SPST JFET Analog Switch
	LFXX201	DG201A		4 × SPST JFET Analog Switch
	LFXX201	DG201A		4 × SPST JFET Analog Switch
	LFXX201	DG201A		4 × SPST JFET Analog Switch
	LFXX202	DG202		4 × SPST JFET Analog Switch
	LFXX202	DG202		4 × SPST JFET Analog Switch
	LFXX202	DG202		4 × SPST JFET Analog Switch
	LFXX506	DG506A		16 × CMOS Analog MUX
	LFXX507	DG507A		8 × Diff CMOS Analog MUX
	LFXX508	DG508A		8 × CMOS Analog MUX
	LFXX509	DG509A		4 × Diff CMOS Analog MUX
PMI	MUX08	DG508A		8 × CMOS Analog MUX
	MUX16	DG506A		16 × CMOS Analog MUX
	MUX24	DG509A		4 × Diff CMOS Analog MUX
	MUX28	DG507A		8 × Diff CMOS Analog MUX
	SW-7510		DG5045	4 × SPST BIFET Analog Switch

IC CROSS REFERENCE GUIDE

Company	Part Number	Siliconix Equivalent Part	Siliconix Similar Function	Function
PMI (Cont.)	SW01	DG201A		4 × SPST BIFET Analog Switch
	SW05	DG200A		2 × SPST BIFET Analog Switch
	SW06		DG5042	4 × SPST BIFET Analog Switch
	SW08		DG5043	4 × SPST BIFET Analog Switch
	SW06		DG243	4 × SPST BIFET Analog Switch
	SW201	DG201A		4 × SPST BIFET Analog Switch
	SW202	DG202		4 × SPST BIFET Analog Switch
RCA	CD4016		DG308A	CMOS Quad Bilateral Switch
	CD4051		DG508A	CMOS Analog MUX
	CD4052		DG509A	CMOS Analog MUX
	CD4066		DG308A	CMOS QUad Bilateral Switch
	CD4067		DG506A	CMOS Analog MUX
	CD4097		DG507A	CMOS Analog MUX
SPI	SD5000	SD5000	SD5400	4 × SPST DMOS Analog Switch
	SD5001	SD5001	SD5401	4 × SPST DMOS Analog Switch
	SD5002	SD5002	SD5402	4 × SPST DMOS Analog Switch
Silicon General	SG1525A	PWM25(A Suffix)		Pulse Width Modulator
	SG1527A	PWM27(A Suffix)		Pulse Width Modulator
	SG2525A	PWM25(B Suffix)		Pulse Width Modulator
	SG2527A	PWM27(B Suffix)		Pulse Width Modulator
	SG3525A	PWM25(C Suffix)		Pulse Width Modulator
	SG3527A	PWM27(C Suffix)		Pulse Width Modulator
Sprague	ULN8125R	PWM25(C Suffix)		Pulse Width Modulator
	ULN8127R	PWM27(C Suffix)		Pulse Width Modulator
	ULQ8125R	PWM25(B Suffix)		Pulse Width Modulator
	ULQ8127R	PWM27(B Suffix)		Pulse Width Modulator
	ULS8125R	PWM25(A Suffix)		Pulse Width Modulator
	ULS8127R	PWM27(A Suffix)		Pulse Width Modulator
Supertex	HV-13		DG589	Dual 4-Channel High Voltage MUX
	HV-15		DG568	8-Channel High Voltage MUX
TI	SN75551	Si9551		EL Row Driver
	SN75552	Si9552		EL Row Driver
	SN75553	Si9553		EL Column Driver
	SN75554	Si9554		EL Column Driver
	TL182	DG182		SPST BIFET Switch
	TL185	DG185		2 × DPST BIFET Switch
	TL188	DG188		SPDT BIFET Switch
	TL191	DG191		2 × SPDT BIFET Switch
	TL520	Si520, Si8601	Si8602	8-Bit 8 Channel DAS
Teledyne	CAG10		DG181(1/2)	SPST JFET Analog Switch, Low r(DS), Fast
	CAG10A		DG180(1/2), DG181(1/2)	SPST JFET Analog Switch, Very Low r(DS)
	CAG10B		DG181(1/2), DG182(1/2)	SPST JFET Analog Switch, Fast r(DS)

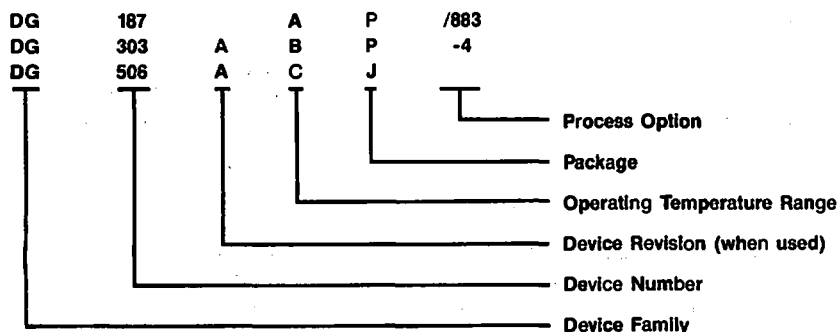
IC CROSS REFERENCE GUIDE

Company	Part Number	Siliconix Equivalent Part	Siliconix Similar Function	Function
Teledyne (Cont.)	CAG10C		DG180(1/2), DG181(1/2)	SPST JFET Analog Switch, Very Low r(DS), Fast
	CAG10D		DG180(1/2)	SPST JFET Analog Switch, Low r(DS)
	CAG13		DG181	2 × SPST JFET Analog Switch, Low r(DS)
	CAG13A		DG181	2 × SPST JFET Analog Switch, Low r(DS)
	CAG13C		DG181	2 × SPST JFET Analog Switch, Low r(DS)
	CAG13D		DG181	2 × SPST JFET Analog Switch, Low r(DS)
	CAG14		DG181	SPST JFET Analog Switch, High Speed
	CAG14A		DG181	SPST JFET Analog Switch, High Speed
	CAG21		DG184	2 × DPST JFET Analog Switch, Low r(DS)
	CAG22		DG181	2 × SPST JFET Analog Switch, Low r(DS)
	CAG23		DG181	2 × SPST JFET Analog Switch, Low r(DS)
	CAG24		DG134	2 × SPST JFET Analog Switch, Low r(DS) Low Power
	CAG27		DG141, DG180	2 × SPST JFET Analog Switch, Very Low r(DS)
	CAG27-10		DG141, DG180	2 × SPST JFET Analog Switch, Very Low r(DS)
	CAG30		DG181(1/2)	SPST JFET Analog Switch, Low r(DS)
	CAG42		DG181	2 × SPST JFET Analog Switch, Low r(DS)
	CAG45		DG181	2 × SPST JFET Analog Switch, Low r(DS)
	CAG45A		DG181	2 × SPST JFET Analog Switch, Low r(DS)
	CAG48		DG184	2 × DPST JFET Analog Switch
	CAG48A		DG184	2 × DPST JFET Analog Switch
	CAG6		DG141(1/2), DG180(1/2)	SPST JFET Analog Switch, Very Low r(DS)
	CAG6-10		DG141(1/2), DG180(1/2)	SPST JFET Analog Switch, Very Low r(DS)
	CAG7		DG145, DG161, DG186, DG187	SPDT JFET Analog Switch, Very Low r(DS)
	CAG7-10		DG145, DG161, DG186, DG187	SPDT JFET Analog Switch, Very Low r(DS)
	CDA18		DG187	SPDT JFET Analog Switch, Fast
	DA18		DG187	SPDT JFET Analog Switch, Fast
	CDA2		DG181	2 × SPST JFET Analog Switch
	CDA23		DG186	SPDT JFET Analog Switch, Fast
	CDR125	D125		6 × FET Driver
	CDR5		DG139(1/2)	Low-Level to High-Level Interface Circuit
	TSC426		D469	Dual Power MOSFET Driver
	TSC427		D469	Dual Power MOSFET Driver
	TSC428		D469	Dual Power MOSFET Driver
	TSC7135	Si7135		4 1/2 Digit BCD A/D Converter
	TSC7660	Si7660	Si7661	Voltage Inverter/Converter
Unitrode	UC1525A	PWM25(A Suffix)		Pulse Width Modulator
	UC1527A	PWM27(A Suffix)		Pulse Width Modulator
	UC2525A	PWM25(B Suffix)		Pulse Width Modulator
	UC2527A	PWM27(B Suffix)		Pulse Width Modulator
	UC3525A	PWM25(C Suffix)		Pulse Width Modulator
	UC3527A	PWM27(C Suffix)		Pulse Width Modulator

TEMPERATURE RANGE AND PACKAGE CROSS REFERENCE

Competitor	Temperature Range		Package	
	Competitor	Siliconix Equivalent	Competitor	Siliconix Equivalent
Analog Devices	A, B, C J, K, L S, T, U	A B C	DN F H N	P, K L A J
AMD	C M	C A	D P	P, K J
Cherry	1 2 3	A B C	J N	K J
EXAR	1 2 3	A B C	C M, N	J K
Harris	2 4, 9 5 8	A B C A/883	1 2 3 9	P, K A J L
Intersil	C I M	C B A	D, P F, L P T, A J	P L J A K
Linear Technology	C M	D A	H J N	A K J
Micro Power	A, S B, J, K C	A B C	A J P	A J P
Motorola	A C	A D	L P	K J
National	1, M 2, C 3	A B C	H N F, W J, D	A J L P, K
PMI	— — —	— — —	K M Y, Q, X	A L P, K, J
RCA	— — —	— — —	D E F	P, K P J
Silicon General	1 2 3	A B C	J	K
SPI	— — —	— — —	I N	I(B) N(B)
Sprague	N Q S	C B A	A R	J K
Supertex	— — —	— — —	C D	P, R K
Teledyne	C I M	C B A	J P T	K J A
Texas Instruments	C L M	B C A	T, FA, J, W JA, JB, JP L, LA N, P	L P, K A J
Unitrode	1 2 3	A B C	N P	J K

Device Ordering Information



DEVICE FAMILY (1, 2 or 3 Letters)

- D** — Drivers for FET Switches
- DF** — Digital Function
- DG** — Analog Switches and Analog Multiplexers
- G** — Multi-Channel FETs
- L** — Linear
- LD** — Linear Digital Combinations
- PWM** — Pulse Width Modulator
- SD** — Siliconix DMOS Product
- SI** — Siliconix Proprietary Integrated Circuit or Second Source Part
- SJM** — QPL Listed Part

DEVICE NUMBER (3 or 4 Digit Numbers)

OPERATING TEMPERATURE RANGE (1 Letter)

- A** — -55 to 125°C
- B** — -25 to 85°C
- C** — 0 to 70°C
- D** — -40 to 85°C

B and **D** temperature range parts receive industrial processing unless a process option dash number is added to the part number.

C temperature range parts are given commercial processing.

All possible combinations of device types, temperature ranges, package types and MIL-883 process options are not necessarily available. Consult individual data book pages for complete information, or sales office.

PACKAGE (1 Letter)

- A** — Metal Can
- J** — Dual-In-Line Package—Plastic
- K** — Dual-In-Line Package—CERDIP
- L** — Flat Package
- P** — Dual-In-Line Package—Side Braze
- R** — Dual-In-Line Package—Side Braze
- Y** — Small Outline Package

PROCESS OPTION

- /883** — MIL-STD-883, Class B Compliant-Non JAN
- 2** — Non Compliant-Non JAN
- 4** — 160 Hour Burn-In
- BS9000** — BS9000 Compliant

SILICONIX QUALITY AND RELIABILITY PROGRAM

INTRODUCTION — The employees and management of Siliconix are dedicated to a Quality Program emphasizing 'defect' prevention. The corporate Quality Policy initiated by our CEO and his staff is: *Siliconix is dedicated to the manufacture of high quality, reliable products that meet the needs defined by our customers. Achieving Customer requirements as defined by the specification is the responsibility of all Siliconix employees.*

This means Quality is the combined responsibility of Design, Engineering, Manufacturing, and all Support Groups, not solely that of the Quality Department.

ORGANIZATION — To insure maximum attention to Quality, Siliconix is organized so that the Reliability and Quality Assurance Worldwide Directorate report at the same level (the Siliconix Vice President of Worldwide Operations) as worldwide manufacturing, design, engineering, and sales.

QUALITY SYSTEM — Siliconix has adopted a "Quality System" approach based on MIL-Q-9858A, AQAP-1 (NATO) and Defense Standard 05-21 (UK) for its overall Quality Program. This approach provides a structured program addressing every aspect of product quality from design through shipment.

PROCESS CONTROL - WAFER FABRICATION

1.0 Process Controls: The Quality Control program utilizes the following methods of control to achieve its objectives: (1) Process audits, (2) Environmental monitors, (3) Process monitors, (4) Lot acceptance inspections, (5) Process qualifications, and (6) Process integrity audits. Together these methods of control, visually and electrically characterize the wafer fabrication operation.

2.0 Definitions: The essential method of the Quality Control Program is defined as follows:

- 2.1 Process Audit** — Audits concerning manufacturing operator conformance to specification. These are performed on all operations critical to product quality and reliability.
- 2.2 Environmental Monitor** — Monitors concerning the process environment, i.e., water purity, temperature/humidity, particulate counts.
- 2.3 Process Monitor** — Periodic inspections and tests are made at designated process steps to verify the use of manufacturing inspections and the maintenance of process averages. These inspections provide both attribute and variable data.
- 2.4 Lot Acceptance** — Lot by lot sampling. This sampling method is reserved for those operations or attributes deemed critical and requiring special attention.

2.5 Process Qualification — Complete distributional analysis is run to specified tolerance limits on $\bar{x}$ and σ . These qualifications are typically conducted on deposition and evaporation processes, i.e., EPI, aluminum, vapox, backside gold, etc.

2.6 Process Integrity Audit — Special audits are conducted on oxidation and metal evaporation processes. (CV drift — oxidation; SEM evaluation — metal evaporation).

3.0 Data Presentation/Reporting:

3.1 The process control data is recorded on an attribute or variable basis as required. P charts, $\bar{X}$ R charts, or $\bar{x}\sigma$ charts are maintained on a regular basis. This data is periodically reviewed and serves as the criteria for judging the acceptability of specific processes.

3.2 Summary data from the various process control operations is quickly relayed to appropriate line, engineering, and management personnel so that if necessary, appropriate corrective action can be taken promptly.

PROCESS CONTROL - ASSEMBLY

1.0 The process control and inspection points of the assembly operation are explained and listed below:

1.1 Die Inspection — After inspection by Manufacturing, In-Process Quality Control samples each lot to internal or customer specifications and standards.

1.2 Die Attach Inspection — Visual inspection of samples is performed periodically on a machine/operator basis. Die attach techniques are monitored and temperatures are verified.

1.3 Die Attach Integrity — Following die attach, die shear strength or thermal resistance testing is performed periodically on a machine/operator basis. Either manual or automatic die attach is used.

1.4 Wire Bond Inspection — Visual inspection of samples is implemented by wire pull test periodically during each shift. These checks are also done on a machine/operator basis. $\bar{X}$ R data is maintained for the wire pull tests.

1.5 Pre-Seal/Pre-Encapsulation Inspection — Following 100% inspection of each lot, samples are taken on a lot acceptance basis and inspected to suit internal or customer criteria.

1.6 Seal Inspection — Periodic monitoring of the sealing operation checks the critical temperature profile of the sealing oven for both glass and metal preform seals.

QUALITY IMPROVEMENT PROGRAMS

Siliconix is addressing the quality improvement issue and has implemented several programs to achieve the necessary changes:

- 1.0 Quality Reporting:** Our Quality Reports have been restructured to provide more meaningful data and increased focus on problem areas, viz -
 - 1.1 Monthly reports of final product quality provide Process Average (PA) and Average Outgoing Quality (AOQ) measurements by product line.
 - 1.2 Weekly reports of In-Process QC results include control charts for percent defective by product line and defect modes and quantities by operator.
 - 1.3 Monthly reports of operator audits, line audits, and environmental monitors by manufacturing area.
 - 1.4 Monthly reports of incoming materials quality by generic family and vendor.
- 2.0 Audit and Corrective Action:** A two-tier audit program with closed-loop corrective action has been implemented.
 - 2.1 Operator audits are performed continuously in each wafer fabrication and assembly area.
 - 2.2 Quality System audits are performed on each element of our total quality system from product design to product shipment.
 - 2.3 Deficiencies observed in the audit programs are addressed to the responsible parties through Notice of Variance (NOV) system. Responses are coordinated and monitored by QC to ensure effective corrective action has been implemented.
- 3.0 Quality Improvement Team:** A task force has been established to direct the quality improvement effort in Siliconix' worldwide facilities:
 - 3.1 Six diagnostic committees cover the product line and geographic matrix of the Siliconix' organization. Three committees are chaired by the respective product line engineering manager, and three are chaired by the respective plant operations manager. The diagnostic committees have the charter to define problems, recommend and implement Quality Improvement projects and actions, and to measure and report the results.
 - 3.2 A steering committee composed of the Vice President of Operations and Manufacturing and Product Line Directors is chaired by the Quality Director. This steering committee directs the activities of the diagnostic committees through project approval, status reviews, and resource provision.
 - 3.3 A facilitator acts as a coordination, reporting, and communication catalyst to ensure worldwide participation and understanding.

RELIABILITY

- 1.0 Reliability Department:** Provides Siliconix with a number of programs to define product reliability levels. Among these programs are (1) Qualification, (2) Monitoring, (3) Failure analysis and (4) Data collection and presentation.
- 2.0 Qualification Program:**
 - 2.1 Qualification of New Products and Processes.
 - 2.1.1 Procedures for qualification of new chip designs require reliability participation or approval in design reviews, documentation, characterization and reliability stress studies.
 - 2.1.2 New package qualification approval and release for production is granted by Reliability after prescribed environmental tests have been successfully completed.
 - 2.1.3 New process qualification approval is granted by Reliability after Quality control and Reliability have completed evaluation of process control engineering studies. Significant modifications to existing processes are considered as new processes for the purpose of qualification.
 - 2.1.4 Proper documentation of all changes in processes or procedures and any new or improved designs or materials is assured by Reliability approval of all changes.
 - 2.2 Qualification of existing products for new applications.
 - 2.2.1 Customer Qualifications. Reliability is responsible for review and acceptance of all customer qualification requirements. When a qualification program or special testing is required, Reliability designs and implements appropriate test plans and coordinates with the customer.
 - 2.3 Reporting and publication of data.
 - 2.3.1 Qualification test reports are prepared and distributed by Reliability for all products or processes which are approved by formal qualification. These reports contain a statement of qualification that certifies the process or product for use.
 - 2.3.2 When new products require reporting of qualification data, Reliability assists Marketing Services by providing this data for customers or for advertising purposes.
 - 2.4 Research and Development: It is the responsibility of Reliability to investigate new or improved methods and techniques for test-

ing and evaluating products. This includes, but is not limited to the following methods:

2.4.1 Design test plans and programs.

2.4.2 Accelerated stress testing.

3.0 Reliability Monitor Programs:

3.1 Device and Package Reliability Monitor Programs are affected for all packages using a variety of device types to maximize data usefulness and cost effectiveness of equipment. Packages are monitored using applicable methods of MIL-STD-883, Class B. Data is reported as specified in detailed procedures for each package-chip combination. Package monitor programs include, but are not limited to, the following general tests using the appropriate conditions specified in MIL-STD-883, Class B, Method 5005.

3.1.1 Biased Humidity Life

3.1.2 Operating Life Method 1005

3.1.3 Steam Pressure

3.1.4 Temperature Cycling Method 1010

3.1.5 Thermal Shock Method 1011

3.1.6 Intermittent Opens

3.1.7 Salt Atmosphere Method 1009

3.1.8 Constant Acceleration Method 2001

3.1.9 Mechanical Shock Method 2002

3.1.10 Solderability Method 2003

3.1.11 Lead Integrity Method 2004

3.1.12 Vibration Method 2007

3.2 Accelerated stress monitor programs are conducted where practical to obtain timely feedback for process effectiveness monitors as well as for ultimate device capability studies. Such tests include the following:

3.2.1 Extended tests, beyond normal device-package expected capabilities, are performed for comparative product evaluation or characterization as well as for quick feedback on component performance trends.

4.0 Failure Analysis and Failure Mode Identification

4.1 Failure analysis in support of in-process quality control process-monitors is handled by Reliability through failure analysis report requests. This support may include such services as visual inspection, cross-sectioning, thickness measurements, selective etching, die probing, and other applicable techniques.

4.2 Customer returns and customer requested failure studies are undertaken by Reliability when required. Reliability will coordinate all replies to customers and approve or originate all correspondence or reports to customers.

4.3 Assembly process failures and failures of finished devices prior to QA acceptance are the responsibility of the product manager, but Reliability provides assistance in analysis when requested by Quality Assurance,

Quality Control, or Engineering personnel.

4.4 Corrective action and follow-up — When Reliability has determined that corrective action is necessary, prior to either releasing the product for shipment or proceeding further in production processing, they generate a corrective action request.

5.0 Data Analysis, Publication and Reporting Data from reliability studies is disseminated to all interested parties within Siliconix:

5.1 Collection and analysis of reliability data is the responsibility of Reliability personnel. It is performed as a routine portion of reliability work.

5.2 Reporting of scheduled monitor programs is provided on a scheduled basis.

5.3 Customer and Marketing Data Support. Reliability will provide reports to parties who clearly indicate an interest in reliability of applicable parts.

MILITARY PROGRAMS

Siliconix has a total commitment to the Military and Aerospace Business.

We maintain the following Line Certifications:

- MIL-M-38510 at our Santa Clara Facility for CMOS and Bipolar/PMOS/JFET Products.
- MIL-S-19500 at our Santa Clara, Hong Kong, and Taiwan facilities for JFET and MOS-POWER products.
- BS9000 (British Standard) at our UK facility for Integrated Circuits.
- CECC (European Harmonized Standard) at UK facility for JFET and MOSPOWER products.

We have numerous parts on the Qualified Products Lists of each of these approval systems.

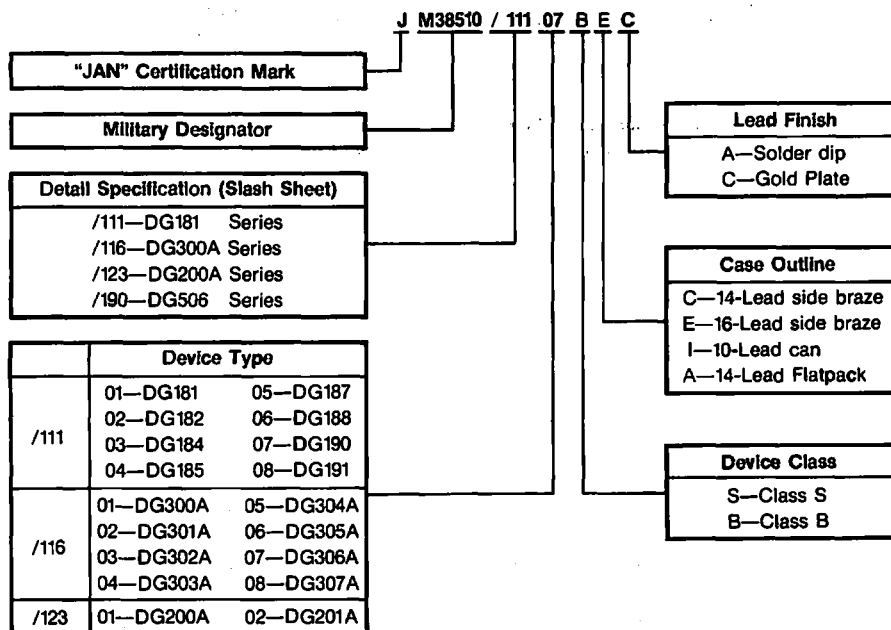
Our Santa Clara facility maintains a LMSC Monitored Line Status and continuously builds product for the major Military and Aerospace Programs.

Analog Switches

JAN38510

Several Siliconix Analog Switches are available fully certified on the QPL (Qualified Parts List) published monthly by Defense Electronics Supply Center (DESC). The QPL numbers follow this format: JM38510/XXXXX. Refer to the current Siliconix Price List for available part types and order numbers.

JAN Part Numbering System



Generic Part Number	JAN Part Number	Order Part Number
DG181AP/883	JM38510/11101BCC	SJM181BCC
DG181AA/883	JM38510/11101BIC	SJM181BIC
DG182AP/883	JM38510/11102BCC	SJM182BCC
DG182AA/883	JM38510/11102BIC	SJM182BIC
DG184AP/883	JM38510/11103BEC	SJM184BEC
DG185AP/883	JM38510/11104BEC	SJM185BEC
DG187AP/883	JM38510/11105BCC	SJM187BCC
DG187AA/883	JM38510/11105BIC	SJM187BIC
DG188AP/883	JM38510/11106BCC	SJM188BCC
DG188AA/883	JM38510/11106BIC	SJM188BIC
DG190AP/883	JM38510/11107BEC	SJM190BEC
DG191AP/883	JM38510/11108BEC	SJM191BEC
DG200AAP	JM38510/12301BCC	SJM200ABCC
DG201AAP	JM38510/12302BEC	SJM201ABEC
DG300AAP	JM38510/11601BCA	SJM300ABCA
DG200AAP	JM38510/12301BCA	SJM200ABCA
DG201AAP	JM38510/12302BEA	SJM201ABEA
DG300AAA	JM38510/11601BIC	SJM300ABIC
DG300AAP	JM38510/11601BCC	SJM300ABCC
DG301AAP	JM38510/11602BCC	SJM301ABCC
DG301AAA	JM38510/11602BIC	SJM301ABIC
DG302AAP	JM38510/11603BCC	SJM302ABCC
DG303AAP	JM38510/11604BCC	SJM303ABCC
DG304AAP	JM38510/11605BCC	SJM304ABCC
DG304AAA	JM38510/11605BIC	SJM304ABIC
DG305AAP	JM38510/11606BCC	SJM305ABCC
DG305AAA	JM38510/11606BIC	SJM305ABIC
DG306AAP	JM38510/11607BCC	SJM306ABCC
DG307AAP	JM38510/11608BCC	SJM307ABCC

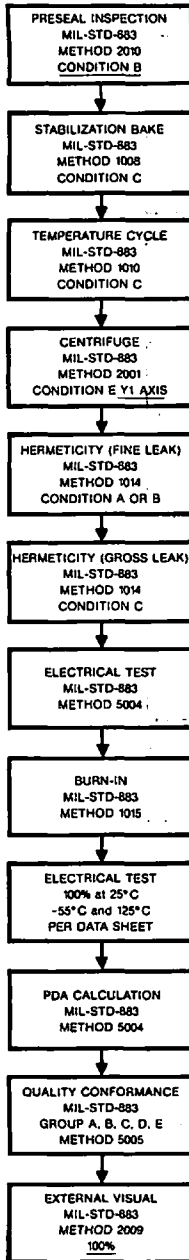
Process Option Flow

The Process Option Flow Chart shows the standard screening options provided by Siliconix for Integrated Circuits

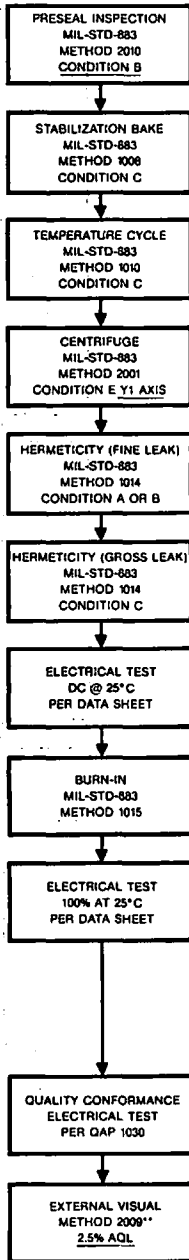
- Column 1:** Denotes the screening process for MIL-STD-883, Class B. To order a part screened to this option, add a "/883" following the package suffix letter. Parts in this classification are carried in inventory.
- Column 2:** Is the screening for the Devices in column 3 but adds a Burn-In to screen out Infant Mortalities.
- Column 3:** Is the screening procedure for military temperature range standard products (A temperature suffix).
- Column 4:** Is the normal screening procedure for industrial and commercial temperature range products (B and C temperature suffixes). An industrial or commercial temperature range product (B and C temperature suffixes) may be given a 160 hour burn-in at 125°C by adding a Dash 4 (-4) following the package suffix letter.

Process Option Flow Chart

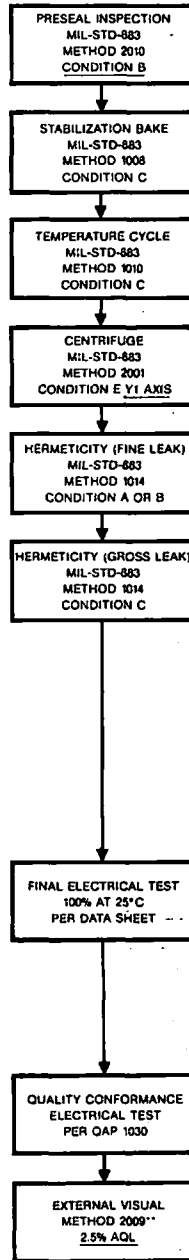
COMPLIANT/NON-JAN /883 MIL-STD-883* CLASS B PRODUCT



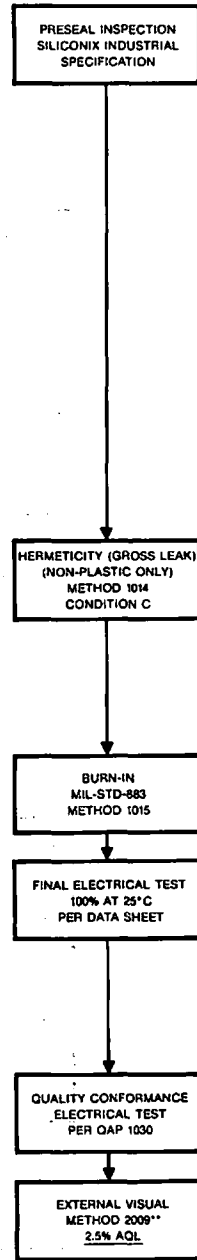
NON-COMPLIANT/ NON-JAN (-2 PRODUCT)



STANDARD PRODUCT (A TEMPERATURE SUFFIX)

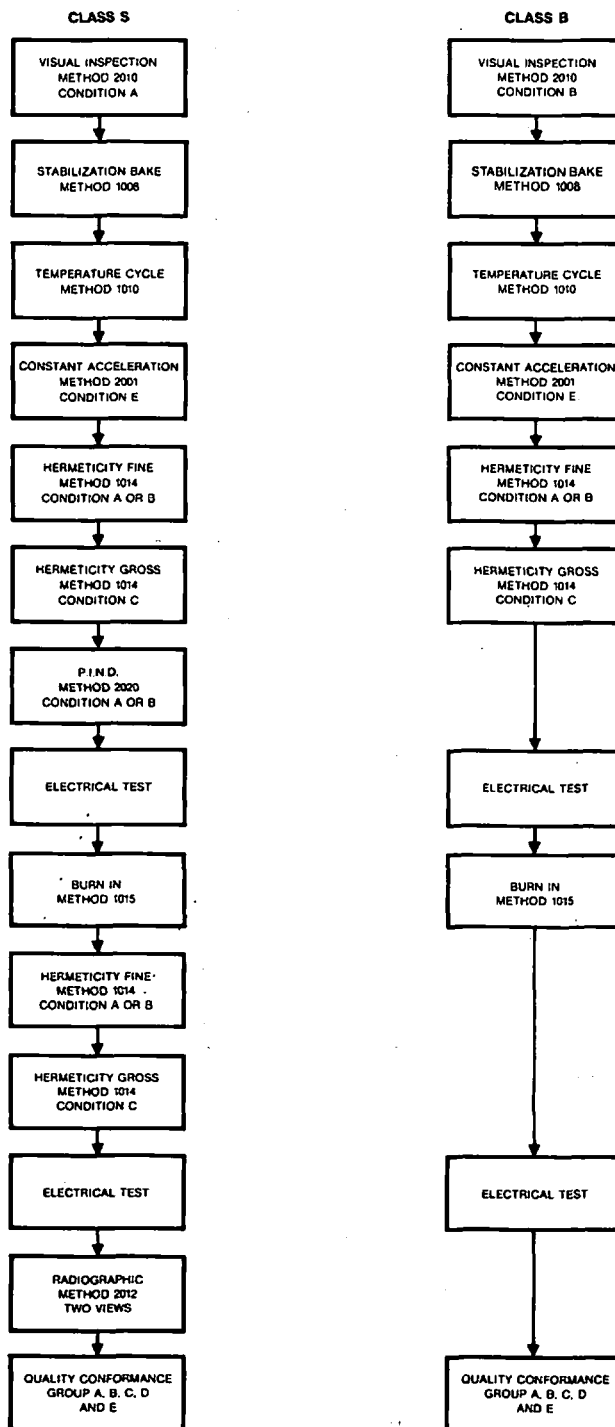


INDUSTRIAL/ COMMERCIAL (B-C-D TEMPERATURE SUFFIX) AND -4 (BURNED-IN)



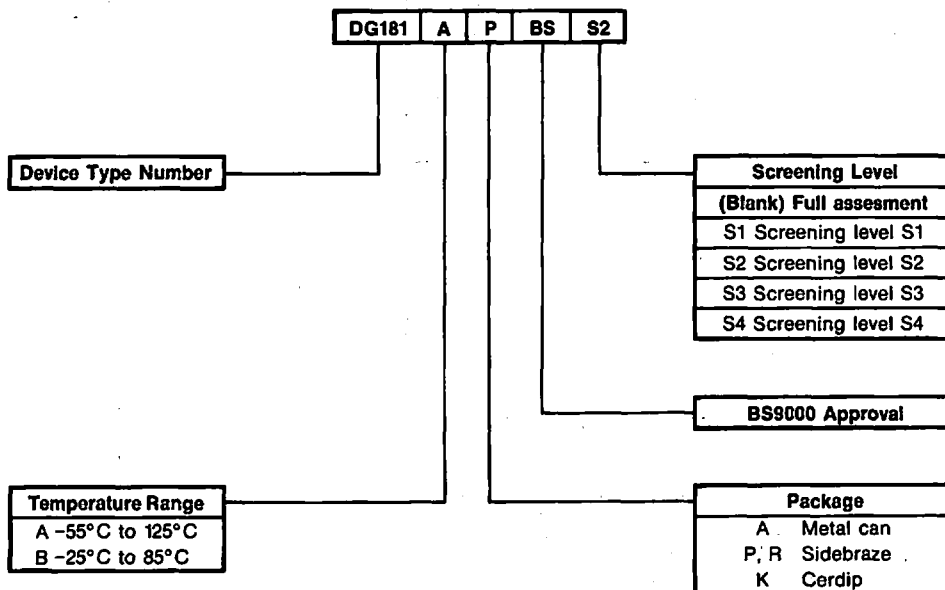
*The latest revision of MIL-STD-883 at time of order is applicable.

JM38510/883 Process Option Flow Chart



Analog Switches and Multiplexers BS9000

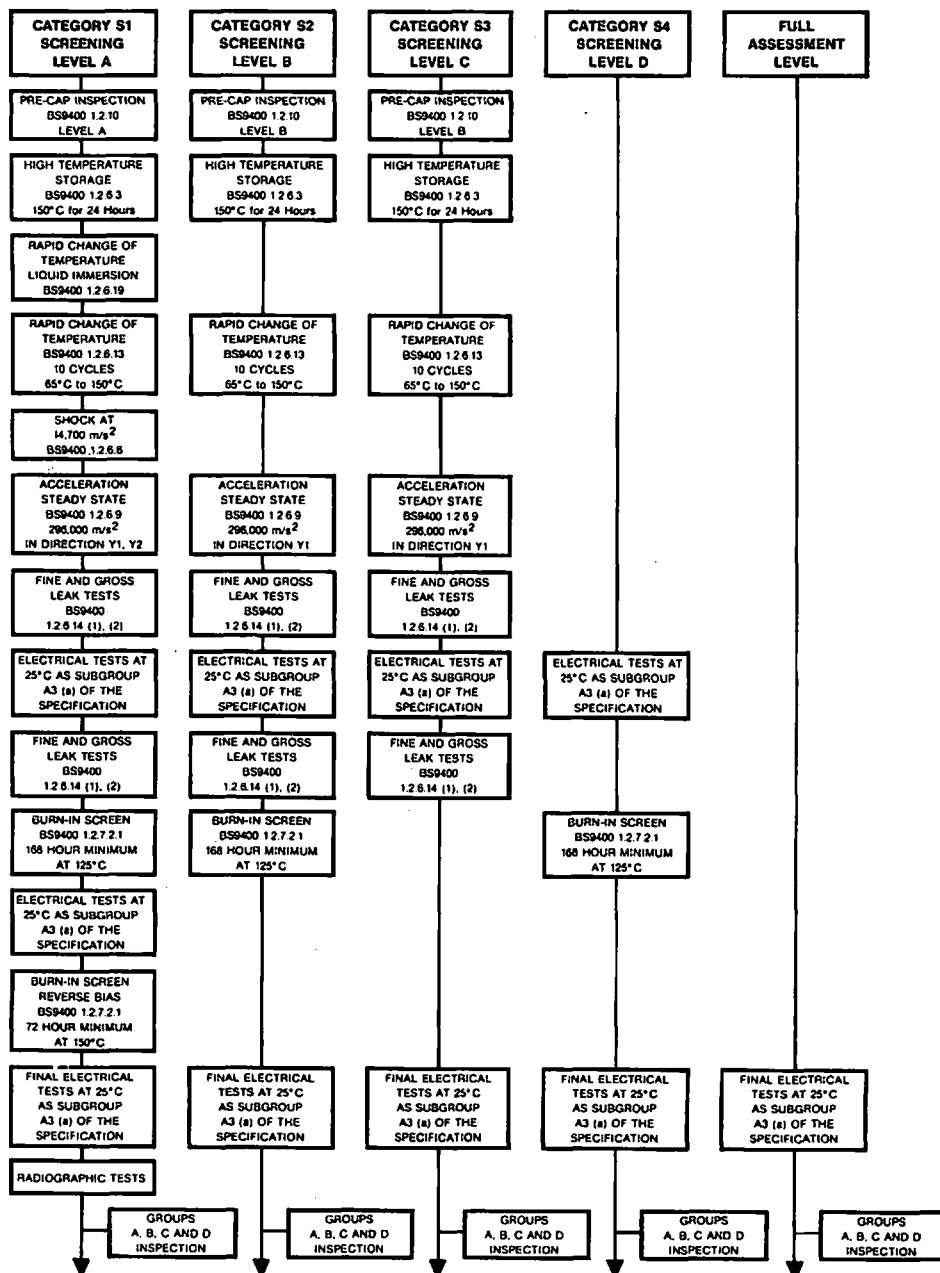
BS9000 Part Numbering System



Approved Parts		
Generic Part No.	Generic Part No.	Generic Part No.
DG126/ /BS	DG180/ /BS	DG300A /BS
DG129/ /BS	DG181/ /BS	DG301A /BS
DG133/ /BS	DG182/ /BS	DG302A /BS
DG134/ /BS	DG183/ /BS	DG303A /BS
DG139/ /BS	DG184/ /BS	DG304A /BS
DG140/ /BS	DG185/ /BS	DG305A /BS
DG141/ /BS	DG186/ /BS	DG306A /BS
DG142/ /BS	DG187/ /BS	DG307A /BS
DG143/ /BS	DG188/ /BS	DG381A /BS
DG144/ /BS	DG189/ /BS	DG384A /BS
DG145/ /BS	DG190/ /BS	DG387A /BS
DG146/ /BS	DG191/ /BS	DG390A /BS
DG151/ /BS	DG200A /BS	
DG152/ /BS	DG201A /BS	
DG153/ /BS	DG501/ /BS	
DG154/ /BS	DG503/ /BS	
DG161/ /BS	DG506A /BS	
DG162/ /BS	DG507A /BS	
DG163/ /BS	DG508A /BS	
DG164/ /BS	DG509A /BS	
	SI3705/ /	

Contact one of the Siliconix sales offices for latest information.

BS9000 Series Process Option Flow Chart



INSPECTION REQUIREMENTS: All tests to be conducted at $T_{amb} = 25^{\circ}\text{C}$ unless otherwise specified. Samples submitted to tests marked 'D' shall not be accepted for release under BS9000 (see 2.6.5 of BS9000 Part 1).

Flow Chart for 100% screening test procedures (See also Inspection Requirements). Production batches containing greater than 10% defective units subsequent to Burn-In will not be issued for release.

The following acceptance/rejection criteria apply to the electrical tests after Burn-In for screening levels A, B, and D.

(a) Lots exhibiting greater than 20% defectives shall be rejected.

(b) Lots exhibiting less than 10% defectives shall be accepted.

(c) Lots exhibiting between 10% and 20% defectives (inclusive) shall have the defectives removed and the remainder of the lot subjected to an identical Burn-In. If such a Lot then exhibits greater than 5% defectives it shall be rejected.

Radiographic test. Each device shall be examined, for extraneous matter and assembly defects, in the X and Y directions.

Burn-In Pin Connections

The following table lists the standard Burn-In Pin Connections for most Siliconix Integrated Circuits. Devices are listed in Alpha-Numerical order according to package type. Following the tables are two examples illustrating Burn-In Pin Connections for different switches and packages.

Part Type	Package Type*	Pins																	
		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
D125	P/L	-30 V	(14)	(14)	(14)	(14)	(14)	(14)	(14)	(14)	(14)	(14)	(14)	(14)	10K - GND				
D129	P/L	(7)	(7)	(7)	GND	(7)	(7)	10K - +5 V	GND	-30 V	(13)	(13)	(13)	10K - +5 V	+5 V				
D139 D169	P/L	-	-	10K - Pin 4	10K - Pin 3	+5 V	+10 V	+5 V	GND	-20 V	GND	10K - Pin 12	10K - Pin 11	-	-				
DG123	P/L	GND	GND	GND	-20 V	4.7K - +5 V	4.7K - +5 V	4.7K - +5 V	4.7K - +5 V	4.7K - +5 V	GND	+5 V	GND	GND	GND				
DG125	P/L	GND	GND	GND	-20 V	GND	GND	GND	GND	GND	+5 V	+5 V	GND	GND	GND				
DG126 DG129 DG133 DG134 DG139 DG140 DG141 DG142 DG143 DG144 DG145 DG146	P/L	10K - GND	+10 V	10K - GND	-	+10 V	10K - GND	10K - GND	+10 V	GND	GND	+10 V	-20 V	GND	+10 V				
DG172	P/L	To Pin 14	GND	GND	-	-20 V	GND	+5 V	+5 V	+5 V	+5 V	GND	+5 V	To Pin 14	7.5K - -20 V				
DG180 DG181 DG182 DG186 DG187 DG188	A	+15 V	10K - GND	GND	+15 V	+5 V	GND	-15 V	GND	10K - GND	+15 V								
DG180 DG181 DG182	P/L	+15 V	10K - GND	-	-	GND	+15 V	+5 V	GND	-15 V	GND	-	-	10K - GND	+15 V				
DG183 DG184 DG185 DG189 DG190 DG191	P	10K - GND	-	10K - GND	-15 V	-15 V	10K - GND	-	10K - GND	+15 V	GND	+15 V	+5 V	GND	-15 V	GND	+15 V		

Parentheses indicate direct connection to indicated pin i.e., (2) = connect to pin 2; All voltages $\pm 5\%$.

* Package types: P = All Dual-In-Line Package, L = All Flat Packages, A = All 10-Lead TO-5s, R = 28 Pin Dual-In-Line Packages.

Burn-In Pin Connections (Continued)

Part Type	Package Type*	Pins																	
		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
DG183 DG184 DG185	L																		
DG186 DG187 DG188	P/L	-15 V	10K - GND	10K - GND	+15 V	GND	+15 V	+5 V	GND	-15 V	GND	+15 V	10K - GND	10K - GND	-15 V				
DG189 DG190 DG191	L																		
DG200A	P/L	+15 V	-	GND	-	(10)	(10)	-15 V	-	(10)	10K - GND	-	+15 V	-	+15 V				
DG201A DG202 DG271	P/L	+15 V	(15)	(15)	-15 V	GND	(15)	(15)	+15 V	+15 V	(15)	(15)	-	+15 V	(15)	10K - GND	+15 V		
DG211 DG212	P	+15 V	(15)	(15)	-15 V	GND	(15)	(15)	+15 V	+15 V	(15)	(15)	+5 V	+15 V	(15)	10K - GND	+15V		
DG300A DG301A DG304A DG305A	A	(9)	(9)	GND	-	GND	-15 V	GND	(9)	10K - GND	+15 V								
DG300A DG301A DG302A DG303A DG304A DG305A DG306A DG307A	P/L	-	(13)	(13)	(13)	(13)	GND	GND	-15 V	GND	(13)	(13)	(13)	10K - GND	+15 V				
DG308A	P	+15 V	(15)	(15)	-15 V	GND	(15)	(15)	+15 V	+15 V	(15)	(15)	-	+15 V	(15)	10K - GND	+15 V		
DG381A	A/P	See DG181																	
DG384A	A/P	See DG184																	
DG387A	A/P	See DG187																	
DG390A	A/P	See DG190																	
DG501 DG503 DG505	P/L	(18)	(4)	(4)	+10 V	(12)	(12)	(12)	(12)	(12)	(12)	(12)	-10 V	-15 V	(16)	(16)	GND		
DG506A DG507A DG526 DG527	R	1 +15 V	2 (28)	3 GND	4 (28)	5 (28)	6 (28)	7 (28)	8 (28)	9 (28)	10 (28)	11 (28)	12 GND	13 GND	14 GND	-	28 Pins		
		15	16	17	18	19	20	21	22	23	24	25	26	27	28				
		GND	GND	GND	GND	(28)	(28)	(28)	(28)	(28)	(28)	(28)	(28)	-15 V	10K - GND				
DG508A	P/L	GND	GND	-15 V	(12)	(12)	(12)	(12)	(12)	(12)	(12)	(12)	10K - GND	+15 V	GND	GND	GND		
DG509A	P/L	GND	GND	-15 V	(13)	(13)	(13)	(13)	(13)	(13)	(13)	(13)	(13)	10K - GND	+15 V	GND	GND		

Parentheses indicate direct connection to indicated pin i.e., (2) = connect to pin 2; All voltages $\pm 5\%$.

* Package types: P = All Dual-In-Line Packages, L = All Flat Packages, A = All 10-Lead TO-5s, R = 28 Pin Dual-In-Line Packages.

Burn-In Pin Connections (Continued)

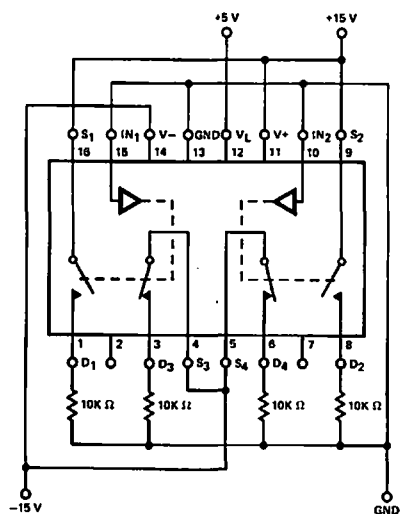
Part Type	Package Type*	Pins																	
		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
DG528	P	GND	GND	GND	-15 V	(13)	(13)	(13)	(13)	(13)	(13)	(13)	(13)	10K→ GND	+15 V	GND	GND	GND	GND
DG529	P	GND	GND	GND	-15 V	(14)	(14)	(14)	(14)	(14)	(14)	(14)	(14)	10K→ GND	+15 V	GND	GND	GND	GND
DG5040 DG5041 DG5042 DG5043 DG5044 DG5045	P	10K→ GND	-	10K→ GND	-15 V	-15 V	10K→ GND	-	10K→ GND	+15 V	GND	+15 V	+5 V	GND	-15 V	GND	+15 V		
DF320	P/J	33Ω to 5V	4.7kΩ to 5V	4.7kΩ to 5V	10kΩ to 5V	(4)	(4)	10kΩ to GND	33kΩ to 5V	4.7kΩ to GND	GND	4.7kΩ to GND	(11)	(11)	(11)	(11)	(11)	(11)	(11)
DF820	P	0 V	2.2kΩ to -12V	100kΩ between 3&4	N/C	N/C	N/C	10kΩ to CLK	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	300kΩ to -12V
G118	P/L	-15 V	-15 V	-15 V	-15 V	-15 V	-15 V	(14)	(14)	(14)	(14)	(14)	(14)	(14)	10K→ +10 V				
G119	P/L	(14)	(14)	-15 V	-15 V	-15 V	(14)	(14)	(14)	(14)	(14)	(14)	(14)	(14)	10K→ +10 V				
L144	P/L	3MΩ→ +15 V	(13)	(11)	GND	GND	(9)	-	-	(6)	220→ -15 V	(3)	GND	(2)	- +15 V				
L181	P	-15 V	+15 V	-15 V	+15 V	-15 V	+15 V	-15 V	+15 V	-15 V	-	-	-	-	-	3MΩ→ +15 V	+15 V		

Parentheses indicate direct connection to indicated pin i.e., (2) = connect to pin 2; All voltages ±5%.

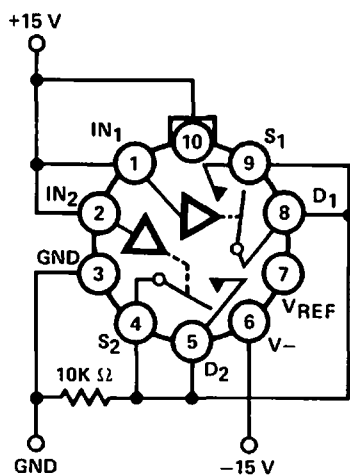
* Package types: P = All Dual-In-Line Package, L = All Flat Packages, A = All 10-Lead TO-5s, R = 28 Pin Dual-In-Line Packages.

Burn-In Pin Connections (Continued)

Examples of Burn-In Circuit Configurations



DG180/DG191 (PACKAGE TYPE P)



DG200A (PACKAGE TYPE A)

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Interface Product Selector Guide¹

Function	Part No. Package Information	Specifications	Features
Power Drivers (Two Channel)	D169 14-pin plastic, 14-pin ceramic DIP	Up to 33V output @ ± 40 mA Switching time—200 ns max. TTL compatible inputs Variable input threshold (V_L pin)	Logic family flexibility Complimentary outputs Can be used to drive MOSFETs or for level translation, analog multiplexing Single ended or dual supply operation
(Four Channel)	D469 14-pin plastic, 14-pin ceramic DIP	High current outputs 500 mA @ 2% duty cycle 100 mA @ 100% duty cycle 150 ns transition time @ 500 pF load TTL or CMOS compatible inputs	Single supply operation Low standby power consumption (60 mW max.) Compelementary logic inputs Can be used to drive MOSFETs
(Bubble Memory)	Si7250 16-pin plastic DIP	High current outputs 250 mA (one output @ 100% duty) 25 ns transition time @ 500 pF load TTL compatible inputs	Easy to interface Power fail reset Single supply operation Low standby power consumption
Display Drivers LCD Driver	DF412 40-pin plastic	4 Digit LCD Driver—BCD to LCD Decoding	CMOS technology, BCD 1111 input blanks digit, internal oscillator develops back plane signal.
E.L. Driver	Si9551/9552 ² 44-pin LCC	Row Driver—32 channel 50 mA output current capability	D/CMOS technology and pin Compatible with TI SN75551/2
E.L. Driver	Si9553/9554 ² 44-pin LCC	Column Driver—32 channel swing capability 90V output Voltage	D/CMOS technology and pin Compatible with TI SN7553/4

NOTE:

1. Devices shown in **boldface** are recommended for new designs.
2. Preliminary product. Specifications subject to change. Contact factory on availability.

INTRODUCTION

The two types of interface circuits shown in this section are MOSPOWER drivers and display drivers. These devices translate TTL or other low level logic into control signals for power MOSFETs or AC devices such as bubble memories or electroluminescent displays.

Large MOSFET geometries are characterized by both high threshold voltages (up to 10 V) and large gate node capacitances (up to 5000 pF). As a result, large voltage swings combined with large source and sink currents are required to charge and discharge the gate capacitance in high speed switching applications. For this reason an interface is needed to translate TTL or low voltage CMOS logic levels to drive levels for power MOSFET switches. This allows direct connection of microprocessor or logic systems to semiconductor switches for such applications as stepper motor control, relay drivers, switching supplies, or bubble memories.

The D169 Dual High Voltage Driver features complementary outputs that can translate up to ± 33 V and handle as much as ± 40 mA. The D469 Quad High Current Power Driver is designed to drive high power MOSFET H-Bridge configurations where up to 500 mA of current drive is required for signals originating from 5 volt TTL or up to 12 Volt CMOS logic signal sources.

The Si7250 Bubble Memory Power Driver is designed to provide up to 200 mA current drive to the Siliconix VQ7250 MOSPOWER driver for driving bubble memory coil crosspoint matrix systems from TTL compatible logic signal sources.

Display drivers are used to interface between microprocessors or logic systems and AC displays. Siliconix DF412 CMOS LCD 4-digit LCD Decoder-Driver or the Si9551/Si9552 and Si9553/Si9554 Row and Column E.L. Display Drivers represent the state of the art in display driver I.C. technology.

The DF412 is designed to decode up to 4 digits of multiplexed BCD information and derive the AC signals needed to directly drive a 4-digit LCD display.

The Si9551/Si9552/Si9553/Si9554 series Row and Column drivers feature 32 channels per device which can drive up to 225 Volt row electrodes at up to 50 mA current and 90 Volt column electrodes at up to 15 mA for the flat panel electroluminescent display applications. Featuring Siliconix state of the art high-voltage D/CMOS silicon gate process, these devices will be available in compact 44-pin LCC packages.

D169

Dual High Voltage Driver



FEATURES

- Variable Input Threshold
- 33 V Output at ± 40 mA
- 70 ns Delay Time
- Complementary Outputs

BENEFITS

- Logic Family Flexibility
- Wide Output Swing
- Fast Switching
- Drive Coupler H Bridge Power Circuit

APPLICATIONS

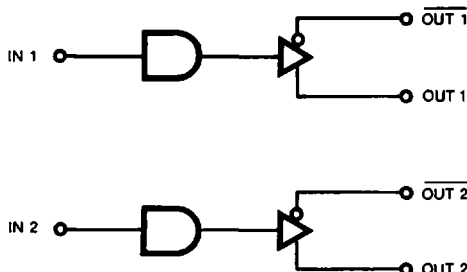
- Analog Multiplexing
- Interface Logic to MOS Power
- Logic Level Translation
- Driver for PIN Diodes and FET Switches
- Line Driver

DESCRIPTION

The D169 is a versatile high-voltage dual driver with complementary outputs. Low-level logic inputs can be translated up to ± 33 V output levels. A differential input stage with adjustable threshold provides high input impedance and easy interfacing to low-level logic or analog inputs. Current-source coupling to the output stage allows wide flexibility in output voltage levels. The complementary emitter-follower outputs can source and sink currents of

up to ± 40 mA with an output swing of up to 33 V. This output stage is excellent for driving capacitive loads; such as power MOSFETs, long cables, or timing capacitors. The output stage can be operated from single or split supplies. Each channel of the dual D169 has two separate outputs that are complementary ($\overline{\text{OUT}}$ and OUT). This two-phase output capability can be very useful for driving power MOSFET configurations.

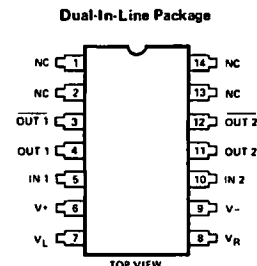
FUNCTIONAL BLOCK DIAGRAM



LOGIC	OUT	$\overline{\text{OUT}}$
0	V-	V+
1	V+	V-

Logic "0" ≤ 0.8 V
Logic "1" ≥ 2.0 V

PIN CONFIGURATION



Order Numbers:
D169AP See Package 11
D169AK See Package 9
D169CJ See Package 7

ABSOLUTE MAXIMUM RATINGS

V^+ to V^- , V^+ to V_R , and V^+ to V_O 36 V
 V_L to V_R , V_{IN} to V_R , and V_L to V_{IN} 10 V
 V_R to V^- , V_L to V^- , and V_O to V^- 36 V
 Current (Any Terminal) DC 40 mA
 Peak (Pulsed 1 ms, 10% Duty Cycle) 150 mA
 Operating Temperature
 (A Suffix) -55 to 125°C
 (C Suffix) 0 to 70°C
 Storage Temperature
 (A Suffix) -65 to 150°C
 (C Suffix) -65 to 125°C

Power Dissipation

"P" Package* 825 mW
 "J" Package* 470 mW
 Thermal Resistance (θ_{JA} , J Package) 0.16°C/mW

*All leads soldered or welded to PC board. Derate P package 11 mW/°C above 75°C. Derate J package 6.5 mW/°C above 25°C.

ELECTRICAL CHARACTERISTICS¹ $T_A = 25^\circ\text{C}$

	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: V ⁺ = 15 V, V _L = 5 V, V ⁻ = -15 V, V _R = 0		LIMITS						UNIT
					D169A			D169C			
					MIN ²	TYP ³	MAX	MIN ²	TYP ³	MAX	
OUTPUT	Output Voltage, High (V ⁺ to V _O)	V _{OH} /V _{OH}	V _{IH} = 2 V for V _{OH} /V _{OL} , V _{IL} = 0.8 V for V _{OH} /V _{OL}	I _{OUT} = 1 mA		0.7	1		0.7	1	V
				I _{OUT} = 40 mA		1.5	2.5		1.5	2.5	
	Output Voltage, Low (V _O to V ⁻)	V _{OL} /V _{OL}		I _{OUT} = 1 mA	-1.2	-0.75		-1.2	-0.75		
				I _{OUT} = 40 mA	-3	-2.2		-3	-2.2		
INPUT	Input Current, Voltage High	I _{INH}	V _{IN} = 3 V			1	5		1	5	nA
	Input Current, Voltage Low	I _{INL}	V _{IN} = 0		-50	-25		-50	-25		μA
DYNAMIC	Switching Time, Low To High, Delay Plus Rise Time	t ₍₊₎	See Switching Time Test Circuit (C _L = 35 pF)			80	170		80	170	ns
	Switching Time, High To Low, Delay Plus Fall Time	t ₍₋₎				90	200		90	200	
SUPPLY	Switching Crossover Level	V _{XO}	V _{IN1} = V _{IN2} = 0 V, No Load			0.001	0.1		0.001	0.1	mA
	Positive Supply Current	I ⁺				3.2	4		3.2	4	
	Logic Supply Current	I _L			-3	-2.2		-3	-2.2		
	Negative Supply Current	I ⁻				0.9			0.9		V
		Reference Supply Current	I _R	V _{IN1} = V _{IN2} = 0 V, No Load			1	1.5		1	1.5

NOTES:

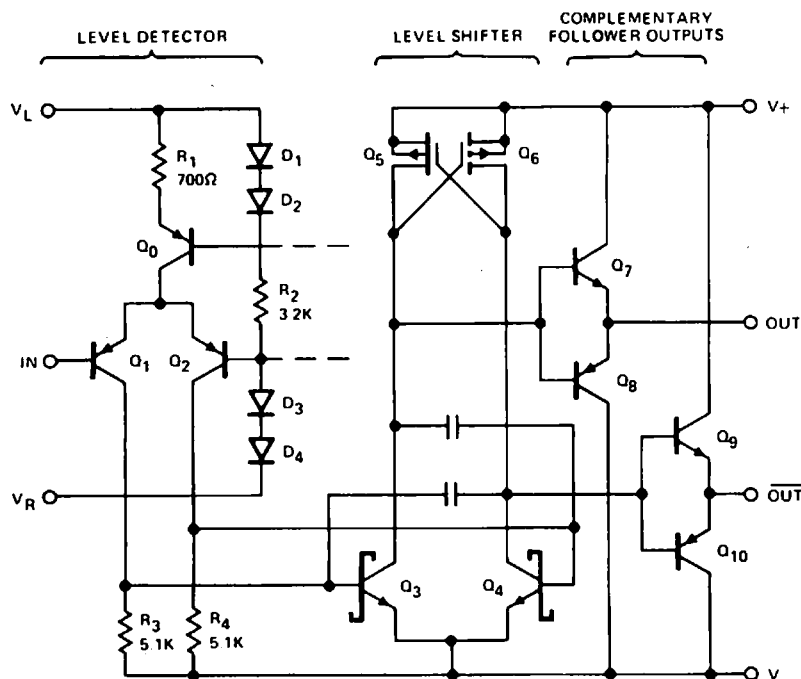
- All DC parameters are 100% tested at 25°C. Lots are sample-tested for AC parameters and high and low temperature limits to assure conformance with specifications.
- The algebraic convention whereby the most negative value is a minimum, and the most positive value is a maximum, is used in this data sheet.
- Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

ELECTRICAL CHARACTERISTICS¹ (Cont.) T_A = Over Temperature Range

	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: V+ = 15 V, VL = 5 V, V- = -15 V, VR = 0		LIMITS						UNIT
					D169AP			D169CJ			
					MIN ²	TYP ³	MAX	MIN ²	TYP ³	MAX	
OUTPUT	Output Voltage, High (V+ to VO)	VOH/VOH	VIH = 2 V for VOH/VOL, VIL = 0.8 V for VOH/VOL	IOUT = 1 mA			1.1			1.1	V
				IOUT = 40 mA			3.1			3.1	
	Output Voltage, Low (VO to V-)	VOL/VOL		IOUT = 1 mA	-1.2			-1.2			
				IOUT = 40 mA	-4			-4			
INPUT	Input Current, Voltage High	IINH	VIN = 5 V				5000			200	nA
	Input Current, Voltage Low	IINL	VIN = 0	-100				-70			μA

NOTES:

1. All DC parameters are 100% tested at 25°C. Lots are sample-tested for AC parameters and high and low temperature limits to assure conformance with specifications.
2. The algebraic convention whereby the most negative value is a minimum, and the most positive value is a maximum, is used in this data sheet.
3. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

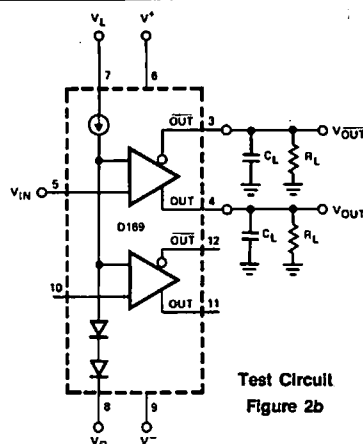
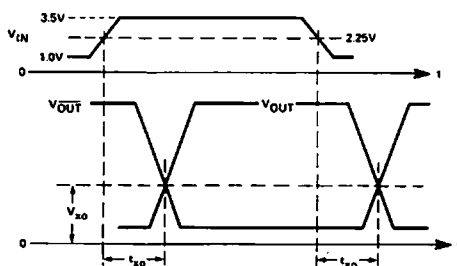
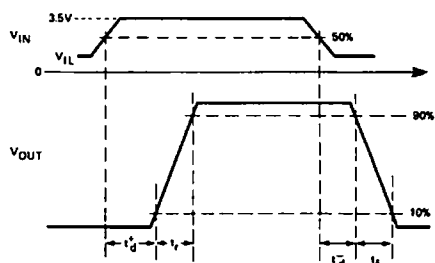


Schematic Diagram, One Channel
Figure 1

ELECTRICAL CHARACTERISTICS (Cont.)

SWITCHING TESTS

TEST	V_L	V_R	V^+	V^-	C_L	R_L	V_{IN}		WAVEFORMS
1	5V	0.7V	10V	0	200 pF	—	1V	3.5V	A
2	5V	0.7V	15V	0	0	510 Ω	1V	3.5V	B
3	5V	0.7V	10V	0	200 pF	—	1V	3.5V	B
4	5V	0.7V	10V	0	1000 pF	—	1V	3.5V	B
5	5V	0	15V	-15V	200 pF	—	0	3.5V	B
6	5V	0	15V	-15V	1000 pF	—	0	3.5V	B

Test Conditions
Figure 2aTest Circuit
Figure 2bSwitching Time Testing
Figure 2Waveforms A
Figure 2cWaveforms B
Figure 2d

Test Conditions	Test 2 (Figure 2)	Tests 5 & 6 (Figure 2)		Tests 3 & 4 (Figure 2)		Units
	Resistive, $I_o = 25\text{ mA}$	$V^+ = +15V, V^- = -15V$		$V^+ = +15V, V^- = 0$		
		Capacitive Load		Capacitive Load		
		200 pF	1000 pF	200 pF	1000 pF	
	Typ	Typ	Typ	Typ	Typ	
Low-to-High Delay Time, t_{d}^{+}	70	95	220	110	230	ns
Rise Time, t_r^{+}	35	60	240	55	200	ns
High-to-Low Delay Time, t_{d}^{-}	50	50	80	55	80	ns
Fall Time, t_f^{-}	25	110	400	80	275	ns

Table 1.

Complementary Emitter-Follower Output

Transistors Q7 through Q10 form complementary emitter-follower outputs connected to each side of the Q3, Q4 level shifter. This permits resistive loads requiring up to 40 mA to be driven at high speeds (rise and fall times under 50 ns—see Figure 10). Also high peak currents are available to drive capacitive loads (see Figure 11 and 12 for capacitive switching data). The switching times are generally independent of output swing, except for the fall time which is influenced by the negative rail, V^- .

The PNP transistors have a relatively high collector series resistance. Consequently, when a steady-state current is being drawn by the PNP which exceeds about 2 mA, the transistor becomes saturated and minority carrier storage takes place in the base and collector regions. Upon a

change of state, a storage delay occurs which can be substantial if a large current is being switched (see Figures 6 and 16). This delay can be utilized when a long "dead time" is needed during change of state and when only the portion of the voltage waveform more positive than zero is of interest. This storage delay does not occur when capacitive loads are being driven, regardless of output levels, or when the load and V^- are returned to ground.

The output level as a function of DC output current are shown in Figures 13 and 14. Note that no current limiting is used in the output stages. Consequently, care must be exercised to avoid exceeding the maximum current rating of the device.

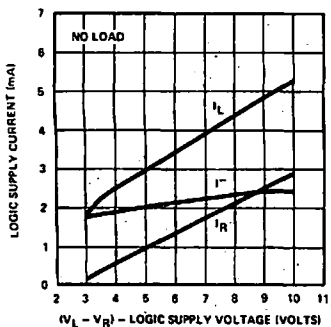


Figure 3. Supply Current Variation with Logic Supply

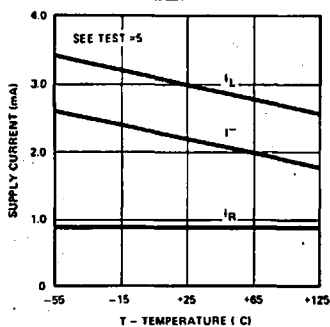


Figure 4. Effect of Temperature on Supply Currents

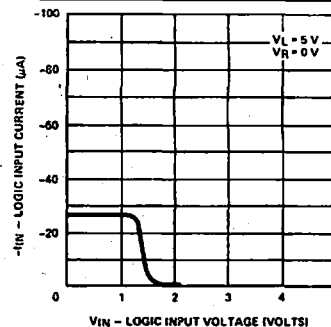


Figure 5. Logic Input Current vs. Logic Input Voltage

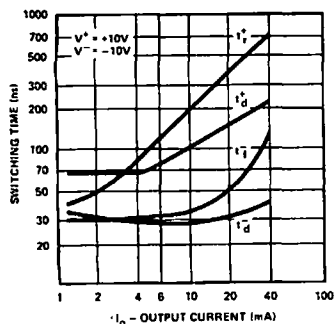


Figure 6. Switching Times with Resistive Load

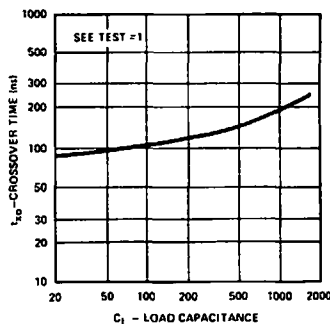


Figure 7. Effect of Load Capacitance on Crossover Time

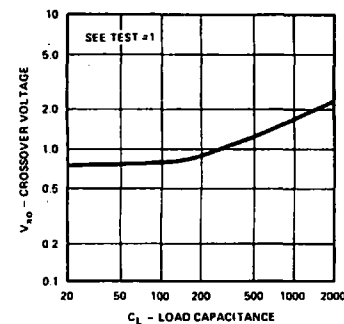


Figure 8. Effect of Load Capacitance on Crossover Level

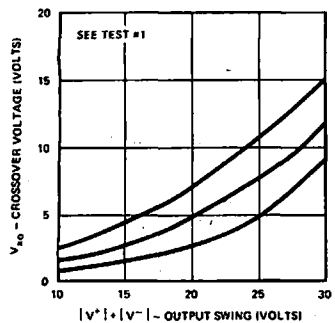


Figure 9. Effect of Voltage Output on Crossover Level

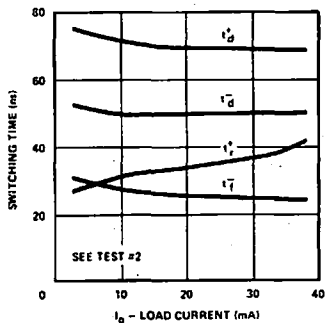


Figure 10. Resistive Load Switching

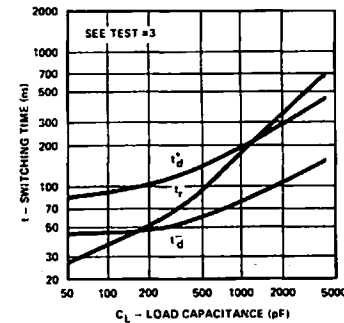


Figure 11. Switching Times with Capacitive Load

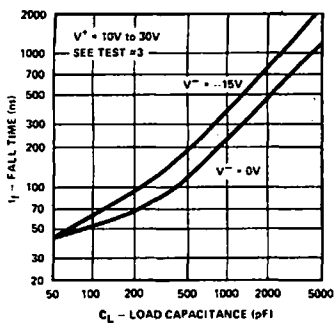


Figure 12. Fall Time with Capacitive Load

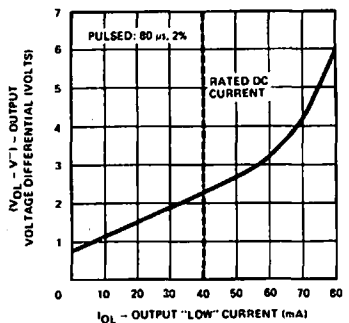


Figure 13. Output "Low" Characteristics

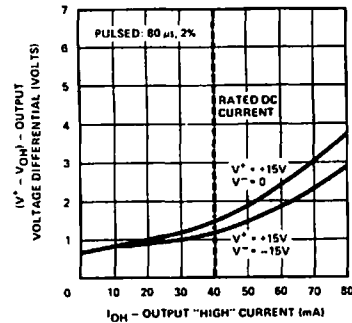
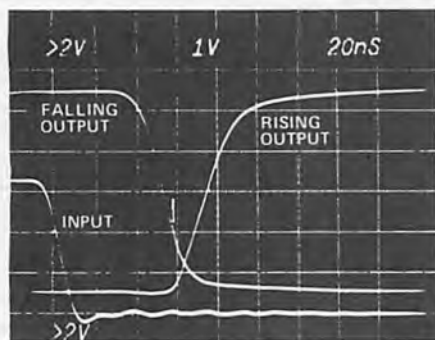
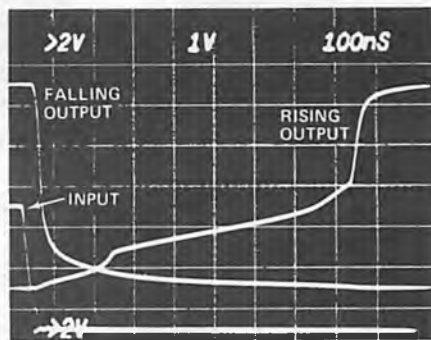


Figure 14. Output "High" Characteristics



Switching Waveform
40 mA Load, $V^+ = 20\text{ V}$,
 $V^- = 0$
Figure 15



Switching Waveform
 $\pm 40\text{ mA}$ Load, $V^+ = 10\text{ V}$,
 $V^- = -10\text{ V}$
Figure 16

OPERATING GUIDELINES

For proper performance of the D169 circuit, certain guidelines must be followed for the power supply and input terminals. These are listed below:

TERMINAL	ALLOWABLE CONDITIONS
V^+ (Pin 6) V^- (Pin 9)	Any positive voltage Any negative voltage or zero volts $10\text{ V} \leq V^+ - V^- \leq 36\text{ V}$
V_R (Pin 8)	$\geq V_{EE} + 1\text{ V}$ (Input Threshold = $V_R + 1.4\text{ V}$)
V_L (Pin 7)	$V_L - V_R \geq 4\text{ V}$
IN1L, IN2L (Pins 5, 10)	$\geq V_{EE} + 1\text{ V}$
IN1H, IN2H (Pins 5, 10)	$\geq V_{EE} + 3\text{ V}$

Table 2

CIRCUIT OPERATION

The D169 circuit has three sections: (1) an input level detector, (2) a level shifter, and (3) a pair of complementary emitter-follower outputs. This arrangement provides a high input impedance, high output drive capability, and compatibility with a wide range of power supply levels. The input threshold level can be easily varied to accept various logic levels. Output swing is set by the V^+ and V^- power supply levels.

Level Detector

Transistors Q_1 and Q_2 form a differential input pair. Transistor Q_0 , resistor R_1 , and diodes D_1 , D_2 form a current source of about 1 mA which drives the common emitter connection. The voltage between supply levels V_L and V_R determines the value of the current source and the current through the bias string (diodes D_1 through D_4 and resistor R_2). The current from the supply V_L and the current out of the terminals V_R and V^- is shown in Figure 3. Temperature variations are shown in Figure 4. The voltage on the base of Q_2 determines the trip point where the circuit changes state. With V_R grounded, the trip point is about 1.4 volts, depending somewhat on the voltage V_L . The input characteristics are shown in Figure 5.

Level Shifter

Schottky-clamped transistors Q_3 and Q_4 along with P-channel MOSFETs Q_5 and Q_6 form a complementary-coupled switching stage. This configuration draws no idle

current and permits a change of state within 100 ns after the input signal passes the trip point. The circuit delays are such that the switching action approaches a "break-before-make" sequence as shown in Figure 15. The response times are essentially independent of the input signal level and rise time.

The time measured from the input signal step to where the output waveforms from OUT and $\overline{\text{OUT}}$ cross is called *crossover time*. The voltage level at that time with respect to V^- is called *crossover voltage*. This point is of importance when driving certain loads where a break-before-make action is necessary to avoid high current surges. The crossover time is essentially independent of output voltage swing, but is affected by the load capacitance as shown in Figure 7. The delay time of the negative going waveform from OUT and $\overline{\text{OUT}}$ is not significantly affected by load capacitance; however, the delay time of the positive going waveform experiences a delay which is fairly sensitive to load capacitance. This feature reduces the dependence of crossover voltage on the load capacitance as shown in Figure 8. However, the output voltage swing does exert considerable influence upon crossover level as indicated in Figure 9.

In order to provide adequate drive to Q_3 and Q_4 , the voltage at the collector of the differential pair must be more positive than the V^- level plus the base emitter drop of the Schottky transistors. This dictates that the "low" level of V_{IN} should exceed V^- by at least one volt.

D469

Quad High Current Power Driver

FEATURES

- High Current Drive
—Up to 500 mA at
2% Duty Cycle
- Single Power-Supply
- TTL Compatible Inputs

BENEFITS

- Low Standby Power Consumption
- Easily Interfaced

APPLICATIONS

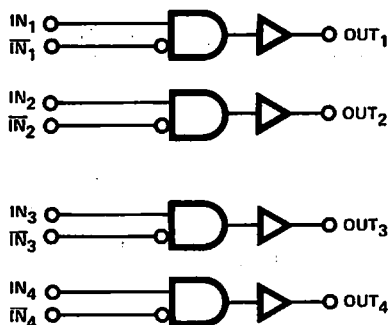
- MOSPOWER H-Bridge Drivers
- Complementary Switching

DESCRIPTION

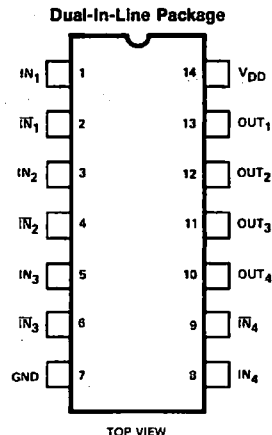
The D469 is a quad high current power driver designed to drive power MOSFET devices for motor control and power control applications. Compatible with TTL or CMOS logic inputs, the D469 can drive up to ± 500 mA at a 2%

duty cycle or ± 100 mA continuously. The D469 is available in 14 pin sidebrazo or plastic DIP packages, and operate over industrial and commercial temperature ranges.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



Order Numbers:
D469AP or D469BP
 See Package 11
D469CJ
 See Package 7

ABSOLUTE MAXIMUM RATINGS

Ambient Temperature Under

Bias -55°C to 125°C

Storage Temperature -65°C to 150°C

Voltage on Any Pin with Respect

to Ground -0.3 to V_{DD} 0.3 VSupply Voltage, V_{DD} -0.3 to 14 V

Output Current 250 mA

(One Output @ 100% Duty Cycle)

	P Package	J Package
Operating Temperature.....	-40 to +85°C	0 to 70°C
Junction Temperature	150°C	125°C
Power Dissipation	825 mW	625 mW
Derating	11 mW/°C	6.25 mW/°C
	above 75°C	above 25°C
θJA	75°C/W	160°C/W
	(No Airflow)	(No Airflow)

ELECTRICAL CHARACTERISTICS¹ $T_A = 25^\circ\text{C}$

	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: $V_+ = 12\text{ V}$	LIMITS			UNIT
				MIN ²	TYP ³	MAX	
INPUT	Input Voltage High	V_{INH}		3			V
	Input Voltage Low	V_{INL}				0.8	
	Input Current With Input Voltage High	I_{INH}	$V_{in} = V_{DD}$		0	10	μA
	Input Current With Input Voltage Low	I_{INL}	$V_{in} = 0\text{ V}$	-10	0		
OUTPUT	Output Voltage High	V_{OUTH}	$I_{out} = -100\text{ mA}$	10	11.8		V
			$I_{out} = -10\text{ mA}$	11.8	11.9		
	Output Voltage Low	V_{OUTL}	$I_{out} = 100\text{ mA}$		0.6	2.0	
			$I_{out} = 10\text{ mA}$		0.07	0.2	
	Output Source Current	I_{OS+}	$V_O = 4.0\text{ V}$, 2% Duty Cycle		500		mA
	Output Sink Current	I_{OS-}	$V_O = 8.0\text{ V}$, 2% Duty Cycle		-500		
DYNAMIC	Propagation Delay Time	t_{PX}	$C_L = 500\text{ pF}$		60	100	ns
	Rise Time	t_R			25		
	Fall Time	t_F			30		
	Input Capacitance	C_{IN}			5		pF
SUPPLY	Supply Current	I_{DD}	$I_{N_x} = \overline{I_{N_x}} = 0\text{ V}$, $V_{DD} = 12.6\text{ V}$		3	7.5	mA
			$I_{N_x} = \overline{I_{N_x}} = 3.0\text{ V}$, $V_{DD} = 12.6\text{ V}$		10	20	
			$f = 100\text{ kHz}$, $V_{DD} = 12.6\text{ V}$, $C_L = 500\text{ pF}$, One Output At A Time		7	20	

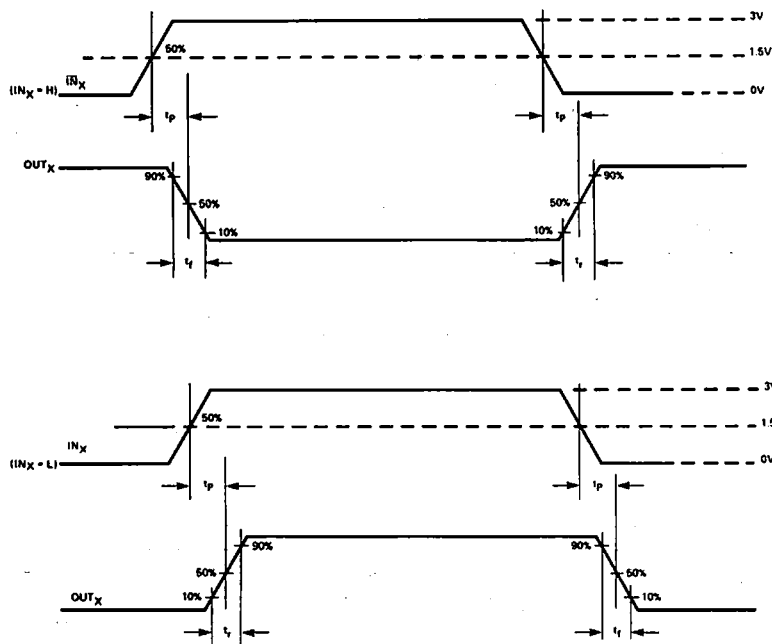
 $T_A = \text{Over Temperature Range}$

	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: $V_+ = 12\text{ V}$	LIMITS			UNIT
				MIN ²	TYP ³	MAX	
INPUT	Input Voltage High	V_{INH}		3			V
	Input Voltage Low	V_{INL}				0.8	
	Input Current With Input Voltage High	I_{INH}	$V_{in} = V_{DD}$			10	μA
	Input Current With Input Voltage Low	I_{INL}	$V_{in} = 0\text{ V}$	-10			
OUTPUT	Output Voltage High	V_{OUTH}	$I_{out} = -100\text{ mA}$	10			V
			$I_{out} = -10\text{ mA}$	11.8			
	Output Voltage Low	V_{OUTL}	$I_{out} = 100\text{ mA}$			2.0	
			$I_{out} = 10\text{ mA}$			0.2	
DYN	Propagation Delay Time	t_{PX}	$C_L = 500\text{ pF}$			150	ns
SUPPLY	Supply Current	I_{DD}	$I_{N_x} = \overline{I_{N_x}} = 0\text{ V}$, $V_{DD} = 12.6\text{ V}$			10	mA
			$I_{N_x} = \overline{I_{N_x}} = 3.0\text{ V}$, $V_{DD} = 12.6\text{ V}$			30	
			$f = 100\text{ kHz}$, $V_{DD} = 12.6\text{ V}$, $C_L = 500\text{ pF}$, One Output At A Time			20	

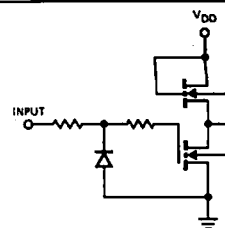
NOTES:

1. Refer to PROCESS OPTION FLOWCHART for additional information.
2. The algebraic convention whereby the most negative value is a minimum, and the most positive value is a maximum, is used in this data sheet.
3. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

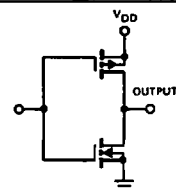
AC TESTING CONDITIONS



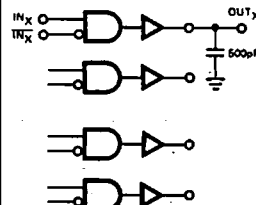
INPUT STRUCTURE



OUTPUT STRUCTURE



SWITCHING TIME TEST CIRCUIT



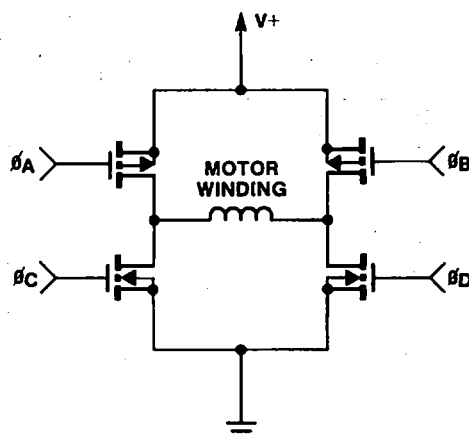
APPLICATIONS OF THE D469 QUAD DRIVER

The D469 quad driver is well suited to applications such as DC motor control. Motors ranging in size from fractional up to several horsepower can be directly driven with power MOSFET devices, if they are provided with suitable gate drive. The D469 fulfills the gate-drive requirements and provides the interface between the MOSFETs and low-power CMOS or TTL control logic.

Figure 1 shows a typical "H-bridge" motor drive circuit in which the winding current flow is bidirectional. N-Channel MOSFETs are invariably used in the lower legs of the bridge since they can be directly driven by the D469. In the upper legs of the bridge, both N and P-channel devices can be used. In each case, driving the upper MOSFETs presents a problem that is common to a number of applications other than motor drives. The problem is that the upper MOSFET switches which control the positive power supply to the load cannot have their gate-drive voltage referenced to ground.

When the P-channel MOSFETs are used as the upper switches, their source terminals are connected to the positive power rail. The gates of these MOSFETs are then driven 10 to 12 volts below the positive rail to turn them on. Because the gate drive is always referenced to the positive rail, the gates of the N and P-channel MOSFETs in each half of the bridge can be driven directly by the D469 if the power supply voltage is 14 V or less. Operation at higher supply voltages, however, requires that the P-channel devices be isolated in some fashion from the D469 which is ground referenced.

The isolation problem crops up again if N-channel MOSFETs are used as the upper switches in the bridge.



A Bipolar H-Bridge Motor Drive Circuit Using N and P-Channel MOSFETs.

Figure 1

APPLICATIONS (Cont.)

Since their source terminals are connected to the load, one can see that the gate waveform must swing to at least 10 or 12 volts above the positive rail if they are to turn on completely. Also, when either of the lower N-channel MOSFETs is conducting, the respective upper N-channel device must be off or cross-conduction will occur. To prevent this, the gate-to-source voltage of the upper MOSFET must be zero when the respective lower MOSFET is on and vice versa. This means that the gate-voltage of the upper N-channel devices must swing from the $R_{DS(on)}$ voltage drop of the lower MOSFETs all the way to 10 or 12 volts above the positive rail. Even with a 12 volt power supply, the gate voltage swing is almost 24 volts, and thus the D469 cannot be used to directly drive the upper MOSFETs. Again, some form of driver isolation is required.

There are many methods of providing isolation between the D469 and the gates of the upper MOSFETs when using elevated supply voltages. As may be expected, certain methods will work better with N-channel MOSFETs, and others will work better with P-channel devices.

Three methods of providing gate-drive isolation will be considered. Two of them provide DC isolation between the D469 and the gates of upper MOSFETs while the third provides isolation between a floating D469 and the control-logic inputs.

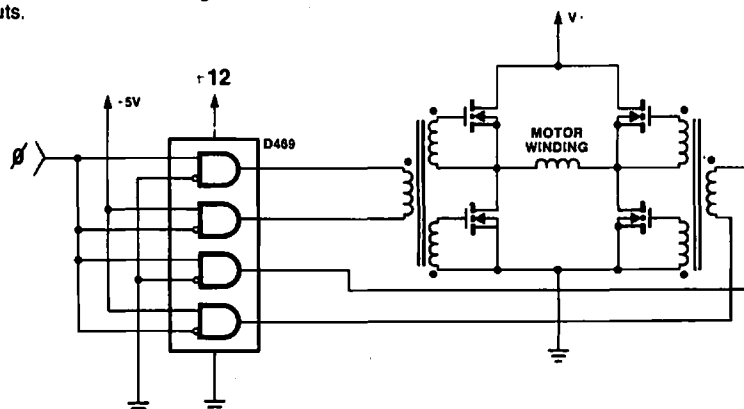
a. Transformer Isolated Gate Drive

Figure 2 shows an all N-channel H-bridge motor drive using transformer isolation between the D469 and the gates of both the upper and lower MOSFETs. Each transformer is driven by an AC waveform generated by two D469 driver channels.

In many cases the transformer will prove to be one of the most compact, least expensive and simplest methods of isolation to implement. It also works well with either N or P-channel MOSFETs in the upper half of the bridge.

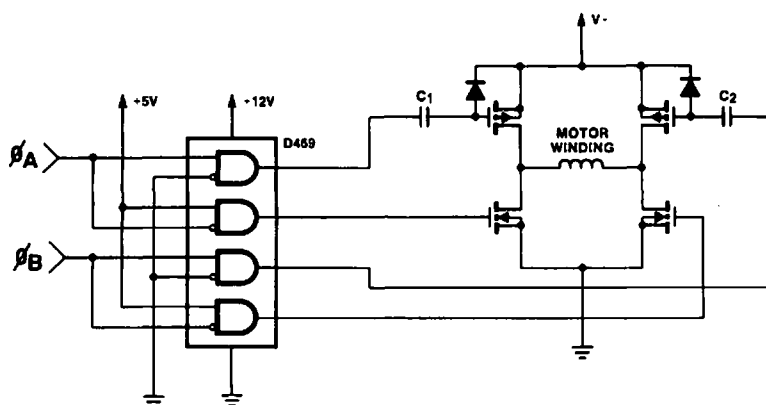
However, there is a drawback with this method. The interwinding capacitance of the isolation transformers allow noise spikes appearing at the MOSFET gates to be coupled back to the D469 and cause possible damage.

Care must be taken to ensure that any transients coupled back to the driver are of sufficiently low magnitude such that no damage is done. They can be minimized by the inclusion of a Faraday shield between the primary and secondary windings of the isolation transformer.



An All N-Channel H-Bridge Drive Using Transformer Isolation.

Figure 2



A H-Bridge Drive Using Capacitive Isolation For The P-Channel MOSFETs.

Figure 3

APPLICATIONS (Cont.)

b. Capacitor Isolated Gate Drive

A capacitor isolated N and P-channel H-bridge motor drive is shown in Figure 3. In this circuit, only the P-channel MOSFETs are isolated from the D469; the N-channel devices are driven directly. The diodes are included to clamp to positive gate-to-source transitions on the P-channel MOSFETs to +0.7 V.

This method of isolation is even more compact and less expensive than that using transformers. Although a coupling capacitor several times the effective input capacitance of the P-channel MOSFETs is required, it is still small and inexpensive. This method does have the drawback of coupling noise spikes appearing at the MOSFET gates back to the outputs of the D469. Also capacitor isolation does not work well with N-channel MOSFETs in the upper half of the bridge. This is because the sources of the upper N-channel MOSFETs are not connected to an AC ground (such as the positive supply rail). Thus, there is no fixed reference for the AC coupled signal on the MOSFET side of the capacitor.

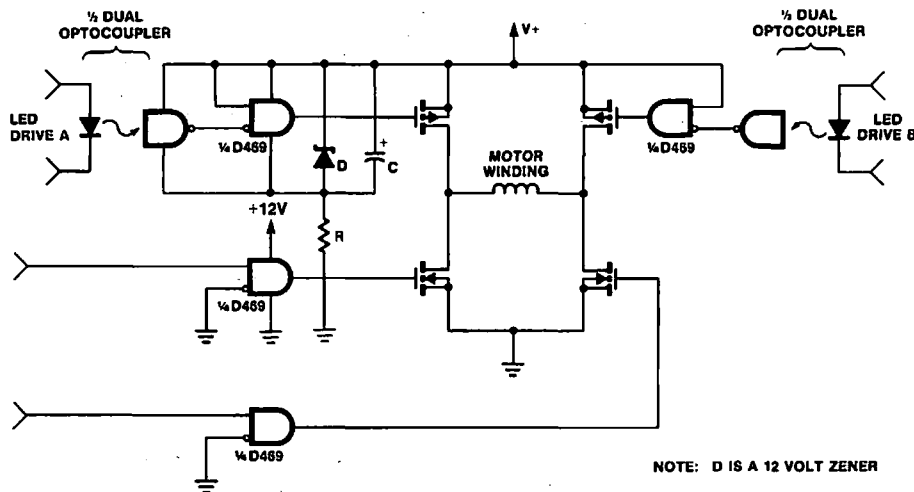
c. Floating D469 With Opto-Isolated Logic Inputs

Figure 4 shows a different method of providing isolation, namely referencing a D469 driver to the positive power rail and using an opto-coupler to provide the DC isolation between it and the low-voltage control logic. A -12 V

power supply, referenced to the positive rail, is generated for the D469's ground pin with a zener-diode, capacitor and resistor. The D469 thus provides gate-drive waveforms to the P-channel MOSFETs that swing from the positive rail to 12 volts below it. If the reservoir capacitor C is made large enough, it will be able to supply enough charge to the D469 for transfer to the gates of the MOSFETs. This ensures that upper MOSFETs will have fast switching times.

Although this circuit is more complex than the previous ones, DC operation of the motor coils is provided if so required. Since the upper D469 floats with respect to the positive power rail, any noise transients on this rail will not affect the operation of the driver or be coupled back to the logic inputs. This method has the disadvantage of being difficult to implement with an all N-channel bridge. The large voltage swing required at the gates of the upper N-channel devices precludes the use of the circuit in this case.

In summarizing this look at motor drive circuits using the D469 as a gate driver, one can see that if the correct methods of isolation are used then the D469 certainly simplifies the task of interfacing logic circuitry to a DC motor.



A Different Method Of Isolation: Floating A D469 Driver And Optically Coupling The Logic Drive For The P-Channel MOSFETs.

Figure 4

Si7250

Bubble Memory Power Driver

FEATURES

- TTL Compatible Inputs
- Transition Time <25 nS with 500pF Load
- Power Fail Reset
- Single Voltage Power Supply

BENEFITS

- Very Low Standby Power
- Easy to Interface
- Protection of Bubble Memories

APPLICATIONS

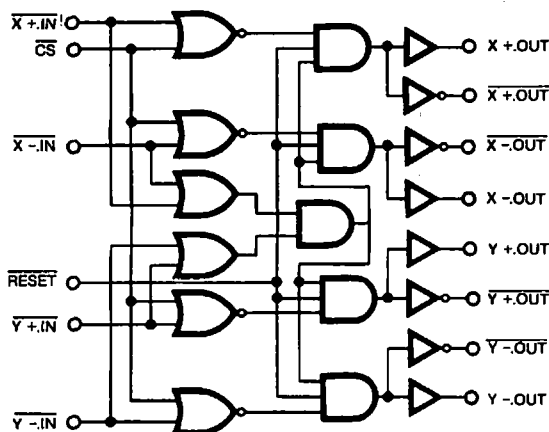
- Bubble Memory Coil Pre-Driver

DESCRIPTION

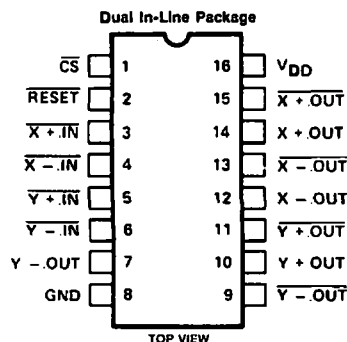
The Si7250 is a low power coil pre-driver for direct use with the Siliconix VQ7254 to drive magnetic bubble memory coils. The Si7250 has TTL compatible inputs and

complementary outputs designed to drive high capacitance, low on resistance MOSPOWER devices.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



Order Number: SI7250CK
See Package 10

ABSOLUTE MAXIMUM RATINGS

Ambient Temperature Under

Bias -20°C to +80°C

Storage Temperature -65°C to +150°C

Voltage on Any Pin with

Respect to Ground -0.5 to $V_{DD} + 0.5$ VSupply Voltage, V_{DD} -0.5 to +14 V

Output Current 250 mA

(One Output @ 100% Duty Cycle)

Maximum Operating Junction Temperature 150°C

 $\theta_{JC} = 25^\circ\text{C/W}$ $\theta_{JA} = 75^\circ\text{C/W}$ (No Airflow)

Operating Temperature 0 to 70°C

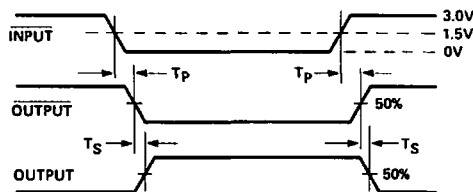
Storage Temperature -65 to 150°C

ELECTRICAL CHARACTERISTICS¹ T_A = Over Temperature Range

	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: $V_{DD} = 12\text{ V} \pm 10\%$	LIMITS			UNIT
				MIN ²	TYP ³	MAX	
INPUT	Input Current	$ I_{IN} $	$V_I = 0.8\text{ V}$			10	μA
	Low Level Input Voltage	V_{IL}				0.8	
	High Level Input Voltage	V_{IH}		2.2			
OUTPUT	Output Low Voltage	V_{OL1}	$I_{OL} = 200\text{ mA}$		1.45	2	V
	Output Low Voltage	V_{OL2}	$I_{OL} = 10\text{ mA}$		0.1	0.2	
	Output High Voltage	V_{OH1}	$I_{OH} = -200\text{ mA}$	$V_{DD} - 2$	$V_{DD} - 1.4$		
	Output High Voltage	V_{OH2}	$I_{OH} = -10\text{ mA}$	$V_{DD} - 0.2$	$V_{DD} - 0.1$		
	Output Sink Current	I_{OL}	$V_{OL} = 2.0\text{ V}$, 30% Duty Cycle	200			mA
	Output Source Current	$ I_{OH} $	$V_{OH} = V_{DD} - 2.0\text{ V}$, 30% Duty Cycle	200			
DYNAMIC	Propagation Delay from $\overline{X+IN}$, $\overline{X-IN}$, $\overline{Y+IN}$, $\overline{Y-IN}$	t_{p1}	500 pF Load		55	100	ns
	Propagation Delay from $\overline{CS}$ or RESET	t_{p2}	500 pF Load		90	150	
	Rise Time (10% to 90%)	t_r	500 pF Load		25	45	
	Fall Time (90% to 10%)	t_f	500 pF Load		25	45	
	Skew Between An Output And Its Complement	t_s	500 pF Load		10	20	
	Input Capacitance	C_{IN}				10	pF
SUPPLY	Supply Current	I_{DD0}	Chip Deselected: $\overline{CS} = V_{IH}$, $V_{DD} = 12.6\text{ V}$		1	4.5	mA
	Supply Current	I_{DD1}	$f = 100\text{ kHz}$, $V_{DD} = 12.6\text{ V}$, Output Unloaded			75	
	Supply Current	I_{DD2}	$f = 200\text{ kHz}$, $V_{DD} = 12.6\text{ V}$, Output Unloaded			90	

NOTES:

1. Refer to PROCESS OPTION FLOWCHART for additional information.
2. The algebraic convention whereby the most negative value is a minimum, and the most positive value is a maximum, is used in this data sheet.
3. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.



PIN DESCRIPTION

 $\overline{CS}$ (Pin 1)

Chip select is active low. When high, chip is deselected and I_{DD} is significantly reduced. Chip Select is most commonly used for system expansion.

RESET (Pin 2)

Active low input from $\overline{RESET.OUT}$ of the Controller results in removal of power from the chip so that bubble memory is protected in the event of power supply failure.

 $\overline{X+}.IN$, $\overline{X-}.IN$ (Pins 3, 4)

Active low inputs from controller which turn on the high current X outputs.

 $\overline{X-}.OUT$, $\overline{X-}.OUT$, $\overline{X+}.OUT$, $X+.OUT$ (Pins 12-15)

High current outputs and their complements for driving the gates of the 7254 QUAD MOSPOWER FETs which in turn drive the X coils of the bubble memory.

 $\overline{Y+}.IN$, $\overline{Y-}.IN$ (Pins 5, 6)

Active low inputs from controller which turn on the high current Y outputs.

 $\overline{Y-}.OUT$, $\overline{Y+}.OUT$, $\overline{Y+}.OUT$, $\overline{Y-}.OUT$ (Pins 9-11 and 7)

High current outputs and their complements for driving the gates of the 7254 QUAD MOSPOWER FETs which in turn drive the Y coils of the bubble memory.

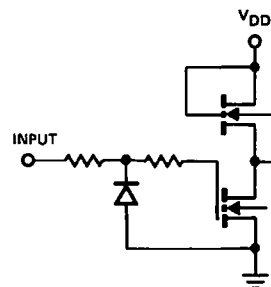
TRUTH TABLE

INPUT PINS						OUTPUT PINS							
1 CS	2 R	3 X ₊	4 X ₋	5 Y ₊	6 Y ₋	7 Y ₋	9 Y ₋	10 Y ₊	11 Y ₊	12 X ₋	13 X ₋	14 X ₊	15 X ₊
1	X	X	X	X	X	0	1	0	1	0	1	0	1
X	0	X	X	X	X	0	1	0	1	0	1	0	1
8 INPUT STATES DECODED													
0	1	0	1	0	1	0	1	1	0	0	1	1	0
0	1	0	1	1	0	1	0	0	1	0	1	1	0
0	1	0	1	1	1	0	1	0	1	0	1	1	0
0	1	1	0	0	1	0	1	1	0	1	0	0	1
0	1	1	0	1	0	1	0	0	1	1	0	0	1
0	1	1	0	1	1	0	1	0	1	1	0	0	1
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0	1	1	1	1	0	1	0	0	1	0	1	0	1

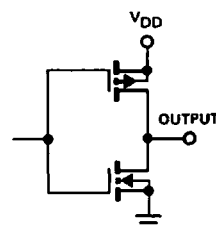
The 8 remaining input states are not decoded resulting in a reset output condition. This is to prevent the inadvertent shorting of any power drivers directly across the supplies in a standard bubble memory configuration

0	1	0	0	0	0	0	1	0	1	0	1	0	1
0	1	0	0	0	1	0	1	0	1	0	1	0	1
0	1	0	0	1	0	0	1	0	1	0	1	0	1
0	1	0	0	1	1	0	1	0	1	0	1	0	1
0	1	0	1	0	0	0	1	0	1	0	1	0	1
0	1	1	0	0	0	0	1	0	1	0	1	0	1
0	1	1	1	0	0	0	1	0	1	0	1	0	1
0	1	1	1	1	1	0	1	0	1	0	1	0	1

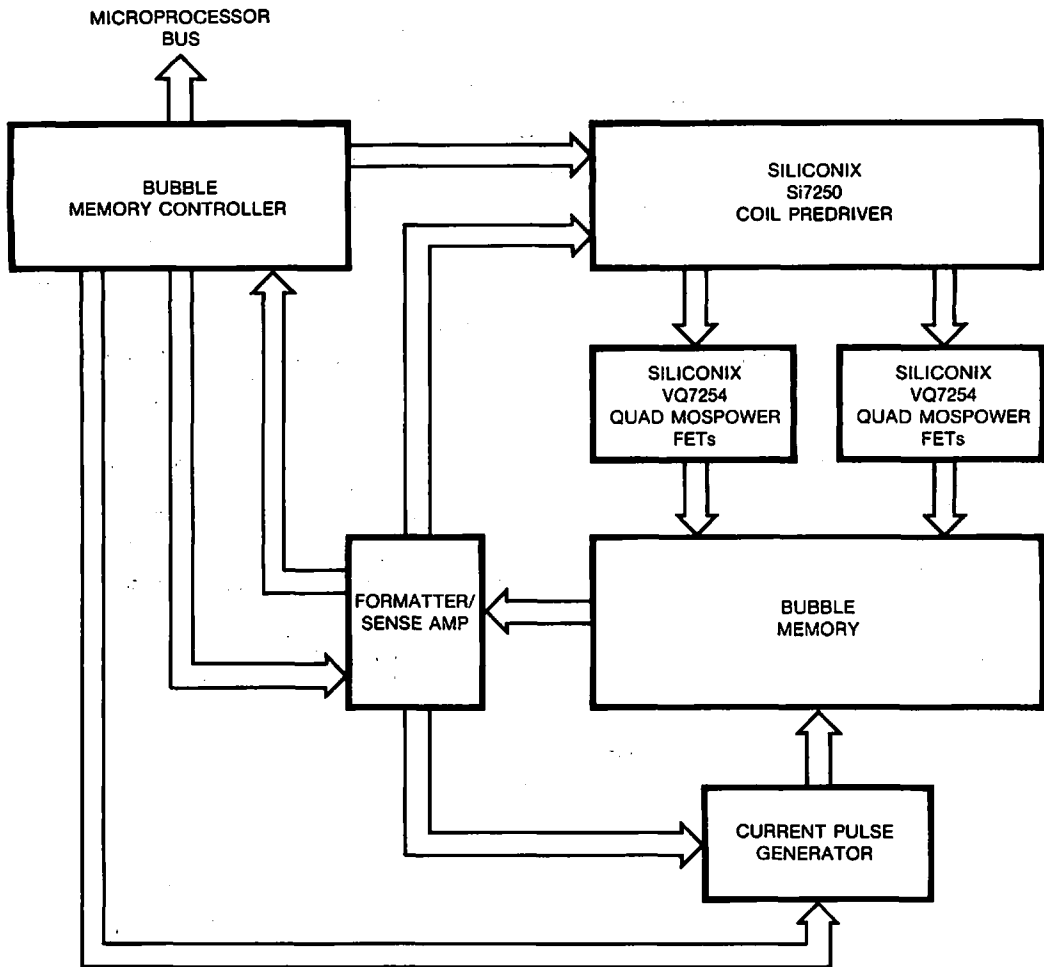
INPUT STRUCTURE



OUTPUT STRUCTURE



BLOCK DIAGRAM SINGLE BUBBLE MEMORY SYSTEM



DF412

Four Digit LCD Decoder Driver



FEATURES

- Decodes up to 4 7-segment BCD Digits
- Interfaces with Most Logic Families
- On Chip Oscillator
- Low Power Consumption —Typically 1.5 mW
- Digit Blanking with Input Code of 1111

BENEFITS

- Reduces Complexity
- Eliminates DC Bias Levels that Degrade Display Lifetime
- One External Component
- No Display Buffering Required

APPLICATIONS

- Driving Liquid Crystal Displays

DESCRIPTION

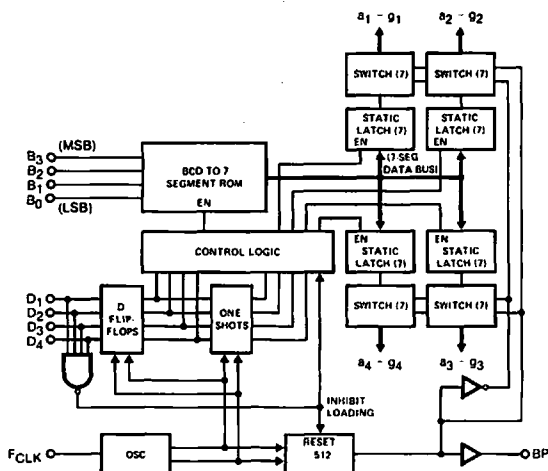
The DF412 Four Digit LCD Decoder Driver is a CMOS Monolithic device employing multiplexed BCD to LCD Decoding. A single DF412 contains all of the circuitry needed to decode up to 4 digits of multiplexed BCD information and derive the AC signals needed to directly drive a 4 digit LCD display. Included is the decoding of BCD input 1111 to blank a digit.

An internal oscillator, its frequency being controlled by an external capacitor, develops a backplane (BP) signal that is a square wave swinging between ground (V_{SS}) and the positive supply (V_{DD}). Segment drivers supply square waves of the same frequency as the backplane but either in phase for an OFF segment or out of phase for an ON seg-

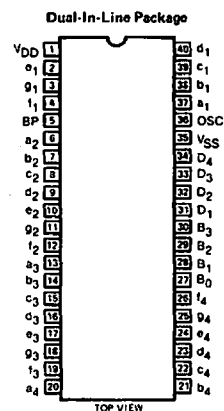
ment. In this manner of LCD digit driving the net DC potential applied between segment and backplane is zero, a necessary requirement for long display life. Digital input levels are defined as input voltages $> 4V$ being a logic "1" and input voltages $< 0.8V$ being a logic "0" with $V_{DD} = 5V$. BCD input data is decoded into 7 segment form using an on board ROM. The 7 segment data is then latched into the appropriate static latches via the digit strobe inputs and control logic.

The pinout of the DF412 allows easy PC board interfaces to Dual-In-Line LCDs as well as edge connecting types of displays.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



Order Number:
DF412CJ
See Package 22

ABSOLUTE MAXIMUM RATINGS

$V_{DD} - V_{SS}$ -0.3 V to 8 V
 Voltage on Any Pin $V_{SS} - 0.3$ V to $V_{DD} + 0.3$ V
 Current at Any Pin 10 mA
 Operating Temperature 0 to 70°C

Storage Temperature -65 to 125°C
 Power Dissipation (Package)* 450 mW
 *Device mounted with all leads welded or soldered to PC board. Derate 6.3 mW/°C above 25°C

ELECTRICAL CHARACTERISTICS¹ $T_A = 25^\circ\text{C}$

	PARAMETER		SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: $V_{DD} = 5$ V, $V_{SS} = 0$ V, $C_{OSC} = 200$ pF	LIMITS			UNIT
					MIN ²	TYP ³	MAX	
INPUT	Digital Input Leakage Current		I_{IN} (Digits)	$V_{IN} = 5$ V		0.01	1	μA
	Oscillator Input Current		I_{IN} (FCLK)	$V_{IN} = 0$ V		350		
	Digital Input Logic Low Voltage		V_{INL}	BCD And DS Inputs Clock Input			0.8 0.5	V
	Digital Input Logic High Voltage		V_{INH}	BCD And DS Inputs Clock Input	4 4.5			
OUTPUT	Segment Output Voltage In "0" State		V_{OL} (Segments)	$I_{OL} = 250 \mu\text{A}$ $I_{OL} = 25 \mu\text{A}$		0.3 0.03	0.7	V
	Segment Output Voltage In "1" State		V_{OH} (Segments)	$I_{OH} = -250 \mu\text{A}$ $I_{OH} = -25 \mu\text{A}$	4.3	4.7 4.97		
	Backplane Output Voltage In "0" State		V_{OL} (Backplane)	$I_{OL} = 5 \text{ mA}$ $I_{OL} = 0.5 \text{ mA}$		0.3 0.03	0.7	
	Backplane Output Voltage In "1" State		V_{OH} (Backplane)	$I_{OH} = -5 \text{ mA}$ $I_{OH} = -0.5 \text{ mA}$	4.3	4.7 4.97		
DYNAMIC	Segment Output Rise Time		t_r (Segments)	$C_{LOAD} = 200$ pF		1		μs
	Segment Output Fall Time		t_f (Segments)			1		
	Backplane Output Rise Time		t_r (Backplane)	$C_{LOAD} = 3900$ pF		0.8		
	Backplane Output Fall Time		t_f (Backplane)			0.8		
	Backplane Frequency	Min LCD	F _{BP1}	$C_{OSC} = 3800$ pF		30		Hz
		Max LCD	F _{BP2}	$C_{OSC} = 1000$ pF		100		
SUPPLY	Supply Current		I_{DD} (Digital Inputs Static)	See Figure 2		140	400	μA
	Supply Current		I_{DD} (Digital Inputs Dynamic)	See Figure 3		155		
	Operating Supply ⁴ Voltage		V_{DD} Range		3.5	5	6	V

NOTES:

1. Refer to PROCESS OPTION FLOWCHART for additional information.
2. The algebraic convention whereby the most negative value is a minimum, and the most positive value is a maximum, is used in this data sheet.
3. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
4. Operation over the supply voltage range is functionally tested. DC and AC parametric testing is performed only at specific test conditions.

DEFINITION OF TERMINOLOGY

Oscillator — A capacitor connected between the oscillator (OSC) and ground completes the integral clock generator. The frequency of the clock generator (f_{OSC}) is determined by the capacitance value and the V_{DD} voltage, as seen in Figure 4. For driving LCDs with a 30 Hz to 100 Hz backplane frequency range, the typical oscillator capacitor is 1000 pF to 3800 pF (for $V_{DD} = 5$ V). The oscillator pin can also be driven with an external clock whose output swings within 10% of V_{DD} and V_{SS} . This is useful when synchronization of more than one DF412 is necessary, such as when driving displays of more than 4 digits on a single backplane.

Backplane — The backplane of the liquid crystal display is driven by this pin whose output is a squarewave swinging between V_{DD} and V_{SS} . The frequency of the backplane signal is $f_{OSC}/512$. Most LCDs require backplane frequencies of between 30 Hz and 100 Hz. See Figure 4 for a graph of oscillator capacitance vs backplane frequency.

Digit Strokes D_1 - D_4 and BCD Inputs B_3 , B_2 , B_1 and B_0 — Multiplexed BCD information is entered into the DF412 by presenting the appropriate BCD code to the inputs B_3 , B_2 , B_1 and B_0 and by pulsing the appropriate digit strobe input D_1 , D_2 , D_3 or D_4 with positive true logic (i.e., $V_{INH} \geq [0.8 \times V_{DD}]$ for logic 1, $V_{INL} \leq 0.8$ V for logic 0). The minimum pulse width of a digit strobe should be not less than one period of the oscillator frequency. Information presented at the BCD inputs (B_3 , B_2 , B_1 , B_0) must be valid during the digit strobe pulse. See the timing requirements in Figure 1.

The digit strobe inputs are shaped by the input logic shown in Figure 8a. This logic causes a strobe signal which is a single clock period wide. The active time of this data load strobe (shown in Figure 8b) enables the BCD to 7-segment decoding ROM, which brings the new 7-segment data to the output latches. Delay time for data to get from BCD input to the segment outputs is typically 2 μ s-3 μ s. The end of the data load strobe is triggered by the second negative clock edge following the digit strobe going high. At this

edge, the segment outputs are latched, storing the 7-segment information for this digit. This input structure is the basis for the timing requirements of the DF412, shown in Figure 1.

The digit strobe input structure can actually load more than one digit at a time from the same BCD input. The loading of multiple digits can save time for microprocessor applications, such as for zeros, or blanks. However, all four digits cannot be simultaneously loaded due to a special decode of $D_1 \cdot D_2 \cdot D_3 \cdot D_4$ which causes a reset of the backplane divider and inhibits loading of the BCD data. Unused Digit Strokes should be tied to ground, to avoid them floating to a logic 1 condition which could cause an inadvertent reset condition. The reset condition stops the backplane square wave, putting the DF412 drive in a steady voltage state which would degrade the LCD for long term application.

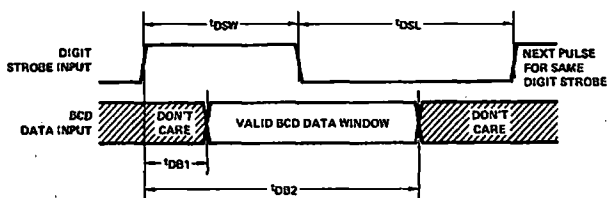
When ganging more than one DF412 together, it is necessary to synchronize the individual backplane signals to insure proper segment-backplane signal phase relationships. This is easily accomplished by initially pulling all digit strobe inputs high and by then driving the ganged DF412s with a common oscillator. By comparing the individual backplane signals of two DF412s with an exclusive or gate (see Figure 10) a continual checking of the backplane phase relationships can be accomplished. Should, for some reason, the individual backplane signals become out of phase an automatic reset will occur and proper phase once again will be established.

Segment Outputs — Segments are driven with the DF412 segment outputs which generate square waves which are either in phase with the backplane for an OFF segment or out of phase with the backplane for an ON segment. Output swings of the drivers are between V_{DD} and V_{SS} . Segment peak to peak voltages are then $2X(V_{DD} - V_{SS})$. The CMOS output drivers provide matched resistance to both V_{DD} and ground, eliminating any net DC voltage component on the LCD to give maximized display life.

TRUTH TABLE

B ₃	B ₂	B ₁	B ₀	DISPLAY CHARACTER
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	A
1	0	1	1	B
1	1	0	0	C
1	1	0	1	D
1	1	1	0	E
1	1	1	1	BLANK

TIMING WAVEFORMS AND DEFINITIONS



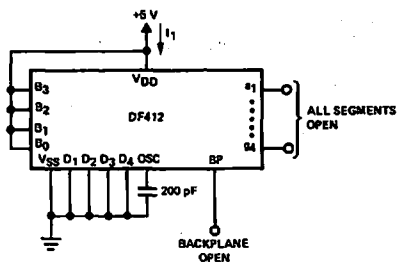
Recommended Drive Conditions*		Min	Max
t _{CP}	Clock Period	19.5 μs**	65 μs**
t _{DSW}	Digit Strobe Pulse Width	t _{CP} + 1 μs	—
t _{DSL}	Digit Strobe Low Time	2 t _{CP}	—
t _{DB1}	Digit Strobe to BCD Setup Time	—∞	t _{CP} - 2 μs
t _{DB2}	Digit Strobe to BCD Hold Time	2 t _{CP} + 2 μs	∞

* These minimum/maximum conditions indicate the necessary conditions to insure operation. They are based on design structure (shown in Figure 8a) with sufficient guardband to allow for propagation delay changes. They are not tested nor guaranteed.

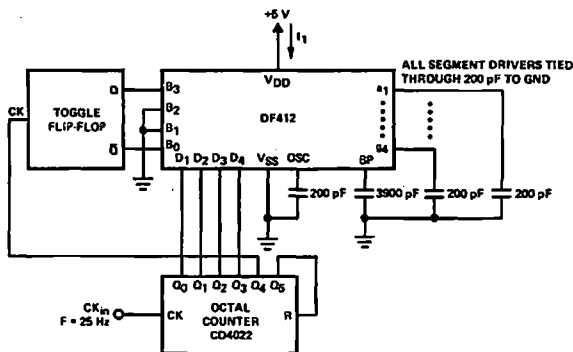
** The min-max clock periods correspond to a 30 Hz–100 Hz LCD backplane frequency range.

Figure 1

TEST CIRCUITS



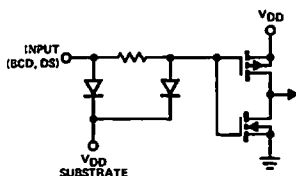
Static Supply Current Test Setup
Figure 2



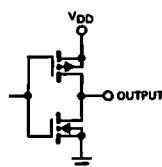
Dynamic Supply Current Test Setup
Figure 3

INPUT-OUTPUT SCHEMATICS

Input Structure



Output Structure



TYPICAL CHARACTERISTICS

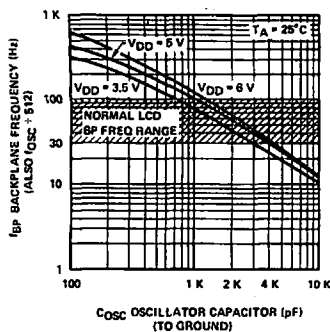
Backplane Frequency Vs.
COSC Vs. VDD

Figure 4

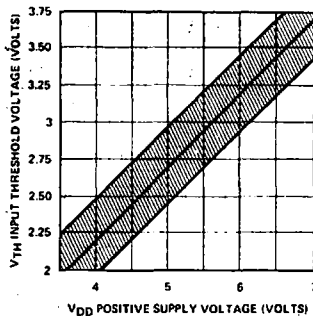
Input Threshold Vs.
Positive Supply Voltage

Figure 5

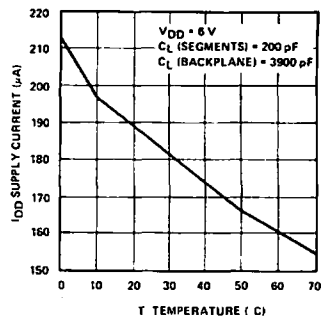
Supply Current Vs.
Temperature

Figure 6

TYPICAL WAVEFORMS

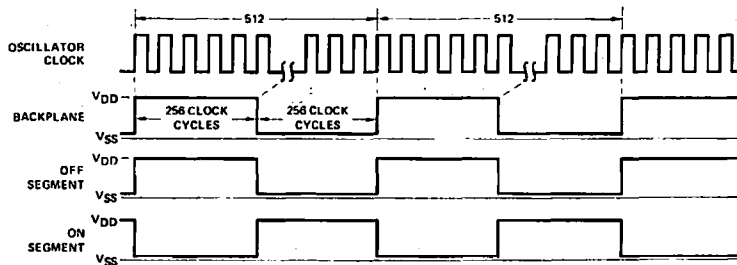
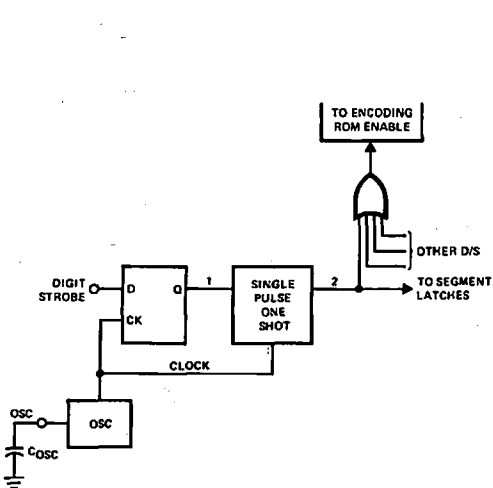
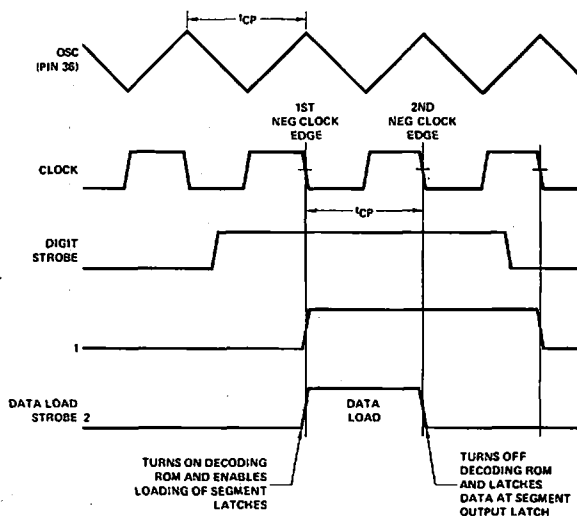
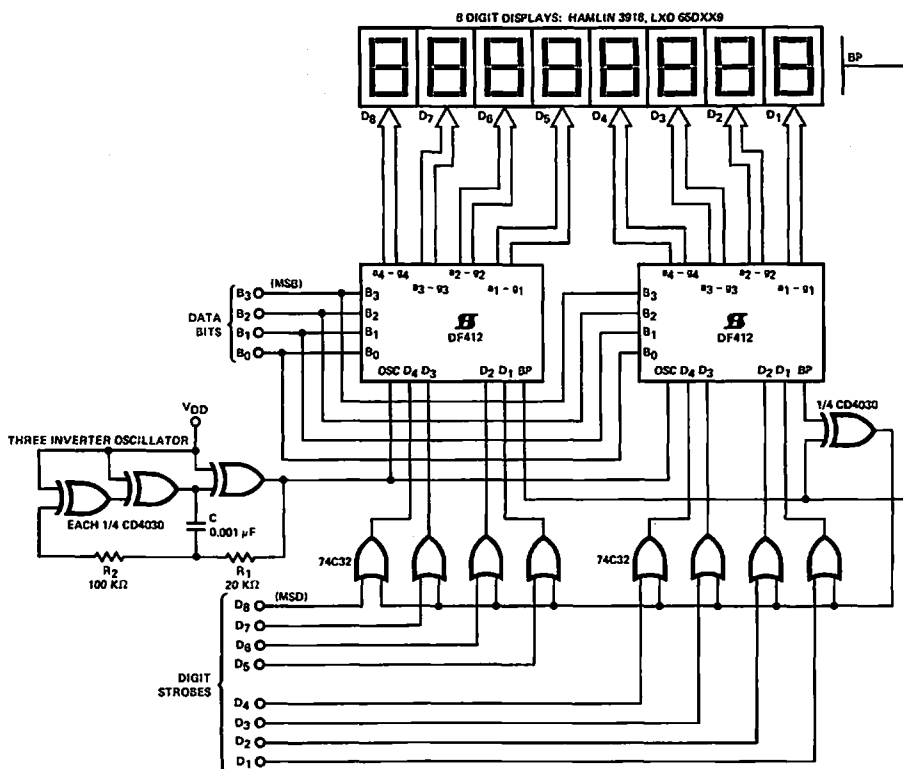


Figure 7

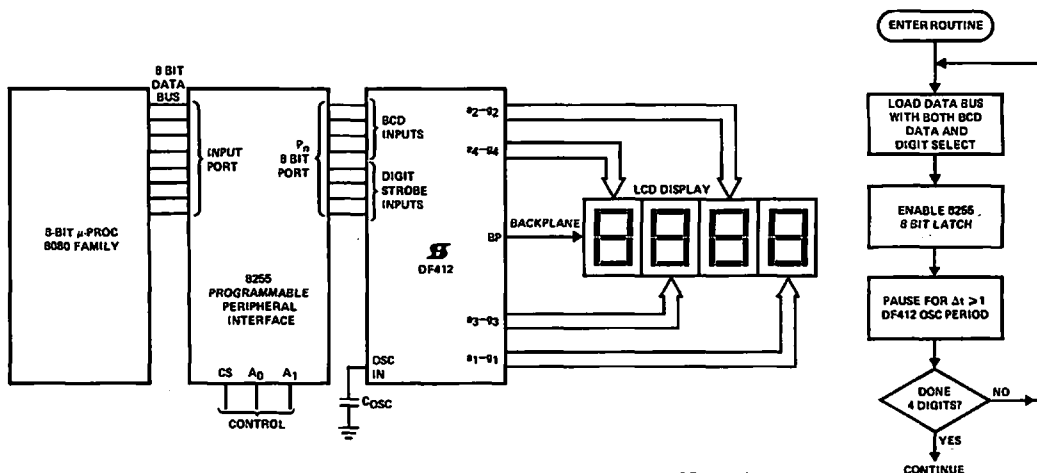
DIGIT STROBE INPUT STAGE

Digit Strobe Input Circuit
Figure 8aDigit Strobe And Clock Timing
Relationships To Data Loading
Figure 8b

APPLICATIONS

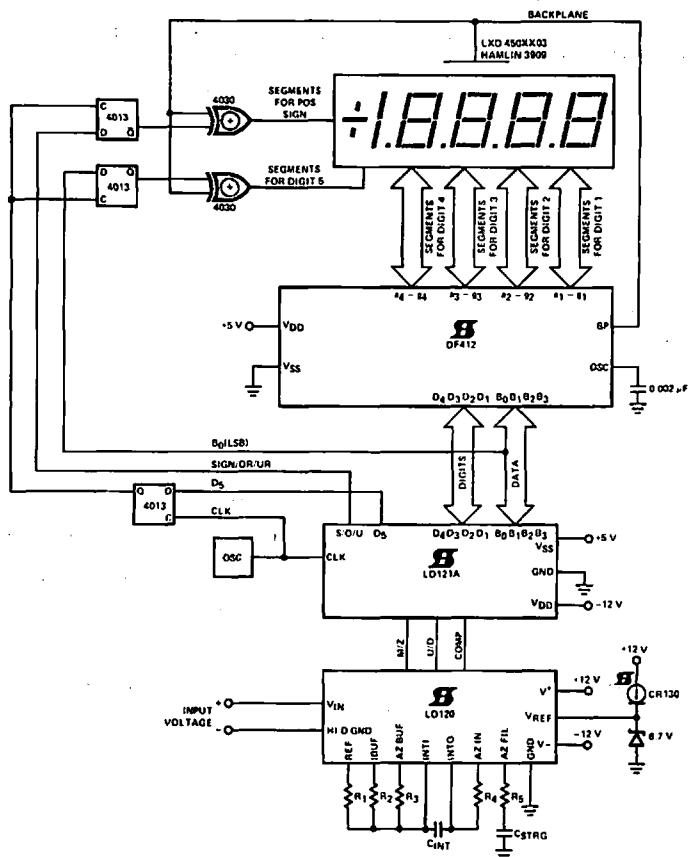


Ganged DF412's Drive 8 Digit LCD
Figure 9

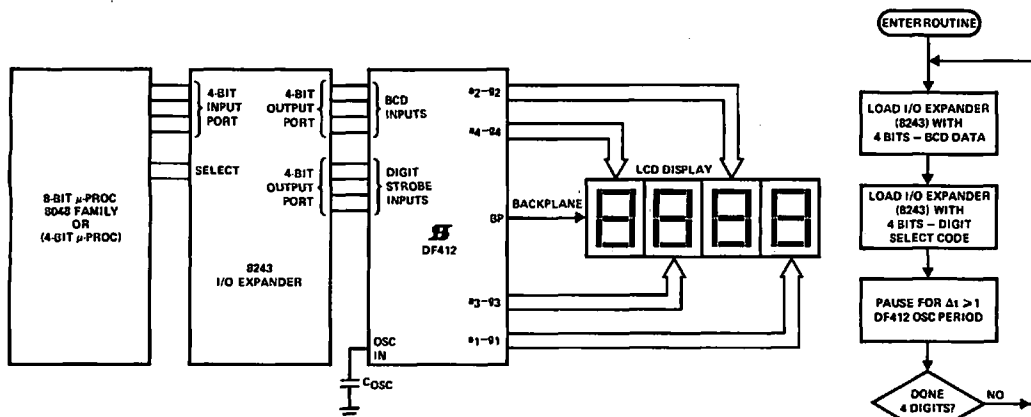


The DF412 Allows Simple Interface To The LCD Display From An 8080 Microprocessor. Data Transfer Is Made With An 8 Bit Dump, Bringing Both The BCD Input And The Digit Strobes To The Chip In Parallel.

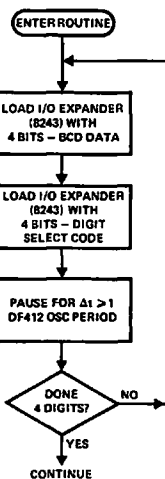
Figure 10



4 1/2 Digit LCD-DVM
Figure 11



Simple LCD Interface With 8048 Family Of Microprocessors.
Data Transfer Is Made With Two 4-Bit Ports, Loaded
With 4-Bit Dumps. Note In The Flow Chart That The BCD
Data Is Latched To The Expander First, Then The Digit Strobe
Is Sent Out. This Insures Proper Data Being Loaded In.
Figure 12





Si9551/Si9552 Electroluminescent Row Drivers

FEATURES

- 32 Channels Per Device
- 225 V, Open-Drain DMOS Outputs
- 50 mA Output Current Capability
- 32-Bit Shift Register
- CMOS Compatible Inputs

BENEFITS

- Reduces Board Space Required for Large X - Y Displays

APPLICATIONS

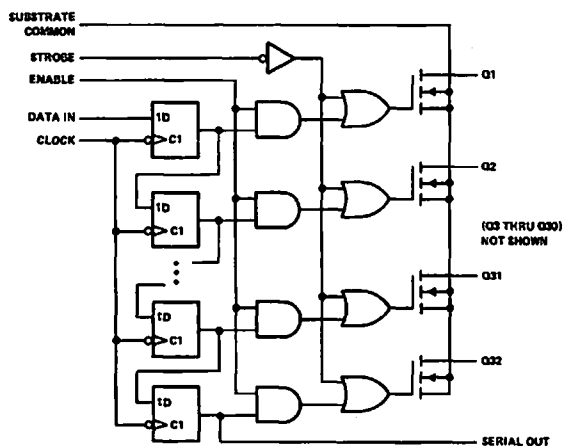
- EL Displays

DESCRIPTION

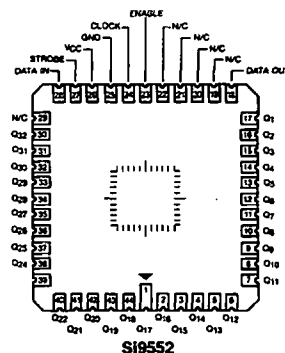
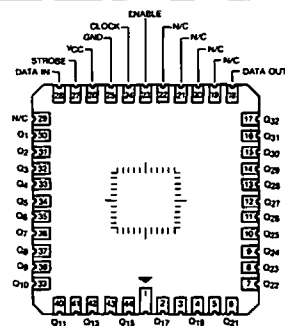
The Si9551 and Si9552 are monolithic D/CMOS integrated circuits designed to drive the row electrodes of electroluminescent displays. Each driver has 32-bit shift register and 32 high voltage outputs. The Si9551 channel pin out has been reversed from the Si9552 for circuit board

layout considerations. Although only preliminary data was available at publication, please contact the local Siliconix sales office or the factory for availability and further data on this part.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



Quad LCC Package

Si9553/Si9554 Electroluminescent Column Drivers



FEATURES

- 32 Channels Per Device
- 90 V, Totem-Pole Outputs
- 15 mA Output Source and Sink Current Capability
- High Speed Serial Data Input
- 32-Bit Latch

BENEFITS

- Reduces Board Space Required for Large X - Y Display

APPLICATIONS

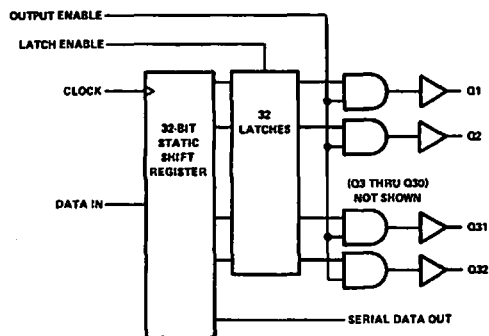
- EL Displays

DESCRIPTION

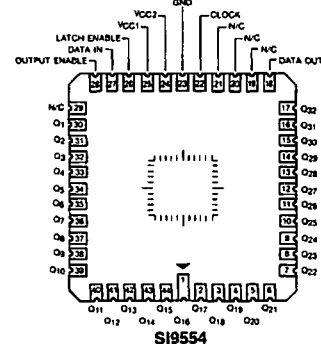
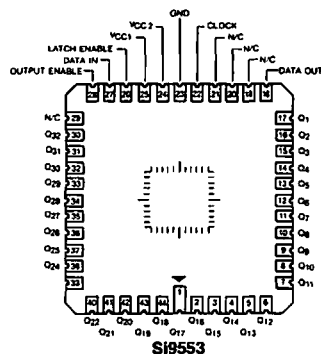
The Si9553 and Si9554 are monolithic D/CMOS integrated circuits designed to drive the column electrodes of electroluminescent displays. Each device has a 32-bit shift register,

32-bit latch, and 32 high voltage, totem-pole output drivers. The Si9553 channel pin out has been reversed from the Si9554 for circuit board layout considerations.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



Quad LCC Package

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ANALOG SWITCHES AND MULTIPLEXERS

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Analog Switch Selector Guide

SWITCHING SPEED ($t_{(on)}$ or $t_{(off)}$, WHICHEVER IS GREATER)

		10ns	75ns	150ns	200ns	250ns	300ns	550/600ns	750ns	1 μ s	1.5/1.6 μ s	2/2.5 μ s		
DRAIN TO SOURCE RESISTANCE: $r_{DS(on)}$	175 Ω							DG201A cO DG262 cO	DG172 pO	DG211 cO DG212 cO	Si3002 p sd	DG123 pO DG125 p●	175 Ω	DRAIN TO SOURCE RESISTANCE: $r_{DS(on)}$
	100 Ω				DG300A cO DG301 cO				Common Drain *(100-450 Ω)		*(100-400 Ω)	Common Drain *(100-450 Ω) 5 per Package	100 Ω	
	90 Ω							†DG221 c●					90 Ω	
	80 Ω to 70 Ω					DG182 j● DG188 jOds DG188 j sd DG191 j sd				DG200A c●	†DG126 jOds †DG134 jO †DG142 j dd †DG143 j sd	Radiation Resistant	80 Ω to 70 Ω	
	50 Ω	SD5000 dO SD5001 dO SD5002 dO *(19-50 Ω)	DG271 cO			DG304A cO DG305A c sd DG306A cOds DG307A c sd	DG300A cO DG301A c sd DG302A cOds DG303A c sd DG381A c● DG384A cOds DG387A c sd DG390A c sd			†DG243 c sd DG5040 cO DG5041 c● DG5042 c sd DG5043 c sd DG5044 cOds DG5045 cOds			50 Ω	
	30 Ω			DG181 j● DG184 jOds DG187 j sd DG190 j sd							†DG129 jOds †DG133 jO †DG139 j dd †DG144 j sd	Radiation Resistant	30 Ω	
	10 Ω						DG180 j● DG183 jOds DG186 j sd DG189 j sd						†DG140 jOds †DG141 jO †DG145 j dd †DG146 j sd	10 Ω
		10ns	75ns	150ns	200ns	250ns	300ns	550/600ns	750ns	1 μ s	1.5/1.6 μ s	2/2.5 μ s		

SWITCHING SPEED ($t_{(on)}$ or $t_{(off)}$, WHICHEVER IS GREATER)

Single (1 per Package)
Dual (2 per Package)
Quad (4 per Package)

c = Plus-40 CMOS Switch
d = DMOS Switch
j = N-JFET Switch
p = PMOS Switch

● = normally closed (logic 0 input)
O = normally open (logic 0 input)

sd = single pole, double throw
ds = double pole, single throw
dd = double pole, double throw
Others = single pole, single throw

* = $r_{DS(on)}$ is a function of drive voltage
† = Make-before-break (Others Break-before-make)
‡ = Latchable inputs

Analog Switch Product Selector Guide¹

Basic Part Number	Switch Type	$r_{DS(on)}$ Max. ² (Ω)	Analog Voltage Range ² (Vp-p)	Switching Time (μ s) t_{on} t_{off}	Logic Input for ON Switch	Logic Levels (V) V_{inL} V_{inH}	Supply Voltages $V+$ $V-$ V_L ³	Comments
One Channel SPST								
DG5040	CMOS Plus-40	50	30	1.0 0.5	1	0.8 2.0	15 -15 5	Latchable Inputs
DG5140 ⁴	CMOS Plus-40	30	30	0.2 0.125	1	0.8 2.0	15 -15 5	
DG5240 ⁴	CMOS Plus-40	30	30	0.2 0.125	1	0.8 2.0	15 -15 5	
Two Channel SPST								
DG133	N-JFET	30	20	0.6 1.6	1	0.8 2.5	12 -18 -	Use DG181 For New Design
DG134	N-JFET	80	20	0.6 1.6	1	0.8 2.5	12 -18 -	Use DG182 For New Design
DG141	N-JFET	10	20	1.0 2.5	1	0.8 2.5	12 -18 -	Use DG180 For New Design
DG180	N-JFET	10	20	0.3 0.25	0	0.8 2.0	10 -20 5	Break-Before-Make
DG181	N-JFET	10	15	0.3 0.25	0	0.8 2.0	15 -15 5	15V Supplies
		30	20	0.15 0.13	0	0.8 2.0	10 -20 5	Break-Before-Make
DG182	N-JFET	30	15	0.15 0.13	0	0.8 2.0	15 -15 5	15V Supplies
		75	20	0.25 0.13	0	0.8 2.0	10 -20 5	Break-Before-Make
DG200A	CMOS Plus-40	75	20	0.25 0.13	0	0.8 2.0	15 -15 5	15V Supplies
		70	30	1.0 0.5	0	0.8 2.4	15 -15 -	
DG300A	CMOS Plus-40	50	30	0.3 0.25	1	0.8 4.0	15 -15 -	
DG381A	CMOS Plus-40	50	30	0.3 0.25	0	0.8 4.0	15 -15 -	
DG304A	CMOS Plus-40	50	30	0.25 0.15	1	3.5 11.0	15 -15 -	CMOS compatible
DG5041	CMOS Plus-40	50	30	1.0 0.5	1	0.8 2.0	15 -15 5	Break-Before-Make
DG5141 ⁴	CMOS Plus-40	30	30	0.2 0.125	1	0.8 2.0	15 -15 5	
DG5241 ⁴	CMOS Plus-40	30	30	0.2 0.125	1	0.8 2.0	15 -15 5	Latchable Inputs
Four Channel SPST								
DG172	PMOS	150-450	20	0.3 0.75	0	0.8 2.0	10 -20 5	Latchable Inputs Fast (75 ns) Switch Single Supply Operation
DG201A	CMOS Plus-40	175	30	0.6 0.45	0	0.8 2.4	15 -15 -	
DG202	CMOS Plus-40	175	30	0.6 0.45	1	0.8 2.4	15 -15 -	
DG211	CMOS Plus-40	175	30	1.0 0.5	0	0.8 2.4	15 -15 5	
DG212	CMOS Plus-40	175	30	1.0 0.5	1	0.8 2.4	15 -15 5	
DG221	CMOS Plus-40	100	30				15 -15	
DG271 ⁴	CMOS Plus-40	50	30	0.05 0.04			15 -15	
DG308A	CMOS Plus-40	100	30	0.2 0.15	1	3.5 11.0	15 -15 -	
DG309	CMOS Plus-40	100	30	0.2 0.15	0	3.5 11.0	15 -15 -	
Five Channel SPST								
DG125	PMOS	100-450	20	0.3 2.0	0	0.5 4.6	10 -20 5	
One Channel SPDT								
DG143	N-JFET	80	20	0.8 1.6	Note 5	2.0 3.0	12 -18 -	Use DG188 For New Design
DG144	N-JFET	30	20	0.8 1.6	Note 5	2.0 3.0	12 -18 -	Use DG187 For New Design
DG146	N-JFET	10	20	1.0 2.5	Note 5	2.0 3.0	12 -18 -	Use DG186 For New Design
DG186	N-JFET	10	20	0.3 0.25	Note 6	0.8 2.0	10 -20 5	Break-Before-Make
DG187	N-JFET	10	15	0.3 0.25	Note 6	0.8 2.0	15 -15 5	15V Supplies
		30	20	0.15 0.13	Note 6	0.8 2.0	10 -20 5	Break-Before-Make
DG188	N-JFET	30	15	0.15 0.13	Note 6	0.8 2.0	15 -15 5	15V Supplies
		75	20	0.25 0.13	Note 6	0.8 2.0	10 -20 5	Break-Before-Make
DG301A	CMOS Plus-40	75	20	0.25 0.13	Note 6	0.8 2.0	15 -15 5	15V Supplies
		50	30	0.3 0.25	Note 6	0.8 4.0	15 -15 -	
DG387A	CMOS Plus-40	50	30	0.3 0.25	Note 6	0.8 4.0	15 -15 -	
DG305A	CMOS Plus-40	50	30	0.25 0.15	Note 6	3.5 11.0	15 -15 -	CMOS compatible
Si3002	PMOS	100-400	20	1.0 1.5	Note 6	0.8 2.0	10 -20 -	
DG5042	CMOS Plus-40	50	30	1.0 0.5	Note 6	0.8 2.0	156 -15 5	Break-Before-Make
DG5142 ⁴	CMOS Plus-40	30	30	0.2 0.125	Note 6	0.8 2.0	15 -15 5	
DG5242 ⁴	CMOS Plus-40	30	30	0.2 0.125	Note 6	0.8 2.0	15 -15 5	Latchable Inputs

Analog Switch Product Selector Guide¹

(Continued)

Basic Part Number	Switch Type	$r_{DS(on)}$ Max. ² (Ω)	Analog Voltage Range ² (Vp-p)	Switching Time (μ s) t_{on} t_{off}	Logic Input for ON Switch	Logic Levels (V) V_{inL} V_{inH}	Supply Voltages V^+ V^- V_L ³	Comments
Two Channel SPDT								
DG189	N-JFET	10	20	0.3 0.25	Note 6	0.8 2.0	10 -20 5	Break-Before-Make
		15	15	0.3 0.25	Note 6	0.8 2.0	15 -15 5	15V Supplies
DG190	N-JFET	30	20	0.15 0.13	Note 6	0.8 2.0	10 -20 5	Break-Before-Make
		30	15	0.15 0.13	Note 6	0.8 2.0	15 -15 5	15V Supplies
DG191	N-JFET	75	20	0.25 0.13	Note 6	0.8 2.0	10 -20 5	Break-Before-Make
		75	20	0.25 0.13	Note 6	0.8 2.0	15 -15 5	15V Supplies
DG243	CMOS Plus-40	50	30	1.0 0.5	Note 6	0.8 2.0	15 -15 5	Make-Before-Break
DG303A	CMOS Plus-40	50	30	0.3 0.25	Note 6	0.8 4.0	15 -15 -	
DG390A	CMOS Plus-40	50	30	0.3 0.25	Note 6	0.8 4.0	15 -15 -	
DG307A	CMOS Plus-40	50	30	0.25 0.15	Note 6	3.5 11.0	15 -15 -	CMOS compatible
DG5043	CMOS Plus-40	50	30	1.0 0.5	Note 6	0.8 2.0	15 -15 5	Break-Before-Make
DG5143 ⁴	CMOS Plus-40	30	30	0.2 0.125	Note 6	0.8 2.0	15 -15 5	
DG5243 ⁴	CMOS Plus-40	30	30	0.2 0.125	Note 6	0.8 2.0	15 -15 5	Latchable Inputs
One Channel DPST								
DG5044	CMOS Plus-40	50	30	1.0 0.5	Note 6	0.8 2.0	15 -15 5	Break-Before-Make
DG5144 ⁴	CMOS Plus-40	30	30	0.2 0.125	Note 6	0.8 2.0	15 -15 5	
DG5244 ⁴	CMOS Plus-40	30	30	0.2 0.125	Note 6	0.8 2.0	15 -15 5	Latchable Inputs
Two Channel DPST								
DG126	N-JFET	80	20	0.6 1.6	1	0.8 2.5	12 -18 -	See DG185 For New Design
DG129	N-JFET	30	20	0.6 1.6	1	0.8 2.5	12 -18 -	See DG184 For New Design
DG140	N-JFET	10	20	1.0 2.5	1	0.8 2.5	12 -18 -	See DG184 For New Design
DG183	N-JFET	10	20	0.3 0.25	1	0.8 2.0	10 -20 5	Break-Before-Make
		15	15	0.3 0.25	1	0.8 2.0	15 -15 5	15V Supplies
DG184	N-JFET	30	20	0.15 0.13	1	0.8 2.0	10 -20 5	Break-Before-Make
		30	15	0.15 0.13	1	0.8 2.0	15 -15 5	15V Supplies
DG185	N-JFET	75	20	0.25 0.13	1	0.8 2.0	10 -20 5	Break-Before-Make
		75	20	0.25 0.13	1	0.8 2.0	15 -15 5	15V Supplies
DG302A	CMOS Plus-40	50	30	0.3 0.25	1	0.8 4.0	15 -15 -	
DG384A	CMOS Plus-40	50	30	0.3 0.25	1	0.8 4.0	15 -15 -	
DG306A	CMOS Plus-40	50	30	0.25 0.15	1	3.5 11.0	15 -15 -	CMOS compatible
DG5045	CMOS Plus-40	50	30	1.0 0.5	1	0.8 2.0	15 -15 5	Break-Before-Make
DG5145 ⁴	CMOS Plus-40	30	30	0.2 0.125	1	0.8 2.0	15 -15 5	
DG5245 ⁴	CMOS Plus-40	30	30	0.2 0.125	1	0.8 2.0	15 -15 5	Latchable Inputs
One Channel DPDT								
DG139	N-JFET	30	20	0.8 1.6	Note 5	2.0 3.0	12 -18 -	See DG191 For New Design
DG142	N-JFET	80	20	0.8 1.6	Note 5	2.0 3.0	12 -18 -	See DG190 For New Design
DG145	N-JFET	10	20	1.0 2.5	Note 5	2.0 3.0	12 -18 -	See DG189 For New Design

Drivers for FET Switches¹

Basic Part Number	I N P U T S	O U T P U T S	Function	Input Logic for V _{OUTL}	V _{inL} (V)	V _{inH} (V)	Output Drive	t _{on} (ns)	t _{off} (ns)	Optimum Supply Voltage (V)			
										V+	V-	V _L ³	V _R ⁷
D125	6	6	Six separate Drivers	0	0.5	4.6	ON ---5 mA Sink OFF---30 V Block (Note 8)	500	1500	10	-20	5	-
D129	7	4	Four Channel (BV = 50V) Driver with Decode	1	0.7	2.2	ON ---10mA Sink OFF---50 V Block (Note 8)	300	1500	10	-20	5	0
D139	2	4	Two Channel (BV = 36V) Driver with Decode	(Note 6)	0	5	ON ---30 V @ 10mA	170	200	10	-20	5	0

Multiple FET Switches¹

Basic Part Number	S O U R C E S	D R A I N S	G A T E S	Switch Type	Pull-up On Gate	r _{DS(on)} Max.		BV _{DSS}	I _S (off) (nA)	V _{GS(th)}		Capacitances (pF)		
						V _S = 10V	V _S = -10V			Min.	Max.	C _{gs} (C _g)	C _{ds} (C _d)	C _{sb} (C _s)
G118	6	1	8	SP6T	No	100	450	-30	0.5	-1.5	-4.0	0.9	0.4	2
G119	6	2	3	DP3T	Yes	100	450	-30	0.5	-1.5	-4.0	1.8	0.4	2
SD5000	4	4	4	4 x SPST	No	50	-	20	10.0	0.1	2.0	(3.5)	(1.6)	(5)
SD5001	4	4	4	4 x SPST	No	50	-	10	10.0	0.1	2.0	(3.5)	(1.6)	(5)
SD5002	4	4	4	4 x SPST	No	50	-	15	10.0	0.1	2.0	(3.5)	(1.6)	(5)
SD5400	4	4	4	4 x SPST	No	50	-	20	10.0	0.1	2.0	(3.5)	(1.6)	(5)
SD5401	4	4	4	4 x SPST	No	50	-	10	10.0	0.1	2.0	(3.5)	(1.6)	(5)
SD5402	4	4	4	4 x SPST	No	50	-	15	10.0	0.1	2.0	(3.5)	(1.6)	(5)

Analog Multiplexer Selector Guide¹

Basic Part Number	Latched Inputs	r _{DS} (on) Max. (Ω)	I _D (off) (nA)	Analog Voltage Range (V)	Transition Time ⁹ (μs)	Logic Levels (V)		Supply Voltages	
						V _{inL}	V _{inH}	V+	V-
Eight Channel MUX + Enable									
DG501 ¹⁰	NO	150-250	8	±5	1.5	0.6	3.5	5	-20
DG503 ¹⁰	NO	150-800	8	±10	1.5	0.6	3.5	10	-20
DG508A	NO	400	10	+10/-15	1.0	0.8	2.4	15	-15
DG528	YES	400	10	±15	1.0	0.8	2.4	15	-15
DG568 ⁴	YES	50-500	120	±30	2.0	4.0	11.0	30	-30
SI3705	NO	150-400	8	±5	1.5	0.6	3.5	5	-20

Analog Multiplexer Selector Guide¹

(Continued)

Basic Part Number	Latched Inputs	$r_{DS(on)}$ Max. (Ω)	$I_D(off)$ (nA)	Analog Voltage Range (V)	Transition Time ⁹ (μs)	Logic Levels (V)		Supply Voltages	
						V_{inL}	V_{inH}	V+	V-
Sixteen Channel MUX + Enable									
DG506A	NO	400	10	± 15	1.0	0.8	2.4	15	-15
DG526	YES	400	10	± 15	1.0	0.8	2.4	15	-15
Four Channel Differential MUX									
DG509A	NO	400	10	± 15	1.0	0.8	2.4	15	-15
DG529	YES	400	10	± 15	1.0	0.8	2.4	15	-15
DG569 ⁴	YES	50-500	120	± 30	2.0	4.0	11.0	30	-30
Eight Channel Differential MUX + Enable									
DG507A	NO	400	5	± 15	1.0	0.8	2.4	15	-15
DG527	YES	400	5	± 15	1.0	0.8	2.4	15	-15

- NOTES:
1. Devices shown in **boldface** are recommended for new designs.
 2. For most products, the analog voltage range is a function of supply voltages. For PMOS or CMOS switches, $r_{DS(on)}$ is also a function of supply voltage and analog voltage. See individual data sheets for more details.
 3. Logic supply voltage required for TTL compatible inputs.
 4. Preliminary product. Specifications subject to change. Contact the factory on availability.
 5. Input reference voltage of 2.5V is required. See individual data sheets for more details.
 6. See data sheets for switch states of differential and multiple switches.
 7. Ground reference voltage.
 8. Device normally operates with output pullup resistor to 10V.
 9. The appropriate switching characteristic for multiplexers is $t_{TRANSITION}$, not t_{on} , t_{off} .
 10. Logic pullup resistors required.

INTRODUCTION

Siliconix is the world's leading supplier of precision solid-state analog switches and multiplexers. Employing state of the art CMOS, bipolar/PMOS, DMOS, and JFET technologies, the products shown in this section of the Integrated Circuits Data Book represent the broadest selection of industrial, military, and commercial grade parts to suit every application and environment.

The products in this section include all of the popular Siliconix "DG" series of single, dual, and quad analog switches, and single-ended and differential multiplexers. Also included are new products such as the SD5000 and SD5400 series video bandwidth switches, the 75 nanosecond, 50 ohm DG271, and the DG5140 and DG5240 series of low power/high speed analog switches.

Finally, Siliconix continues to expand the increasingly popular lines of U.S. MIL-M38510 QPL and European BS9000 approved parts which have been screened for use in military applications.

The following paragraphs discuss important selection criteria for analog switches and multiplexers. A detailed selector guide is included as well as a complete short form guide to make the job of selecting the correct part for a specific application easier.

FUNCTIONAL DESCRIPTION

One of the most common control elements in electrical circuitry is the simple ON-OFF switch. The switch has evolved over the years from the manually operated circuit breaker of the early experimenters to the multi-switch integrated circuits of today. However, the function of the switch has remained the same; to isolate or connect two sections of an electrical circuit. The ideal switch has the characteristics of zero ON resistance, infinite OFF resistance, and instantaneous turn-on and turn-off times. Although an analog switch is not perfect and can have many different parasitic elements (Figure 1), it can still be a very good approximation of the ideal switch. ON resistance [$r_{DS(on)}$] can be as low as 10 ohms, OFF isolation can be as high as 90 dB (at 1

MHz), and switching speeds can reach 75 ns for a CMOS part, while DMOS technology can attain speeds of around 1 ns.

The advantage that has led to the widespread use of FET analog switches over bipolar or diode switches is the absence of P-N junction offset voltages. Since the conducting channel is made up of only one (n or p) type of material, no offset voltage, and hence no distortion of the signal due to this, will be seen.

ANALOG SWITCH TYPES

Before discussing specific parameters of the Siliconix analog switch product line, a brief description and the prime differences between the four device families used in analog switches should be provided.

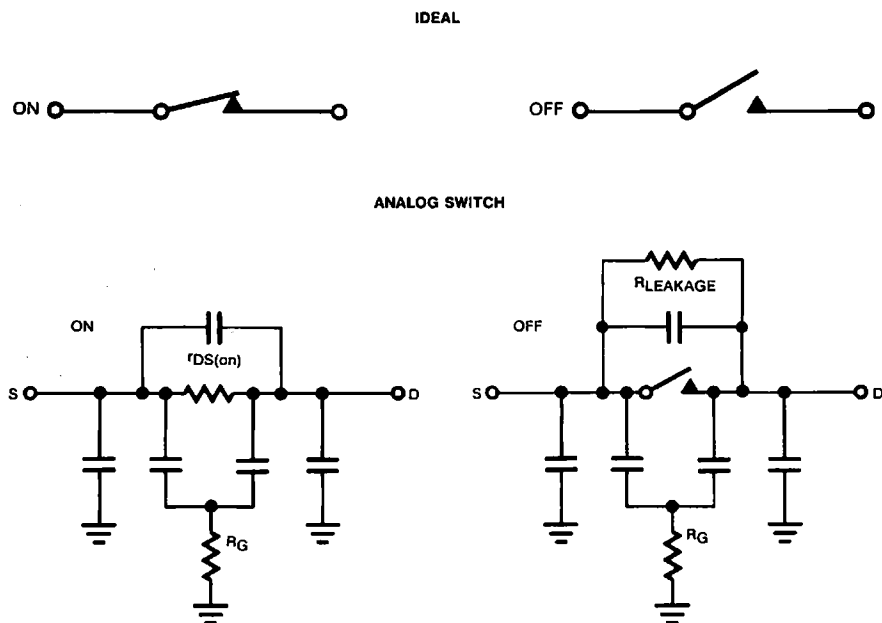
JFET

The n-channel JFETs used in analog switches such as the DG180 family are depletion mode devices. To maintain a depletion mode JFET switch in the ON state, the value of V_{GS} should be at or near zero. The switch is turned off by making V_{GS} more negative than 6 volts. When the switch is on, V_{GS} is maintained at zero by a floating gate drive circuit (for more information on driving a JFET switch, see AN73-5). This makes the ON resistance extremely constant over the entire analog signal range (see Figure 2).

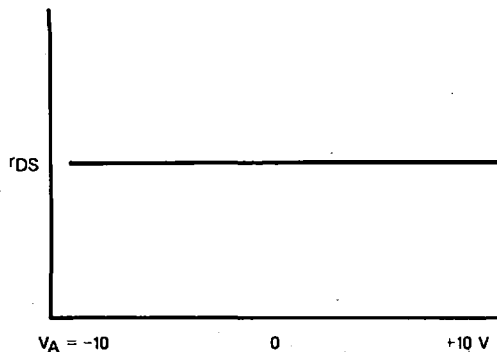
PMOS

To maintain a PMOS switch in the ON state, the gate is held at some reference voltage that ensures that V_{GS} exceeds the threshold voltage of the FET even when the analog signal is at the extremes of its range. However, since the $r_{DS(on)}$ of a MOSFET is a function of V_{GS} , the $r_{DS(on)}$ will vary with the analog signal voltage (see Figure 3).

The variation in ON resistance of the PMOS analog switch is a serious limitation in some applications since it can cause distortion of the analog signal. This effect can be minimized if the load resistance is high compared to the switch resistance.



Comparison of the "Ideal" Switch
to a Solid-State Analog Switch
Figure 1



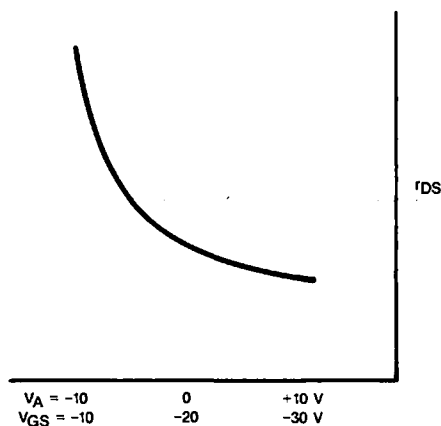
JFET "ON" Resistance
Figure 2

DMOS

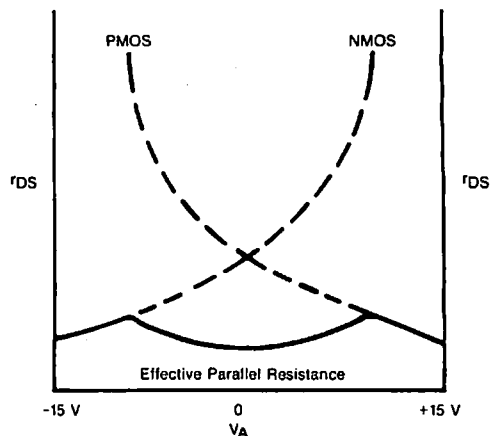
DMOS (Double diffused MOS) switches are n-channel (NMOS) enhancement mode devices capable of subnanosecond switching speeds due to their short channel length and lateral, as opposed to vertical, current flow. Lateral construction also allows low parasitic capacitances which makes DMOS switches ideal for broadband signals (>500 MHz). However, they suffer the same drawback of signal modulated ON resistance as the PMOS switches.

CMOS

Since CMOS analog switches are parallel combinations of p- and n-channel MOSFETs, the effective ON resistance of a CMOS switch is a combination of the PMOS and NMOS resistance curves (see Figure 4). This gives a fairly constant $r_{DS(on)}$ over the entire analog voltage range. The CMOS switch also has the advantage of very low quiescent supply current because other than for channel leakage, no current flows in the driver except when a control input transition occurs.



Variation of PMOS Switch Resistance
With Signal Voltage
Figure 3



Graph of CMOS Switch Resistance
vs. Analog Signal
Figure 4

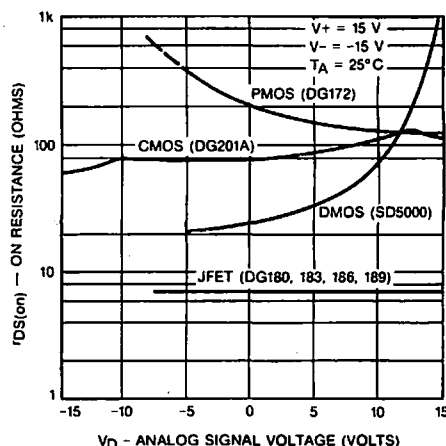
Figure 5 gives a comparison of the $r_{DS(on)}$ curves for a JFET (DG180), a PMOS (DG172), a DMOS (SD5000), and a CMOS (DG201A) analog switch.

IMPORTANT SWITCH PARAMETERS

Each switch family in the Siliconix product line has a set of distinct characteristics that make it suitable for certain types of applications. Several major specifications should be compared and prioritized before selecting an analog switch for a particular circuit.

$r_{DS(on)}$

This specification is simply the resistance of the channel when the analog switch is in the ON state. As explained earlier, however, the $r_{DS(on)}$ of a particular analog switch depends upon the device structure and analog signal size. Although the resistance may vary across the entire analog signal range, the worst case is usually specified on the data sheet.



Performance of FET Switches
Figure 5

Switching Speed

Switching speed is the elapsed time from the application of the control signal to the appearance (or disappearance) of the analog signal at the output. Switching speed can be greatly affected by the load on the analog switch. Each data sheet shows a switching time test circuit with a standard load for comparison.

Switch Current

The amount of current that can be fed through the switch channel is sometimes important. For example, the DG201A can handle up to 70 mA of pulsed current or 20 mA of continuous current, while the DG180 can pass up to 200 mA of continuous current.

Break-before-Make vs. Make-before-Break

For most analog switch applications, break-before-make switching is desired. This is the case because in most applications it is necessary to disconnect one signal source before connecting another to avoid source crosstalk. However, make-before-break switching is critical in some control circuits such as the feedback resistor gain selector for programmable gain op-amps, to avoid opening the loop.

Power Supplies and Power Consumption

There are many possibilities for powering a particular analog switch. Bipolar supplies are the most common, but single supply operation is possible. Each data sheet gives application hints on power supply range versus analog signal range.

Interfacing

This can be one of the most important parameters of an analog switch application since so many possibilities exist. The two most important interface criteria are logic compatibility and microprocessor compatibility.

The two most common logic levels are, of course, TTL and CMOS. Figure 6 shows the standard logic levels for both. Not all analog switches are compatible with both types of logic. Refer to the functional diagram section of each data sheet to determine the required logic levels. Note that the SD5000 and SD5400 switches have no driver circuit and therefore present a special interface problem. See AN83-15 for an example of driving the SD5000 as a video switch.

TTL	CMOS
Logic "0" $\leq 0.8V$	Logic "0" $\leq 1.5V$
Logic "1" $\geq 2.4V$	Logic "1" $\geq V_{CC} - 1.5V$

Logic levels for TTL and CMOS compatibility
Figure 6.

Microprocessor compatibility is a growing concern when designing with analog switches. Standard analog switches require a constant control signal present on the input to hold the switch in the desired position. This could tie up a microprocessor control system unless external latches are added to control the switch. The DG221 and DG5240 series have incorporated these latches, complete with control logic, onboard to minimize parts count and ease interface to microprocessor-based control systems.

MULTIPLEXING

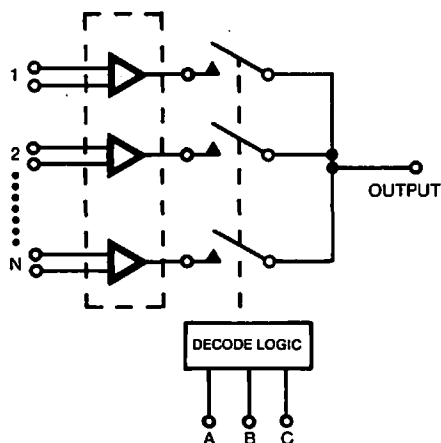
Multiplexers are a subset of analog switches which have many (4, 8, 16, or more) inputs with only 1 common output. They are used where it is necessary to transfer information from many signal

channels at a transmitting point to a central or common receiving point, or vice versa. This is most often used when only one transmission line is available for all data transfer between points. The signals to be transmitted may be in one of two forms: analog or digital. The multiplexers in this section are analog multiplexers that pass bipolar voltages or currents which are often obtained from transducers. The analog signals may represent any physical phenomenon such as temperature, pressure, velocity, speech, etc. Examples of this can be found in industrial process control, medical electronics, aircraft systems monitoring, telemetry, and communications.

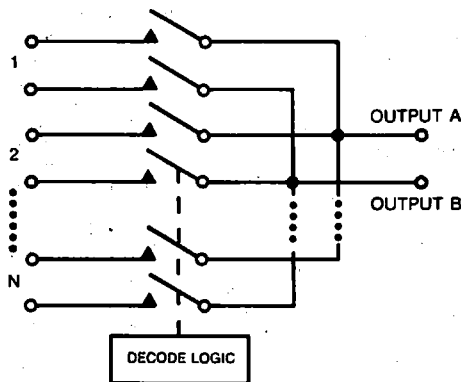
DIFFERENTIAL vs. SINGLE-ENDED MULTIPLEXING

When is it better to select a differential multiplexer versus a single-ended configuration? Figures 7 and 8 demonstrate these options. Single-ended multiplexing, as shown in Figure 7, applies to systems that have signal sources that are close to full-scale range and are referenced to a common point (usually ground). Another case is where differential signal sources with small signal amplitude (millivolt range) are generated by transducers. Instrumentation amplifiers can be used to provide a common reference for all of the signals and reduce feedthrough errors and losses while tailoring each signal source to a desired voltage (or current) to obtain the maximum resolution available in an A/D converter or other device driven by the multiplexer.

Differential multiplexing, as shown in Figure 8, is utilized when all signal sources are uniform or close to full-scale range and can tolerate switching transients or some mismatch without a significant degradation of the signal accuracy via the multiplexer. Major considerations are switch matching ($r_{DS(on)}$, $I_{D(off)}$, $I_{S(off)}$, and capacitance), common-mode rejection, and the system's tolerance to switching transients introduced by the break-before-make switching sequence.



Single-Ended Multiplexing
Figure 7



Differential Multiplexing
Figure 8

FACTORS AFFECTING SYSTEM PERFORMANCE

In any multiplexer application, the following factors should be considered:

- 1) **System Attenuation** — Includes loss in analog signal due to the multiplexing and demultiplexing devices and the transmission path. This is a frequency dependent factor.
- 2) **Channel Isolation** — At low frequencies, this is principally a function of channel OFF leakage currents, and at high frequencies, it is a function of device and system capacitances.
- 3) **Crosstalk** — There are several sources of crosstalk, the main ones being overlap between switching channels due to imperfect break-before-make switching, switch leakages, OFF switch capacitances, inter-switch capacitances, stray circuit capacitances, distortion in the transmission medium, etc.

4) **Noise** — There are several sources of noise, including thermal or Johnson noise generated in any resistive components, crosstalk, leakages, switching transients, as well as thermal EMFs and transmission path pickup.

5) **Switching Rate** — This is important in sampling systems where it determines the maximum analog signal handling frequency of the multiplexer (via the sampling theorem) and defines crosstalk errors.

SOME GENERAL COMMENTS

The Analog Switch Selector Guides in this section give listings of all of the standard switch and multiplexer products that Siliconix provides. The Short Form Selector Guide gives a matrix of $r_{DS(on)}$ vs. switching speed for analog switches to provide a quick approximation of which switches will be the most likely to work in your application. The long form allows comparison between switches and multiplexers in the same functional (SPST, DPST, 4 channel differential, etc.) category.

DG123

5-Channel SPST

PMOS Analog Switch



FEATURES

- Low Level Logic Control
- Low OFF Leakage
- Very Low Standby Power Requirements

BENEFITS

- Reduces External Components
- Reduces Switching Errors

APPLICATIONS

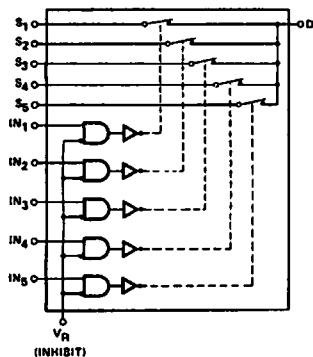
- Commutation Systems
- Feedback Switching for Op Amps
- Portable and Battery Operation

DESCRIPTION

The DG123 is a 5-channel single-pole, single-throw analog switch designed for low level logic controlled analog switching in instrumentation, process control, and communications systems. Featuring make-before-break action, the DG123 can be used inside closed loop systems to select one of five inputs for multiplexing/demultiplexing of analog signals, or for gain bandwidth control (by switching passive elements), without opening the loop. The reference pin (V_R) is normally connected to ground to allow a low-level input (0.4 V to 1.3 V) to control the

ON-OFF condition of each switch. In standby or OFF state, power consumption is less than 0.5 mW. The DG123 is a bi-directional MOS switch, rated to handle ± 10 V analog signals at up to 30 mA continuous current. Each switch will block 20 V peak-to-peak signals when OFF. Package options are the 14-pin ceramic DIP and flatpack. The former is characterized for operation over the standard industrial and military temperature ranges, while the latter is specified for the military range only.

FUNCTIONAL BLOCK DIAGRAM



One 5-Channel Switch Per Package*

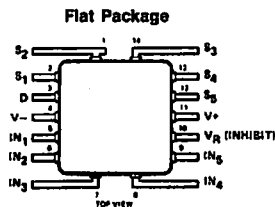
LOGIC	SWITCH
0	OFF
1	ON

Logic "0" ≤ 0.4 V

Logic "1" ≥ 1.3 V

*Switches Shown for Logic "1" Input

PIN CONFIGURATION

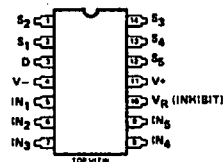


Order Number:

DG123AL

See Package 5

Dual-In-Line Package



Order Numbers:

DG123AP or DG123BP

See Package 11

ABSOLUTE MAXIMUM RATINGS

V+ to V-	36 V
V _D to V-	36 V
V _S to V-	36 V
V _D to V _S	25 V
V _S to V _D	25 V
V _R to V-	30 V
V _{IN} to V-	30 V
V _R to V _{IN}	6 V
V _{IN} to V _R	2 V
Current (Any Terminal)	30 mA

Storage Temperature	-65 to 150°C
Operating Temperature (A Suffix)	-55 to 125°C
(B Suffix)	-25 to 85°C
Power Dissipation (Package)*	
Flat Package**	750 mW
14 Pin DIP***	825 mW

*All leads soldered or welded to PC board.

**Derate 10 mW/°C above 75°C

***Derate 11 mW/°C above 75°C

ELECTRICAL CHARACTERISTICS¹

T_A = 25°C

	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: V+ = 10 V, V- = -20 V, V _R = 0		LIMITS						UNIT
					DG123A			DG123B			
					MIN ²	TYP ³	MAX	MIN ²	TYP ³	MAX	
SWITCH	Analog Signal Range	V _{ANALOG}			-10		10	-10		10	V
	Drain-Source ON Resistance	r _{DS(on)}	I _S = -1 mA I _{in} = 1 mA	V _D = 10 V V _D = 0 V _D = -10 V			100 200 450			125 225 500	Ω
	Source OFF Leakage Current	I _{S(off)}	V _S = -10 V, V _D = 10 V, V _{in} = 0.4 V	-1			-5				nA
	Drain OFF Leakage Current	I _{D(off)}	V _D = -10 V, V _S = 10 V, V _{in} = 0.4 V	-1			-10				
	Channel ON Leakage Current	I _{D(on)} + I _{S(on)}	V _D = V _S = 10 V, I _{in} = 1 mA			4			10		
	INPUT	Input Voltage, High	V _{INH}	I _{in} = 1 mA			1			1	V
Input Current with Input Voltage Low		I _{INL}	V _{in} = 0.4 V			1			5	μA	
DYNAMIC	Turn-ON Time	t _{on}	See Switching Time Test Circuit			0.3			0.5	μs	
	Turn-OFF Time	t _{off}				2			2		
	Source OFF Capacitance	C _{S(off)}	V _S = 0 V, I _D = 0, f = 1 MHz		5			5		pF	
	Drain OFF Capacitance	C _{D(off)}	V _D = 0 V, I _S = 0, f = 1 MHz		18			18			
	OFF Isolation		R _L = 100 Ω, C _L = 3 pF, f = 5 MHz		>-50			>-50		dB	
	Positive Supply Current	I+	One Channel ON I _{in} = 1 mA			3			3	mA	
Negative Supply Current	I-	-6				-6					
SUPPLY	Reference Supply Current	I _R		-0.5			-0.5				
	Positive Supply Current	I+	All Channels OFF V _{in} = 0.4 V			15			25	μA	
	Negative Supply Current	I-		-20			-40				
	Reference Supply Current	I _R		-10			-20				

T_A = Over Temperature Range

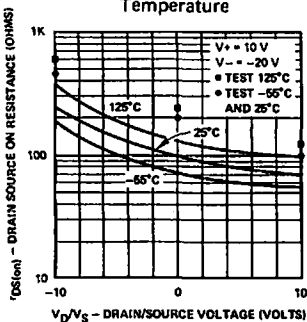
	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: V+ = 10 V, V- = -20 V, V _R = 0, V _L = 5 V		LIMITS						UNIT
					DG123A			DG123B			
					MIN ²	TYP ³	MAX	MIN ²	TYP ³	MAX	
SWITCH	Analog Signal Range	V _{ANALOG}			-10		10	-10		10	V
	Drain-Source ON Resistance	r _{DS(on)}	I _S = -1 mA I _{in} = 1 mA	V _D = 10 V		125				150	Ω
				V _D = 0		250			300		
				V _D = -10 V		600			600		
	Source OFF Leakage Current	I _{S(off)}	V _S = -10 V, V _D = 10 V, V _{in} = 0.4 V		-1000			-100			nA
	Drain OFF Leakage Current	I _{D(off)}	V _D = -10 V, V _S = 10 V, V _{in} = 0.4 V		-4000			-300			
Channel ON Leakage Current	I _{D(on)} + I _{S(on)}	V _D = V _S = 10 V, I _{in} = 1 mA				4000			300		
INPUT	Input Voltage, High	V _{INH}	I _{in} = 1 mA				1.3			1.3	V
	Input Current with Input Voltage Low	I _{INL}	V _{in} = 0.4 V				100			100	μA

NOTES:

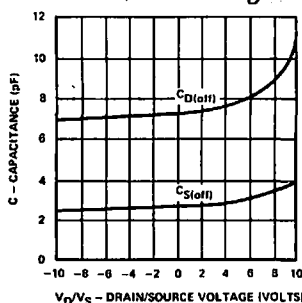
1. Refer to PROCESS OPTION FLOWCHART for additional information.
2. The algebraic convention whereby the most negative value is a minimum, and the most positive is a maximum, is used in this data sheet.
3. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

TYPICAL CHARACTERISTICS

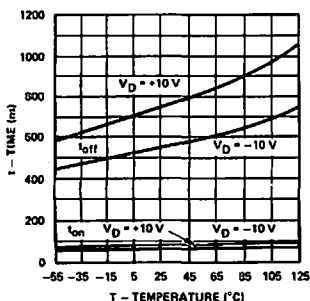
$r_{DS(on)}$ vs V_D and Temperature



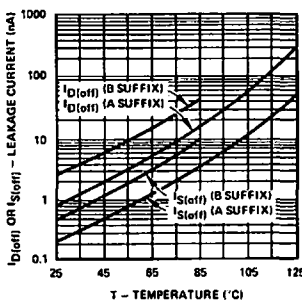
Capacitance vs V_D



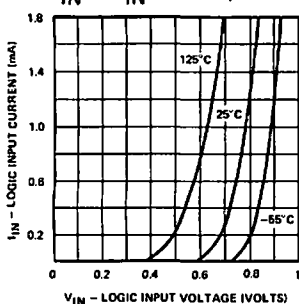
Switching Time vs V_D and Temperature



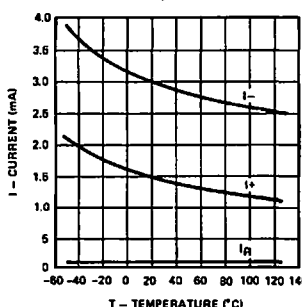
$I_D(off)$ / $I_S(off)$ vs Temperature



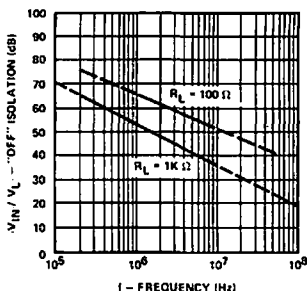
I_{IN} vs V_{IN} and Temperature



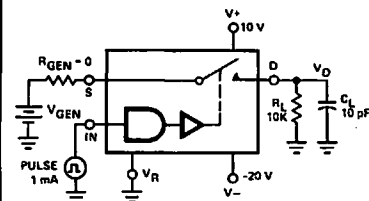
Supply Current vs Temperature



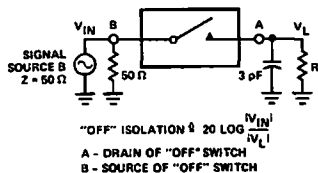
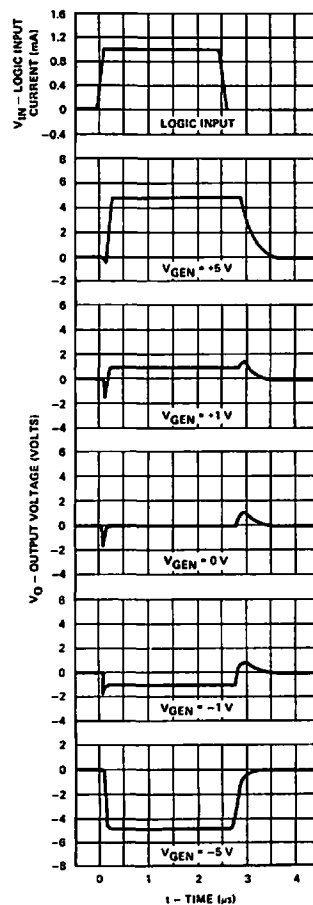
"OFF" Isolation vs R_L and Frequency



Typical delay, rise, fall, settling times, and switching transients in this circuit.



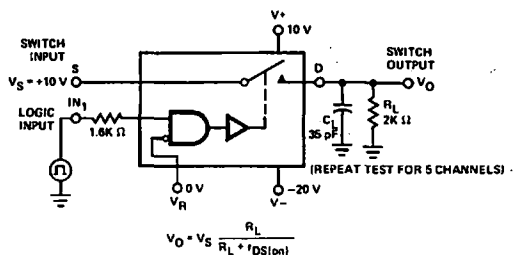
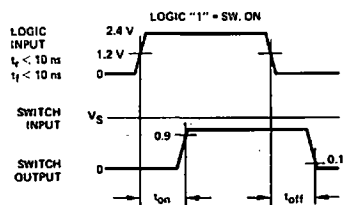
If R_{GEN} , R_L or C_L is increased, there will be proportional increases in rise and/or fall RC times.



"OFF" ISOLATION $\approx 20 \log \frac{V_{IN}}{V_L}$
A - DRAIN OF "OFF" SWITCH
B - SOURCE OF "OFF" SWITCH

SWITCHING TIME TEST CIRCUIT

Switch output waveform shown for $V_S = \text{constant}$ with logic input waveform as shown. Note that V_S may be + or - as per switching time test circuit. V_O is the steady state output with switch on. Feedthrough via gate capacitance may result in spikes at leading and trailing edge of output waveform.



DG125

5-Channel SPST

PMOS Analog Switch



FEATURES

- Internal Zener Diode Protection
- Low Standby Power Requirements
- Low OFF Leakage
- Low Level Logic Control

BENEFITS

- Reduces External Components
- Reduces Switching Errors

APPLICATIONS

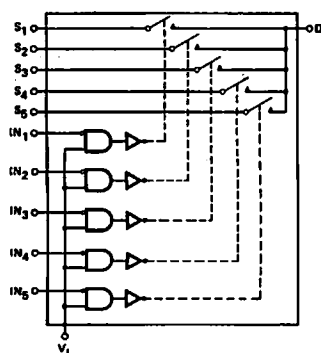
- Communication Systems
- Portable and Battery Operation
- Op Amp Switching
- Variable Gain Switching

DESCRIPTION

The DG125 is a 5-channel single-pole, single-throw analog switch designed for low level logic controlled analog switching in instrumentation, process control, and communications systems. Featuring make-before-break action, the DG125 can be used inside closed loop systems to select one of five inputs for multiplexing/demultiplexing of analog signals, or for gain bandwidth control (by switching passive elements), without opening the loop. The reference pin (V_R) is normally connected to ground to allow a low-level input (0.4 V to 1.3 V) to control the

ON-OFF condition of each switch. In standby or OFF state, power consumption is less than 0.5 mW. The DG125 is a bi-directional MOS switch, rated to handle ± 10 V analog signals at up to 30 mA continuous current. Each switch will block 20 V peak-to-peak signals when OFF. Package options are the 14-pin ceramic DIP and flatpack. The former is characterized for operation over the standard industrial and military temperature ranges, while the latter is specified for the military range only.

FUNCTIONAL BLOCK DIAGRAM



One 5-Channel Switch Per Package*

Truth Table

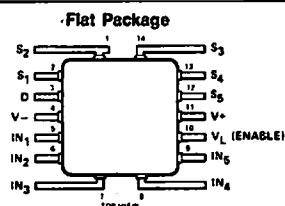
LOGIC	SWITCH
0	ON
1	OFF

Logic "0" ≤ 0.5 V

Logic "1" ≥ 4.1 V

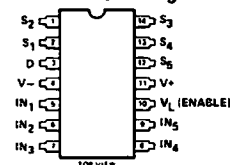
*Switches Shown for Logic "1" Input

PIN CONFIGURATION



Order Number:
DG125AL
See Package 5

Dual-In-Line Package



Order Numbers:
DG125AP or DG125BP
See Package 11

ABSOLUTE MAXIMUM RATINGS

V ₊ to V ₋	36 V
V _D to V ₋	36 V
V _S to V ₋	36 V
V _D to V _S	25 V
V _S to V _D	25 V
V _L to V ₋	30 V
V _{IN} to V ₋	30 V
V _L to V _{IN}	6 V
Current (Any Terminal)	30 mA
Storage Temperature	-65 to 150°C

Operating Temperature (A Suffix)	-55 to 125°C
(B Suffix)	-25 to 85°C
Power Dissipation (Package)*	
Flat Package**	750 mW
14 Pin DIP***	825 mW

*All leads soldered or welded to PC board.

**Derate 10 mW/°C above 75°C

***Derate 11 mW/°C above 75°C

ELECTRICAL CHARACTERISTICS¹

T_A = 25°C

	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: V ₊ = 10 V, V ₋ = -20 V, V _L = 4.5 V	LIMITS						UNIT	
				DG125A			DG125B				
				MIN ²	TYP ³	MAX	MIN ²	TYP ³	MAX		
SWITCH	Analog Signal Range	V _{ANALOG}		-10		10	-10		10	V	
	Drain-Source ON Resistance	r _{DS(on)}	I _S = -1 mA, V _{in} = 0.5 V		V _D = 10 V	65	100		70	125	Ω
			V _D = 0		95	200		100	225		
			V _D = -10 V		260	450		270	500		
	Source OFF Leakage Current	I _{S(off)}	V _S = -10 V, V _D = 10 V, V _{in} = 4.1 V	-1	-0.02		-5	-0.02		nA	
Drain OFF Leakage Current	I _{D(off)}	V _D = -10 V, V _S = 10 V, V _{in} = 4.1 V	-1	-0.7		-10	-0.7				
Channel ON Leakage Current	I _{D(on)} + I _{S(on)}	V _D = 10 V, V _{in} = 0.5 V, I _S = 0		-0.003	4		-0.003	10			
INPUT	Input Current with Input Voltage High	I _{INH}	V _{in} = 4.1 V	-1	0.006	1	-10	0.006	10	μA	
	Input Current with Input Voltage Low	I _{INL}	V _{in} = 0.5 V	-0.7	-0.8		-1	-0.8		mA	
DYNAMIC	Turn-ON Time	t _{on}	See Switching Time Test Circuit		0.1	0.3		0.1	0.5	μs	
	Turn-OFF Time	t _{off}			0.65	2		0.65	2		
	Source OFF Capacitance	C _{S(off)}	V _S = 0 V, I _D = 0, f = 1 MHz		3			3		pF	
	Drain OFF Capacitance	C _{D(off)}	V _D = 0 V, I _S = 0, f = 1 MHz		7			7			
	OFF Isolation		R _L = 100 Ω, C _L = 3 pF, f = 5 MHz		>-50			>-50		dB	
SUPPLY	Positive Supply Current	I ₊	One Channel ON V _{in} = 0.5 V		1.4	3			3	mA	
	Negative Supply Current	I ₋		-6	-2.4		-6	-2.4			
	Logic Supply Current	I _L			1.15	3		1.15	3		
	Positive Supply Current	I ₊	All Channels OFF V _{in} = 4.1 V		0.1	15		0.1	25	μA	
	Negative Supply Current	I ₋		-20	-0.02		-40	-0.02			
	Logic Supply Current	I _L			0.04	20		0.04	20		

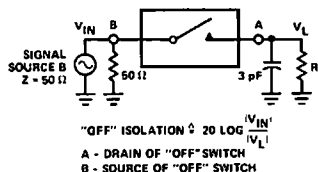
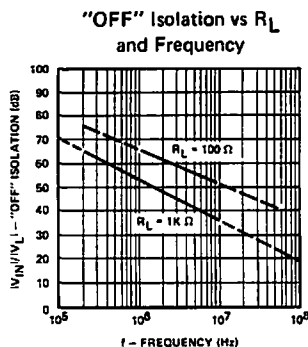
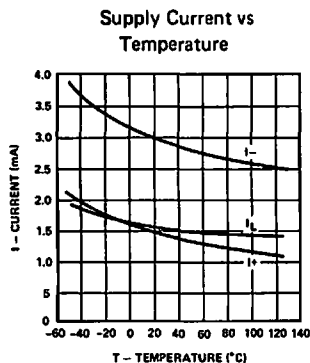
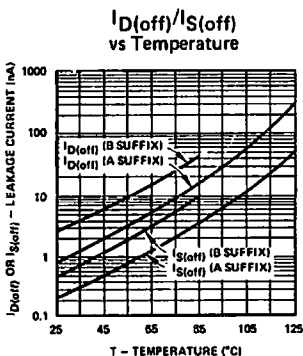
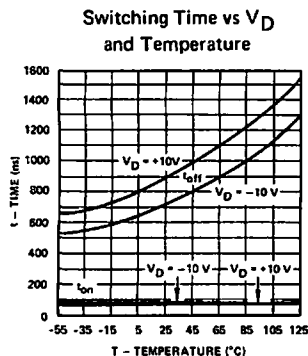
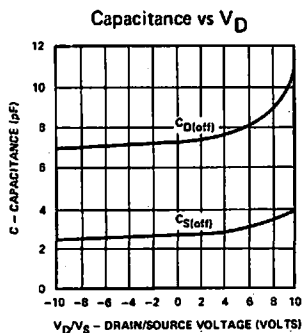
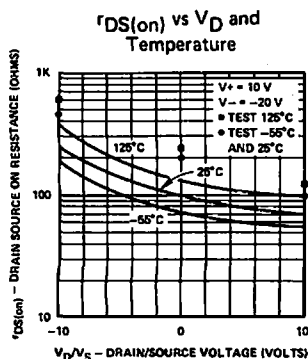
T_A = Over Temperature Range

	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: V ₊ = 10 V, V ₋ = -20 V, V _R = 0, V _L = 5 V		LIMITS						UNIT
					DG125A			DG125B			
					MIN ²	TYP ³	MAX	MIN ²	TYP ³	MAX	
SWITCH	Analog Signal Range	V _{ANALOG}			-10		10	-10		10	V
	Drain-Source ON Resistance	r _{DS(on)}	I _S = -1 mA, V _{in} = 0.5 V	V _D = 10 V			125			150	Ω
				V _D = 0			250			300	
				V _D = -10 V			600			600	
	Source OFF Leakage Current	I _{S(off)}	V _S = -10 V, V _D = 10 V, V _{in} = 4.1 V		-1000			-100			nA
	Drain OFF Leakage Current	I _{D(off)}	V _D = -10 V, V _S = 10 V, V _{in} = 4.1 V		-4000			-300			
Channel ON Leakage Current	I _{D(on)} + I _{S(on)}	V _D = 10 V, V _{in} = 0.5 V, I _S = 0				4000			300		
INPUT	Input Current with Input Voltage High	I _{INH}	V _{in} = 4.1 V		-10		10	-10		10	μA
	Input Current with Input Voltage Low	I _{INL}	V _{in} = 0.5 V		-0.7				-1		mA

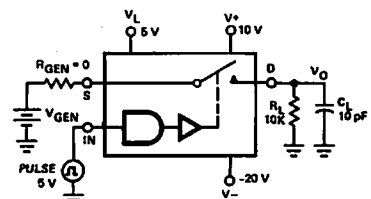
NOTES:

1. Refer to PROCESS OPTION FLOWCHART for additional information.
2. The algebraic convention whereby the most negative value is a minimum, and the most positive is a maximum, is used in this data sheet.
3. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

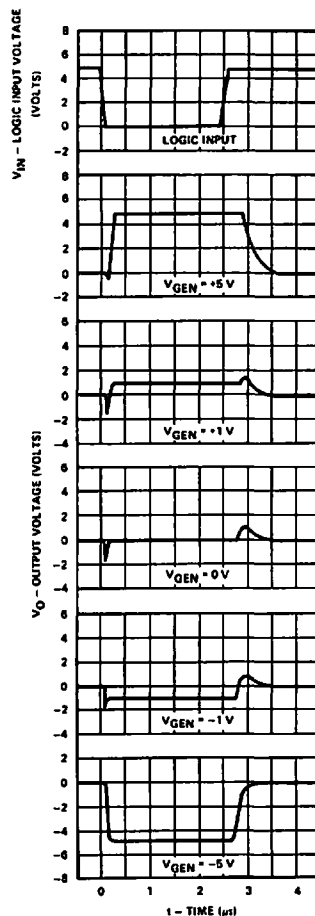
TYPICAL CHARACTERISTICS



Typical delay, rise, fall, settling times, and switching transient in this circuit.



If R_{GEN} , R_L or C_L is increased, there will be proportional increases in rise and/or fall RC times.



APPLICATION HINTS

V+ Positive Supply Voltage (V)	V- Negative Supply Voltage (V)	V _L Logic Supply Voltage (V)	V _{in} Logic Input Voltage V _{INH} Min/ V _{INL} Max (V)	V _S or V _D Analog Voltage Range (V)
10	-20	4.5	4.1/0.5	-10 to 10
15	-15	4.5	4.1/0.5	-5 to 15
20	-10	4.5	4.1/0.5	0 to 20

DG126/DG129/DG140

Dual DPST JFET

Analog Switches



FEATURES

- $<1 \mu\text{W}$ Standby Power
- Bipolar Drivers
- Constant $r_{DS(on)}$ Over Signal Range
- OFF Isolation $>60 \text{ dB}$

BENEFITS

- Minimizes Standby Power Requirements
- Better Radiation Tolerance than CMOS
- Less Distortion than CMOS
- Higher Frequency Switching

APPLICATIONS

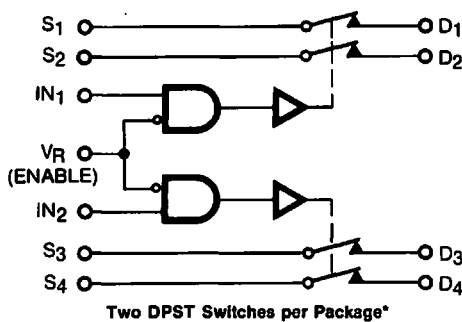
- Portable and Battery Powered Systems
- Switching in Satellite Applications
- Low Distortion Circuits
- High Frequency Switching Circuits

DESCRIPTION

The DG126, DG129, and DG140 are dual double-pole, single-throw analog switches for use in instrumentation, process control, and audio communication systems. Each contain four junction-type field-effect transistors (JFETs) to achieve constant on resistance across their rated analog signal range. Level-shifting drivers enable low-level inputs (0.8 to 2.5 V) to control the ON-OFF state of each switch. With a positive logic "0" at the driver input the switches will be OFF. With a positive logic "1" at the input the switches will be ON. In the ON state each switch will con-

duct current in either direction, and in the OFF state each switch will block voltages up to 20 peak-to-peak. ON resistance of the DG126 is $<80 \Omega$, the DG129 $<30 \Omega$ and the DG140 $<10 \Omega$, and ON shunt leakage for all three is $<2 \text{ nA}$. With both drivers in the "switch OFF" state total power consumption is $<750 \mu\text{W}$. Switches have Make-Before-Break action and due to the processing are relatively Radiation tolerant. An enable pin (V_R) simplifies interfacing with microprocessor, or other command function logic. Package options are the 14 pin side braze and flat pack.

FUNCTIONAL BLOCK DIAGRAM



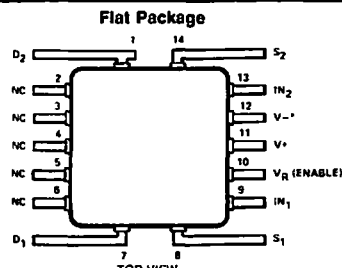
Truth Table

LOGIC	SWITCH
0	OFF
1	ON

Logic "0" $\leq 0.8 \text{ V}$
Logic "1" $\geq 2.5 \text{ V}$

*Switches Shown for Logic "1" Input

PIN CONFIGURATION

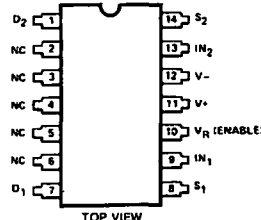


Order Numbers:

DG126AL, DG129AL,
DG140AL

See Package 5

Dual-In-Line Package



Order Numbers:

DG126AP, DG126BP,
DG129AP, DG129BP

See Package 11

ABSOLUTE MAXIMUM RATINGS

V+ to V-	36 V
V+ to V _D	36 V
V _D or V _S to V-	36 V
V _D to V _S	±22 V
V+ to V _R	25 V
V _R to V-	25 V
V _{in} to V-	30 V
V+ to V _{in}	25 V
V _{in} to V _R	±6 V
Current (Any Terminal)	30 mA

Storage Temperature	-65 to 150°C
Operating Temperature (A Suffix)	-55 to 125°C
(B Suffix)	-25 to 85°C
Power Dissipation*	
Flat Package**	750 mW
14 Pin DIP***	825 mW

*All leads welded or soldered to PC board

**Derate 10 mW/°C above 75°C

***Derate 11 mW/°C above 75°C

ELECTRICAL CHARACTERISTICS¹

T_A = 25°C

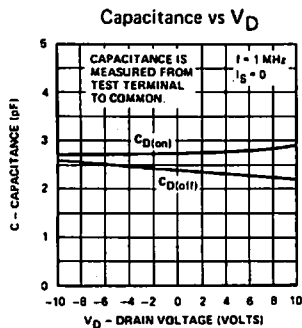
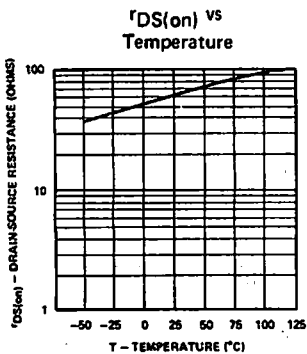
	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: V+ = 12 V, V- = -18 V, V _R = 0	LIMITS						UNIT
				DG126A			DG126B			
				MIN ²	TYP ³	MAX	MIN ²	TYP ³	MAX	
SWITCH	Analog Signal Range	V _{ANALOG}		-10		10	-8		8	V
	Drain-Source ON Resistance	r _{DS(on)}	I _S = -10 mA V _{in} = 2.5 V		20	80				Ω
			V _D = 10 V							
			V _D = 8 V				25	100		
	Source OFF Leakage Current ⁴	I _{S(off)}	V _{in} = 0.8 V		0.01	1				nA
			V _S = 10 V, V _D = -10 V							
INPUT										
	Drain OFF Leakage Current ⁴	I _{D(off)}	V _{in} = 0.8 V		0.005	1		0.05	5	nA
DYNAMIC	Channel ON Leakage Current ⁴	I _{D(on)} + I _{S(on)}	V _{in} = 2.5 V	-2	-0.02			0.025	5	nA
SUPPLY	Input Current With Input Voltage High	I _{INH}	V _{in} = 2.5 V		10	60		20	100	μA
	Input Current With Input Voltage Low	I _{INL}	V _{in} = 0.8 V		0.001	0.1		0.004	4	μA
	Turn-ON Time	t _{on}	See Switching Time Test Circuit		0.3	0.6		0.4	1	μs
	Turn-OFF Time	t _{off}			1.2	1.6		1.3	2	μs
	Source OFF Capacitance	C _{S(off)}	f = 1 MHz		2.4			2.4		pF
	Drain OFF Capacitance	C _{D(off)}	V _S = 0, I _D = 0. V _D = 0, I _S = 0.		2.4			2.4		pF
SUPPLY	Channel OFF Capacitance	C _D + S _(on)	V _D = V _S = 0.		2.8			2.8		pF
	OFF Isolation	OIRR	R _L = 75 Ω, 1 MHz		>60dB			>60dB		dB
	Positive Supply Current	I+	One Channel ON V _{in} = 2.5 V		2.1	3.0		2.1	3.3	mA
	Negative Supply Current	I-		-1.8	-1.15		-2.0	-1.2		mA
	Reference Supply Current	I _R		-1.4	-1.0		-1.5	-1.0		mA
	Positive Supply Current	I+	All Channels OFF Both V _{in} = 0		0.1	25		0.1	25	μA
Negative Supply Current	I-	-25		-0.5		-25	-0.5		μA	
Reference Supply Current	I _R	-25		0		-25			μA	

T_A = Over Temperature Range

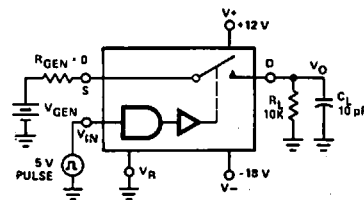
	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: V+ = 12 V, V- = -18 V, V _R = 0	LIMITS						UNIT	
				DG126A			DG126B				
				MIN ²	TYP ³	MAX	MIN ²	TYP ³	MAX		
SWITCH	Analog Signal Range	V _{ANALOG}		-10		10	-8		8	V	
	Drain-Source ON Resistance	r _{DS(on)}	I _S = -10 mA V _{in} = 2.5 V			150			150	Ω	
	Source OFF Leakage Current ⁴	I _{S(off)}	V _{in} = 0.8 V			100				nA	
			V _S = 10 V, V _D = -10 V						100		
			V _S = 8 V, V _D = -8 V						100		
			V _D = 10 V, V _S = -10 V			100					
Drain OFF Leakage Current ⁴	I _{D(off)}				100			100			
			V _D = 8 V, V _S = -8 V						100		
	Channel ON Leakage Current ⁴	I _{D(on)} + I _{S(on)}	V _{in} = 2.5 V			V _D = V _S = -10 V -100					
									V _D = V _S = -8 V		
INPUT	Input Current With Input Voltage High	I _{INH}	V _{in} = 2.5 V			120			150	μA	
	Input Current With Input Voltage Low	I _{INL}	V _{in} = 0.8 V			2			4		

NOTES:

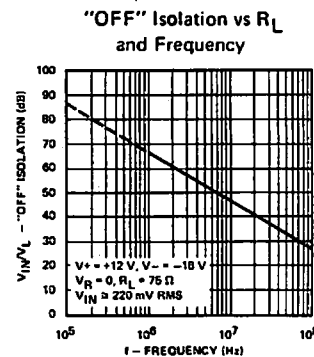
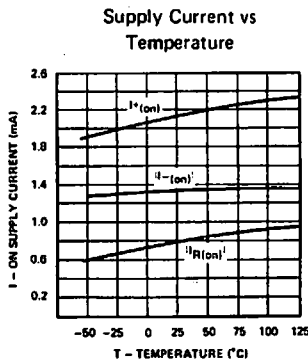
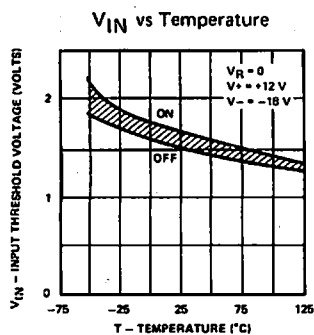
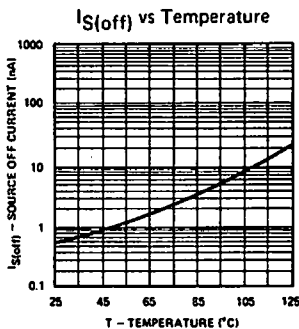
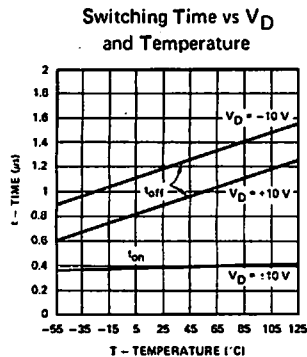
1. Refer to PROCESS OPTION FLOWCHART for additional information.
2. The algebraic convention whereby the most negative value is a minimum, and the most positive is a maximum, is used in this data sheet.
3. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
4. V_{in} must be a step function with a minimum rise and fall time of 1 V/μs.



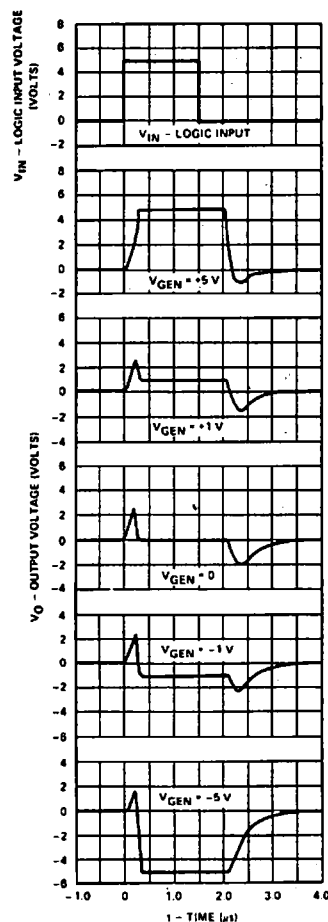
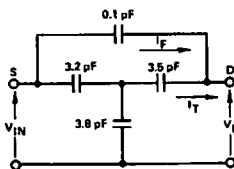
Typical delay, rise, fall, settling times, and switching transients in this circuit.



If R_{GEN} , R_L or C_L is increased, there will be proportional increases in rise and/or fall times.



Equivalent "OFF" Circuit



ABSOLUTE MAXIMUM RATINGS

V+ to V-	36 V
V+ to V _D	36 V
V _D or V _S to V-	36 V
V _D to V _S	±22 V
V+ to V _R	25 V
V _R to V-	25 V
V _{in} to V-	30 V
V+ to V _{in}	25 V
V _{in} to V _R	±6 V
Current (Any Terminal)	30 mA

Storage Temperature	-65 to 150°C
Operating Temperature (A Suffix)	-55 to 125°C
(B Suffix)	-20 to 85°C
Power Dissipation*	
Flat Package**	750 mW
14 Pin DIP***	825 mW

*All leads welded or soldered to PC board

**Derate 10 mW/°C above 75°C

***Derate 11 mW/°C above 75°C

ELECTRICAL CHARACTERISTICS¹ (Cont.)T_A = 25°C

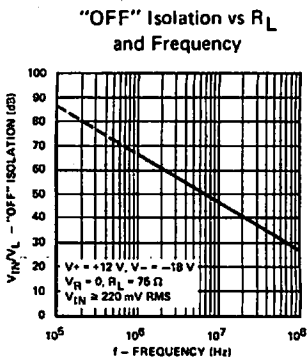
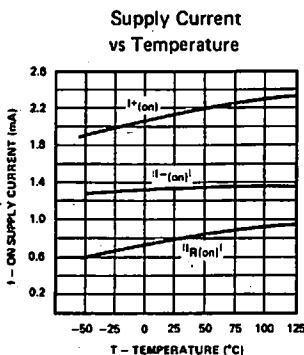
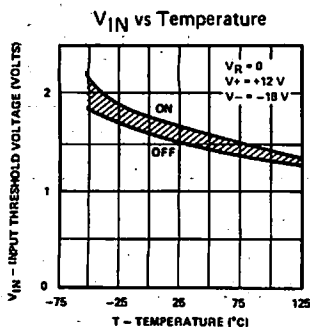
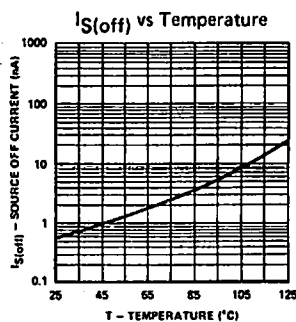
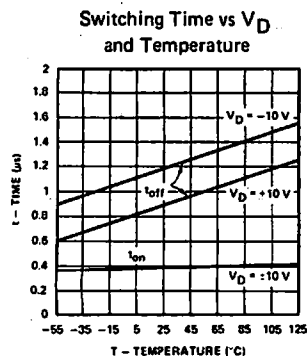
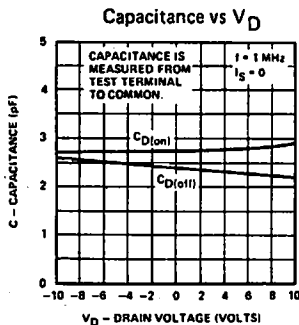
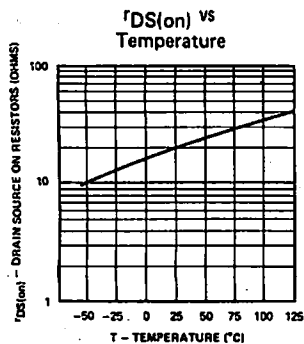
	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: V+ = 12 V, V- = -18 V, V _R = 0	LIMITS						UNIT	
				DG129A			DG129B				
				MIN ²	TYP ³	MAX	MIN ²	TYP ³	MAX		
SWITCH	Analog Signal Range	V _{ANALOG}		-10		10	-8		8	V	
	Drain-Source ON Resistance	r _{DS(on)}	I _S = -10 mA V _{in} = 2.5 V		20	30				Ω	
	Source OFF Leakage Current ⁴	I _{S(off)}	V _{in} = 0.8 V		0.03	1				nA	
	Drain OFF Leakage Current ⁴	I _{D(off)}	V _{in} = 0.8 V		0.02	1				nA	
	Channel ON Leakage Current ⁴	I _{D(on)} + I _{S(on)}	V _{in} = 2.5 V		-2	-0.03				nA	
							-5	-0.08		nA	
INPUT	Input Current With Input Voltage High	I _{INH}	V _{in} = 2.5 V		11	60		15	100	μA	
	Input Current With Input Voltage Low	I _{INL}	V _{in} = 0.8 V		0.001	0.1		0.005	4	μA	
DYNAMIC	Turn-ON Time	t _{on}	See Switching Time Test Circuit		0.3	0.6		0.5	1	μs	
	Turn-OFF Time	t _{off}			1.05	1.6		1.1	2	μs	
	Source OFF Capacitance	C _{S(off)}	f = 1 MHz		2.4			2.4		pF	
	Drain OFF Capacitance	C _{D(off)}			2.4			2.4		pF	
	Channel OFF Capacitance	C _D + S(on)			2.8			2.8		pF	
	OFF Isolation	OIRR		R _L = 75 Ω, 1 MHz		>60dB			>60dB		dB
SUPPLY	Positive Supply Current	I+	One Channel ON V _{in} = 2.5 V		2.4	3.0		2.5	3.3	mA	
	Negative Supply Current	I-			-1.8	-1.5		-2.0	-1.6		mA
	Reference Supply Current	I _R			-1.4	-1.0		-1.5	-1.1		mA
	Positive Supply Current	I+	All Channels OFF Both V _{in} = 0		0.1	25		0.1	25	μA	
	Negative Supply Current	I-			-25	-0.5		-25	-0.5		μA
	Reference Supply Current	I _R			-25	0		-25	0		μA

T_A = Over Temperature Range

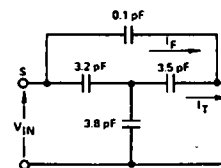
	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: V+ = 12 V, V- = -18 V, V _R = 0		LIMITS						UNIT
					DG129A			DG129B			
					MIN ²	TYP ³	MAX	MIN ²	TYP ³	MAX	
SWITCH	Analog Signal Range	V _{ANALOG}			-10		10	-8		8	V
	Drain-Source ON Resistance	r _{DS(on)}	I _S = -10 mA V _{in} = 2.5 V	V _D = 10 V			60				Ω
		V _D = 8 V						75			
	Source OFF Leakage Current ⁴	I _{S(off)}	V _{in} = 0.8 V	V _S = 10 V, V _D = -10 V			100				
		V _S = 8 V, V _D = -8 V						100			
	Drain OFF Leakage Current ⁴	I _{D(off)}	V _D = 10 V, V _S = -10 V V _D = 8 V, V _S = -8 V			100				100	nA
Channel ON Leakage Current ⁴	I _{D(on)} + I _{S(on)}	V _{in} = 2.5 V		V _D = V _S = -10 V	-100						
			V _D = V _S = -8 V				-100				
INPUT	Input Current With Input Voltage High	I _{INH}	V _{in} = 2.5 V				120			150	μA
	Input Current With Input Voltage Low	I _{INL}	V _{in} = 0.8 V				2			4	

NOTES:

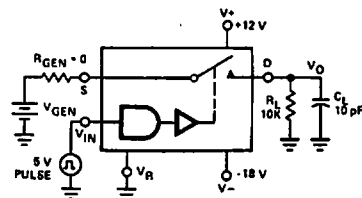
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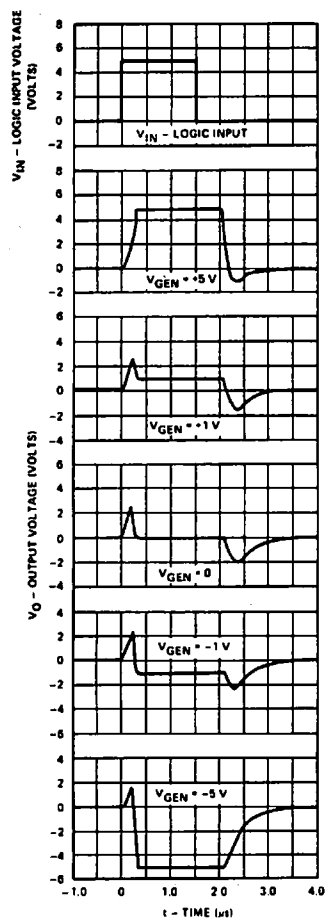
Equivalent "OFF" Circuit



Typical delay, rise, fall, settling times, and switching transients in this circuit.



If R_{GEN} , R_L or C_L is increased, there will be proportional increases in rise and/or fall RC times.



ABSOLUTE MAXIMUM RATINGS

V+ to V-	36 V
V+ to V _D	36 V
V _D or V _S to V-	36 V
V _D to V _S	±22 V
V+ to V _R	25 V
V _R to V-	25 V
V _{in} to V-	30 V
V+ to V _{in}	25 V
V _{in} to V _R	±6 V
Current (Any Terminal)	30 mA

Storage Temperature	-65 to 150°C
Operating Temperature (A Suffix)	-55 to 125°C
(B Suffix)	-20 to 85°C
Power Dissipation*	
Flat Package**	750 mW
14 Pin DIP***	825 mW

*All leads welded or soldered to PC board

**Derate 10 mW/°C above 75°C

***Derate 11 mW/°C above 75°C

ELECTRICAL CHARACTERISTICS¹ (Cont.)
T_A = 25°C

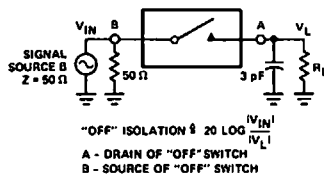
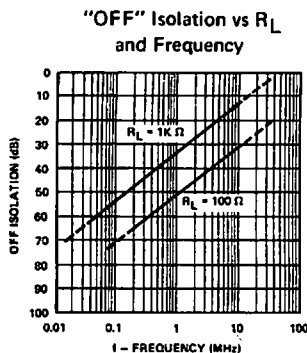
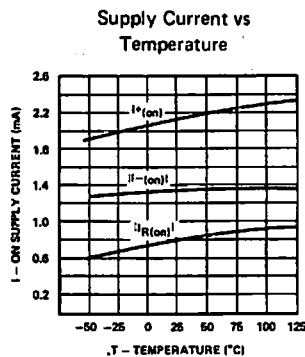
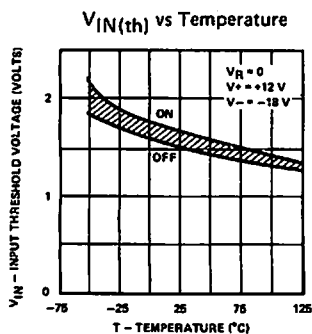
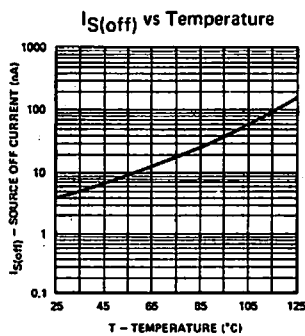
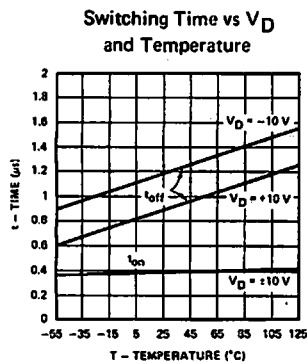
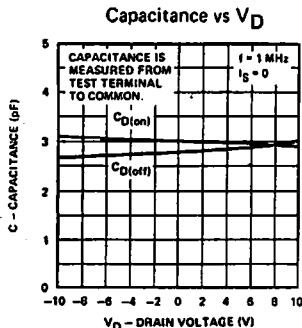
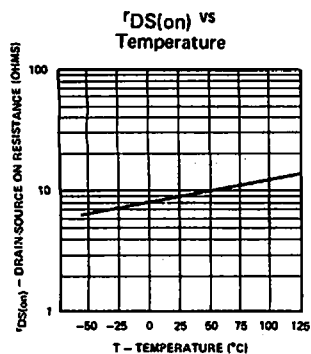
	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: V+ = 12 V, V- = -18 V, V _R = 0		LIMITS						UNIT
					DG140A			DG140B			
					MIN ²	TYP ³	MAX	MIN ²	TYP ³	MAX	
SWITCH	Analog Signal Range	V _{ANALOG}			-10		10	-8		8	V
	Drain-Source ON Resistance	r _{DS(on)}	I _S = -10 mA V _{in} = 2.5 V	V _D = 10 V		6.3	10				Ω
		V _D = 8 V					9.5	1.5			
	Source OFF Leakage Current ⁴	I _{S(off)}	V _{in} = 0.8 V	V _S = 10 V, V _D = -10 V		0.04	10				nA
		V _S = 8 V, V _D = -8 V					0.06	15			
	Drain OFF Leakage Current ⁴	I _{D(off)}		V _D = 10 V, V _S = -10 V			10				
		V _D = 8 V, V _S = -8 V						15			
	Channel ON Leakage Current ⁴	I _{D(on)} ⁺ I _{S(on)}	V _{in} = 2.5 V	V _D = V _S = -10 V	-2	-0.4					
				V _D = V _S = -8 V				-5	-1.0		
INPUT	Input Current With Input Voltage High	I _{INH}	V _{in} = 2.5 V			8	60		13	100	μA
	Input Current With Input Voltage Low	I _{INL}	V _{in} = 0.8 V			0.001	0.1		0.004	4	
DYNAMIC	Turn-ON Time	t _{on}	See Switching Time Test Circuit			0.4	1		0.6	1.5	μs
	Turn-OFF Time	t _{off}				1.15	2.5		1.15	2.5	
	Source OFF Capacitance	C _{S(off)}	f = 1 MHz	V _S = 0, I _D = 0,		3			3		pF
	Drain OFF Capacitance	C _{D(off)}		V _D = 0, I _S = 0,		3			3		
				V _D = 0, I _S = 0,		3			3		
	Channel OFF Capacitance	C _D + S _(on)		V _D = V _S = 0,		2.8			2.8		
OFF Isolation	OIRR	R _L = 75 Ω 1 MHz			>50dB			>50dB		dB	
SUPPLY	Positive Supply Current	I ⁺	One Channel ON V _{in} = 2.5 V			2.3	3.0		2.4	3.3	mA
	Negative Supply Current	I ⁻			-1.8	-1.4		-2	-1.5		
	Reference Supply Current	I _R			-1.4	0.9		-1.5	-1.0		
	Positive Supply Current	I ⁺	All Channels OFF Both V _{in} = 0			0.1	25		0.1	25	μA
	Negative Supply Current	I ⁻			-25	-0.5		-25	-0.5		
	Reference Supply Current	I _R			-25			-25			

T_A = Over Temperature Range

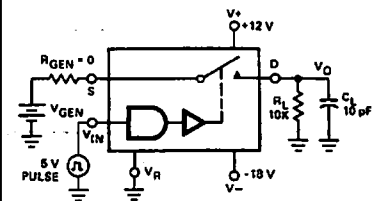
	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: V+ = 12 V, V- = -18 V, VR = 0		LIMITS						UNIT
					DG140A			DG140B			
					MIN ²	TYP ³	MAX	MIN ²	TYP ³	MAX	
SWITCH	Analog Signal Range	VANALOG			-10		10	-8		8	V
	Drain-Source ON Resistance	rDS(on)	IS = -10 mA VIN = 2.5 V	VD = 10 V VD = 8 V			20			25	Ω
	Source OFF Leakage Current ⁴	IS(off)	VIN = 0.8 V	VS = 10 V, VD = -10 V VS = 8 V, VD = -8 V			1000			300	nA
	Drain OFF Leakage Current ⁴	ID(off)		VD = 10 V, VS = -10 V VD = 8 V, VS = -8 V			1000			300	
	Channel ON Leakage Current ⁴	ID(on)* IS(on)		VIN = 2.5 V	VD = VS = -10 V VD = VS = -8 V	-100			-100		
	INPUT	Input Current With Input Voltage High	IINH	VIN = 2.5 V			120			150	μA
Input Current With Input Voltage Low		IINL	VIN = 0.8 V			2			4		

NOTES:

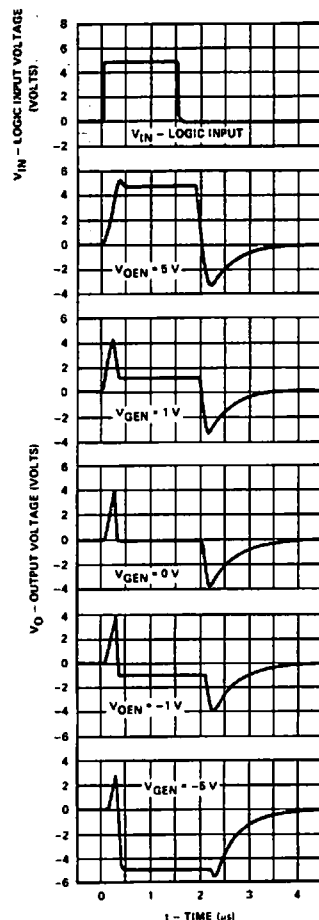
- Refer to PROCESS OPTION FLOWCHART for additional information.
- The algebraic convention whereby the most negative value is a minimum, and the most positive is a maximum, is used in this data sheet.
- Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- V_{in} must be a step function with a minimum rise and fall time of 1 V/μs.



Typical delay, rise, fall, settling times, and switching transients in this circuit.

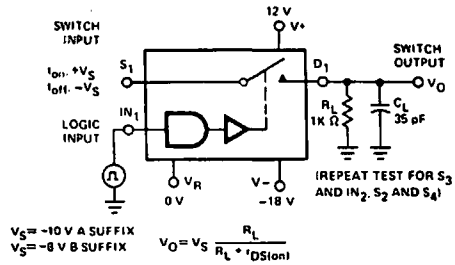
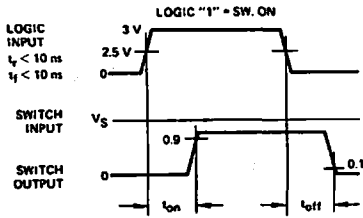


If R_{GEN} , R_L or C_L is increased, there will be proportional increases in rise and/or fall RC times.



SWITCHING TIME TEST CIRCUIT

Switch output waveform shown for V_S = constant with logic input waveform as shown. Note that V_S may be + or - as per switching time test circuit. V_O is the steady state output with switch on. Feedthrough via gate capacitance may result in spikes at leading and trailing edge of output waveform.


APPLICATION HINTS

V_+ Positive Supply Voltage (V)	V_- Negative Supply Voltage (V)	V_R Reference Voltage (V)	V_{in} Logic Input Voltage V_{INH} Min/ V_{INL} Max (V)	V_S or V_D Analog Voltage Range (V)
12	-18	0	2.5/0.8	-15 to 10
15	-15	0	2.5/0.8	-10 to 13
5	-15	0	2.5/0.8	-10 to 3
5	-10	0	2.5/0.8	-5 to 3

DG133/DG134/DG141

Dual SPST JFET Analog Switches



FEATURES

- $<1 \mu\text{W}$ Standby Power
- Bipolar Drivers
- Constant $r_{DS(on)}$ Over Signal Range
- OFF Isolation $>60 \text{ dB}$ @ 1 MHz

BENEFITS

- Minimizes Standby Power Requirement
- Better Radiation Tolerance than CMOS
- Less Signal Distortion than CMOS
- Higher Frequency Switching

APPLICATIONS

- Portable and Battery Powered Systems
- Switching in Satellite Applications
- Low Distortion Circuits
- High Frequency Switching Circuits

DESCRIPTION

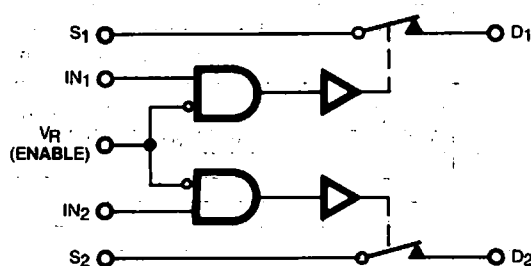
DG133/DG134/DG141 are dual precision single-pole, single-throw analog switches designed for applications where constant ON resistance over the entire analog range is an important consideration. The major design difference is in ON resistance, being 10, 30 and 80 Ω for the DG141, DG133, DG134 respectively.

The DG133, DG134, and DG141 each contain two junction-type field-effect transistors (JFETs) designed to function as two single-pole, single-throw electronic switches. Level-shifting drivers enable low-level inputs (0.8 to 2.5 V) to control the ON-OFF state of each switch. With a positive logic "0" at the driver input the switches will be OFF. With a positive logic "1" at the input the

switches will be ON. In the ON state each switch will conduct current in either direction, and in the OFF state each switch will block voltages up to 20 V peak-to-peak. ON resistance of the DG133 is $<80 \Omega$, the DG134 $<30 \Omega$ and the DG141 $<10 \Omega$, and ON shunt leakage for all three is $<2 \text{ nA}$. With both drivers in the "switch OFF" state total power consumption is $<750 \mu\text{W}$. Due to the processing all three analog switches are relatively Radiation tolerant.

These parts are available in the 14-lead dual-in-line side-brazed and flatpack, and are specified over the industrial (-25 to 85°C), and military (-55 to 125°C) temperature ranges.

FUNCTIONAL BLOCK DIAGRAM



Two SPST Switches per Package*

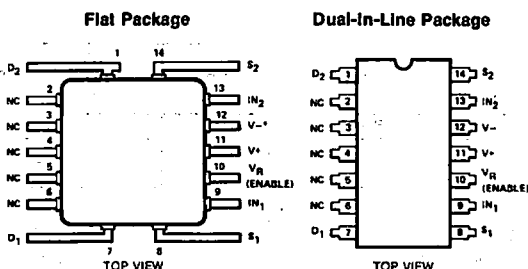
Truth Table

LOGIC	SWITCH
0	OFF
1	ON

Logic "0" $\leq 0.8 \text{ V}$
Logic "1" $\geq 2.5 \text{ V}$

*Switches Shown for Logic "1" Input

PIN CONFIGURATION



Order Numbers:
DG133AL, DG134AL,
or DG141AL
See Package 5

Order Numbers:
DG133AP, DG133BP
DG134AP, DG134BP
DG141AP, DG141BP
See Package 11

*Common to Substrate and Base of Package

ABSOLUTE MAXIMUM RATINGS

V ₊ to V ₋	36 V
V ₊ to V _D	36 V
V _D or V _S to V ₋	36 V
V _D to V _S	±22 V
V ₊ to V _R	25 V
V _R to V ₋	25 V
V _{in} to V ₋	30 V
V ₊ to V _{in}	25 V
V _{in} to V _R	±6 V
Current (Any Terminal)	30 mA

Storage Temperature	-65 to 150°C
Operating Temperature (A Suffix)	-55 to 125°C
(B Suffix)	-25 to 85°C
Power Dissipation*	
Flat Package**	750 mW
14 Pin DIP***	825 mW

*All leads welded or soldered to PC board.

**Derate 10 mW/°C above 75°C.

***Derate 11 mW/°C above 75°C.

ELECTRICAL CHARACTERISTICS¹

T_A = 25°C

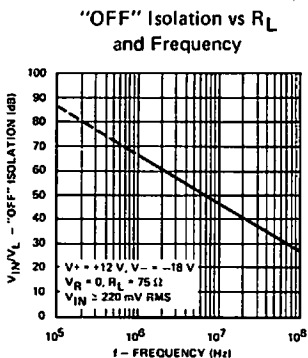
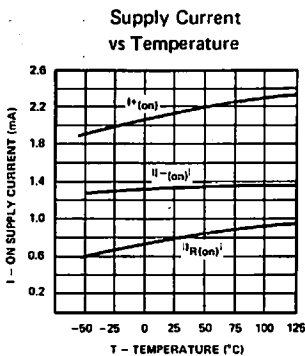
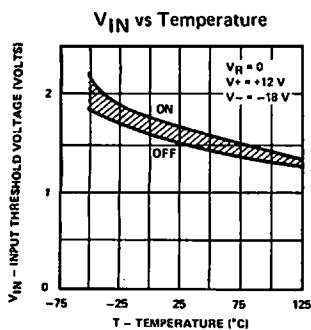
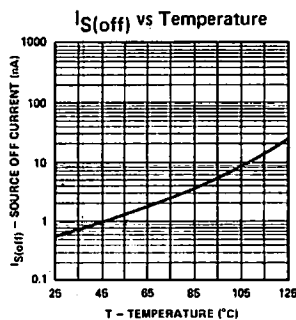
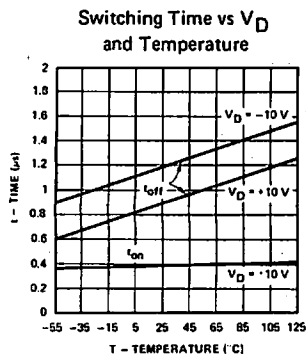
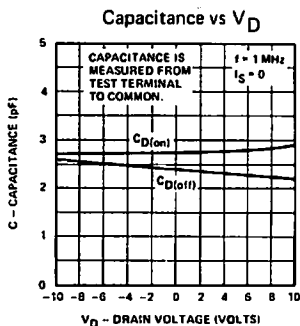
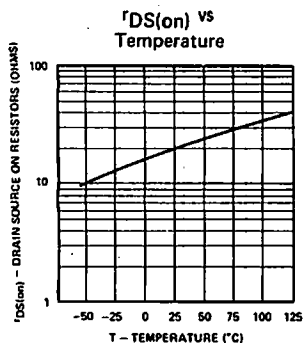
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				DG133A			DG133B			
				MIN ²	TYP ³	MAX	MIN ²	TYP ³	MAX	
SWITCH	Analog Signal Range	VANALOG		-10		10	-8		8	V
	Drain-Source ON Resistance	rDS(on)	IS = -10 mA VIN = 2.5 V		20	30				Ω
			VD = 10 V							
			VD = 8 V					30	50	
	Source OFF Leakage Current	IS(off)	VIN = 0.8 V		0.03	1				nA
			VS = 10 V, VD = -10 V							
INPUT			VS = 8 V, VD = -8 V						5	
	Drain OFF Leakage Current	ID(off)	VD = 10 V, VS = -10 V		0.02	1				nA
			VD = 8 V, VS = -8 V					0.1	5	
	Channel ON Leakage Current	ID(on)+ IS(on)	VIN = 2.5 V	-2	-0.03					
			VD = VS = -10 V				-5	-0.08		
			VD = VS = -8 V							
INPUT	Input Current With Input Voltage High	IINH	VIN = 2.5 V		11	60		15	100	μA
	Input Current With Input Voltage Low	IINL	VIN = 0.8 V		0.001	0.1		0.005	4	
DYNAMIC	Turn-ON Time	ton	See Switching Time Test Circuit		0.3	0.6		0.5	1	μs
	Turn-OFF Time	toff	See Switching Time Test Circuit		1.05	1.6		1.1	2	
	Source OFF Capacitance	CS(off)	f = 1 MHz		2.4			2.4		pF
	Drain OFF Capacitance	CD(off)	VD = 0, IS = 0,		2.4			2.4		
	Channel OFF Capacitance	CD + S(on)	VD = VS = 0,		2.8			2.8		
	OFF Isolation	OIRR	RL = 75 Ω, f = 1 MHz		>60			>60		dB
SUPPLY	Positive Supply Current	I+	One Channel ON VIN = 2.5 V		2.4	3.0		2.5	3.3	mA
	Negative Supply Current	I-	One Channel ON VIN = 2.5 V	-1.8	-1.5		-2.0	-1.6		
	Reference Supply Current	IR	One Channel ON VIN = 2.5 V	-1.4	-1.0		-1.5	-1.1		
	Positive Supply Current	I+	All Channels OFF Both VIN = 0		0.1	25		0.1	25	μA
	Negative Supply Current	I-	All Channels OFF Both VIN = 0	-25	-0.5		-25	-0.5		
	Reference Supply Current	IR	All Channels OFF Both VIN = 0	-25	0		-25	0		

T_A = Over Temperature Range

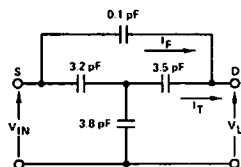
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					DG133A						
					MIN ²	TYP ³	MAX	MIN ²	TYP ³	MAX	
SWITCH	Analog Signal Range	VANALOG			-10		10	-8		8	V
	Drain-Source ON Resistance	rDS(on)	IS = -10 mA VIN = 2.5 V	VD = 10 V			60				Ω
		VD = 8 V						75			
	Source OFF Leakage Current	IS(off)	VIN = 0.8 V	VS = 10 V, VD = -10 V			100				nA
		VS = 8 V, VD = -8 V						100			
	Drain OFF Leakage Current	ID(off)		VD = 10 V, VS = -10 V			100				
			VD = 8 V, VS = -8 V					100			
Channel ON Leakage Current	ID(on)+ IS(on)	VIN = 2.5 V	VD = VS = -10 V	-100							
			VD = VS = -8 V				-100				
INPUT	Input Current With Input Voltage High	IINH	VIN = 2.5 V				120			150	μA
	Input Current With Input Voltage Low	IINL	VIN = 0.8 V				2			4	

NOTES:

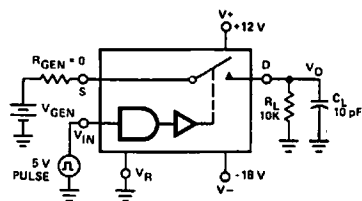
1. Refer to PROCESS OPTION FLOWCHART for additional information.
2. The algebraic convention whereby the most negative value is a minimum, and the most positive is a maximum, is used in this data sheet.
3. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
4. V_{in} must be a step function with a minimum rise and fall time of 1 V/μs.



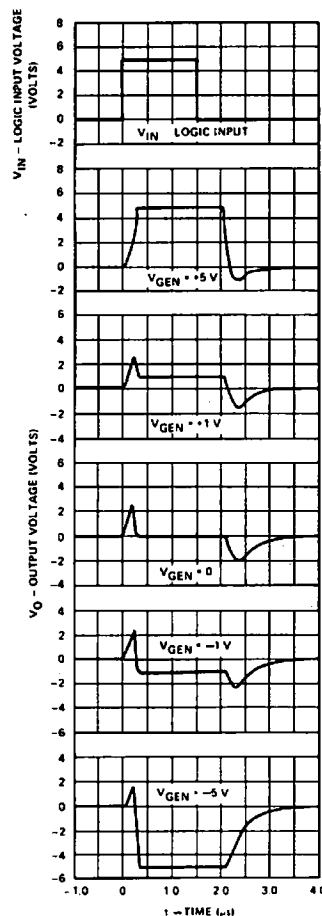
Equivalent "OFF" Circuit



Typical delay, rise, fall, settling times, and switching transients in this circuit.



If R_{GEN} , R_L or C_L is increased, there will be proportional increases in rise and/or fall times.



ELECTRICAL CHARACTERISTICS¹ (Cont.)T_A = 25°C

DG133/DG134/DG141

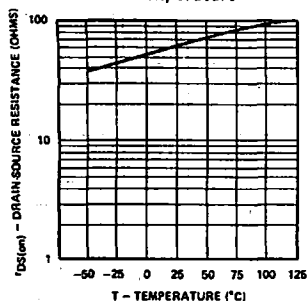
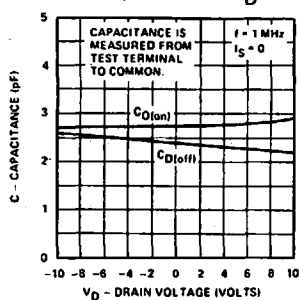
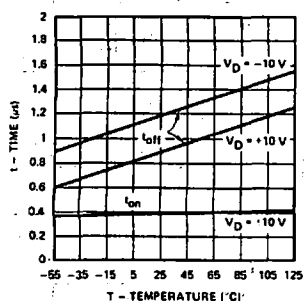
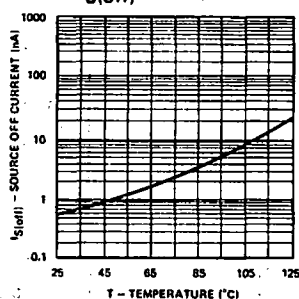
	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: V+ = 12 V, V- = -18 V, VR = 0		LIMITS						UNIT
					DG134A			DG134B			
					MIN ²	TYP ³	MAX	MIN ²	TYP ³	MAX	
SWITCH	Analog Signal Range	VANALOG			-10		10	-8		8	V
	Drain-Source ON Resistance	rDS(on)	IS = -10 mA VIN = 2.5 V	VD = 10 V		20	80				Ω
		VD = 8 V					25	100			
	Source OFF Leakage Current	IS(off)	VIN = 0.8 V	VS = 10 V, VD = -10 V	0.01	1					nA
		VS = 8 V, VD = -8 V					0.05	5			
		VD = 10 V, VS = -10 V		0.005	1						
	Drain OFF Leakage Current	ID(off)	VD = 8 V, VS = -8 V				0.025	5			
Channel ON Leakage Current	ID(on)+ IS(on)	VIN = 2.5 V	VD = VS = -10 V	-2	-0.02						
			VD = VS = -8 V				-5	-0.05			
INPUT	Input Current With Input Voltage High	IINH	VIN = 2.5 V			10	60		20	100	μA
	Input Current With Input Voltage Low	IINL	VIN = 0.8 V			0.001	0.1		0.004	4	
DYNAMIC	Turn-ON Time	ton	See Switching Time Test Circuit			0.3	0.6		0.4	1	μs
	Turn-OFF Time	toff				1.2	1.6		1.3	2	
	Source OFF Capacitance	CS(off)	f = 1 MHz	VS = 0, ID = 0,		2.4			2.4		pF
	Drain OFF Capacitance	CD(off)		VD = 0, IS = 0,		2.4			2.4		
	Channel OFF Capacitance	CD + S(on)		VD = VS = 0,		2.8			2.8		
	OFF Isolation	OIRR	RL = 75 Ω, f = 1 MHz			>60			>60		dB
SUPPLY	Positive Supply Current	I+	One Channel ON VIN = 2.5 V			2.1	3.0		2.1	3.3	mA
	Negative Supply Current	I-			-1.8	-1.15		-2.0	-1.2		
	Reference Supply Current	IR			-1.4	-1.0		-1.5	-1.0		
	Positive Supply Current	I+	All Channels OFF Both VIN = 0			0.1	25		0.1	25	μA
	Negative Supply Current	I-			-25	-0.5		-25	-0.5		
	Reference Supply Current	IR			-25	0		-25			

T_A = Over Temperature Range

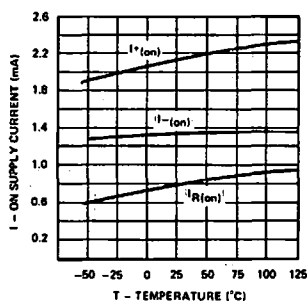
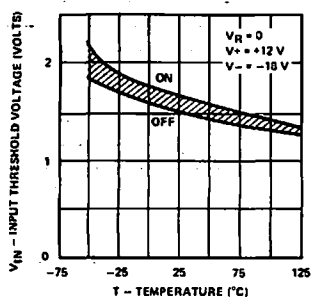
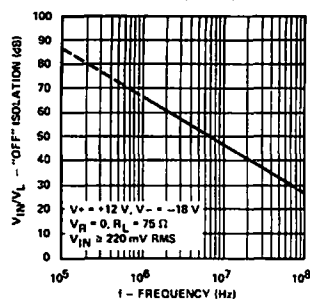
	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: V+ = 12 V, V- = -18 V, VR = 0		LIMITS						UNIT
					DG134A			DG134B			
					MIN ²	TYP ³	MAX	MIN ²	TYP ³	MAX	
SWITCH	Analog Signal Range	VANALOG			-10		10	-8		8	V
	Drain-Source ON Resistance	rDS(on)	IS = -10 mA VIN = 2.5 V	VD = 10 V			150			150	Ω
		VD = 8 V									
	Source OFF Leakage Current	IS(off)	VIN = 0.8 V	VS = 10 V, VD = -10 V			100				nA
		VS = 8 V, VD = -8 V						100			
	Drain OFF Leakage Current	ID(off)		VD = 10 V, VS = -10 V			100				
			VD = 8 V, VS = -8 V					100			
Channel ON Leakage Current	ID(on)+ IS(on)	VIN = 2.5 V	VD = VS = -10 V	-100							
			VD = VS = -8 V				-100				
INPUT	Input Current With Input Voltage High	IINH	VIN = 2.5 V				120			150	μA
	Input Current With Input Voltage Low	IINL	VIN = 0.8 V				2			4	

NOTES:

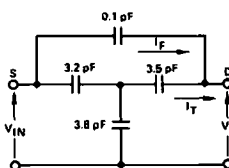
1. Refer to PROCESS OPTION FLOWCHART for additional information.
2. The algebraic convention whereby the most negative value is a minimum, and the most positive is a maximum, is used in this data sheet.
3. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
4. V_{in} must be a step function with a minimum rise and fall time of 1 V/μs.

$r_{DS(on)}$ vs TemperatureCapacitance vs V_D Switching Time vs V_D and Temperature $I_{S(off)}$ vs Temperature

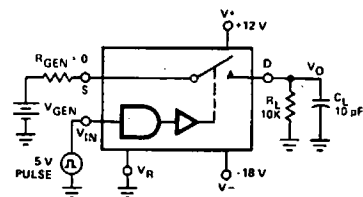
Supply Current vs Temperature

 V_{IN} vs Temperature"OFF" Isolation vs R_L and Frequency

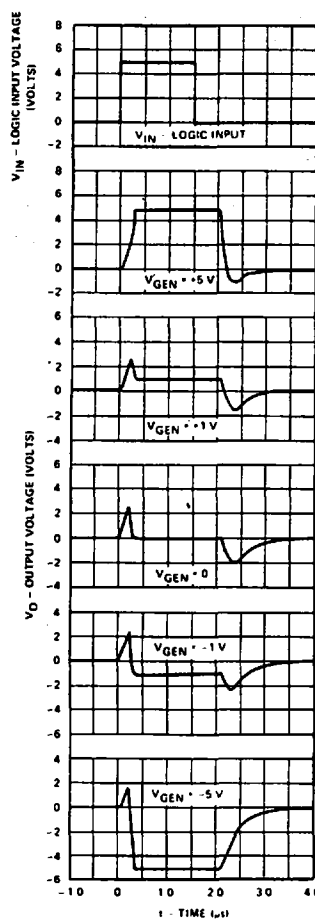
Equivalent "OFF" Circuit



Typical delay, rise, fall, settling times, and switching transients in this circuit.



If R_{GEN} , R_L or C_L is increased, there will be proportional increases in rise and/or fall RC times.



ELECTRICAL CHARACTERISTICS¹ (Cont.) $T_A = 25^\circ\text{C}$

DG133/DG134/DG141

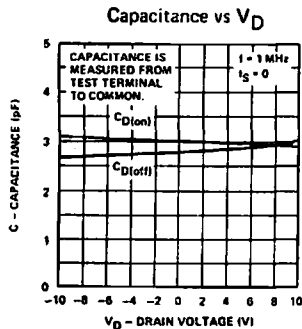
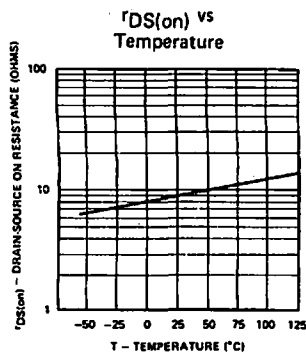
	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: V+ = 12 V, V- = -18 V, VR = 0		LIMITS						UNIT
					DG141A			DG141B			
					MIN ²	TYP ³	MAX	MIN ²	TYP ³	MAX	
SWITCH	Analog Signal Range	VANALOG			-10		10	-8		8	V
	Drain-Source ON Resistance	rDS(on)	IS = -10 mA VIN = 2.5 V	VD = 10 V		6.3	10				Ω
		VD = 8 V					9.5	15			
	Source OFF Leakage Current	IS(off)	VIN = 0.8 V	VS = 10 V, VD = -10 V		0.04	10				nA
		VS = 8 V, VD = -8 V					0.06	15			
	Drain OFF Leakage Current	ID(off)	VD = 10 V, VS = -10 V			10					
		VD = 8 V, VS = -8 V						15			
	Channel ON Leakage Current	ID(on)+IS(on)	VIN = 2.5 V	VD = VS = -10 V	-2	-0.4					
				VD = VS = -8 V				-5	-1.0		
INPUT	Input Current With Input Voltage High	IINH	VIN = 2.5 V			8	60		13	100	μA
	Input Current With Input Voltage Low	IINL	VIN = 0.8 V			0.001	0.1		0.004	4	
DYNAMIC	Turn-ON Time	ton	See Switching Time Test Circuit			0.4	1		0.6	1.5	μs
	Turn-OFF Time	toff				1.15	2.5		1.15	2.5	
	Source OFF Capacitance	CS(off)	f = 1 MHz	VS = 0, ID = 0,		3			3		pF
	Drain OFF Capacitance	CD(off)		VD = 0, IS = 0,		3			3		
	Channel OFF Capacitance	CD + S(on)		VD = VS = 0,		2.8			2.8		
	OFF Isolation	OIRR	RL = 75 Ω, f = 1 MHz			>50			>50		dB
SUPPLY	Positive Supply Current	I+	One Channel ON VIN = 2.5 V			2.3	3.0		2.4	3.3	mA
	Negative Supply Current	I-			-1.8	-1.4		-2	-1.5		
	Reference Supply Current	IR			-1.4	-0.9		-1.5	-1.0		
	Positive Supply Current	I+	All Channels OFF Both VIN = 0			0.1	25		0.1	25	μA
	Negative Supply Current	I-			-25	-0.5		-25	-0.5		
	Reference Supply Current	IR			-25			-25			

 $T_A = \text{Over Temperature Range}$

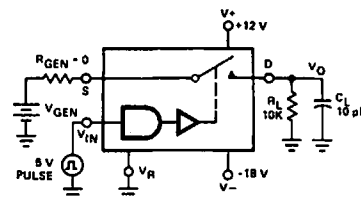
	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: V+ = 12 V, V- = -18 V, VR = 0		LIMITS						UNIT
					DG141A			DG141B			
					MIN ²	TYP ³	MAX	MIN ²	TYP ³	MAX	
SWITCH	Analog Signal Range	VANALOG			-10		10	-8		8	V
	Drain-Source ON Resistance	rDS(on)	IS = -10 mA VIN = 2.5 V	VD = 10 V		10	20				Ω
				VD = 8 V					11	25	
	Source OFF Leakage Current	IS(off)	VIN = 0.8 V	VS = 10 V, VD = -10 V		11	1000				nA
				VS = 8 V, VD = -8 V						5	
	Drain OFF Leakage Current	ID(off)		VD = 10 V, VS = -10 V		2.5	1000				
				VD = 8 V, VS = -8 V					2.5	300	
Channel ON Leakage Current	ID(on)+IS(on)	VIN = 2.5 V	VD = VS = -10 V	-100	-1.4						
			VD = VS = -8 V				-100	-1.4			
INPUT	Input Current With Input Voltage High	IINH	VIN = 2.5 V			15	120		50	150	μA
	Input Current With Input Voltage Low	IINL	VIN = 0.8 V				2			4	

NOTES:

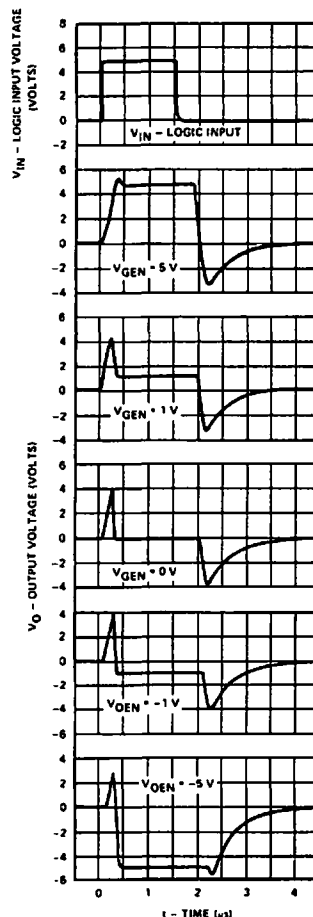
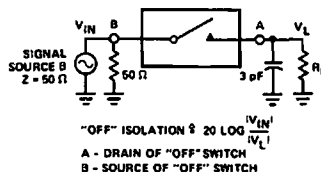
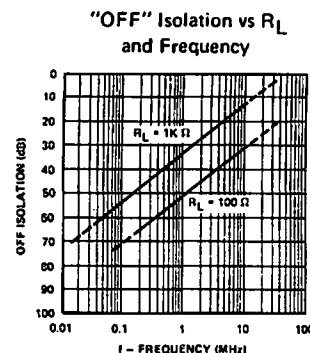
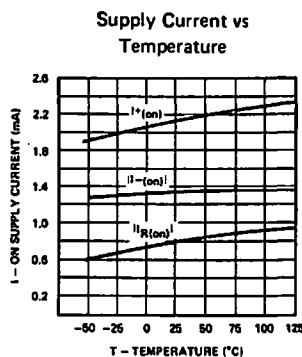
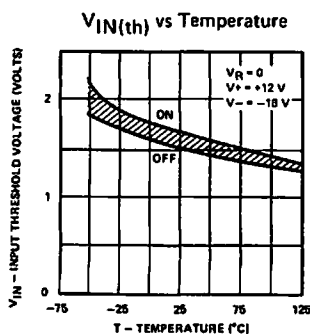
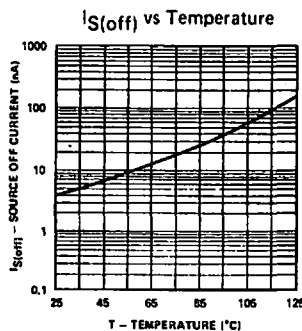
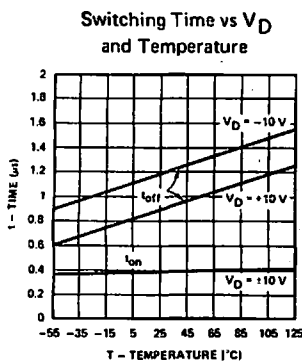
1. Refer to PROCESS OPTION FLOWCHART for additional information.
2. The algebraic convention whereby the most negative value is a minimum, and the most positive is a maximum, is used in this data sheet.
3. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
4. V_{in} must be a step function with a minimum rise and fall time of $1\text{ V}/\mu\text{s}$.



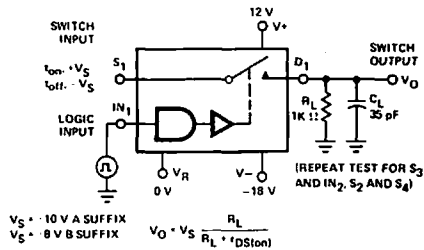
Typical delay, rise, fall, settling times, and switching transients in this circuit.



If R_{GEN} , R_L or C_L is increased, there will be proportional increases in rise and/or fall RC times.



Timing diagram for the 74VHC00. The diagram shows three signals: LOGIC INPUT, SWITCH INPUT, and SWITCH OUTPUT. The LOGIC INPUT signal is a square wave between 0V and 3V, with rise and fall times $t_1 < 10 \text{ ns}$. The SWITCH INPUT signal is a square wave between 0V and V_S , with a high-level voltage of 0.9. The SWITCH OUTPUT signal is a square wave between 0V and V_S , with rise time t_{on} and fall time t_{off} .



APPLICATION HINTS

V+ Positive Supply Voltage (V)	V- Negative Supply Voltage (V)	V _R Reference Voltage (V)	V _{IN} Logic Input Voltage V _{INH} Min/ V _{INL} Max (V)	V _S or V _D Analog Voltage Range (V)
12	-18	0	2.5/0.8	-10 to 10
15	-15	0	2.5/0.8	-5 to 13
10	-10	0	2.5/0.8	0 to 8

DG139/DG142/DG145

Dual DPDT JFET

Analog Switches



FEATURES

- < 1 μ W Standby Power
- Bipolar Drivers
- Constant $r_{DS(on)}$ Over Signal Range
- Off Isolation > 60 dB @ 1 MHz

BENEFITS

- Minimizes Standby Power Requirement
- Better Radiation Tolerance Than CMOS
- Less Signal Distortion Than CMOS
- Higher Frequency Switching

APPLICATIONS

- Portable and Battery Powered Systems
- Switching In Satellite Applications
- Low Distortion Circuits
- High Frequency Switching Circuits

DESCRIPTION

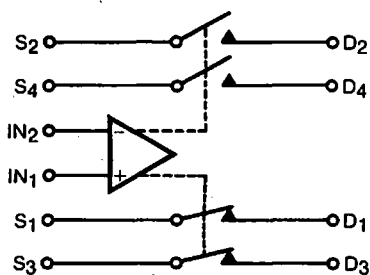
DG139/DG142/DG145 are precision dual double-pole double-throw analog switches designed for applications where constant ON resistance over the entire analog range is an important consideration. The major design difference is in ON resistance, being 10, 30 and 80 Ω for the DG145, DG139 and DG142 respectively.

The DG139, DG142 and DG145 each contain four junction-type field-effect transistors (JFETs) designed to function as two double-pole double-throw electronic switches. Level-shifting drivers enable low-level inputs (2.0 to 3.0 V) to control the ON-OFF state of the switches. The driver inputs are connected differentially so that with input IN2 connected to a 2.5 voltage reference, a positive logic "0" at the input IN1 will turn switches 1 and 3 OFF and switches 2 and 4 ON. A positive logic "1" at IN1 will turn switches 1 and 3 ON and switches 2 and 4 OFF. The normally

grounded VR terminal may be used as an "inhibit" terminal, in which case all switches may be held OFF with a positive voltage applied to VR. In the ON state each switch conducts equally well in either direction, and in the OFF state each switch will block voltages up to 20 V peak-to-peak. ON resistance of the DG139 is < 30 Ω , the DG142 < 80 Ω and the DG145 is < 10 Ω and ON shunt leakage for all three is < 2 nA. With both drivers in the "switch OFF" state total power consumption is < 750 μ W. Due to the processing all three analog switches are relatively Radiation tolerant.

These parts are available in the 14-lead dual-in-line side-braze and flatpack, and are specified over the industrial (-25 to 85°C), and military (-55 to 125°C) temperature ranges.

FUNCTIONAL BLOCK DIAGRAM



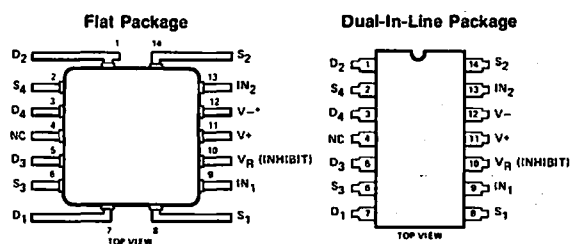
Two DPDT Switches per Package*

Truth Table

LOGIC	SW 1 SW 3	SW 2 SW 4
0	OFF	ON
1	ON	OFF

*Switches Shown For Logic "1" Input at IN1 and a 2.5 V reference at IN2

PIN CONFIGURATION



Order Numbers:
DG139AL, DG142AL,
or DG145AL
See Package 5

Order Numbers:
DG139AP, DG139BP,
DG142AP, DG142BP
See Package 11

ABSOLUTE MAXIMUM RATINGS

V+ to V-, V _D or V _S	36 V
V _D or V _S to V-	36 V
V _D to V _S	±22 V
V+ to V _R	25 V
V+ to V _{IN1} or V _{IN2}	25 V
V _R to V-	25 V
V _{IN1} to V _{IN2}	±6 V
V _{IN1} or V _{IN2} to V _R	±6 V
V _{IN1} or V _{IN2} to V-	30 V
Current (Any Terminal)	30 mA

Storage Temperature	-65 to 150°C
Operating Temperature (A Suffix)	-55 to 125°C
(B Suffix)	-25 to 85°C

Power Dissipation*

Flat Package**	750 mW
14 Pin DIP***	825 mW

*All leads welded or soldered to PC board.

**Derate 10 mW/°C above 75°C.

***Derate 11 mW/°C above 75°C.

ELECTRICAL CHARACTERISTICS¹

T_A = 25°C

	PARAMETER	SYMBOL	TEST CONDITIONS. UNLESS OTHERWISE NOTED: V+ = 12 V, V- = -18 V, V _R = 0 V _{IN2} = 2.5 V		LIMITS						UNITS
					DG139A			DG139B			
					MIN ²	TYP ³	MAX	MIN ²	TYP ³	MAX	
SWITCH	Analog Signal Range	V _{ANALOG}			-10		10	-8		8	V
	Drain-Source ON Resistance	r _{DS(on)}	IS = -10 mA V _{IN1} = 3 V (SW ₁ , 3 ON)	V _D = 10 V		20	30				Ω
			V _{IN1} = 2 V (SW ₂ , 4 ON)	V _D = 8 V				35	50		
	Source OFF Leakage Current	I _{S(off)}	V _{IN1} = 2 V (SW ₁ , 3 OFF)	V _S = 10 V, V _D = -10 V		0.15	1				nA
			V _{IN1} = 3 V (SW ₂ , 4 OFF)	V _S = 8 V, V _D = -8 V				0.75	5		
	Drain OFF Leakage Current	I _{D(off)}	V _{IN1} = 3 V (SW ₁ , 3 OFF)	V _D = 10 V, V _S = -10 V		0.03	1				
			V _{IN1} = 2 V (SW ₂ , 4 OFF)	V _D = 8 V, V _S = -8 V				0.15	5		
Channel ON Leakage Current	I _{D(on)} + I _{S(on)}	V _{IN1} = 3 V (SW ₁ , 3 ON)	V _D = V _S = -10 V	-2	-0.05						
		V _{IN1} = 2 V (SW ₂ , 4 ON)	V _D = V _S = -8 V				-5	-0.12			
INPUT	Input 1 Current Input 1 Voltage Low	I _{IN1L}	V _{IN1} = 2 V			.0003	0.1		0.012	4	μA
	Input 2 Current Input 2 Voltage Low	I _{IN2L}	V _{IN2} = 2 V, V _{IN1} = 2.5 V			.0005	0.1		0.02	4	
	Input 1 Current Input 1 Voltage High	I _{IN1H}	V _{IN1} = 3 V			24	60		40	100	
	Input 2 Current Input 2 Voltage High	I _{IN2H}	V _{IN2} = 3 V, V _{IN1} = 2.5 V			25	60		40	100	
DYNAMIC	Turn-ON Time	t _{on}	See Switching Time Test Circuit			0.5	0.8		0.6	1	μs
	Turn-OFF Time	t _{off}				1.2	1.6		1.5	2	
	Drain OFF Capacitance	C _{D(off)}	f = 1 MHz	V _D = 0 V, I _S = 0	2.4			2.4		pF	
	Source OFF Capacitance	C _{S(off)}		V _S = 0 V, I _D = 0	2.4			2.4			
	Channel ON Capacitance	C _D + S (on)		V _D = V _S = 0	2.8			2.8			
	OFF Isolation		R _L = 75 Ω, f = 1 MHz			>60			>60		dB
SUPPLY	Positive Supply Current	I ₊	One Channel ON V _{IN1} = 2 V or V _{IN1} = 3 V			2.6	4.2		2.6	4.5	mA
	Negative Supply Current	I ₋			-2	-1.3		-2.2	-1.3		
	Reference Supply Current	I _R			-2.2	-1.4		-2.4	-1.4		
	Positive Supply Current	I ₊	All Channel OFF V _{IN1} = V _{IN2} = 0.8 V			0.75	25		0.75	25	μA
	Negative Supply Current	I ₋			-25	1		-25	1		
	Reference Supply Current	I _R			-25	-0.2		-25	-0.2		

NOTES:

1. Refer to PROCESS OPTION FLOWCHART for additional information.
2. The algebraic convention whereby the most negative value is a minimum, and the most positive value is a maximum, is used in this data sheet.
3. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
4. V_{IN} must be a step function with a minimum rise and fall time of 1 V/μs.

DG139/DG142/DG145

ELECTRICAL CHARACTERISTICS¹ (Cont.)

T_A = Over Temperature Range

	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: V+ = 12 V, V- = -18 V, VR = 0 VIN2 = 2.5 V	LIMITS						UNITS
				DG139A			DG139B			
				MIN ²	TYP ³	MAX	MIN ²	TYP ³	MAX	
SWITCH	Analog Signal Range	VANALOG		-10		10	-8		8	V
	Drain-Source ON Resistance	rDS(on)	IS = -10 mA VIN1 = 3 V (SW1, 3 ON) VD = 10 V			60				Ω
			VIN1 = 2 V (SW2, 4 ON) VD = 8 V					75		
	Source OFF Leakage Current	IS(off)	VIN1 = 2 V (SW1, 3 OFF) VS = 10 V, VD = -10 V VIN1 = 3 V (SW2, 4 OFF) VS = 8 V, VD = -8 V			100			100	nA
	Drain OFF Leakage Current	ID(off)	VIN1 = 3 V (SW1, 3 OFF) VD = 10 V, VS = -10 V VIN1 = 2 V (SW2, 4 OFF) VD = 8 V, VS = -8 V			100			100	
	Channel ON Leakage Current	ID(on) + IS(on)	VIN1 = 3 V (SW1, 3 ON) VD = VS = -10 V	-100						
VIN1 = 2 V (SW2, 4 ON) VD = VS = -8 V						-100				
INPUT	Input 1 Current Input 1 Voltage Low	IIN1L	VIN1 = 2 V			2			4	μA
	Input 2 Current Input 2 Voltage Low	IIN2L	VIN2 = 2 V, VIN1 = 2.5 V			2			4	
	Input 1 Current Input 1 Voltage High	IIN1H	VIN1 = 3 V			120			150	
	Input 2 Current Input 2 Voltage High	IIN2H	VIN2 = 3 V, VIN1 = 2.5 V			120			150	

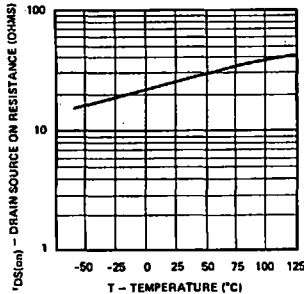
NOTES:

1. Refer to PROCESS OPTION FLOWCHART for additional information.
2. The algebraic convention whereby the most negative value is a minimum, and the most positive value is a maximum, is used in this data sheet.
3. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
4. V_{IN} must be a step function with a minimum rise and fall time of $1\text{ V}/\mu\text{s}$.

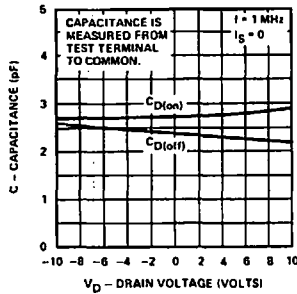
2

TYPICAL CHARACTERISTICS

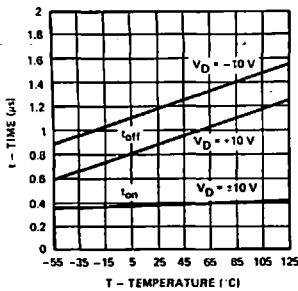
$r_{DS(on)}$ vs Temperature



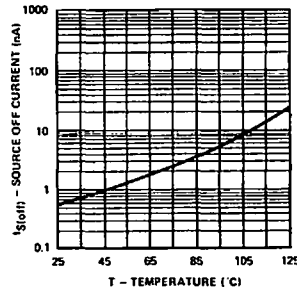
Capacitance vs V_D



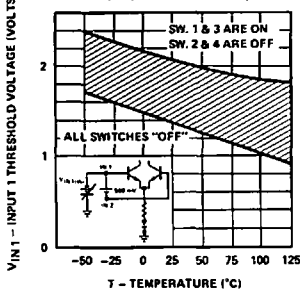
Switching Time vs V_D and Temperature



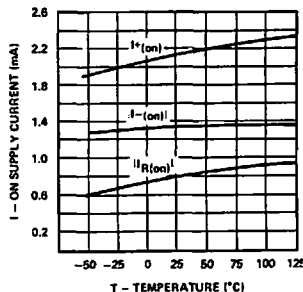
$I_{S(off)}$ vs Temperature



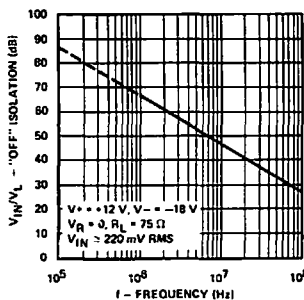
$V_{IN(th)}$ vs Temperature



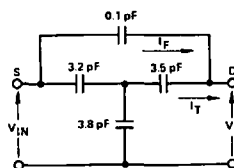
Supply Current vs Temperature



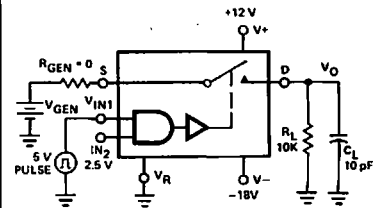
"OFF" Isolation vs R_L and Frequency



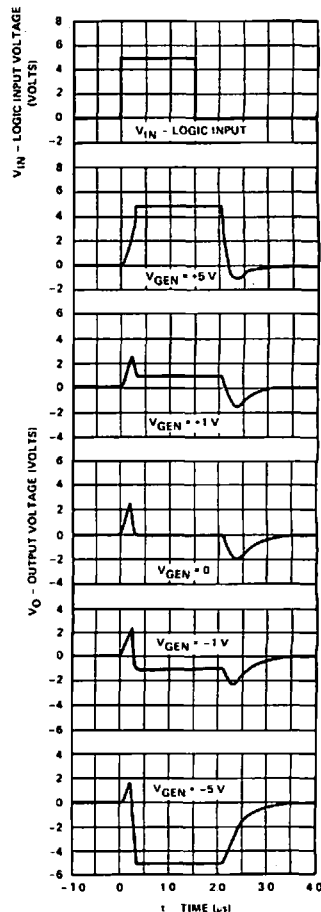
Equivalent "OFF" Circuit



Typical delay, rise, fall, settling times, and switching transient in this circuit.



If R_{GEN} , R_L or C_L is increased, there will be proportional increases in rise and/or fall RC times.



ELECTRICAL CHARACTERISTICS¹ (Cont.)DG139/DG142/DG145
T_A = 25°C

	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: V _I = 12 V, V _S = -18 V, V _R = 0 V _{IN2} = 2.5 V		LIMITS						UNITS
					DG142A			DG142B			
					MIN ²	TYP ³	MAX	MIN ²	TYP ³	MAX	
SWITCH	Analog Signal Range	V _{ANALOG}			-10		10	-8		8	V
	Drain-Source ON Resistance	r _{DS(on)}	IS = -10 mA VIN1 = 3 V (SW1, 3 ON)	VD = 10 V			80				Ω
			VIN1 = 2 V (SW2, 4 ON)	VD = 8 V				100			
	Source OFF Leakage Current	IS(off)	VIN1 = 2 V (SW1, 3 OFF)	VS = 10 V, VD = -10 V			1				
			VIN1 = 3 V (SW2, 4 OFF)	VS = 8 V, VD = -8 V					5		
	Drain OFF Leakage Current	ID(off)	VIN1 = 3 V (SW1, 3 OFF)	VD = 10 V, VS = -10 V			1				nA
			VIN1 = 2 V (SW2, 4 OFF)	VD = 8 V, VS = -8 V					5		
	Channel ON Leakage Current	ID(on) + IS(on)	VIN1 = 3 V (SW1, 3 ON)	VD = VS = -10 V	-2						
			VIN1 = 2 V (SW2, 4 ON)	VD = VS = -8 V				-5			
	INPUT	Input 1 Current Input 1 Voltage Low	IIN1L	VIN1 = 2 V			.0005	0.1			4
Input 2 Current Input 2 Voltage Low		IIN2L	VIN2 = 2 V, VIN1 = 2.5 V			0.001	0.1			4	
Input 1 Current Input 1 Voltage High		IIN1H	VIN1 = 3 V			25	60			100	
Input 2 Current Input 2 Voltage High		IIN2H	VIN2 = 3 V, VIN1 = 2.5 V			25	60			100	
DYNAMIC	Turn-ON Time	t _{on}	See Switching Time Test Circuit			0.5	0.8			1	μs
	Turn-OFF Time	t _{off}				1.1	1.6			2.0	
	Drain OFF Capacitance	CD(off)	f = 1 MHz	VD = 0 V, IS = 0		2.4			2.4		pF
	Source OFF Capacitance	CS(off)		VS = 0 V, ID = 0		2.4			2.4		
	Channel ON Capacitance	CD + S (on)		VD = VS = 0		2.8			2.8		
	OFF Isolation		RL = 75 Ω, f = 1 MHz			>60			>60		dB
SUPPLY	Positive Supply Current	I ₊	One Channel ON VIN1 = 2 V or VIN1 = 3 V				4.2			4.5	mA
	Negative Supply Current	I ₋			-2		-2.2				
	Reference Supply Current	IR			-2.2		-2.4				
	Positive Supply Current	I ₊	All Channel OFF VIN1 = VIN2 = 0.8 V				25			25	μA
	Negative Supply Current	I ₋			-25		-25				
	Reference Supply Current	IR			-25		-25				

NOTES:

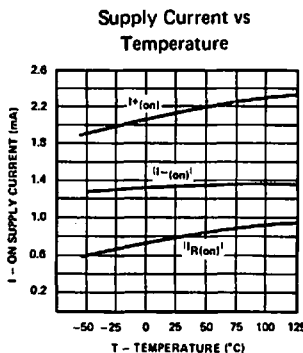
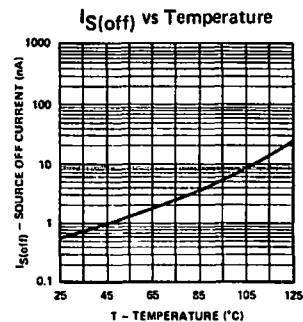
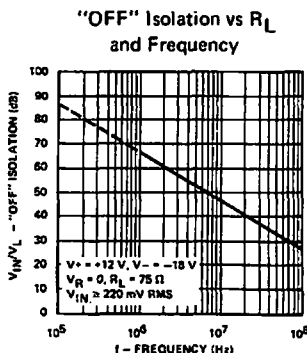
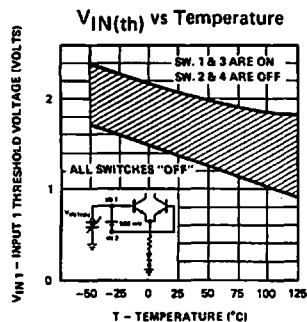
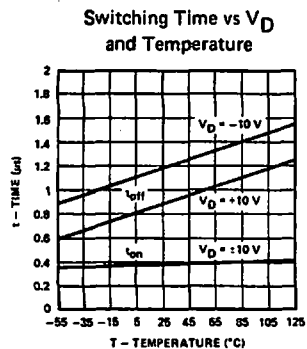
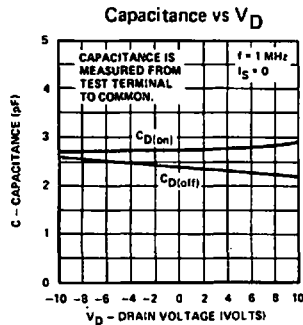
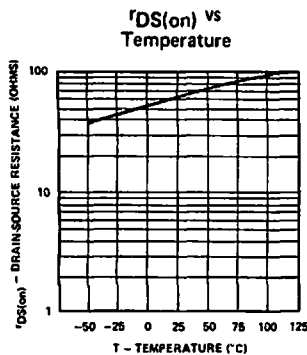
1. Refer to PROCESS OPTION FLOWCHART for additional information.
2. The algebraic convention whereby the most negative value is a minimum, and the most positive value is a maximum, is used in this data sheet.
3. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
4. VIN must be a step function with a minimum rise and fall time of 1 V/μs.

ELECTRICAL CHARACTERISTICS¹ (Cont.)
 T_A = Over Temperature Range

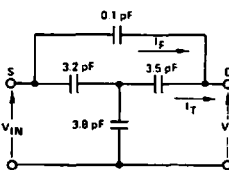
	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: V+ = 12 V, V- = -18 V, VR = 0 VIN2 = 2.5 V		LIMITS						UNITS
					DG142A			DG142B			
					MIN ²	TYP ³	MAX	MIN ²	TYP ³	MAX	
SWITCH	Analog Signal Range	VANALOG			-10		10	-8		8	V
	Drain-Source ON Resistance	rDS(on)	IS = -10 mA VIN1 = 3 V (SW1, 3 ON) VIN1 = 2 V (SW2, 4 ON)	VD = 10 V			150				Ω
				VD = 8 V						150	
	Source OFF Leakage Current	IS(off)	VIN1 = 2 V (SW1, 3 OFF) VIN1 = 3 V (SW2, 4 OFF)	VS = 10 V, VD = -10 V			100				nA
				VS = 8 V, VD = -8 V						100	
	Drain OFF Leakage Current	ID(off)	VIN1 = 3 V (SW1, 3 OFF) VIN1 = 2 V (SW2, 4 OFF)	VD = 10 V, VS = -10 V			100				
				VD = 8 V, VS = -8 V						100	
	Channel ON Leakage Current	ID(on) + IS(on)	VIN1 = 3 V (SW1, 3 ON) VIN1 = 2 V (SW2, 4 ON)	VD = VS = -10 V	-100						
				VD = VS = -8 V				-100			
INPUT	Input 1 Current Input 1 Voltage Low	IIN1L	VIN1 = 2 V				2			4	μA
	Input 2 Current Input 2 Voltage Low	IIN2L	VIN2 = 2 V, VIN1 = 2.5 V				2			4	
	Input 1 Current Input 1 Voltage High	IIN1H	VIN1 = 3 V				120			150	
	Input 2 Current Input 2 Voltage High	IIN2H	VIN2 = 3 V, VIN1 = 2.5 V				120			150	

NOTES:

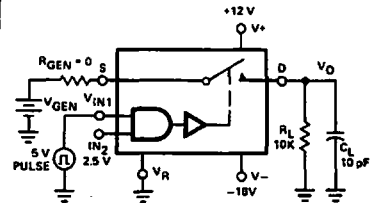
1. Refer to PROCESS OPTION FLOWCHART for additional information.
2. The algebraic convention whereby the most negative value is a minimum, and the most positive value is a maximum, is used in this data sheet.
3. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
4. V_{IN} must be a step function with a minimum rise and fall time of $1\text{ V}/\mu\text{s}$.



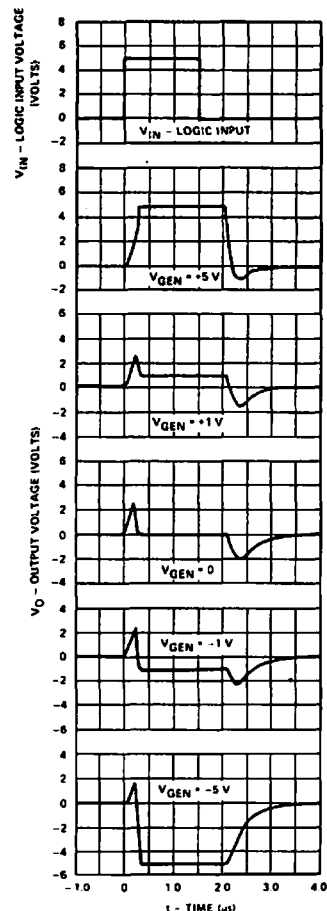
Equivalent "DFF" Circuit



Typical delay, rise, fall, settling times, and switching transients in this circuit.



If R_{GEN} , R_L or C_L is increased, there will be proportional increases in rise and/or fall RC times.



ELECTRICAL CHARACTERISTICS¹ (Cont.)DG139/DG142/DG145
T_A = 25°C

	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: V ₊ = 12 V, V ₋ = -18 V, V _R = 0 V _{IN2} = 2.5 V		LIMITS						UNITS
					OG145A			DG145B			
					MIN ²	TYP ³	MAX	MIN ²	TYP ³	MAX	
SWITCH	Analog Signal Range	V _{ANALOG}			-10		10	-8		8	V
	Drain-Source ON Resistance	r _{DS(on)}	IS = -10 mA V _{IN1} = 3 V (SW ₁ , 3 ON)	V _D = 10 V		7	10				Ω
			V _{IN1} = 2 V (SW ₂ , 4 ON)	V _D = 8 V					15		
	Source OFF Leakage Current	I _{S(off)}	V _{IN1} = 2 V (SW ₁ , 3 OFF)	V _S = 10 V, V _D = -10 V		0.1	10				nA
			V _{IN1} = 3 V (SW ₂ , 4 OFF)	V _S = 8 V, V _D = -8 V					15		
	Drain OFF Leakage Current	I _{D(off)}	V _{IN1} = 3 V (SW ₁ , 3 OFF)	V _D = 10 V, V _S = -10 V		0.1	10				
			V _{IN1} = 2 V (SW ₂ , 4 OFF)	V _D = 8 V, V _S = -8 V					15		
Channel ON Leakage Current	I _{D(on)} + I _{S(on)}	V _{IN1} = 3 V (SW ₁ , 3 ON)	V _D = V _S = -10 V	-2	-0.04						
		V _{IN1} = 2 V (SW ₂ , 4 ON)	V _D = V _S = -8 V				-5				
INPUT	Input 1 Current Input 1 Voltage Low	I _{IN1L}	V _{IN1} = 2 V			0.001	0.1			4	μA
	Input 2 Current Input 2 Voltage Low	I _{IN2L}	V _{IN2} = 2 V, V _{IN1} = 2.5 V			0.001	0.1			4	
	Input 1 Current Input 1 Voltage High	I _{IN1H}	V _{IN1} = 3 V			20	60			100	
	Input 2 Current Input 2 Voltage High	I _{IN2H}	V _{IN2} = 3 V, V _{IN1} = 2.5 V			20	60			100	
DYNAMIC	Turn-ON Time	t _{on}	See Switching Time Test Circuit			0.5	1			1.5	μs
	Turn-OFF Time	t _{off}				1.2	2.5			2.5	
	Drain OFF Capacitance	C _{D(off)}	f = 1 MHz	V _D = 0 V, I _S = 0		3			3		pF
	Source OFF Capacitance	C _{S(off)}		V _S = 0 V, I _D = 0		3			3		
	Channel ON Capacitance	C _D + S (on)		V _D = V _S = 0		2.8			2.8		
	OFF Isolation		R _L = 75 Ω, f = 1 MHz			>50			>50		dB
SUPPLY	Positive Supply Current	I ₊	One Channel ON V _{IN1} = 2 V or V _{IN1} = 3 V			2.6	4.2			4.5	mA
	Negative Supply Current	I ₋			-2	-1.2		-2.2			
	Reference Supply Current	I _R			-2.2	-1.4		-2.4			
	Positive Supply Current	I ₊	All Channel OFF V _{IN1} = V _{IN2} = 0.8 V				25			25	μA
	Negative Supply Current	I ₋			-25			-25			
Reference Supply Current	I _R	-25					-25				

NOTES:

1. Refer to PROCESS OPTION FLOWCHART for additional information.
2. The algebraic convention whereby the most negative value is a minimum, and the most positive value is a maximum, is used in this data sheet.
3. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
4. V_{IN} must be a step function with a minimum rise and fall time of 1 V/μs.

ELECTRICAL CHARACTERISTICS¹ (Cont.)
 T_A = Over Temperature Range

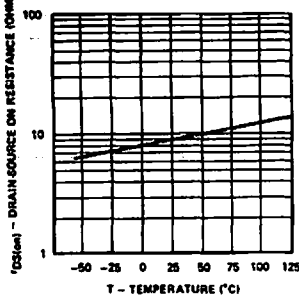
	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: V+ = 12 V, V- = -18 V, V _R = 0 V _{IN2} = 2.5 V		LIMITS						UNITS
					DG145A			DG145B			
					MIN ²	TYP ³	MAX	MIN ²	TYP ³	MAX	
SWITCH	Analog Signal Range	V _{ANALOG}			-10		10	-8		8	V
	Drain-Source ON Resistance	r _{DS(on)}	I _S = -10 mA V _{IN1} = 3 V (SW ₁ , 3 ON)	V _D = 10 V			20				Ω
			V _{IN1} = 2 V (SW ₂ , 4 ON)	V _D = 8 V					25		
	Source OFF Leakage Current	I _{S(off)}	V _{IN1} = 2 V (SW ₁ , 3 OFF)	V _S = 10 V, V _D = -10 V			1000				nA
			V _{IN1} = 3 V (SW ₂ , 4 OFF)	V _S = 8 V, V _D = -8 V					300		
	Drain OFF Leakage Current	I _{D(off)}	V _{IN1} = 3 V (SW ₁ , 3 OFF)	V _D = 10 V, V _S = -10 V			1000				
			V _{IN1} = 2 V (SW ₂ , 4 OFF)	V _D = 8 V, V _S = -8 V					300		
	Channel ON Leakage Current	I _{D(on)} + I _{S(on)}	V _{IN1} = 3 V (SW ₁ , 3 ON)	V _D = V _S = -10 V	-100						
			V _{IN1} = 2 V (SW ₂ , 4 ON)	V _D = V _S = -8 V			-100				
INPUT	Input 1 Current Input 1 Voltage Low	I _{IN1L}	V _{IN1} = 2 V				2			4	μA
	Input 2 Current Input 2 Voltage Low	I _{IN2L}	V _{IN2} = 2 V, V _{IN1} = 2.5 V				2			4	
	Input 1 Current Input 1 Voltage High	I _{IN1H}	V _{IN1} = 3 V				120			150	
	Input 2 Current Input 2 Voltage High	I _{IN2H}	V _{IN2} = 3 V, V _{IN1} = 2.5 V				120			150	

NOTES:

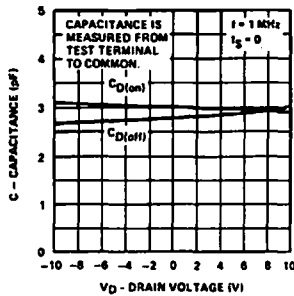
1. Refer to PROCESS OPTION FLOWCHART for additional information.
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4. V_{IN} must be a step function with a minimum rise and fall time of 1 V/ μs .

TYPICAL CHARACTERISTICS

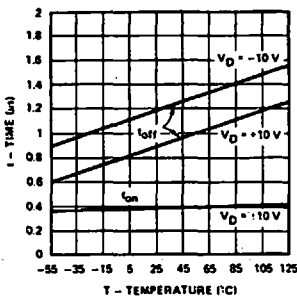
$r_{DS(on)}$ vs Temperature



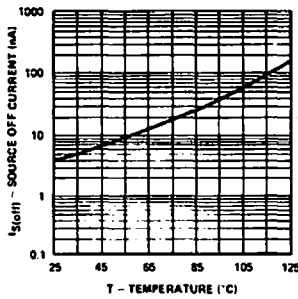
Capacitance vs V_D



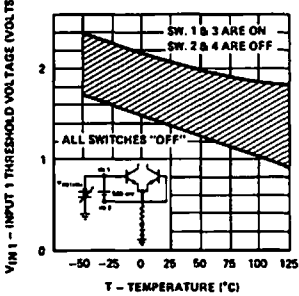
Switching Time vs V_D and Temperature



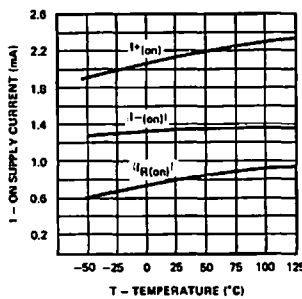
$I_S(off)$ vs Temperature



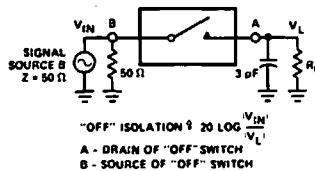
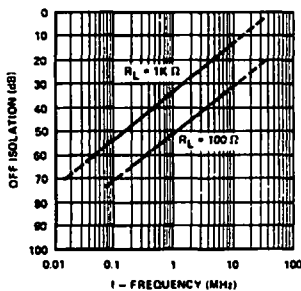
$V_{IN(th)}$ vs Temperature



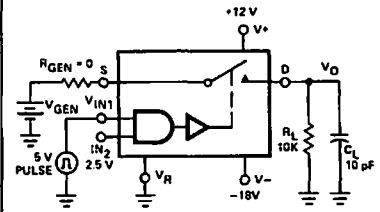
Supply Current vs Temperature



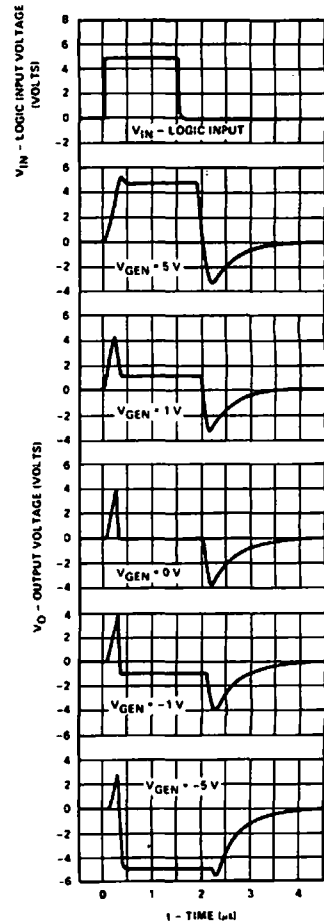
"OFF" Isolation vs R_L and Frequency



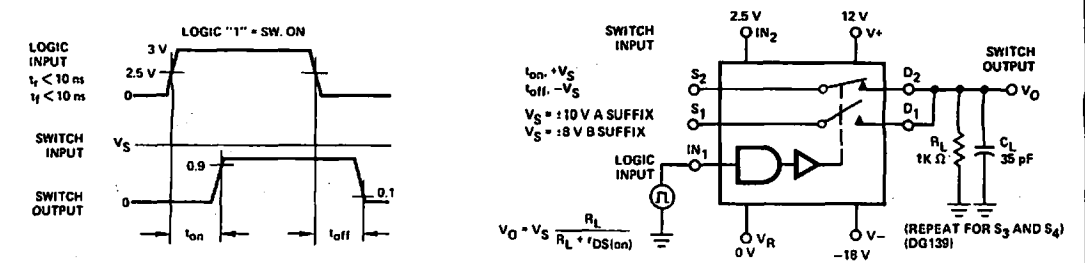
Typical delay, rise, fall, settling times, and switching transients in this circuit.



If R_{GEN} , R_L or C_L is increased, there will be proportional increases in rise and/or fall RC times.



Switch output waveform shown for V_S = constant with logic input waveform as shown. Note that V_S may be + or - as per switching time test circuit. V_O is the steady state output with switch on. Feedthrough via gate capacitance may result in spikes at leading and trailing edge of output waveform.



APPLICATION HINTS

V+ Positive Supply Voltage (V)	V- Negative Supply Voltage (V)	VR Reference Voltage (V)	VIn1 Input 1 Voltage VINH/VINL (V)	VIn2 Input 2 Voltage (V)	VS or VD Analog Voltage Range (V)
12	-18	0	3/2	2.5	-10 to 10
15	-15	0	3/2	2.5	-5 to 13
5	-15	0	3/2	2.5	-5 to 3

2

DYNAL	Drain OFF Capacitance	CD(off)	f = 1 MHz	VD = 0 V, IS = 0	2.4		2.4	pF
	Source OFF Capacitance	CS(off)		VS = 0 V, ID = 0	2.4		2.4	
	Channel ON Capacitance	CD - S (on)		VD = VS = 0	2.8		2.8	
	OFF Isolation		RL = 75 Ω, f = 1 MHz		>60		>60	dB
SUPPLY	Positive Supply Current	I+	One Channel ON VIN1 = 2 V or VIN1 = 3 V		4.2		4.5	mA
	Negative Supply Current	I-		-2		-2.2		
	Reference Supply Current	IR		-2.2		-2.4		
	Positive Supply Current	I+	All Channel OFF VIN1 = VIN2 = 0.8 V		25		25	μA
	Negative Supply Current	I-		-25		-25		
	Reference Supply Current	IR		-25		-25		

- NOTES:
1. Refer to PROCESS OPTION FLOWCHART for additional information.
 2. The algebraic convention whereby the most negative value is a minimum, and the most positive value is a maximum, is used in this data sheet.
 3. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
 4. VIN must be a step function with a minimum rise and fall time of 1 V/μs.

DG143/DG144/DG146

SPDT JFET

Analog Switches



FEATURES

- $< 1 \mu\text{W}$ Standby Power
- Bipolar Drivers
- Constant $r_{DS(on)}$ Over Signal Range
- Off Isolation $> 60 \text{ dB}$ @ 1 MHz

BENEFITS

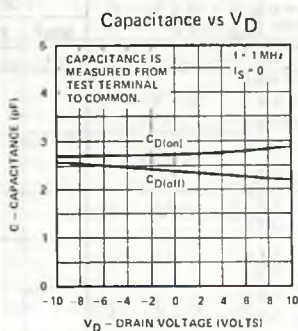
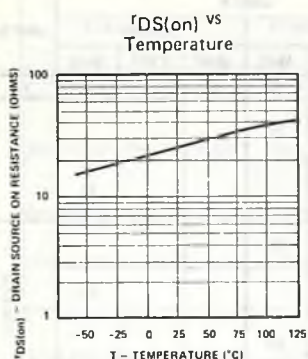
- Minimizes Standby Power Requirement
- Better Radiation Tolerance Than CMOS
- Less Signal Distortion Than CMOS

APPLICATIONS

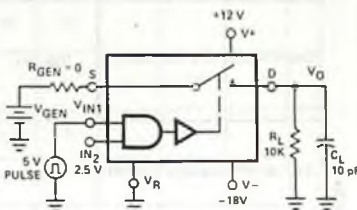
- Portable and Battery Powered Systems
- Switching In Satellite Applications
- Low Distortion Circuits
- High Frequency Switching

TYPICAL CHARACTERISTICS

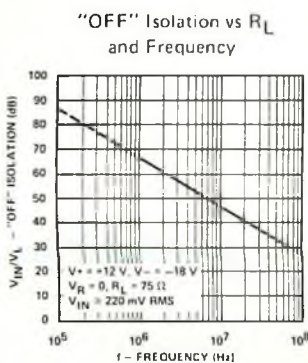
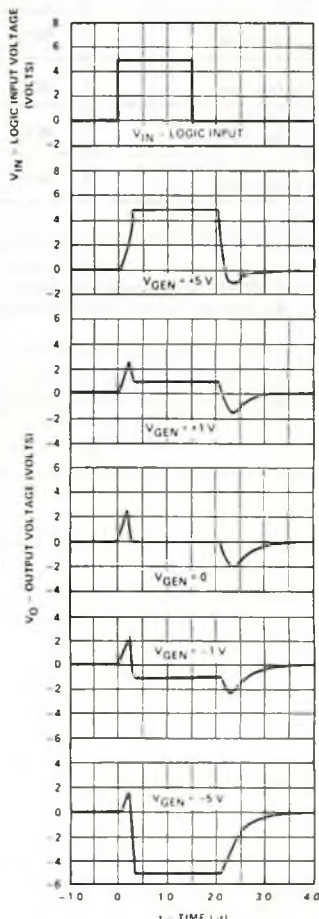
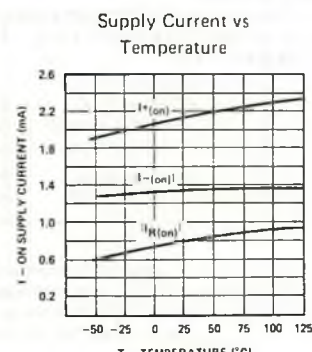
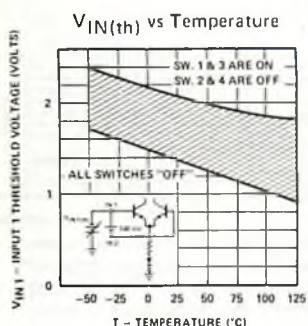
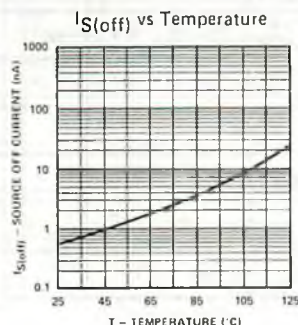
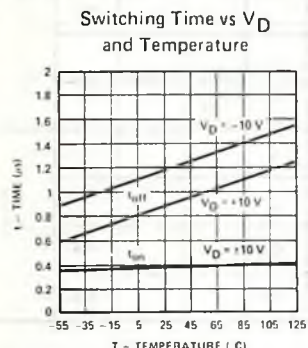
DG143/DG144/DG146



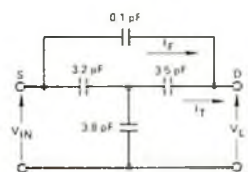
Typical delay, rise, fall, settling times, and switching transients in this circuit.



If R_{GEN} , R_L or C_L is increased, there will be proportional increases in rise and/or fall RC times.

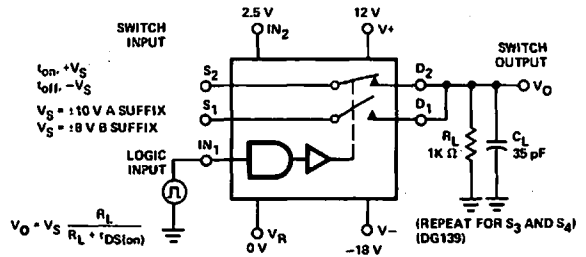
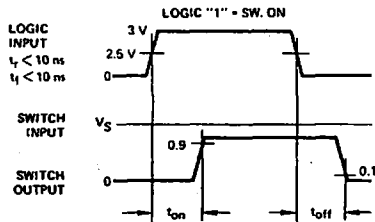


Equivalent "OFF" Circuit



SWITCHING TIME TEST CIRCUIT

Switch output waveform shown for $V_S = \text{constant}$ with logic input waveform as shown. Note that V_S may be + or - as per switching time test circuit. V_O is the steady state output with switch on. Feedthrough via gate capacitance may result in spikes at leading and trailing edge of output waveform.



APPLICATION HINTS

V+ Positive Supply Voltage (V)	V- Negative Supply Voltage (V)	V _R Reference Voltage (V)	V _{in1} Input 1 Voltage V _{INH} /V _{INL} (V)	V _{in2} Input 2 Voltage (V)	V _S or V _D Analog Voltage Range (V)
12	-18	0	3/2	2.5	-10 to 10
15	-15	0	3/2	2.5	-5 to 13
5	-15	0	3/2	2.5	-5 to 3

DG143/DG144/DG146

SPDT JFET

Analog Switches



FEATURES

- $< 1 \mu\text{W}$ Standby Power
- Bipolar Drivers
- Constant $r_{DS(on)}$ Over Signal Range
- Off Isolation $> 60 \text{ dB}$ @ 1 MHz

BENEFITS

- Minimizes Standby Power Requirement
- Better Radiation Tolerance Than CMOS
- Less Signal Distortion Than CMOS
- Higher Frequency Switching

APPLICATIONS

- Portable and Battery Powered Systems
- Switching In Satellite Applications
- Low Distortion Circuits
- High Frequency Switching Circuits

DESCRIPTION

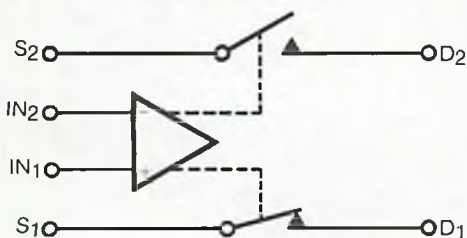
DG143/DG144/DG146 are precision single-pole double-throw analog switches designed for applications where constant ON resistance over the entire analog range is an important consideration. The major design difference is in ON resistance, being 10, 30 and 80 Ω for the DG146, DG144, DG143 respectively.

The DG143, DG144 and DG146 each contain two junction-type field-effect transistors (JFETs) designed to function as single-pole double-throw electronic switches. Level-shifting drivers enable low-level inputs (2.0 to 3.0 V) to control the ON-OFF state of the switches. The driver inputs are connected differentially so that with input IN2 connected to a 2.5 voltage reference, a positive logic "0" at the input IN1 will turn switches 1 and 3 OFF and switches 2 and 4 ON. A positive logic "1" at IN1 will turn switches 1

and 3 ON and switches 2 and 4 OFF. The normally grounded VR terminal may be used as an "inhibit" terminal, in which case all switches may be held OFF with a positive voltage applied to VR. In the ON state each switch conducts equally well in either direction, and in the OFF state each switch will block voltages up to 20 V peak-to-peak. ON resistance of the DG143 is $< 80 \Omega$, the DG144 $< 30 \Omega$ and the DG146 is $< 10 \Omega$ and ON shunt leakage for all three $< 2 \text{ nA}$. With the driver in the "switch OFF" state total power consumption is $< 750 \mu\text{W}$. Due to the processing all three analog switches are relatively radiation tolerant.

DG143/DG144/DG146 are available in the 14-lead dual-inline sidebrazed and flatpack, and are specified over the industrial (-25 to 85°C), and military (-55 to 125°C) temperature ranges.

FUNCTIONAL BLOCK DIAGRAM



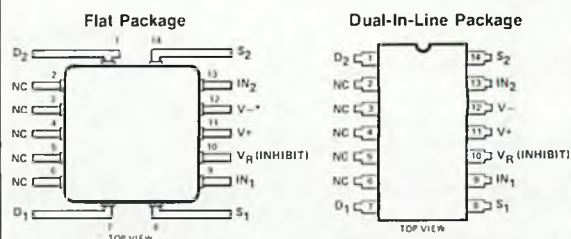
One SPDT Switch per Package*

Truth Table

LOGIC	SW 1	SW 2
0	OFF	ON
1	ON	OFF

*Switches Shown for Logic "1" Input at IN₁, and 2.5 V Reference at IN₂.

PIN CONFIGURATION



Order Numbers:
DG143AL, DG144AL,
or DG146AL
See Package 5

Order Numbers:
DG143AP, DG143BP,
DG144AP, DG144BP,
DG146AP, DG146BP
See Package 11

*Common to Substrate and Base of Package

ABSOLUTE MAXIMUM RATINGS

V+ to V-, V _D or V _S	36 V
V _D or V _S to V-	36 V
V _D to V _S	±22 V
V+ to V _R	25 V
V+ to V _{IN1} or V _{IN2}	25 V
V _R to V-	25 V
V _{IN1} to V _{IN2}	±6 V
V _{IN1} or V _{IN2} to V _R	±6 V
V _{IN1} or V _{IN2} to V-	30 V
Current (Any Terminal)	30 mA

Storage Temperature	-65 to 150°C
Operating Temperature (A Suffix)	-55 to 125°C
(B Suffix)	-25 to 85°C
Power Dissipation*	
Flat Package**	750 mW
14 Pin DIP***	825 mW

*All leads welded or soldered to PC board.

**Derate 10 mW/°C above 75°C.

***Derate 11 mW/°C above 75°C.

ELECTRICAL CHARACTERISTICS¹T_A = 25°C

	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: V ₊ = 12 V, V ₋ = -18 V, V _R = 0 V _{IN2} = 2.5 V		LIMITS						UNITS
					DG143A			DG143B			
					MIN ²	TYP ³	MAX	MIN ²	TYP ³	MAX	
SWITCH	Analog Signal Range	V _{ANALOG}			-10		10	-8		8	V
	Drain-Source ON Resistance	r _{DS(on)}	IS = -10 mA VIN1 = 3 V (SW1, 3 ON)	VD = 10 V			80				Ω
			VIN1 = 2 V (SW2, 4 ON)	VD = 8 V				100			
	Source OFF Leakage Current	IS(off)	VIN1 = 2 V (SW1, 3 OFF)	VS = 10 V, VD = -10 V			1				nA
	VIN1 = 3 V (SW2, 4 OFF)	VS = 8 V, VD = -8 V				5					
	Drain OFF Leakage Current	ID(off)	VIN1 = 3 V (SW1, 3 OFF)	VD = 10 V, VS = -10 V			1				
	VIN1 = 2 V (SW2, 4 OFF)	VD = 8 V, VS = -8 V				5					
	Channel ON Leakage Current	ID(on) + IS(on)	VIN1 = 3 V (SW1, 3 ON)	VD = VS = -10 V	-2						
VIN1 = 2 V (SW2, 4 ON)			VD = VS = -8 V				-5				
INPUT	Input 1 Current Input 1 Voltage Low	IIN1L	VIN1 = 2 V			.0005	0.1			4	μA
	Input 2 Current Input 2 Voltage Low	IIN2L	VIN2 = 2 V, VIN1 = 2.5 V			0.001	0.1			4	
	Input 1 Current Input 1 Voltage High	IIN1H	VIN1 = 3 V			25	60			100	
	Input 2 Current Input 2 Voltage High	IIN2H	VIN2 = 3 V, VIN1 = 2.5 V			25	60			100	
DYNAMIC	Turn-ON Time	t _{on}	See Switching Time Test Circuit			0.5	0.8			1.0	μs
	Turn-OFF Time	t _{off}				1.1	1.6			2.0	
	Drain OFF Capacitance	CD(off)	f = 1 MHz	VD = 0 V, IS = 0		2.4			2.4	pF	
	Source OFF Capacitance	CS(off)		VS = 0 V, ID = 0		2.4			2.4		
	Channel ON Capacitance	CD + S (on)		VD = VS = 0		2.8			2.8		
	OFF Isolation		RL = 75 Ω, f = 1 MHz			>60			>60		dB
SUPPLY	Positive Supply Current	I+	One Channel ON VIN1 = 2 V or VIN1 = 3 V			4.2			4.5	mA	
	Negative Supply Current	I-		-2			-2.2				
	Reference Supply Current	IR		-2.2			-2.4				
	Positive Supply Current	I+	All Channel OFF VIN1 = VIN2 = 0.8 V			25			25	μA	
	Negative Supply Current	I-		-25			-25				
	Reference Supply Current	IR		-25			-25				

NOTES:

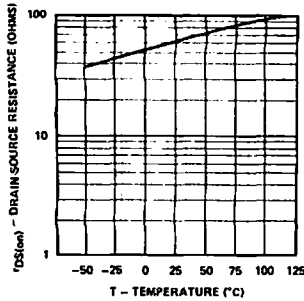
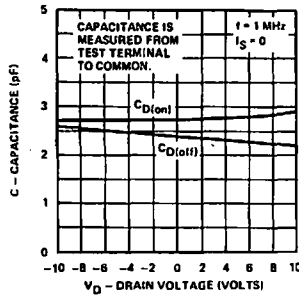
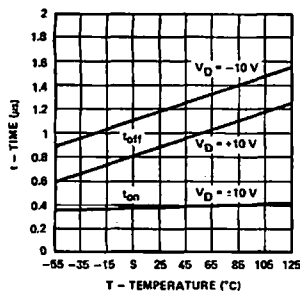
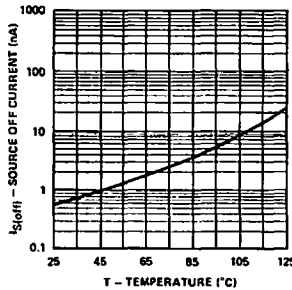
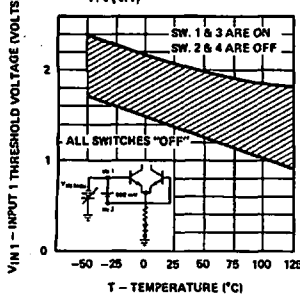
1. Refer to PROCESS OPTION FLOWCHART for additional information.
2. The algebraic convention whereby the most negative value is a minimum, and the most positive value is a maximum, is used in this data sheet.
3. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
4. V_{IN} must be a step function with a minimum rise and fall time of 1 V/μs.

ELECTRICAL CHARACTERISTICS¹ (Cont.) T_A = Over Temperature Range

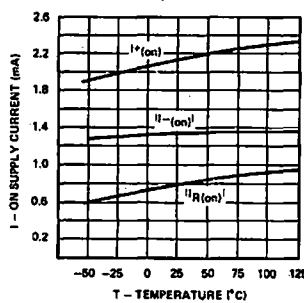
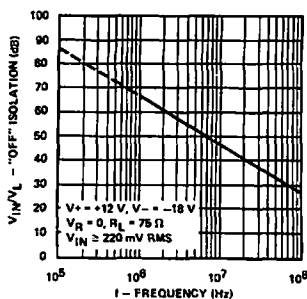
	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: $V_+ = 12\text{ V}$, $V_- = -18\text{ V}$, $V_R = 0$ $V_{IN2} = 2.5\text{ V}$		LIMITS						UNITS
					DG143A			DG143B			
					MIN ²	TYP ³	MAX	MIN ²	TYP ³	MAX	
SWITCH	Analog Signal Range	V_{ANALOG}			-10		10	-8		8	V
	Drain-Source ON Resistance	$r_{DS(on)}$	$I_S = -10\text{ mA}$ $V_{IN1} = 3\text{ V}$ (SW1, 3 ON)	$V_D = 10\text{ V}$			150				Ω
			$V_{IN1} = 2\text{ V}$ (SW2, 4 ON)	$V_D = 8\text{ V}$				150			
	Source OFF Leakage Current	$I_{S(off)}$	$V_{IN1} = 2\text{ V}$ (SW1, 3 OFF)	$V_S = 10\text{ V}$, $V_D = -10\text{ V}$			100				
			$V_{IN1} = 3\text{ V}$ (SW2, 4 OFF)	$V_S = 8\text{ V}$, $V_D = -8\text{ V}$				100			
	Drain OFF Leakage Current	$I_{D(off)}$	$V_{IN1} = 3\text{ V}$ (SW1, 3 OFF)	$V_D = 10\text{ V}$, $V_S = -10\text{ V}$			100				nA
			$V_{IN1} = 2\text{ V}$ (SW2, 4 OFF)	$V_D = 8\text{ V}$, $V_S = -8\text{ V}$				100			
Channel ON Leakage Current	$I_{D(on)} + I_{S(on)}$	$V_{IN1} = 3\text{ V}$ (SW1, 3 ON)	$V_D = V_S = -10\text{ V}$	-100							
		$V_{IN1} = 2\text{ V}$ (SW2, 4 ON)	$V_D = V_S = -8\text{ V}$				-100				
INPUT	Input 1 Current Input 1 Voltage Low	I_{IN1L}	$V_{IN1} = 2\text{ V}$				2			4	μA
	Input 2 Current Input 2 Voltage Low	I_{IN2L}	$V_{IN2} = 2\text{ V}$, $V_{IN1} = 2.5\text{ V}$				2			4	
	Input 1 Current Input 1 Voltage High	I_{IN1H}	$V_{IN1} = 3\text{ V}$			35	120			150	
	Input 2 Current Input 2 Voltage High	I_{IN2H}	$V_{IN2} = 3\text{ V}$, $V_{IN1} = 2.5\text{ V}$			35	120			150	

NOTES:

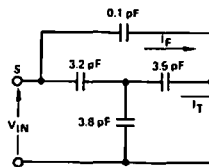
1. Refer to PROCESS OPTION FLOWCHART for additional information.
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$r_{DS(on)}$ vs TemperatureCapacitance vs V_D Switching Time vs V_D and Temperature $I_S(off)$ vs Temperature $V_{IN(th)}$ vs Temperature

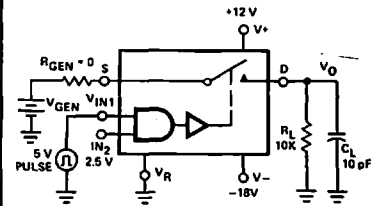
Supply Current vs Temperature

"OFF" Isolation vs R_L and Frequency

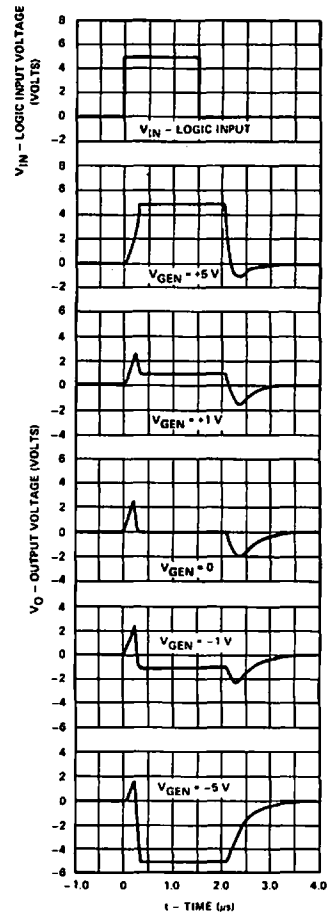
Equivalent "OFF" Circuit



Typical delay, rise, fall, settling times, and switching transient in this circuit.



If R_{GEN} , R_L or C_L is increased, there will be proportional increases in rise and/or fall RC times.



ELECTRICAL CHARACTERISTICS¹ (Cont.) $T_A = 25^\circ\text{C}$

	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: V+ = 12 V, V- = -18 V, VR = 0 VIN2 = 2.5 V	LIMITS						UNITS	
				DG144A			DG144B				
				MIN ²	TYP ³	MAX	MIN ²	TYP ³	MAX		
SWITCH	Analog Signal Range	VANALOG		-10		10	-8		8	V	
	Drain-Source ON Resistance	rDS(on)	IS = -10 mA VIN1 = 3 V (SW1, 3 ON)		20	30				Ω	
			VIN1 = 2 V (SW2, 4 ON)				35	50			
	Source OFF Leakage Current	IS(off)	VIN1 = 2 V (SW1, 3 OFF)	VS = 10 V, VD = -10 V	0.15	1				nA	
			VIN1 = 3 V (SW2, 4 OFF)	VS = 8 V, VD = -8 V			0.75	5			
	Drain OFF Leakage Current	ID(off)	VIN1 = 3 V (SW1, 3 OFF)	VD = 10 V, VS = -10 V	0.03	1				nA	
			VIN1 = 2 V (SW2, 4 OFF)	VD = 8 V, VS = -8 V			0.15	5			
	Channel ON Leakage Current	ID(on) + IS(on)	VIN1 = 3 V (SW1, 3 ON)	VD = VS = -10 V	-2	-0.05					
			VIN1 = 2 V (SW2, 4 ON)	VD = VS = -8 V			-5	-0.12			
	INPUT	Input 1 Current Input 1 Voltage Low	IIN1L	VIN1 = 2 V		.0003	0.1		0.012	4	μA
		Input 2 Current Input 2 Voltage Low	IIN2L	VIN2 = 2 V, VIN1 = 2.5 V		.0005	0.1		0.02	4	
Input 1 Current Input 1 Voltage High		IIN1H	VIN1 = 3 V		24	60		40	100		
Input 2 Current Input 2 Voltage High		IIN2H	VIN2 = 3 V, VIN1 = 2.5 V		25	60		40	100		
DYNAMIC	Turn-ON Time	ton	See Switching Time Test Circuit		0.5	0.8		0.6	1	μs	
	Turn-OFF Time	toff			1.2	1.6		1.5	2		
	Drain OFF Capacitance	CD(off)	f = 1 MHz	VD = 0 V, IS = 0		2.4		2.4		pF	
	Source OFF Capacitance	CS(off)		VS = 0 V, ID = 0		2.4		2.4			
	Channel ON Capacitance	CD + S (on)		VD = VS = 0		2.8		2.8			
	OFF Isolation			RL = 75 Ω, f = 1 MHz		>60		>60			
SUPPLY	Positive Supply Current	I+	One Channel ON VIN1 = 2 V or VIN1 = 3 V		2.6	4.2		2.6	4.5	mA	
	Negative Supply Current	I-		-2	-1.3		-2.2	-1.3			
	Reference Supply Current	IR		-2.2	-1.4		-2.4	-1.4			
	Positive Supply Current	I+	All Channel OFF VIN1 = VIN2 = 0.8 V		0.75	25		0.75	25	μA	
	Negative Supply Current	I-		-25			-25				
	Reference Supply Current	IR		-25			-25				

NOTES:

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- V_{IN} must be a step function with a minimum rise and fall time of $1\text{ V}/\mu\text{s}$.

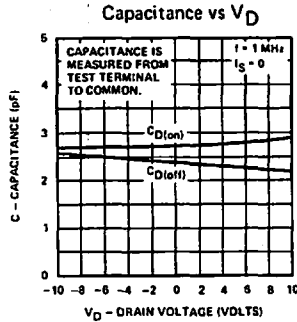
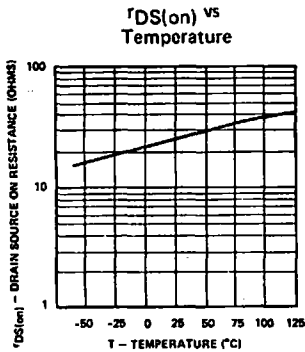
ELECTRICAL CHARACTERISTICS¹ (Cont.) T_A = Over Temperature Range

	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: V+ = 12 V, V- = -18 V, VR = 0 VIN2 = 2.5 V		LIMITS						UNITS
					DG144A			DG144B			
					MIN2	TYP3	MAX	MIN2	TYP3	MAX	
SWITCH	Analog Signal Range	VANALOG			-10		10	-8		8	V
	Drain-Source ON Resistance	rDS(on)	IS = -10 mA VIN1 = 3 V (SW1, 3 ON)	VD = 10 V			60				Ω
			VIN1 = 2 V (SW2, 4 ON)	VD = 8 V					75		
	Source OFF Leakage Current	IS(off)	VIN1 = 2 V (SW1, 3 OFF)	VS = 10 V, VD = -10 V			100				nA
			VIN1 = 3 V (SW2, 4 OFF)	VS = 8 V, VD = -8 V					100		
	Drain OFF Leakage Current	ID(off)	VIN1 = 3 V (SW1, 3 OFF)	VD = 10 V, VS = -10 V			100				
			VIN1 = 2 V (SW2, 4 OFF)	VD = 8 V, VS = -8 V					100		
	Channel ON Leakage Current	ID(on) + IS(on)	VIN1 = 3 V (SW1, 3 ON)	VD = VS = -10 V	-100						
			VIN1 = 2 V (SW2, 4 ON)	VD = VS = -8 V				-100			
INPUT	Input 1 Current Input 1 Voltage Low	IIN1L	VIN1 = 2 V				2			4	μA
	Input 2 Current Input 2 Voltage Low	IIN2L	VIN2 = 2 V, VIN1 = 2.5 V				2			4	
	Input 1 Current input 1 Voltage High	IIN1H	VIN1 = 3 V				120			150	
	Input 2 Current Input 2 Voltage High	IIN2H	VIN2 = 3 V, VIN1 = 2.5 V				120			150	

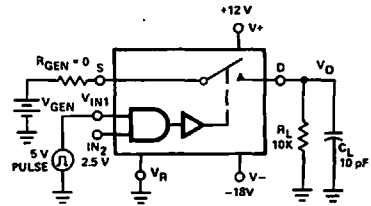
NOTES:

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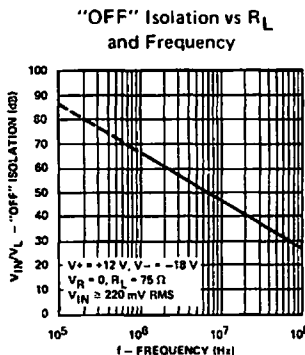
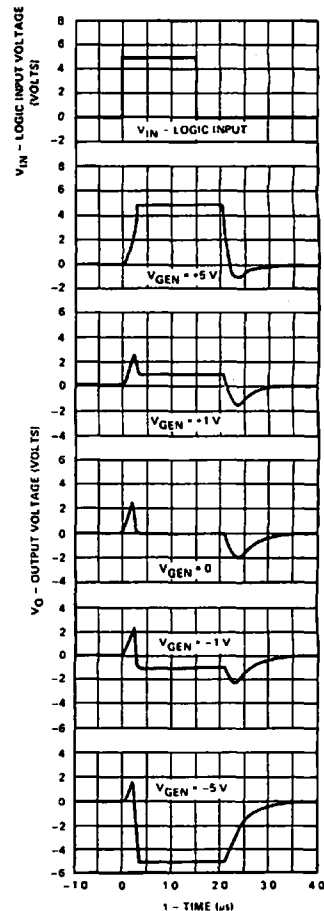
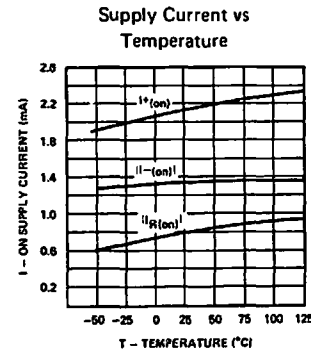
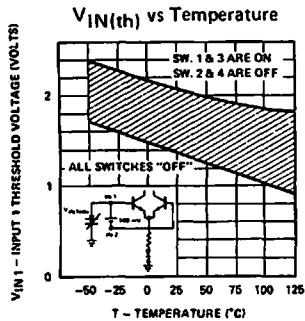
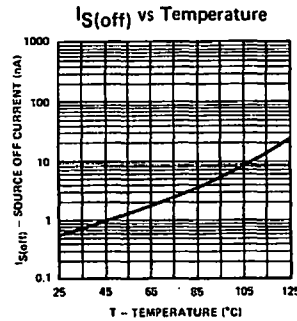
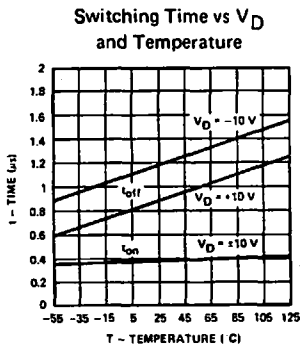
TYPICAL CHARACTERISTICS



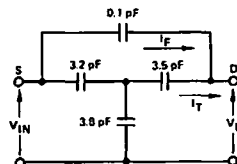
Typical delay, rise, fall, settling times, and switching transients in this circuit.



If R_{GEN} , R_L or C_L is increased, there will be proportional increases in rise and/or fall RC times.



Equivalent "OFF" Circuit



ELECTRICAL CHARACTERISTICS¹ (Cont.) $T_A = 25^\circ\text{C}$

DG143/DG144/DG146

	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: V+ = 12 V, V- = -18 V, VR = 0 VIN2 = 2.5 V		LIMITS						UNITS
					DG146A			DG146B			
					MIN ²	TYP ³	MAX	MIN ²	TYP ³	MAX	
SWITCH	Analog Signal Range	VANALOG			-10		10	-8		8	V
	Drain-Source ON Resistance	rDS(on)	IS = -10 mA VIN1 = 3 V (SW1, 3 ON) VD = 10 V		7	10					Ω
			VIN1 = 2 V (SW2, 4 ON) VD = 8 V						15		
	Source OFF Leakage Current	IS(off)	VIN1 = 2 V (SW1, 3 OFF) VS = 10 V, VD = -10 V		0.1	10					
			VIN1 = 3 V (SW2, 4 OFF) VS = 8 V, VD = -8 V						15		
	Drain OFF Leakage Current	ID(off)	VIN1 = 3 V (SW1, 3 OFF) VD = 10 V, VS = -10 V		0.1	10					nA
		VIN1 = 2 V (SW2, 4 OFF) VD = 8 V, VS = -8 V						15			
Channel ON Leakage Current	ID(on) + IS(on)	VIN1 = 3 V (SW1, 3 ON) VD = VS = -10 V	-2	-0.04							
		VIN1 = 2 V (SW2, 4 ON) VD = VS = -8 V					-5				
INPUT	Input 1 Current Input 1 Voltage Low	IIN1L	VIN1 = 2 V			0.001	0.1			4	μA
	Input 2 Current Input 2 Voltage Low	IIN2L	VIN2 = 2 V, VIN1 = 2.5 V			0.001	0.1			4	
	Input 1 Current Input 1 Voltage High	IIN1H	VIN1 = 3 V			20	60			100	
	Input 2 Current Input 2 Voltage High	IIN2H	VIN2 = 3 V, VIN1 = 2.5 V			20	60			100	
DYNAMIC	Turn-ON Time	tON	See Switching Time Test Circuit			0.5	1			1.5	μs
	Turn-OFF Time	tOFF				1.2	2.5			2.5	
	Drain OFF Capacitance	CD(off)	f = 1 MHz	VD = 0 V, IS = 0		3			3		pF
	Source OFF Capacitance	CS(off)		VS = 0 V, ID = 0		3			3		
	Channel ON Capacitance	CD + S (on)		VD = VS = 0		2.8			2.8		
OFF Isolation		RL = 75 Ω, f = 1 MHz			>50			>50		dB	
SUPPLY	Positive Supply Current	I+	One Channel ON VIN1 = 2 V or VIN1 = 3 V			2.6	4.2			4.5	mA
	Negative Supply Current	I-			-2	-1.2		-2.2			
	Reference Supply Current	IR			-2.2	-1.4		-2.4			
	Positive Supply Current	I+	All Channel OFF VIN1 = VIN2 = 0.8 V				25			25	μA
	Negative Supply Current	I-			-25			-25			
	Reference Supply Current	IR			-25			-25			

NOTES:

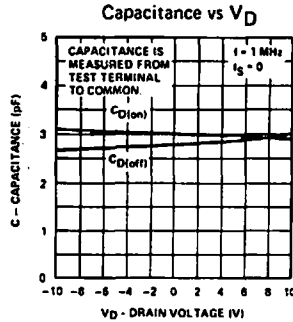
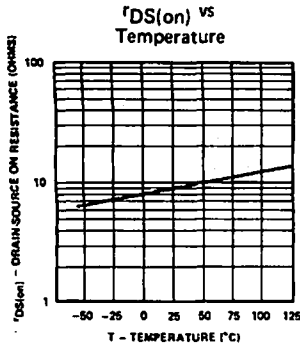
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ELECTRICAL CHARACTERISTICS¹ (Cont.) T_A = Over Temperature Range

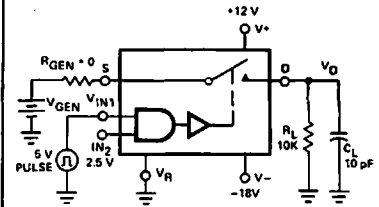
	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: V+ = 12 V, V- = -18 V, VR = 0 VIN2 = 2.5 V		LIMITS						UNITS
					DG146A			DG146B			
					MIN ²	TYP ³	MAX	MIN ²	TYP ³	MAX	
SWITCH	Analog Signal Range	VANALOG		-10		10	-8		8	V	
	Drain-Source ON Resistance	rDS(on)	IS = -10 mA VIN1 = 3 V (SW1, 3 ON)	VD = 10 V			20			Ω	
			VIN1 = 2 V (SW2, 4 ON)	VD = 8 V					25		
	Source OFF Leakage Current	IS(off)	VIN1 = 2 V (SW1, 3 OFF)	VS = 10 V, VD = -10 V			1000			nA	
			VIN1 = 3 V (SW2, 4 OFF)	VS = 8 V, VD = -8 V					300		
	Drain OFF Leakage Current	ID(off)	VIN1 = 3 V (SW1, 3 OFF)	VD = 10 V, VS = -10 V			1000				
			VIN1 = 2 V (SW2, 4 OFF)	VD = 8 V, VS = -8 V					300		
	Channel ON Leakage Current	ID(on) + IS(on)	VIN1 = 3 V (SW1, 3 ON)	VD = VS = -10 V		-100					
VIN1 = 2 V (SW2, 4 ON)			VD = VS = -8 V				-100				
INPUT	Input 1 Current Input 1 Voltage Low	IIN1L	VIN1 = 2 V			2			4	μA	
	Input 2 Current Input 2 Voltage Low	IIN2L	VIN2 = 2 V, VIN1 = 2.5 V			2			4		
	Input 1 Current Input 1 Voltage High	IIN1H	VIN1 = 3 V			120			150		
	Input 2 Current Input 2 Voltage High	IIN2H	VIN2 = 3 V, VIN1 = 2.5 V			120			150		

NOTES:

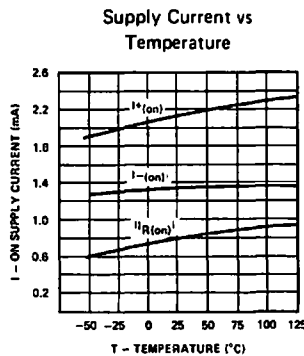
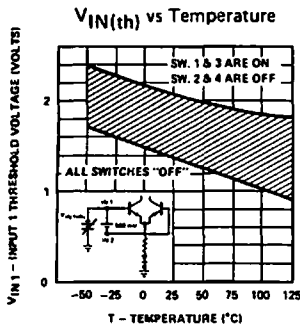
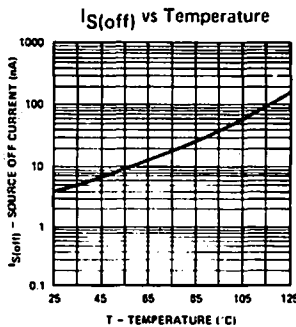
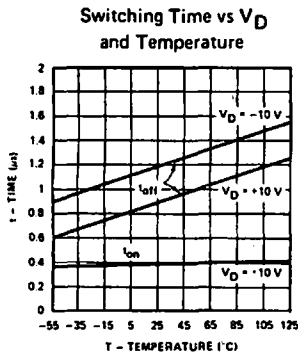
1. Refer to PROCESS OPTION FLOWCHART for additional information.
2. The algebraic convention whereby the most negative value is a minimum, and the most positive value is a maximum, is used in this data sheet.
3. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
4. V_{IN} must be a step function with a minimum rise and fall time of 1 V/μs.



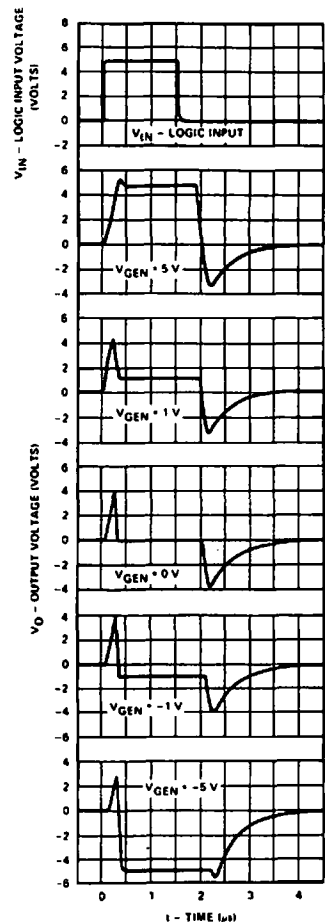
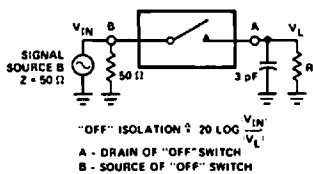
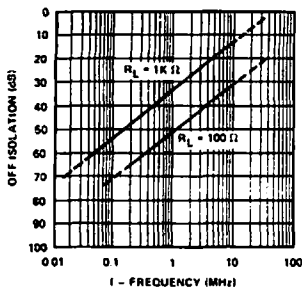
Typical delay, rise, fall, settling times, and switching transients in this circuit.



If R_{GEN} , R_L or C_L is increased, there will be proportional increases in rise and/or fall RC times.

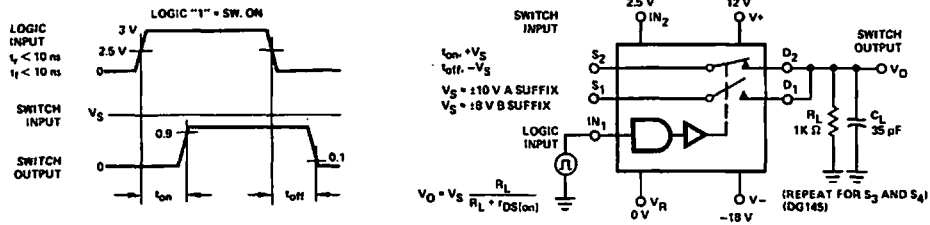


"OFF" Isolation vs R_L and Frequency



SWITCHING TIME TEST CIRCUIT

Switch output waveform shown for $V_S =$ constant with logic input waveform as shown. Note that V_S may be + or - as per switching time test circuit. V_O is the steady state output with switch on. Feedthrough via gate capacitance may result in spikes at leading and trailing edge of output waveform.


APPLICATION HINTS

V+ Positive Supply Voltage (V)	V- Negative Supply Voltage (V)	V _R Reference Voltage (V)	V _{in1} Input 1 Voltage V _{INH} /V _{INL} (V)	V _{in2} Input 2 Voltage (V)	V _S or V _D Analog Voltage Range (V)
+12	-18	0	3/2	2.5	-10 to +10
+15	-15	0	3/2	2.5	-5 to +13
+10	-15	0	3/2	2.5	-5 to +3

DG172

Monolithic 4-Channel PMOS Analog Switch



FEATURES

- TTL, CMOS, DTL Direct Interface
- Voltage Limiting Diodes Protect PMOS Gates
- Four Independent Switches
- Chip Select Pin (V_L)
- Make-Before-Break Switching

BENEFITS

- Easy Interface
- Reduces External Protection Components
- Easily Expandable
- Will Not Leave Op Amp Input Floating

APPLICATIONS

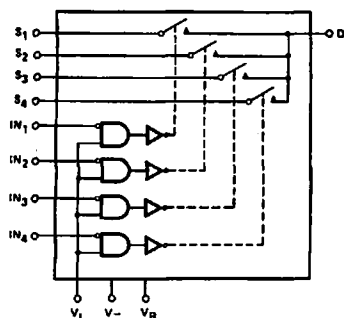
- Programmable Gain Amplifiers
- Sample/Hold
- Solid-State Logic Trees

DESCRIPTION

The DG172 is a 4-channel single-pole, single-throw analog switch designed for low level logic controlled analog switching in instrumentation, process control, and communications. Featuring make-before-break action, DG172 can be used inside closed loop systems to select one of four inputs for multiplexing/demultiplexing of analog signals or for gain bandwidth control (by switching passive elements) without opening the loop. The reference pin (V_R) is normally connected to ground to allow a low-level

input (0.4 V to 1.3 V) to control the ON-OFF condition of each switch. DG172 is a bi-directional MOS switch rated to handle 20 V peak-to-peak analog signals at up to 30 mA continuous current. Each switch will block 20 V peak-to-peak signals when OFF. Package options are the 14-pin ceramic DIP and flatpack. The former is characterized for operation over the standard industrial and military temperature ranges, while the latter is specified for the military range only.

FUNCTIONAL BLOCK DIAGRAM



One 4-Channel Switch per Package*

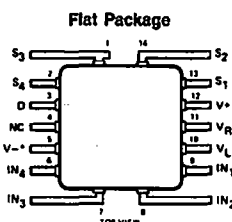
Truth Table

LOGIC	SWITCH
0	ON
1	OFF

Logic "0" ≤ 0.8 V
Logic "1" ≥ 2.0 V

*Switches Shown for Logic "1" Input

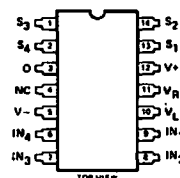
PIN CONFIGURATION



Order Number:
DG172AL
See Package 5

*Common to Substrate and Base of Package

Dual-In-Line Package



Order Numbers:
DG172AP or DG172BP
See Package 11
DG172CJ
See Package 7

ABSOLUTE MAXIMUM RATINGS

V+ to V-	36 V
V+ to V _D	25 V
V+ to V _S	25 V
V _S to V-	36 V
V _D to V-	36 V
V _S to V _D	25 V
V _L to V-	30 V
V _L to V _{IN}	±6 V
V _L to V _R	±6 V
V _{IN} to V _R	±6 V
Current (Any Terminal)	20 mA
Storage Temperature (A & B Suffix)	-65 to 150°C
(C Suffix)	-65 to 125°C

Operating Temperature (A Suffix) -55 to 125°C
 (B Suffix) -25 to 85°C
 (C Suffix) 0 to 70°C

Power Dissipation (Package)*

Flat Package** 750 mW
 14 Pin Ceramic DIP*** 825 mW
 14 Pin Plastic DIP**** 470 mW

*All leads welded or soldered to PC board

**Derate 10 mW/°C above 75°C

***Derate 11 mW/°C above 75°C

****Derate 6.3 mW/°C above 75°C

ELECTRICAL CHARACTERISTICS¹T_A = 25°C

	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: V ₊ = 10 V, V ₋ = -20 V, V _R = 0 V, V _L = 5 V	LIMITS									UNIT
				DG172A			DG172B			DG172C			
				MIN ²	TYP ³	MAX	MIN ²	TYP ³	MAX	MIN ²	TYP ³	MAX	
SWITCH	Analog Signal Range	V _{ANALOG}		-10		10	-10		10	-10		10	V
	Drain-Source ON Resistance	r _{DS(on)}	I _S = 1 nA, V _{in} = 0.8 V			V _D = 10 V	100	150		150		200	Ω
						V _D = 0	130	200		225		300	
						V _D = 10 V	300	450		500		600	
	Source OFF Leakage Current	I _{S(off)}	V _S = -10 V, V _D = 10 V, V _{in} = 0.8 V	-1	-0.03		-5		-10			nA	
	Drain OFF Leakage Current	I _{D(off)}	V _D = -10 V, V _S = 10 V, V _{in} = 2 V	-4	-0.12		-10		-10				
Channel ON Leakage Current	I _{D(on)} ⁺ I _{S(on)}	V _D = V _S = 10 V, V _{in} = 0.8 V			4		10		10				
INPUT	Input Current With Input Voltage High	I _{INH}	V _{in} = 5 V			0.1		1		1	μA		
	Input Current With Input Voltage Low	I _{INL}	V _{in} = 0	-0.5			-1		-1		mA		
DYNAMIC	Turn-ON Time	t _{on}	See Switching Time Test Circuit			0.3		0.5		0.08	μs		
	Turn-OFF Time	t _{off}				0.75		1.0		0.5			
	Source OFF Capacitance	C _{S(off)}	V _S = 0 V, I _D = 0, f = 1 MHz		5		5		5	pF			
	Drain OFF Capacitance	C _{D(off)}	V _D = 0 V, I _S = 0, f = 1 MHz		18		18		18				
	Channel ON Capacitance	C _{D + S (on)}	V _D = V _S = 0 V, V _{in} = 0 V, f = 140 kHz		28		28		28				
	OFF Isolation		R _L = 100 Ω, C _L = 3 pF, f = 5 MHz		>50		>50		>50		dB		
	Positive Supply Current	I ₊			1.3	3		3		3			
Negative Supply Current	I ₋			-5.1	-2.0		-5.1						
SUPPLY	Logic Supply Current	I _L	One Channel ON V _{in} = 0		2.5	5.7		5.7		5.7	mA		
				I _R = 0		0.8	2.1		2.1			2.1	
	Reference Supply Current	I _R		-3.6	-1.5		-3.6		-3.6				
	Positive Supply Current	I ₊	All Channels OFF V _{in} = 5 V		0.1	10		10		10	μA		
	Negative Supply Current	I ₋			-20	-0.01		-20		-20			
					2.0	4.5		4.5		4.5	mA		
Logic Supply Current	I _L			I _R = 0		0.1	10		10		μA		
	Reference Supply Current	I _R		-4.5	-2.0		-4.5		-4.5		mA		

NOTES:

1. Refer to PROCESS OPTION FLOWCHART for additional information.
2. The algebraic convention whereby the most negative value is a minimum, and the most positive is a maximum, is used in this data sheet.
3. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

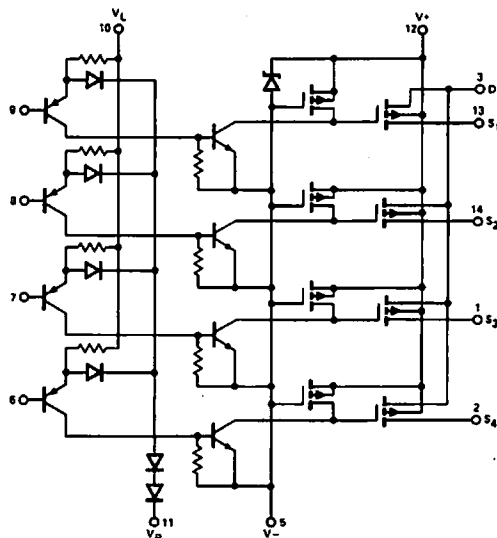
ELECTRICAL CHARACTERISTICS¹ (Cont.) T_A = Over Temperature Range**DG172**

	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: V _I = 10 V, V ₋ = -20 V, V _R = 0 V, V _L = 5 V	LIMITS						UNIT
				DG172A			DG172B			
				MIN ²	TYP ³	MAX	MIN ²	TYP ³	MAX	
SWITCH	Analog Signal Range	V _{ANALOG}		-10		10	-10		10	V
	Drain-Source ON Resistance	r _{DS(on)}	I _S = -1 mA V _{in} = 0.8 V		250				200	Ω
			V _D = 0		350				300	
			V _D = -10 V		600				600	
	Source OFF Leakage Current	I _{S(off)}	V _S = -10 V, V _D = 10 V, V _{in} = 2 V	-1000			-100			nA
	Drain OFF Leakage Current	I _{D(off)}	V _D = -10 V, V _S = 10 V, V _{in} = 2 V	-4000			-300			
Channel ON Leakage Current	I _{D(on)} ⁺ I _{S(on)}	V _D = V _S = 10 V, V _{in} = 2 V			4000			300		
INPUT	Input Current With Input Voltage High	I _{INH}	V _{in} = 5 V			10			10	μA
	Input Current With Input Voltage Low	I _{INL}	V _{in} = 0	-0.5			-1			mA

NOTES:

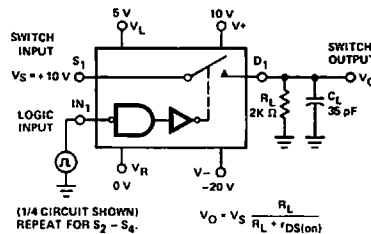
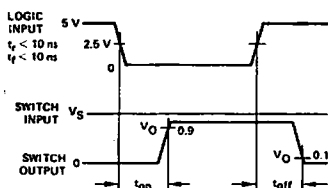
1. Refer to PROCESS OPTION FLOWCHART for additional information.
2. The algebraic convention whereby the most negative value is a minimum, and the most positive is a maximum, is used in this data sheet.
3. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

SCHEMATIC DIAGRAM



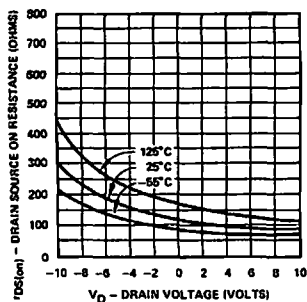
SWITCHING TIME TEST CIRCUIT

Switch output waveform shown for $V_S = \text{constant}$ with logic input waveform as shown. Note that V_S may be + or - as per switching time test circuit. V_O is the steady state output with switch on. Feedthrough via gate capacitance may result in spikes at leading and trailing edge of output waveform.

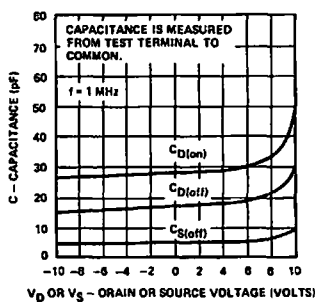


TYPICAL CHARACTERISTICS

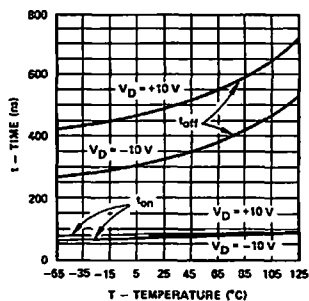
$r_{DS(on)}$ vs V_D and Temperature



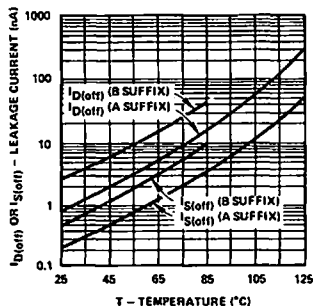
Capacitance vs V_D or V_S



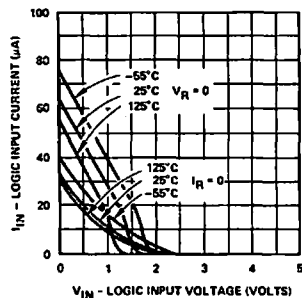
Switching Time vs V_D and Temperature



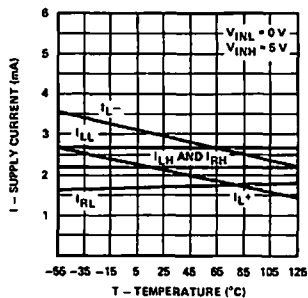
$I_D(off)/I_S(off)$ vs Temperature



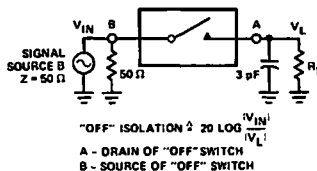
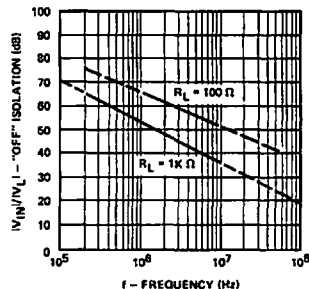
I_{IN} vs V_{IN} and Temperature



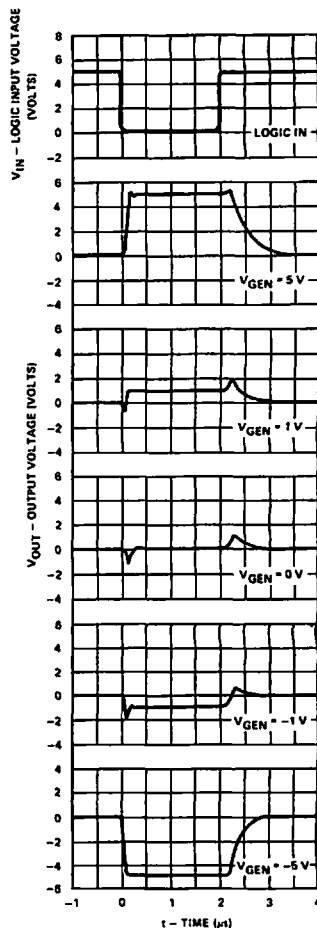
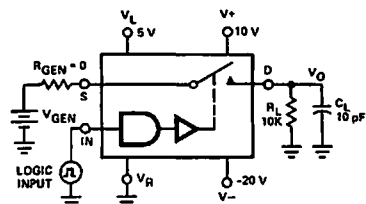
Supply Current vs Temperature



"OFF" Isolation vs R_L and Frequency



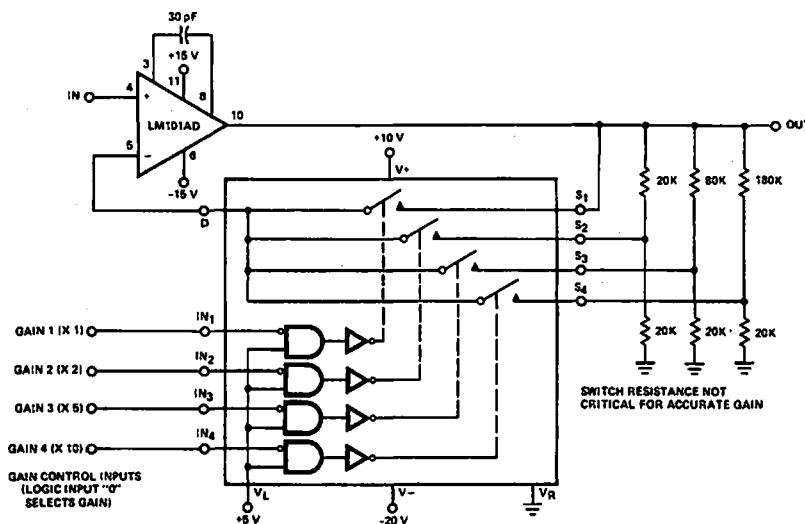
Typical delay, rise, fall, settling times, and switching transients in this circuit.



V+	V-	V _R	V _L	V _{IN}	V _S
Positive Supply Voltage (V)	Negative Supply Voltage (V)	Reference Pin Connection	Logic Supply Voltage (V)	Logic Input Voltage V _{INH} Min/ V _{INL} Max (V)	Analog Signal Range (V)
10*	-20	Gnd	5	2.0/0.8	-10 to +10
10*	-20	Open	5	4.6/0.5	-10 to +10
15	-15	Gnd	5	2.0/0.8	-5 to +15
20	-10	Gnd	5	2.0/0.8	0 to +20
5	-15	Gnd	5	2.0/0.8	-5 to +5
5	-25	Gnd	5	2.0/0.8	-15 to +5

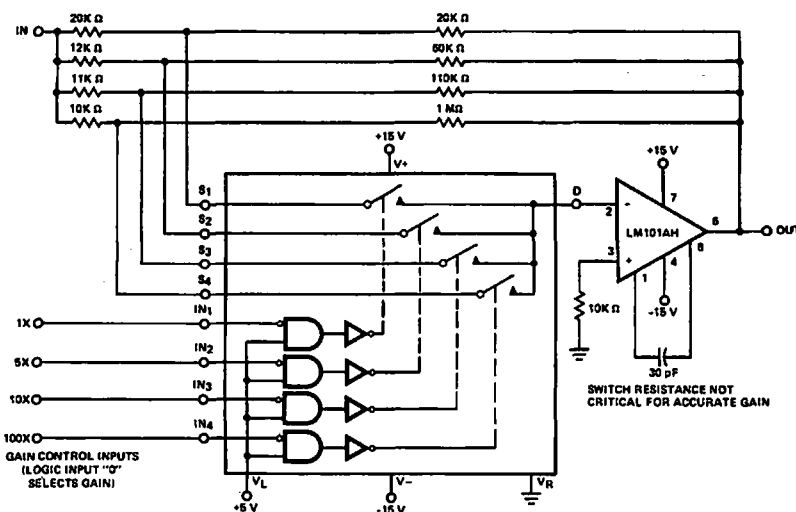
Application Hints are for DESIGN AID ONLY, not guaranteed and not subject to production testing.

*Electrical Characteristics are based on V+ = +10 V, V- = -20 V only.



Non-Inverting Programmable Gain Amplifier

Figure 1



Inverting Programmable Gain Amplifier

Figure 2

DG180/DG181/DG182

High-Speed Driver with Dual SPST JFET Switches



FEATURES

- Constant ON Resistance over Entire Analog Range
- Low Leakage
- Low Crosstalk

BENEFITS

- Low Distortion
- Eliminates Large Signal Errors
- High Bandwidth Capability

APPLICATIONS

- Video Switching
- Audio Switching
- Sample/Hold
- D/A Ladder Switches

DESCRIPTION

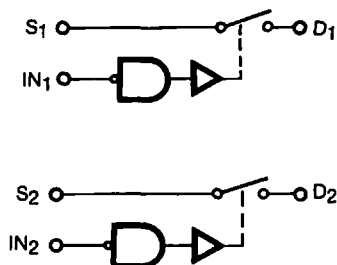
The DG180-182 are precision 2-channel single-pole, single-throw analog switches designed for applications where constant ON resistance over the entire analog range is an important consideration. The major design difference is in ON resistance, being 10, 30 and 75 Ω for the DG180, DG181 and DG182 respectively.

Each device comprises two N-channel JFET transistor and a CMOS driver (TTL compatible) to achieve state of the art performance. The JFET switches provide constant ON resistance, independent of the analog input, insuring

low distortion in precision audio and process control applications. The driver is designed to achieve Break-Before-Make action, in the ON state each switch conducts current equally well in either direction. In the OFF condition the switches will block up to 20 V peak-to-peak, with feedthrough less than -60 dB at 10 MHz.

DG180-182 are available in the 10 lead metal can, 16-lead sidebrake and flatpack packages, specified over the industrial (-25 to 85°C), and military (-55 to 125°C) temperature ranges.

FUNCTIONAL BLOCK DIAGRAM



Two SPST Switches per Package*

Truth Table

LOGIC	SWITCH
0	ON
1	OFF

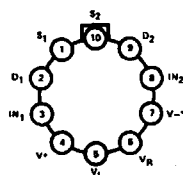
Logic "0" ≤ 0.8 V

Logic "1" ≥ 2.0 V

*Switches Shown for Logic "1" Input

PIN CONFIGURATION

Metal Can Package

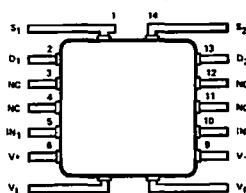


TOP VIEW

Order Numbers:
DG180AA or DG180BA
DG181AA or DG181BA
DG182AA or DG182BA
See Package 2

*Common to Substrate and Case

Flat Package

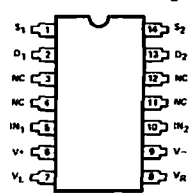


TOP VIEW

Order Numbers:
DG181AL
See Package 5

*Common to Substrate and Base of Package

Dual-In-Line Package

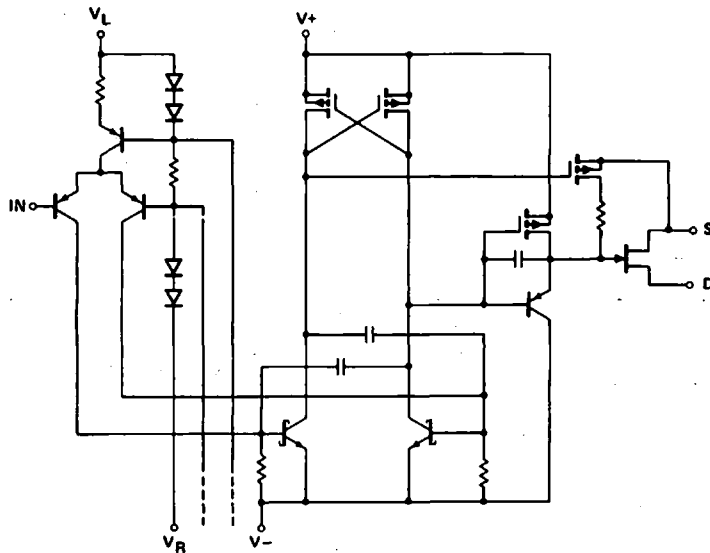


TOP VIEW

Order Numbers:
DG180AP or DG180BP
DG181AP or DG181BP
DG182AP or DG182BP
See Package 11

ABSOLUTE MAXIMUM RATINGS

V_+ to V_-	36 V	Storage Temperature	-65 to 150°C
V_+ to V_D	33 V	Operating Temperature	
V_D to V_-	33 V	A Suffix.....	-55 to 125°C
V_D to V_S	± 35 V	B Suffix.....	-25 to 85°C
V_L to V_-	8 V	Power Dissipation*	
V_L to V_{in}	8 V	Metal Can**.....	450 mW
V_L to V_R	8 V	14 Pin DIP***.....	825 mW
V_{in} to V_R	8 V	Flat Pack****.....	900 mW
V_R to V_-	27 V		
V_R to V_{in}	8 V	*All leads welded or soldered to PC board	
Current (S or D)		**Derate 6 mW/°C above 75°C	
DG180	200 mA	***Derate 11 mW/°C above 75°C	
DG181, DG182	30 mA		
Current (All Other Pins)	30 mA	****Derate 10 mW/°C above 75°C	

SCHEMATIC DIAGRAM (Typical Channel)


ELECTRICAL CHARACTERISTICS¹
 $T_A = 25^\circ\text{C}$

	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: V ⁺ = 15 V, V ⁻ = -15 V, V _L = 5 V, V _R = 0 V	LIMITS						UNIT
				DG180A			DG180B			
				MIN ²	TYP ³	MAX	MIN ²	TYP ³	MAX	
SWITCH	Analog Signal Range	V _{ANALOG}		-7.5		15	-7.5		15	V
	Drain-Source ON Resistance	r _{DS(on)}	I _S = -1 mA, V _D = 7.5 V, V _{in} = 0.8 V		7.5	10			15	Ω
	Source OFF Leakage Current	I _{S(off)}	V _{in} = 2.0 V	V _S = 10 V, V _D = -10 V V ⁺ = 10 V, V ⁻ = -20 V	0.05	10			15	nA
		V _S = 7.5 V, V _D = -7.5 V		0.05	10			15		
	Drain OFF Leakage Current	I _{D(off)}		V _S = 10 V, V _D = -10 V V ⁺ = 10 V, V ⁻ = -20 V	0.04	10			15	
		V _S = 7.5 V, V _D = -7.5 V	0.03	10			15			
	Channel ON Leakage Current	I _{D(on)} ⁺ I _{S(on)}	V _D = V _S = 7.5 V, V _{in} = 0.8 V	-2	-0.1		-10		15	
Saturation Drain Current	I _{DSS}	2 ms Pulse Duration		300		300			mA	
INPUT	Input Current With Input Voltage High	I _{INH}	V _{in} = 5 V		<0.01	10			10	μA
	Input Current With Input Voltage Low	I _{INL}	V _{in} = 0	-250	-30		-250			
DYNAMIC	Turn-ON Time	t _{on}	See Switching Time Test Circuit		240	300			300	ns
	Turn-OFF Time	t _{off}			140	250			300	
	Source OFF Capacitance	C _{S(off)}	f = 1 MHz	V _S = -5 V, I _D = 0	21			21		pF
	Drain OFF Capacitance	C _{D(off)}		V _D = -5 V, I _S = 0	17			17		
	Channel ON Capacitance	C _D + S (on)		V _D = V _S = 0	17			17		
	OFF Isolation		f = 1 MHz, R _L = 75 Ω	>55			>55			dB
SUPPLY	Positive Supply Current	I ⁺	V _{in(all)} = 0 V		0.6	1.5		0.6	1.5	mA
	Negative Supply Current	I ⁻		-5	-2.7		-5	-2.7		
	Reference Supply Current	I _R		-2	-0.9		-2	-0.9		
	Positive Supply Current	I ⁺	V _{in(all)} = 5 V		0.6	1.5		0.6	1.5	
	Negative Supply Current	I ⁻		-5	-2.7		-5	-2.7		
	Logic Supply Current	I _L			3.0	4.5		3.0	4.5	
	Reference Supply Current	I _R		-2	-1.0		-2	-1.0		

 $T_A = \text{Over Temperature Range}$

	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: V+ = 15 V, V- = -15 V, VL = 5 V, VR = 0 V	LIMITS						UNIT
				DG180A			DG180B			
				MIN ²	TYP ³	MAX	MIN ²	TYP ³	MAX	
SWITCH	Analog Signal Range	VANALOG		-7.5		15	-7.5		15	V
	Drain-Source ON Resistance	rDS(on)	IS = -1 mA, VD = 7.5 V, VIN = 0.8 V			20			25	Ω
	Source OFF Leakage Current	IS(off)	VIN = 2.0 V	VS = 10 V, VD = -10 V V+ = 10 V, V- = -20 V		1000			300	nA
		VS = 7.5 V, VD = - 7.5 V			1000			300		
	Drain OFF Leakage Current	ID(off)		VS = 10 V, VD = -10 V V+ = 10 V, V- = -20 V		1000			300	
			VS = 7.5 V, VD = - 7.5 V		1000			300		
	Channel ON Leakage Current	ID(on)+ IS(on)	VD = VS = 7.5 V, VIN = 0.8 V	-200			-200			
INPUT	Input Current With Input Voltage High	IINH	VIN = 5 V			20			20	μA
	Input Current With Input Voltage Low	IINL	VIN = 0	-250			-250			

NOTES:

1. Refer to PROCESS OPTION FLOWCHART for additional information
2. The algebraic convention whereby the most negative value is a minimum, and the most positive value is a maximum, is used in this data sheet.
3. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

ELECTRICAL CHARACTERISTICS¹ (Cont.)T_A = 25°C

DG180/DG181/DG182

	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: V ₊ = 15 V, V ₋ = -15 V, V _L = 5 V, V _R = 0 V	LIMITS						UNIT		
				DG181A			DG181B					
				MIN ²	TYP ³	MAX	MIN ²	TYP ³	MAX			
SWITCH	Analog Signal Range	V _{ANALOG}				-7.5		15	-7.5		15	V
	Drain-Source ON Resistance	r _{DS(on)}	I _S = -1 mA, V _D = 7.5 V, V _{in} = 0.8 V				18	30			50	Ω
	Source OFF Leakage Current	I _{S(off)}	V _{in} = 2.0 V	V _S = 10 V, V _D = -10 V V ₊ = 10 V, V ₋ = -20 V			0.06	1			5	nA
		V _S = 7.5 V, V _D = -7.5 V			0.1	1			5			
	Drain OFF Leakage Current	I _{D(off)}		V _S = 10 V, V _D = -10 V V ₊ = 10 V, V ₋ = -20 V			0.5	1			5	
		V _S = 7.5 V, V _D = -7.5 V			0.6	1				5		
	Channel ON Leakage Current	I _{D(on)} ⁺ I _{S(on)}	V _D = V _S = 7.5 V, V _{in} = 0.8 V			-2	-0.02		-10			
INPUT	Input Current With Input Voltage High	I _{INH}	V _{in} = 5 V					10			10	μA
	Input Current With Input Voltage Low	I _{INL}	V _{in} = 0			-250	-30		-250			
DYNAMIC	Turn-ON Time	t _{on}	See Switching Time Test Circuit				85	150			180	ns
	Turn-OFF Time	t _{off}					95	130			150	
	Source OFF Capacitance	C _{S(off)}	f = 1 MHz	V _S = -5 V, I _D = 0			9			9		pF
	Drain OFF Capacitance	C _{D(off)}		V _D = -5 V, I _S = 0			6			6		
	Channel ON Capacitance	C _D + S (on)		V _D = V _S = 0			14			14		
SUPPLY	OFF Isolation		f = 1 MHz, R _L = 75 Ω				>50			>50		dB
	Positive Supply Current	I ₊	V _{in(all)} = 0 V				0.6	1.5		0.6	1.5	mA
	Negative Supply Current	I ₋				-5.0	-2.7		-5.0	-2.7		
	Logic Supply Current	I _L					3.1	4.5		3.1	4.5	
	Reference Supply Current	I _R				-2.0	-1.0		-2.0	-1.0		
	Positive Supply Current	I ₊	V _{in(all)} = 5 V				0.6	1.5		0.6	1.5	
	Negative Supply Current	I ₋				-5.0	-2.7		-2.7			
	Logic Supply Current	I _L					3.1	4.5		3.1	4.5	
	Reference Supply Current	I _R				-2.0	-1.0		-2.0	-1.0		

T_A = Over Temperature Range

	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: V+ = 15 V, V- = -15 V, VL = 5 V, VR = 0 V	LIMITS						UNIT
				DG181A			DG181B			
				MIN ²	TYP ³	MAX	MIN ²	TYP ³	MAX	
SWITCH	Analog Signal Range	VANALOG		-7.5		15	-7.5		15	V
	Drain-Source ON Resistance	rDS(on)	IS = -1 mA, VD = 7.5 V, VIN = 0.8 V			60			75	Ω
	Source OFF Leakage Current	IS(off)	VIN = 2.0 V	VS = 10 V, VD = -10 V V+ = 10 V, V- = -20 V		100			100	nA
		VS = 7.5 V, VD = -7.5 V			100			100		
	Drain OFF Leakage Current	ID(off)		VS = 10 V, VD = -10 V V+ = 10 V, V- = -20 V		100			100	
			VS = 7.5 V, VD = -7.5 V		100			100		
Channel ON Leakage Current	ID(on)+ IS(on)	VD = VS = 7.5 V, VIN = 0.8 V	-200			-200				
INPUT	Input Current With Input Voltage High	IINH	VIN = 5 V			20			20	μA
	Input Current With Input Voltage Low	IINL	VIN = 0	-250			-250			

NOTES:

1. Refer to PROCESS OPTION FLOWCHART for additional information
2. The algebraic convention whereby the most negative value is a minimum, and the most positive value is a maximum, is used in this data sheet.
3. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

ELECTRICAL CHARACTERISTICS¹ (Cont.) $T_A = 25^\circ\text{C}$

	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: V+ = 15 V, V- = -15 V, VL = 5 V, VR = 0 V		LIMITS						UNIT
					DG182A			DG182B			
					MIN ²	TYP ³	MAX	MIN ²	TYP ³	MAX	
SWITCH	Analog Signal Range	VANALOG			-10		15	-10		15	V
	Drain-Source ON Resistance	rDS(on)	IS = -1 mA, VD = 7.5 V, VIN = 0.8 V			35	75			100	Ω
	Source OFF Leakage Current	IS(off)	VIN = 2.0 V	VS = 10 V, VD = -10 V V+ = 10 V, V- = -20 V		0.05	1			5	nA
		VS = 7.5 V, VD = -7.5 V			0.5	1			5		
	Drain OFF Leakage Current	ID(off)		VS = 10 V, VD = -10 V V+ = 10 V, V- = -20 V		6.4	1			5	
		VS = 7.5 V, VD = -7.5 V			0.5	1			5		
Channel ON Leakage Current	ID(on)+ IS(on)	VD = VS = 7.5 V, VIN = 0.8 V		-2	-0.03		-10				
INPUT	Input Current With Input Voltage High	IINH	VIN = 5 V				10				μA
	Input Current With Input Voltage Low	IINL	VIN = 0		-250	-35		-250			
DYNAMIC	Turn-ON Time	ton	See Switching Time Test Circuit			120	250			300	ns
	Turn-OFF Time	toff				100	130			150	
	Source OFF Capacitance	CS(off)	f = 1 MHz	VS = -5 V, ID = 0		9			9		pF
	Drain OFF Capacitance	CD(off)		VD = -5 V, IS = 0		6			6		
	Channel ON Capacitance	CD + S (on)		VD = VS = 0		14			14		
	OFF Isolation		f = 1 MHz, RL = 75 Ω			>50			>50		dB
SUPPLY	Positive Supply Current	I+	VIN(all) = 0 V				1.5			1.5	mA
	Negative Supply Current	I-			-5			-5			
	Logic Supply Current	IL					4.5			4.5	
	Reference Supply Current	IR			-2			-2			
	Positive Supply Current	I+	VIN(all) = 5 V				1.5			1.5	mA
	Negative Supply Current	I-			-5			-5			
	Logic Supply Current	IL					4.5			4.5	
	Reference Supply Current	IR			-2			-2			

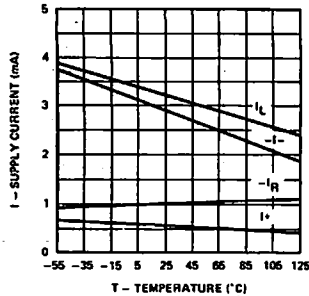
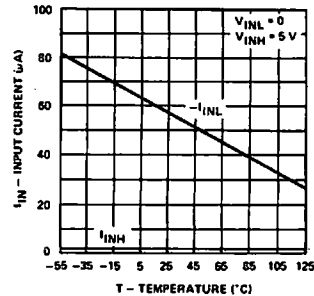
 $T_A = \text{Over Temperature Range}$

	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: V+ = 15 V, V- = -15 V, VL = 5 V, VR = 0 V		LIMITS						UNIT	
					DG182A			DG182B				
					MIN ²	TYP ³	MAX	MIN ²	TYP ³	MAX		
SWITCH	Analog Signal Range	VANALOG			-10			15	-10		15	V
	Drain-Source ON Resistance	rDS(on)	IS = -1 mA, VD = 7.5 V, VIN = 0.8 V					150			150	Ω
	Source OFF Leakage Current	IS(off)	VIN = 2.0 V	VS = 10 V, VD = -10 V V+ = 10 V, V- = -20 V				100			100	nA
				VS = 7.5 V, VD = -7.5 V				100		100		
	Drain OFF Leakage Current	ID(off)		VS = 10 V, VD = -10 V V+ = 10 V, V- = -20 V				100		100		
				VS = 7.5 V, VD = -7.5 V				100		100		
Channel ON Leakage Current	ID(on)+ IS(on)	VD = VS = 7.5 V, VIN = 0.8 V		-200				-200				
INPUT	Input Current With Input Voltage High	IINH	VIN = 5 V					20			20	μA
	Input Current With Input Voltage Low	IINL	VIN = 0		-250				-250			

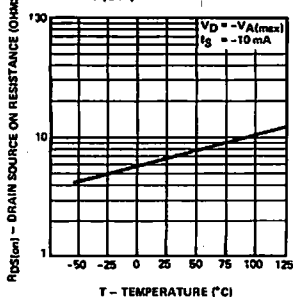
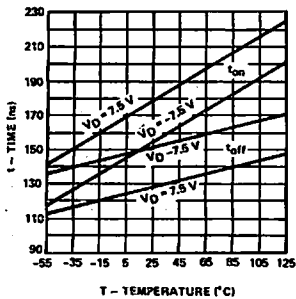
NOTES:

1. Refer to PROCESS OPTION FLOWCHART for additional information.
2. The algebraic convention whereby the most negative value is a minimum, and the most positive is a maximum, is used in this data sheet.
3. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

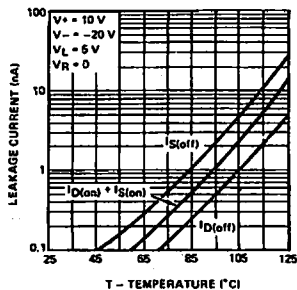
Supply Current vs Temperature


 I_{IN} vs V_{IN} and Temperature

10 Ω

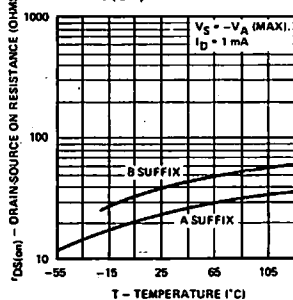
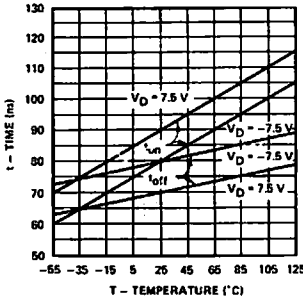
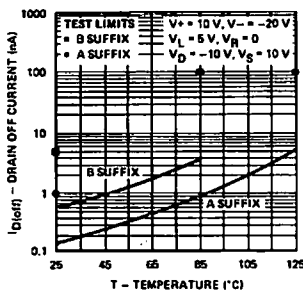
DG180

 $r_{DS(on)}$ vs Temperature

Switching Time vs V_D and Temperature


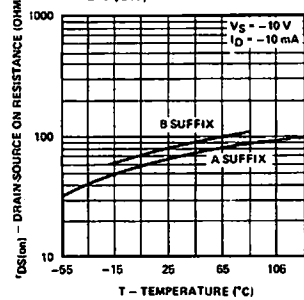
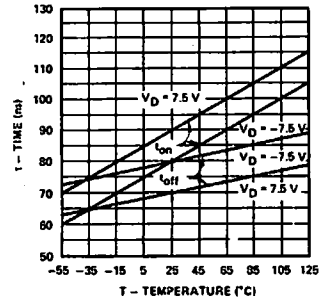
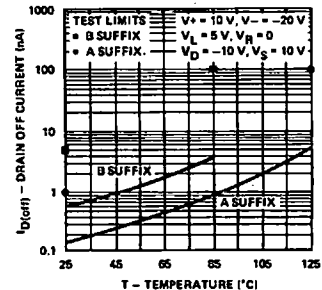
Leakage vs Temperature


30 Ω

DG181

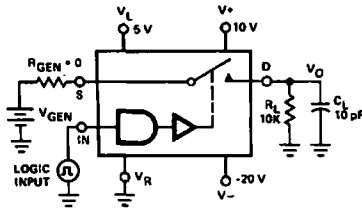
 $r_{DS(on)}$ vs Temperature

Switching Time vs V_D and Temperature

 $I_D(off)$ vs Temperature

75 Ω

DG182

 $r_{DS(on)}$ vs Temperature

Switching Time vs V_D and Temperature

 $I_D(off)$ vs Temperature


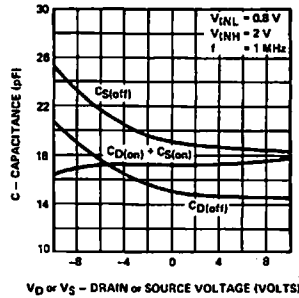
TYPICAL CHARACTERISTICS (Cont.)

Typical delay, rise, fall, settling times, and switching transients in this circuit.

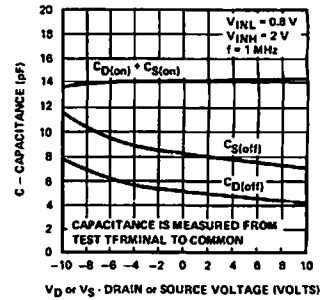


If R_{GEN} , R_L or C_L is increased, there will be proportional increases in rise and/or fall times.

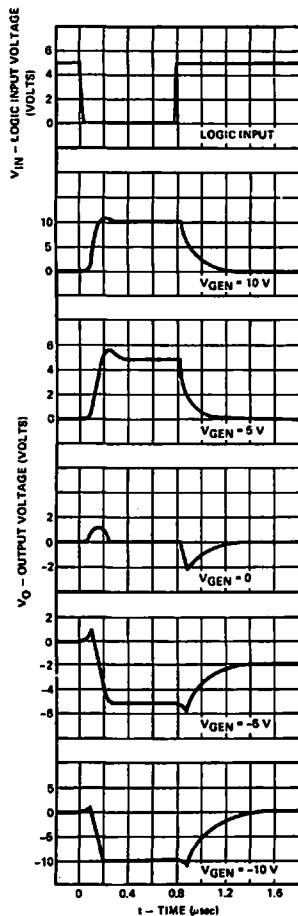
Capacitance vs V_D or V_S
10 Ω FET



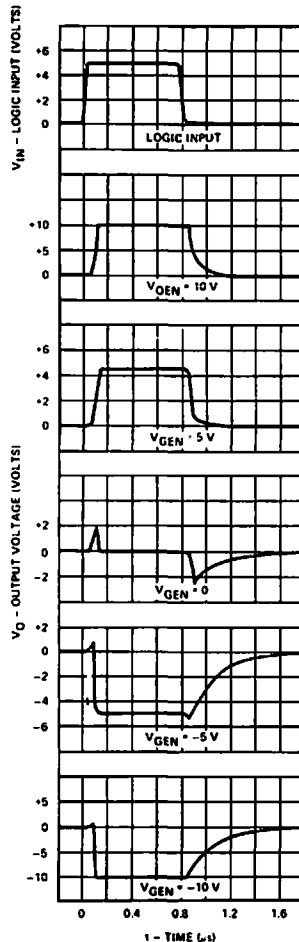
Capacitance vs V_D or V_S
30-75 Ω FET



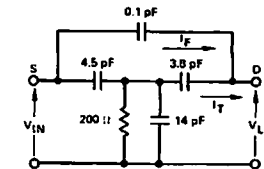
DG180



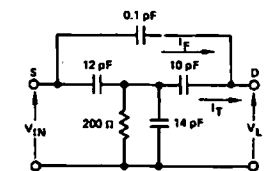
DG181, DG182



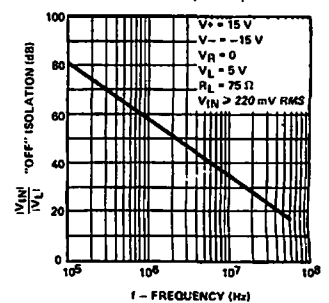
Equivalent "OFF" Circuit 30-75 Ω FET



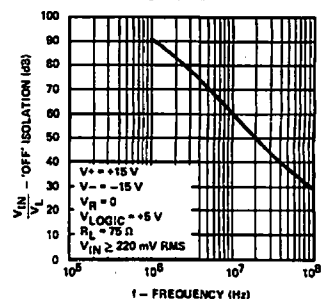
Equivalent "OFF" Circuit 10 Ω FET



"OFF" Isolation vs Frequency 10 Ω FET

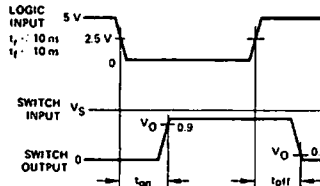
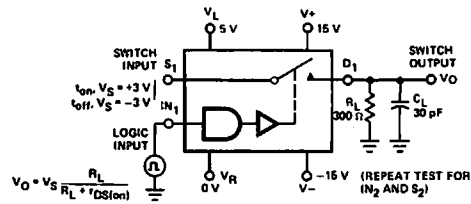


"OFF" Isolation vs Frequency
30-75 Ω FET



SWITCHING TIME TEST CIRCUIT

Switch output waveform shown for $V_S = \text{constant}$ with logic input waveform as shown. Note that V_S may be + or - as per switching time test circuit. V_O is the steady state output with switch on. Feedthrough via gate capacitance may result in spikes at leading and trailing edge of output waveform.


APPLICATION HINTS*

Switch Family	V+ Positive Supply Voltage (V)	V- Negative Supply Voltage (V)	VL Logic Supply Voltage (V)	VR Reference Supply Voltage (V)	VIN Logic Input Voltage VINH Min/ VINL Max (V)	VS Analog Voltage Range (V)
10 Ω	+15**	-15	+5	Gnd	2.0/0.8	-7.5 to +15
and	+10	-20	+5	Gnd	2.0/0.8	-12.5 to +10
30 Ω	+12	-12	+5	Gnd	2.0/0.8	-4.5 to +12
75 Ω	+15**	-15	+5	Gnd	2.0/0.8	-10 to +15
	+10	-20	+5	Gnd	2.0/0.8	-15 to +10
	+12	-12	+5	Gnd	2.0/0.8	-7 to +12

*Application Hints are for DESIGN AID ONLY, not guaranteed and not subject to production testing.

**Electrical Parameter Chart based on $V+ = +15\text{ V}$, $V- = -15\text{ V}$, $V_L = 5\text{ V}$, $V_R = \text{Gnd}$.

DG183/DG184/DG185 High-Speed Driver with Dual DPST JFET Switches



FEATURES

- Constant ON Resistance over Entire Analog Range
- Low Leakage
- Low Crosstalk

BENEFITS

- Low Distortion
- Eliminates Large Signal Errors
- High Bandwidth Capability

APPLICATIONS

- Video Switching
- Audio Switching
- Sample/Hold
- D/A Ladder Switches

DESCRIPTION

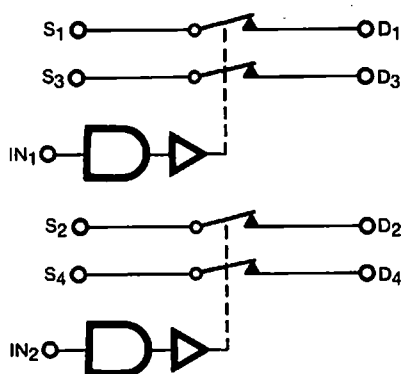
The DG183-185 are precision 2-channel double-pole, single-throw analog switches designed for applications where constant ON resistance over the entire analog range is an important consideration. The major design difference is in ON resistance, being 10, 30 and 75 Ω for the DG183, DG184 and DG185 respectively.

Each device comprises four N-channel JFET transistors and a CMOS driver (TTL compatible) to achieve state of the art performance. The JFET switches provide constant ON resistance, independent of the analog input, insuring

low distortion in precision audio and process control applications. The driver is designed to achieve Break-Before-Make action. In the ON state each switch conducts current equally well in either direction. In the OFF condition the switches will block up to 20 V peak-to-peak, with leakage through less than -60 dB at 10 MHz.

DG183-185 are available in the 16-lead sidebraze and flat-pack packages, specified over the industrial (-25 to 85°C), and military (-55 to 125°C) temperature ranges.

FUNCTIONAL BLOCK DIAGRAM



Two DPST Switches per Package*

Truth Table

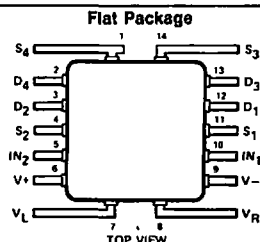
LOGIC	SWITCH
0	OFF
1	ON

Logic "0" $\leq$ 0.8 V

Logic "1" $\geq$ 2.0 V

*Switches Shown for Logic "1" Input

PIN CONFIGURATION



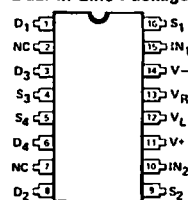
Order Numbers:

DG184AL or DG185AL

See Package 5

*Common to Substrate and Base of Package

Dual-In-Line Package



Order Numbers:

DG183AP or DG183BP

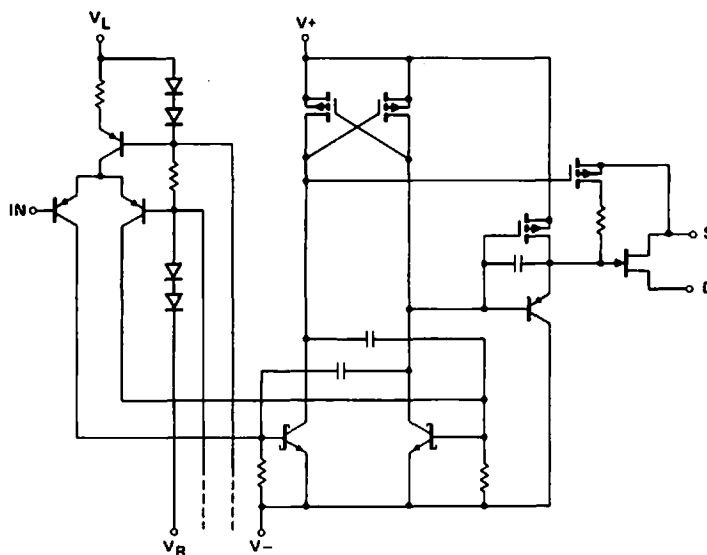
DG184AP or DG184BP

DG185AP or DG185BP

See Package 12

V_+ to V_-	36 V	Current (All Other Pins)	30 mA
V_+ to V_D	33 V	Storage Temperature	-65 to 150°C
V_D to V_-	33 V	Operating Temperature	
V_D to V_S	± 35 V	A Suffix.....	-55 to 125°C
V_L to V_-	8 V	B Suffix.....	-25 to 85°C
V_L to V_{in}	8 V	Power Dissipation*	
V_L to V_R	8 V	16 Pin DIP**	900 mW
V_{in} to V_R	8 V	Flat Pack***	900 mW
V_R to V_-	27 V		
V_R to V_{in}	8 V		
Current (S or D)		*All leads welded or soldered to PC board	
DG183.....	200 mA	**Derate 12 mW/°C above 75°C	
DG184, DG185	30 mA	***Derate 10 mW/°C above 75°C	

SCHEMATIC DIAGRAM (Typical Channel)



ELECTRICAL CHARACTERISTICS¹
 $T_A = 25^\circ\text{C}$

	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: V ₊ = 15 V, V ₋ = -15 V, V _L = 5 V, V _R = 0 V	LIMITS						UNIT
				DG183A			DG183B			
				MIN ²	TYP ³	MAX	MIN ²	TYP ³	MAX	
SWITCH	Analog Signal Range	V _{ANALOG}		-7.5		15	-7.5		15	V
	Drain-Source ON Resistance	r _{DS(on)}	I _S = -1 mA, V _D = 7.5 V, V _{in} = 2.0 V		7.5	10			15	Ω
	Source OFF Leakage Current	I _{S(off)}	V _{in} = 0.8 V	V _S = 10 V, V _D = -10 V V ₊ = 10 V, V ₋ = -20 V		0.05	10		15	nA
		V _S = 7.5 V, V _D = -7.5 V		0.05	10		15			
	Drain OFF Leakage Current	I _{D(off)}		V _S = 10 V, V _D = -10 V V ₊ = 10 V, V ₋ = -20 V		0.04	10		15	
		V _S = 7.5 V, V _D = -7.5 V		0.03	10		15			
	Channel ON Leakage Current	I _{D(on)} + I _{S(on)}	V _D = V _S = 7.5 V, V _{in} = 2.0 V	-2	-0.1		-10			
	Saturation Drain Current	I _{DSS}	2 ms Pulse Duration		300		300			mA
INPUT	Input Current With Input Voltage High	I _{INH}	V _{in} = 5 V		<0.01	10			10	μA
	Input Current With Input Voltage Low	I _{INL}	V _{in} = 0	-250	-30		-250			
DYNAMIC	Turn-ON Time	t _{on}	See Switching Time Test Circuit		240	300			300	ns
	Turn-OFF Time	t _{off}			140	250			300	
	Source OFF Capacitance	C _{S(off)}	f = 1 MHz	V _S = -5 V, I _D = 0		21		21		pF
	Drain OFF Capacitance	C _{D(off)}		V _D = -5 V, I _S = 0		17		17		
	Channel ON Capacitance	C _D + S (on)		V _D = V _S = 0		17		17		
	OFF Isolation		f = 1 MHz, R _L = 75 Ω		>55			>55		dB
SUPPLY	Positive Supply Current	I ₊	V _{in(all)} = 0 V			3			3	mA
	Negative Supply Current	I ₋		-5.5			-5.5			
	Logic Supply Current	I _L				4.5			4.5	
	Reference Supply Current	I _R		-2			-2			
	Positive Supply Current	I ₊	V _{in(all)} = 5 V			0.1			0.1	
	Negative Supply Current	I ₋		-4			-4			
	Logic Supply Current	I _L				4.5			4.5	
	Reference Supply Current	I _R		-2			-2			

 $T_A = \text{Over Temperature Range}$

	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: V+ = 15 V, V- = -15 V, VL = 5 V, VR = 0 V	LIMITS						UNIT
				DG183A			DG183B			
				MIN ²	TYP ³	MAX	MIN ²	TYP ³	MAX	
SWITCH	Analog Signal Range	VANALOG		-7.5		15	-7.5		15	V
	Drain-Source ON Resistance	rDS(on)	IS = -1 mA, VD = 7.5 V, VIN = 2.0 V			20			25	Ω
	Source OFF Leakage Current	IS(off)	VIN = 0.8 V	VS = 10 V, VD = -10 V V+ = 10 V, V- = -20 V		1000			300	nA
				VS = 7.5 V, VD = -7.5 V		1000			300	
	Drain OFF Leakage Current	ID(off)		VS = 10 V, VD = -10 V V+ = 10 V, V- = -20 V		1000			300	
				VS = 7.5 V, VD = -7.5 V		1000			300	
	Channel ON Leakage Current	ID(on) + IS(on)	VD = VS = 7.5 V, VIN = 2.0 V	-200			-200			
INPUT	Input Current With Input Voltage High	IINH	VIN = 5 V			20			20	μA
	Input Current With Input Voltage Low	IINL	VIN = 0	-250			-250			

NOTES:

1. Refer to PROCESS OPTION FLOWCHART for additional information
2. The algebraic convention whereby the most negative value is a minimum, and the most positive value is a maximum, is used in this data sheet.
3. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

ELECTRICAL CHARACTERISTICS¹ (Cont.)
 $T_A = 25^\circ\text{C}$

	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: V ⁺ = 15 V, V ⁻ = -15 V, V _L = 5 V, V _R = 0 V	LIMITS						UNIT	
				DG184A			DG184B				
				MIN ²	TYP ³	MAX	MIN ²	TYP ³	MAX		
SWITCH	Analog Signal Range	V _{ANALOG}		-7.5		15	-7.5		15	V	
	Drain-Source ON Resistance	r _{DS(on)}	I _S = -1 mA, V _D = 7.5 V, V _{in} = 2.0 V		18	30			50	Ω	
	Source OFF Leakage Current	I _{S(off)}	V _{in} = 0.8 V	V _S = 10 V, V _D = -10 V V ⁺ = 10 V, V ⁻ = -20 V	0.06	1			5	nA	
				V _S = 7.5 V, V _D = -7.5 V		0.1	1				5
	Drain OFF Leakage Current	I _{D(off)}		V _S = 10 V, V _D = -10 V V ⁺ = 10 V, V ⁻ = -20 V		0.5	1				5
				V _S = 7.5 V, V _D = -7.5 V		0.6	1				5
Channel ON Leakage Current	I _{D(on)} + I _{S(on)}	V _D = V _S = 7.5 V, V _{in} = 2.0 V	-2	-0.02		-10					
INPUT	Input Current With Input Voltage High	I _{INH}	V _{in} = 5 V			10			10	μA	
	Input Current With Input Voltage Low	I _{INL}	V _{in} = 0	-250	-30		-250				
DYNAMIC	Turn-ON Time	t _{on}	See Switching Time Test Circuit		85	150			180	ns	
	Turn-OFF Time	t _{off}			95	130			150		
	Source OFF Capacitance	C _{S(off)}	f = 1 MHz		V _S = -5 V, I _D = 0	9		9		pF	
	Drain OFF Capacitance	C _{D(off)}			V _D = -5 V, I _S = 0	6		6			
	Channel ON Capacitance	C _D + S (on)			V _D = V _S = 0	14		14			
	OFF Isolation				f = 1 MHz, R _L = 75 Ω	>50		>50			
SUPPLY	Positive Supply Current	I ⁺	V _{in(all)} = 0 V			3.0			3.0	mA	
	Negative Supply Current	I ⁻		-5.5			-5.5				
	Logic Supply Current	I _L				4.5			4.5		
	Reference Supply Current	I _R		-2.0			-2.0				
	Positive Supply Current	I ⁺	V _{in(all)} = 5 V			0.1			0.1		
	Negative Supply Current	I ⁻		-4.0			-4.0				
	Logic Supply Current	I _L				4.5			4.5		
	Reference Supply Current	I _R		-2.0			-2.0				

 $T_A = \text{Over Temperature Range}$

	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: V+ = 15 V, V- = -15 V, VL = 5 V, VR = 0 V	LIMITS						UNIT
				DG184A			DG184B			
				MIN ³	TYP ⁴	MAX	MIN ³	TYP ⁴	MAX	
SWITCH	Analog Signal Range	VANALOG		-7.5		15	-7.5		15	V
	Drain-Source ON Resistance	rDS(on)	IS = -1 mA, VD = 7.5 V, VIN = 2.0 V			60			75	Ω
	Source OFF Leakage Current	IS(off)	VIN = 0.8 V	VS = 10 V, VD = -10 V V+ = 10 V, V- = -20 V		100			100	nA
				VS = 7.5 V, VD = -7.5 V		100			100	
	Drain OFF Leakage Current	ID(off)		VS = 10 V, VD = -10 V V+ = 10 V, V- = -20 V		100			100	
				VS = 7.5 V, VD = -7.5 V		100			100	
Channel ON Leakage Current	ID(on) + IS(on)	VD = VS = 7.5 V, VIN = 2.0 V	-200			-200				
INPUT	Input Current With Input Voltage High	IINH	VIN = 5 V			20			20	μA
	Input Current With Input Voltage Low	IINL	VIN = 0	-250			-250			

NOTES:

1. Refer to PROCESS OPTION FLOWCHART for additional information.
2. The algebraic convention whereby the most negative value is a minimum, and the most positive value is a maximum, is used in this data sheet.
3. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

ELECTRICAL CHARACTERISTICS¹ (Cont.)
 $T_A = 25^\circ\text{C}$

	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: V+ = 15 V, V- = -15 V, VL = 5 V, VR = 0 V	LIMITS						UNIT
				DG185A			DG185B			
				MIN ²	TYP ³	MAX	MIN ²	TYP ³	MAX	
SWITCH	Analog Signal Range	VANALOG		-10		15	-10		15	V
	Drain-Source ON Resistance	rDS(on)	IS = -1 mA, VD = 7.5 V, VIN = 2.0 V		35	75			100	Ω
	Source OFF Leakage Current	IS(off)	VIN = 0.8 V	VS = 10 V, VD = -10 V V+ = 10 V, V- = -20 V		0.05	1		5	nA
		VS = 7.5 V, VD = -7.5 V			0.07	1		5		
	Drain OFF Leakage Current	ID(off)		VS = 10 V, VD = -10 V V+ = 10 V, V- = -20 V		0.04	1		5	
		VS = 7.5 V, VD = -7.5 V			0.05	1		5		
Channel ON Leakage Current	ID(on) + IS(on)	VD = VS = 7.5 V, VIN = 2.0 V	-2	-0.03		-10				
INPUT	Input Current With Input Voltage High	IINH	Vin = 5 V			10				μA
	Input Current With Input Voltage Low	IINL	Vin = 0	-250	-35		-250			
DYNAMIC	Turn-ON Time	ton	See Switching Time Test Circuit		120	250			300	ns
	Turn-OFF Time	toff			100	130			150	
	Source OFF Capacitance	CS(off)	f = 1 MHz	VS = -5 V, ID = 0		9		9		pF
	Drain OFF Capacitance	CD(off)		VD = -5 V, IS = 0		6		6		
	Channel ON Capacitance	CD + S (on)		VD = VS = 0		14		14		
	OFF Isolation			f = 1 MHz, RL = 75 Ω		>50		>50		
SUPPLY	Positive Supply Current	I+	Vin(all) = 0 V			3			3	mA
	Negative Supply Current	I-		-5.5			-5.5			
	Logic Supply Current	IL				4.5			4.5	
	Reference Supply Current	IR		-2			-2			
	Positive Supply Current	I+	Vin(all) = 5 V			0.1			0.1	
	Negative Supply Current	I-		-4			-4			
	Logic Supply Current	IL				4.5			4.5	
	Reference Supply Current	IR		-2			-2			

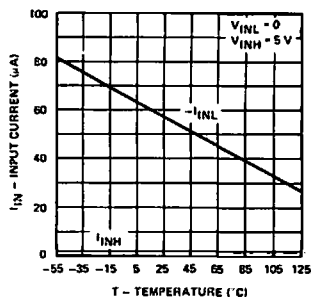
 $T_A = \text{Over Temperature Range}$

	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: V+ = 15 V, V- = -15 V, VL = 5 V, VR = 0 V	LIMITS						UNIT
				DG185A			DG185B			
				MIN ²	TYP ³	MAX	MIN ²	TYP ³	MAX	
SWITCH	Analog Signal Range	VANALOG		-10		15	-10		15	V
	Drain-Source ON Resistance	rDS(on)	IS = -1 mA, VD = 7.5 V, VIN = 2.0 V			150			150	Ω
	Source OFF Leakage Current	IS(off)	VIN = 0.8 V	VS = 10 V, VD = -10 V V+ = 10 V, V- = -20 V		100			100	nA
		VS = 7.5 V, VD = - 7.5 V			100			100		
	Drain OFF Leakage Current	ID(off)		VS = 10 V, VD = -10 V V+ = 10 V, V- = -20 V		100			100	
		VS = 7.5 V, VD = - 7.5 V			100			100		
Channel ON Leakage Current	ID(on) + IS(on)	VD = VS = 7.5 V, VIN = 2.0 V	-200			-200				
INPUT	Input Current With Input Voltage High	IINH	VIN = 5 V			20			20	μA
	Input Current With Input Voltage Low	IINL	VIN = 0	-250			-250			

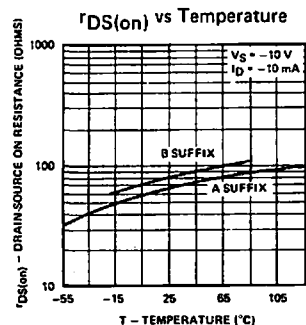
NOTES:

1. Refer to PROCESS OPTION FLOWCHART for additional information.
2. The algebraic convention whereby the most negative value is a minimum, and the most positive value is a maximum, is used in this data sheet.
3. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

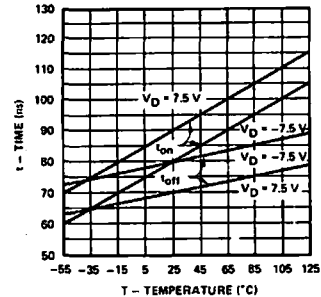
I_{IN} vs V_{IN} and Temperature



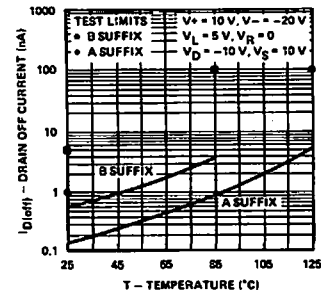
75 Ω
DG185



Switching Time vs V_D and Temperature

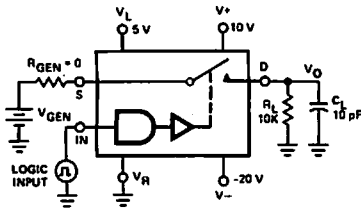


$I_{D(off)}$ vs Temperature



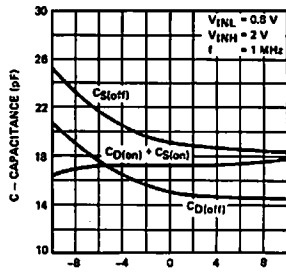
TYPICAL CHARACTERISTICS (Cont.)

Typical delay, rise, fall, settling times, and switching transients in this circuit.



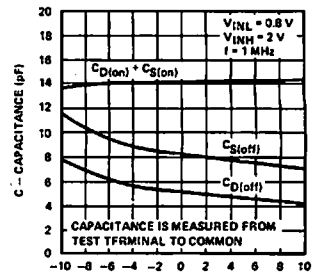
If R_{GEN} , R_L or C_L is increased, there will be proportional increases in rise and/or fall times.

Capacitance vs V_D or V_S
10 Ω FET



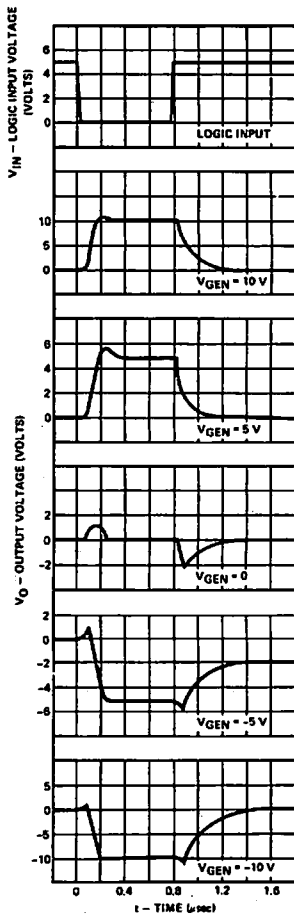
V_D or V_S - DRAIN or SOURCE VOLTAGE (VOLTS)

Capacitance vs V_D or V_S
30-75 Ω FET

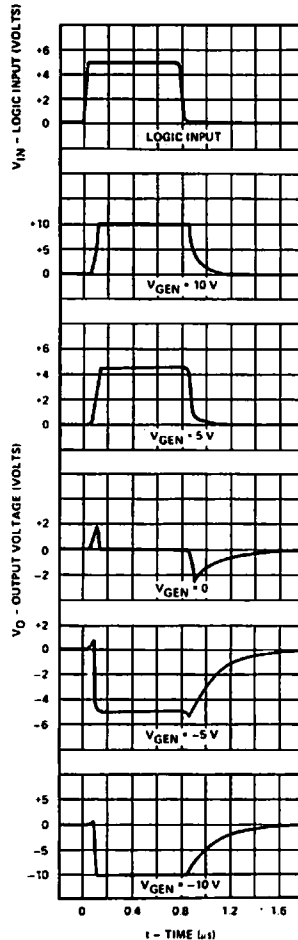


V_D or V_S - DRAIN or SOURCE VOLTAGE (VOLTS)

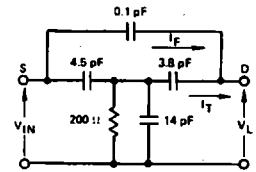
DG183



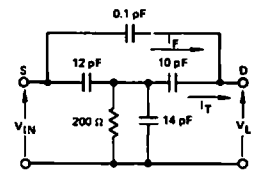
DG184/DG185



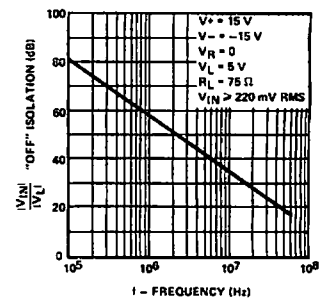
Equivalent "OFF" Circuit 30-75 Ω FET



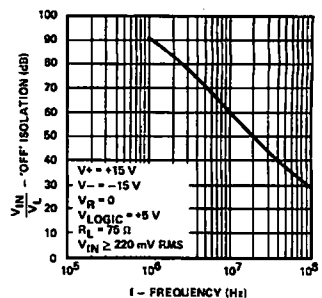
Equivalent "OFF" Circuit 10 Ω FET



"OFF" Isolation vs Frequency 10 Ω FET

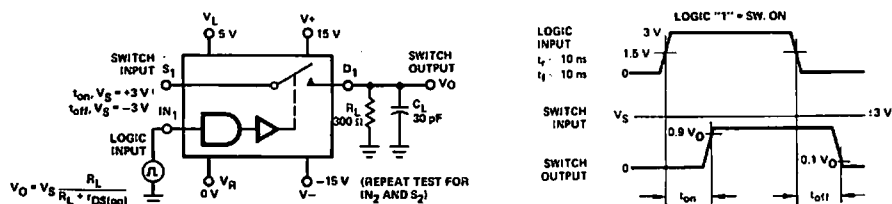


"OFF" Isolation vs Frequency
30-75 Ω FET



SWITCHING TIME TEST CIRCUIT

Switch output waveform shown for $V_S = \text{constant}$ with logic input waveform as shown. Note that V_S may be + or - as per switching time test circuit. V_O is the steady state output with switch on. Feedthrough via gate capacitance may result in spikes at leading and trailing edge of output waveform.



APPLICATIONS HINTS*

Switch Family	V+ Positive Supply Voltage (V)	V- Negative Supply Voltage (V)	VL Logic Supply Voltage (V)	VR Reference Supply Voltage (V)	Vin Logic Input Voltage VINH Min/ VINL Max (V)	VS Analog Voltage Range (V)
10 Ω	15**	-15	5	Gnd	2.0/0.8	-7.5 to 15
and	10	-20	5	Gnd	2.0/0.8	-12.5 to 10
30 Ω	12	-12	5	Gnd	2.0/0.8	4.5 to 12
75 Ω	15**	-15	5	Gnd	2.0/0.8	-10 to 15
	10	20	5	Gnd	2.0/0.8	-15 to 10
	12	12	5	Gnd	2.0/0.8	-7 to 12

* Application Hints are for DESIGN AID ONLY, not guaranteed and not subject to production testing.

** Electrical Parameter Chart based on $V+ = +15 \text{ V}$, $V- = -15 \text{ V}$, $V_L = 5 \text{ V}$, $V_R = \text{Gnd}$.

DG186/DG187/DG188

High-Speed Driver with SPDT JFET Switch



FEATURES

- Constant ON Resistance over Entire Analog Range
- Low Leakage
- Low Crosstalk

BENEFITS

- Low Distortion
- Eliminates Large Signal Errors
- High Bandwidth Capability

APPLICATIONS

- Video Switching
- Audio Switching
- Sample/Hold
- D/A Ladder Switches

DESCRIPTION

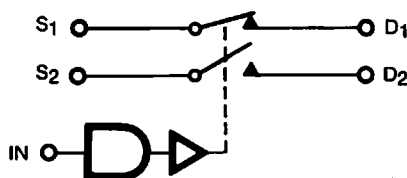
The DG186-188 are precision single-pole, double-throw analog switches designed for applications where constant ON resistance over the entire analog range is an important consideration. The major design difference is in ON resistance, being 10, 30 and 75 Ω for the DG186, DG187 and DG188 respectively.

Each device comprises two N-channel JFET transistors and a CMOS driver (TTL compatible) to achieve state of the art performance. The JFET switches provide constant ON resistance, independent of the analog input, insuring

low distortion in precision audio and process control applications. The driver is designed to achieve Break-Before-Make action. In the ON state each switch conducts current equally well in either direction. In the OFF condition the switches will block up to 20 V peak-to-peak, with feedthrough less than -60 dB at 10 MHz.

DG186-188 are available in the 14-lead sidebraze and flat-pack, and the 10-lead metal can packages, specified over the industrial (-25 to 85°C), and military (-55 to 125°C) temperature ranges.

FUNCTIONAL BLOCK DIAGRAM



One SPDT Switch per Package*

Truth Table

LOGIC	SW 1	SW 2
0	OFF	ON
1	ON	OFF

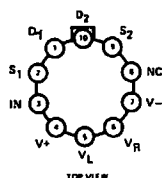
Logic "0" ≤ 0.8 V

Logic "1" ≥ 2.0 V

*Switches Shown for Logic "1" Input

PIN CONFIGURATION

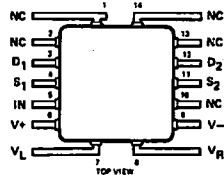
Metal Can Package



Order Numbers:
DG186AA or DG186BA
DG187AA or DG187BA
DG188AA or DG188BA
See Package 2

*Common to Substrate and Case

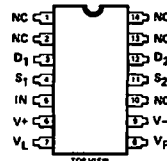
Flat Package



Order Numbers:
DG187AL or DG188AL
See Package 5

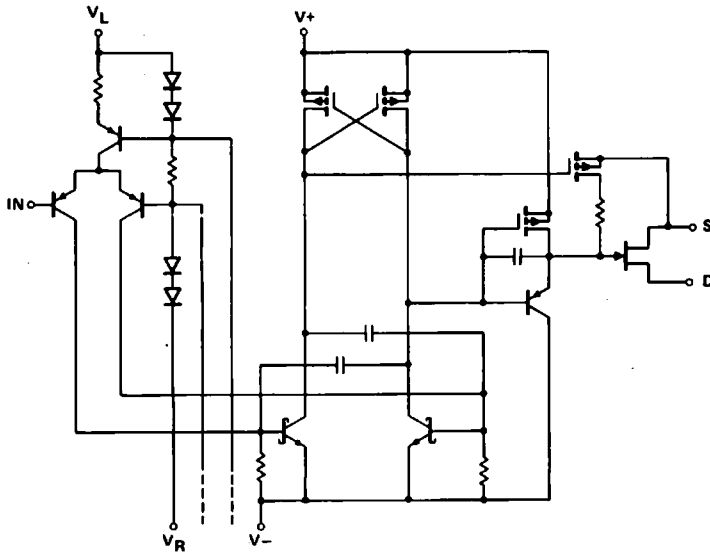
*Common to Substrate and Base of Package

Dual-In-Line Package



Order Numbers:
DG186AP or DG186BP
DG187AP or DG187BP
DG188AP or DG188BP
See Package 11

SCHEMATIC DIAGRAM (Typical Channel)



ELECTRICAL CHARACTERISTICS¹
 $T_A = 25^\circ\text{C}$

	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: V+ = 15 V, V- = -15 V, VL = 5 V, VR = 0 V	LIMITS						UNIT
				DG186A			DG188B			
				MIN ²	TYP ³	MAX	MIN ²	TYP ³	MAX	
SWITCH	Analog Signal Range	VANALOG		-7.5		15	-7.5		15	V
	Drain-Source ON Resistance	rDS(on)	IS = -1 mA, VD = 7.5 V, VIN = 0.8 V or 2.0 V ⁴		7.5	10			15	Ω
	Source OFF Leakage Current	IS(off)	VIN = 0.8 V or 2.0 V ⁴		VS = 10 V, VD = -10 V V+ = 10 V, V- = -20 V	0.05	10		15	nA
				VS = 7.5 V, VD = -7.5 V	0.05	10		15		
	Drain OFF Leakage Current	ID(off)			VS = 10 V, VD = -10 V V+ = 10 V, V- = -20 V	0.04	10		15	
				VS = 7.5 V, VD = -7.5 V	0.03	10		15		
	Channel ON Leakage Current	ID(on)+ IS(on)	VD = VS = 7.5 V, VIN = 0.8 V or 2.0 V ⁴	-2	-0.1		-10			
Saturation Drain Current	IDSS	2 ms Pulse Duration		300		300			mA	
INPUT	Input Current With Input Voltage High	IINH	VIN = 5 V	-250	-30		-250			μA
	Input Current With Input Voltage Low	IINL	VIN = 0		<0.01	10			10	
DYNAMIC	Turn-ON Time	tON	See Switching Time Test Circuit		240	300			300	ns
	Turn-OFF Time	tOFF			140	250			300	
	Source OFF Capacitance	CS(off)	f = 1 MHz		VS = -5 V, ID = 0	21		21		pF
	Drain OFF Capacitance	CD(off)			VD = -5 V, IS = 0	17		17		
	Channel ON Capacitance	CD + S (on)			VD = VS = 0	17		17		
	OFF Isolation		f = 1 MHz, RL = 75 Ω		>55			>55		dB
SUPPLY	Positive Supply Current	I+	VIN(all) = 0 V			0.8			0.8	mA
	Negative Supply Current	I-			-3		-3			
	Logic Supply Current	IL				3.2			3.2	
	Reference Supply Current	IR			-2		-2			
	Positive Supply Current	I+	VIN(all) = 5 V			0.8			0.8	
	Negative Supply Current	I-			-3		-3			
	Logic Supply Current	IL				3.2			3.2	
	Reference Supply Current	IR			-2		-2			

 $T_A = \text{Over Temperature Range}$

	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: V+ = 15 V, V- = -15 V, VL = 5 V, VR = 0 V		LIMITS						UNIT
					DG186A			DG188B			
					MIN ²	TYP ³	MAX	MIN ²	TYP ³	MAX	
SWITCH	Analog Signal Range	VANALOG			-7.5		15	-7.5		15	V
	Drain-Source ON Resistance	rDS(on)	IS = -1 mA, VD = 7.5 V, VIN = 0.8 V or 2.0 V ⁴				20			25	Ω
	Source OFF Leakage Current	IS(off)	VIN = 0.8 V or 2.0 V ⁴	VS = 10 V, VD = -10 V V+ = 10 V, V- = -20 V			1000			300	nA
		VS = 7.5 V, VD = -7.5 V				1000			300		
	Drain OFF Leakage Current	ID(off)		VS = 10 V, VD = -10 V V+ = 10 V, V- = -20 V			1000			300	
		VS = 7.5 V, VD = -7.5 V				1000			300		
Channel ON Leakage Current	ID(on)+ IS(on)	VD = VS = 7.5 V, VIN = 0.8 V or 2.0 V ⁴		-200			-200				
INPUT	Input Current With Input Voltage High	IINH	VIN = 5 V				20			20	μA
	Input Current With Input Voltage Low	IINL	VIN = 0		-250			-250			

NOTES:

1. Refer to PROCESS OPTION FLOWCHART for additional information.
2. The algebraic convention whereby the most negative value is a minimum, and the most positive is a maximum, is used in this data sheet.
3. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
4. V_{in} = input voltage to perform proper function.

ELECTRICAL CHARACTERISTICS¹ (Cont.)T_A = 25°C

DG186/DG187/DG188

	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: V ₊ = 15 V, V ₋ = -15 V, V _L = 5 V, V _R = 0 V	LIMITS						UNIT
				DG187A			DG187B			
				MIN ²	TYP ³	MAX	MIN ²	TYP ³	MAX	
SWITCH	Analog Signal Range	V _{ANALOG}		-7.5		15	-7.5		15	V
	Drain-Source ON Resistance	r _{DS(on)}	I _S = -1 mA, V _D = 7.5 V, V _{in} = 0.8 V or 2.0 V ⁴		18	30			50	Ω
	Source OFF Leakage Current	I _{S(off)}	V _{in} = 0.8 V or 2.0 V ⁴	V _S = 10 V, V _D = -10 V V ₊ = 10 V, V ₋ = -20 V	0.06	1			5	nA
		V _S = 7.5 V, V _D = -7.5 V		0.1	1			5		
	Drain OFF Leakage Current	I _{D(off)}		V _S = 10 V, V _D = -10 V V ₊ = 10 V, V ₋ = -20 V	0.5	1			5	
		V _S = 7.5 V, V _D = -7.5 V		0.6	1			5		
Channel ON Leakage Current	I _{D(on)} ⁺ I _{S(on)}	V _D = V _S = 7.5 V, V _{in} = 0.8 V or 2.0 V ⁴	-2	-0.02		-10				
INPUT	Input Current With Input Voltage High	I _{INH}	V _{in} = 5 V			10			10	μA
	Input Current With Input Voltage Low	I _{INL}	V _{in} = 0	-250	-30		-250			
DYNAMIC	Turn-ON Time	t _{on}	See Switching Time Test Circuit		85	150			180	ns
	Turn-OFF Time	t _{off}			95	130			150	
	Source OFF Capacitance	C _{S(off)}	f = 1 MHz	V _S = -5 V, I _D = 0	9			9		pF
	Drain OFF Capacitance	C _{D(off)}		V _D = -5 V, I _S = 0	6			6		
	Channel ON Capacitance	C _D + S (on)		V _D = V _S = 0	14			14		
	OFF Isolation		f = 1 MHz, R _L = 75 Ω		>50			>50		dB
SUPPLY	Positive Supply Current	I ₊	V _{in(all)} = 0 V			0.8			0.8	mA
	Negative Supply Current	I ₋		-3.0			-3.0			
	Logic Supply Current	I _L				3.2			3.2	
	Reference Supply Current	I _R		-2.0			-2.0			
	Positive Supply Current	I ₊	V _{in(all)} = 5 V			0.8			0.8	
	Negative Supply Current	I ₋		-3.0			-3.0			
	Logic Supply Current	I _L				3.2			3.2	
	Reference Supply Current	I _R		-2.0			-2.0			

T_A = Over Temperature Range

	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: V+ = 15 V, V- = -15 V, VL = 5 V, VR = 0 V	LIMITS						UNIT
				DG187A			DG187B			
				MIN ²	TYP ³	MAX	MIN ²	TYP ³	MAX	
SWITCH	Analog Signal Range	VANALOG		-7.5		15	-7.5		15	V
	Drain-Source ON Resistance	rDS(on)	IS = -1 mA, VD = 7.5 V, VIN = 0.8 V or 2.0 V ⁴			60			75	Ω
	Source OFF Leakage Current	IS(off)	VIN = 0.8 V or 2.0 V ⁴		VS = 10 V, VD = -10 V V+ = 10 V, V- = -20 V	100			100	nA
				VS = 7.5 V, VD = -7.5 V	100			100		
	Drain OFF Leakage Current	ID(off)			VS = 10 V, VD = -10 V V+ = 10 V, V- = -20 V	100			100	
				VS = 7.5 V, VD = -7.5 V	100			100		
Channel ON Leakage Current	ID(on) ⁺ IS(on)	VD = VS = 7.5 V, VIN = 0.8 V or 2.0 V ⁴	-200			-200				
INPUT	Input Current With Input Voltage High	IINH	VIN = 5 V			20			20	μA
	Input Current With Input Voltage Low	IINL	VIN = 0	-250			-250			

NOTES:

1. Refer to PROCESS OPTION FLOWCHART for additional information.
2. The algebraic convention whereby the most negative value is a minimum, and the most positive is a maximum, is used in this data sheet.
3. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
4. V_{in} = input voltage to perform proper function.

ELECTRICAL CHARACTERISTICS ¹ (Cont.)
 $T_A = 25^\circ\text{C}$

	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: V+ = 15 V, V- = -15 V, VL = 5 V, VR = 0 V		LIMITS						UNIT
					DG188A			DG188B			
					MIN ²	TYP ³	MAX	MIN ²	TYP ³	MAX	
SWITCH	Analog Signal Range	VANALOG			-10		15	-10		15	V
	Drain-Source ON Resistance	rDS(on)	IS = -1 mA, VD = 7.5 V, VIN = 0.8 V or 2.0 V ⁴			35	75			100	Ω
	Source OFF Leakage Current	IS(off)	VIN = 0.8 V or 2.0 V ⁴	VS = 10 V, VD = -10 V V+ = 10 V, V- = -20 V		0.05	1			5	nA
		VS = 7.5 V, VD = -7.5 V			0.07	1		5			
	Drain OFF Leakage Current	ID(off)		VS = 10 V, VD = -10 V V+ = 10 V, V- = -20 V		0.04	1		5		
		VS = 7.5 V, VD = -7.5 V			0.05	1		5			
Channel ON Leakage Current	ID(on)+ IS(on)	VD = VS = 7.5 V, VIN = 0.8 V or 2.0 V ⁴		-2	-0.03		-10				
INPUT	Input Current With Input Voltage High	IINH	VIN = 5 V				10				μA
	Input Current With Input Voltage Low	IINL	VIN = 0		-250	-35		-250			
DYNAMIC	Turn-ON Time	tON	See Switching Time Test Circuit			120	250			300	ns
	Turn-OFF Time	tOFF				100	130			150	
	Source OFF Capacitance	CS(off)	f = 1 MHz	VS = -5 V, ID = 0		9		9		pF	
	Drain OFF Capacitance	CD(off)		VD = -5 V, IS = 0		6		6			
	Channel ON Capacitance	CD + S (on)		VD = VS = 0		14		14			
	OFF Isolation		f = 1 MHz, RL = 75 Ω			>50		>50		dB	
SUPPLY	Positive Supply Current	I+	VIN(all) = 0 V				0.8			0.8	mA
	Negative Supply Current	I-			-3			-3			
	Logic Supply Current	IL					3.2			3.2	
	Reference Supply Current	IR			-2			-2			
	Positive Supply Current	I+	VIN(all) = 5 V				0.8			0.8	
	Negative Supply Current	I-			-3			-3			
	Logic Supply Current	IL					3.2			3.2	
	Reference Supply Current	IR			-2			-2			

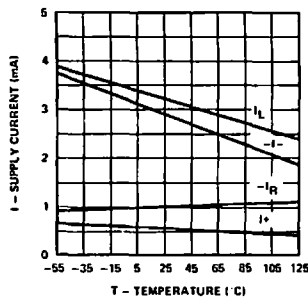
 $T_A = \text{Over Temperature Range}$

	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: V+ = 15 V, V- = -15 V, VL = 5 V, VR = 0 V	LIMITS						UNIT
				DG188A			DG188B			
				MIN ²	TYP ³	MAX	MIN ²	TYP ³	MAX	
SWITCH	Analog Signal Range	VANALOG		-10		15	-10		15	V
	Drain-Source ON Resistance	rDS(on)	IS = -1 mA, VD = 7.5 V, VIN = 0.8 V or 2.0 V ⁴			150			150	Ω
	Source OFF Leakage Current	IS(off)	VIN = 0.8 V or 2.0 V ⁴	VS = 10 V, VD = -10 V V+ = 10 V, V- = -20 V		100			100	nA
		VS = 7.5 V, VD = -7.5 V			100			100		
	Drain OFF Leakage Current	ID(off)		VS = 10 V, VD = -10 V V+ = 10 V, V- = -20 V		100			100	
		VS = 7.5 V, VD = -7.5 V			100			100		
Channel ON Leakage Current	ID(on) ⁺ IS(on)	VD = VS = 7.5 V, VIN = 0.8 V or 2.0 V ⁴	-200			-200				
INPUT	Input Current With Input Voltage High	IINH	VIN = 5 V			20			20	μA
	Input Current With Input Voltage Low	IINL	VIN = 0	-250			-250			

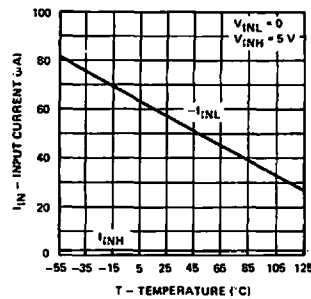
NOTES:

1. Refer to **PROCESS OPTION FLOWCHART** for additional information.
2. The algebraic convention whereby the most negative value is a minimum, and the most positive is a maximum, is used in this data sheet.
3. Typical values are for **DESIGN AID ONLY**, not guaranteed nor subject to production testing.
4. V_{in} = Input voltage to perform proper function.

Supply Current vs Temperature

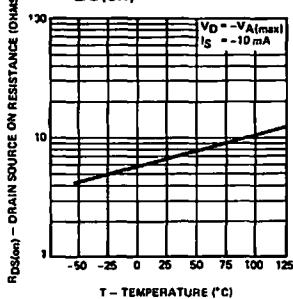


I_{IN} vs V_{IN} and Temperature

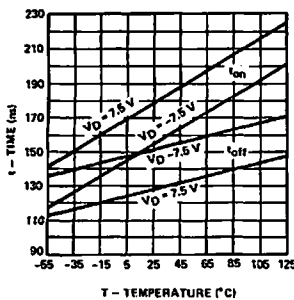


10 Ω
DG186

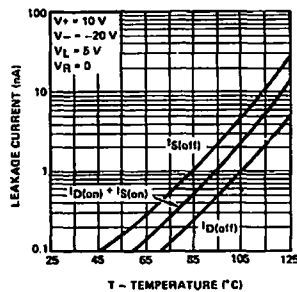
$r_{DS(on)}$ vs Temperature



Switching Time vs V_D
and Temperature

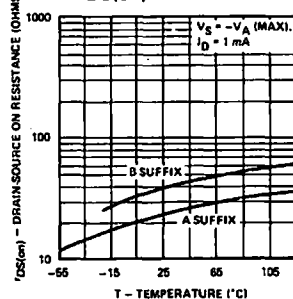


Leakage vs Temperature

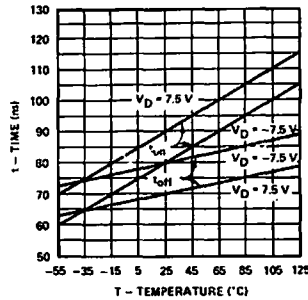


30 Ω
DG187

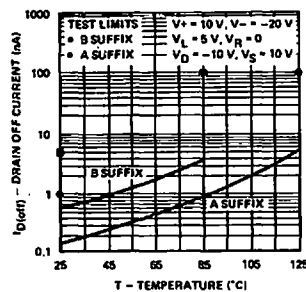
$r_{DS(on)}$ vs Temperature



Switching Time vs V_D
and Temperature

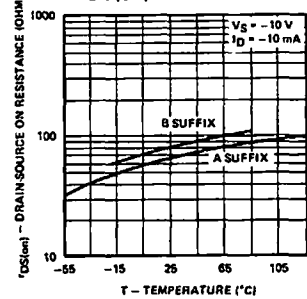


$I_D(off)$ vs Temperature

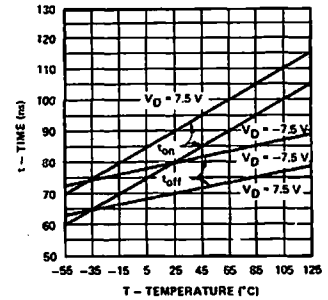


75 Ω
DG188

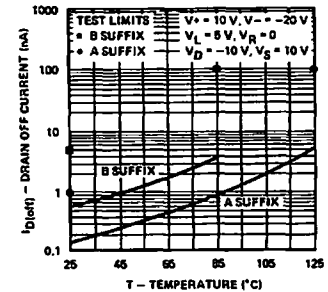
$r_{DS(on)}$ vs Temperature



Switching Time vs V_D
and Temperature

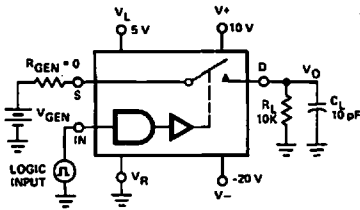


$I_D(off)$ vs Temperature



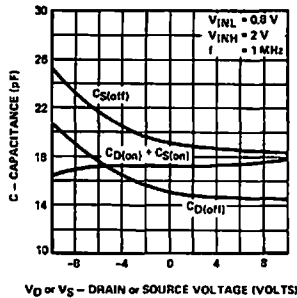
TYPICAL CHARACTERISTICS (Cont.)

Typical delay, rise, fall, settling times, and switching transient in this circuit.

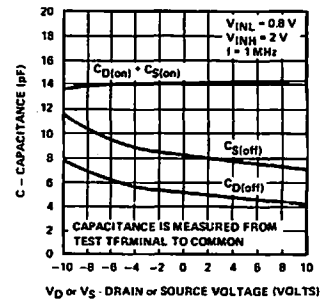


If R_{GEN} , R_L or C_L is increased, there will be proportional increases in rise and/or fall times.

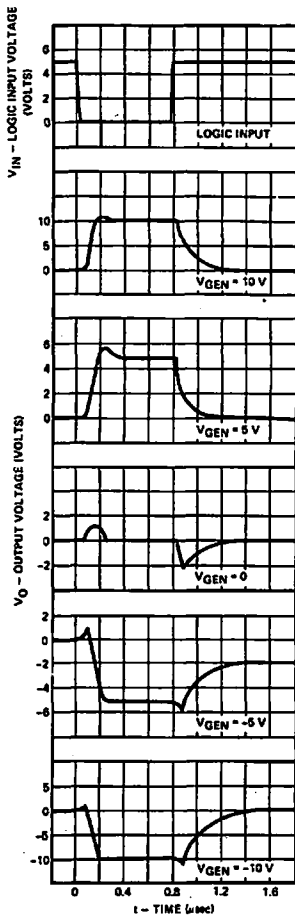
Capacitance vs V_D or V_S
10 Ω FET



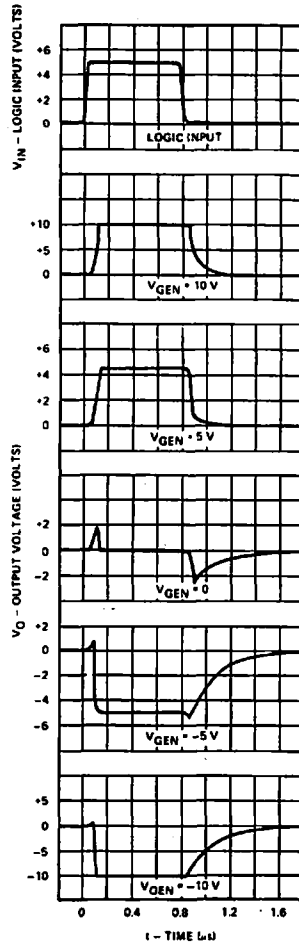
Capacitance vs V_D or V_S
30-75 Ω FET



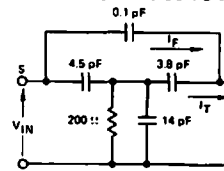
DG186



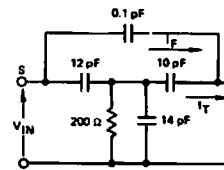
DG187, DG188



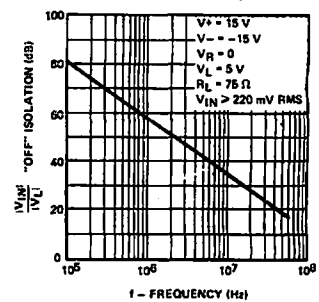
Equivalent "OFF" Circuit 30-75 Ω FET



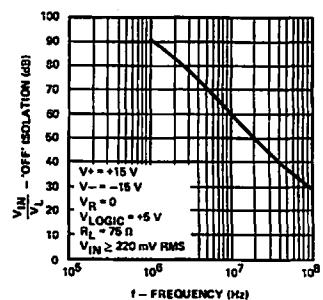
Equivalent "OFF" Circuit 10 Ω FET



"OFF" Isolation vs Frequency 10 Ω FET

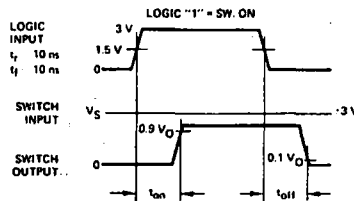
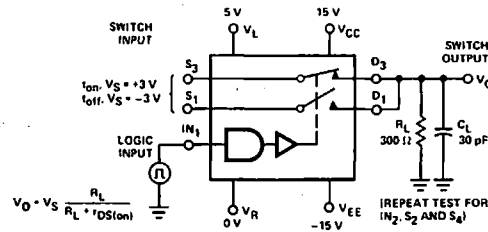


"OFF" Isolation vs Frequency
30-75 Ω FET



SWITCHING TIME TEST CIRCUIT

Switch output waveform shown for V_S = constant with logic input waveform as shown. Note that V_S may be + or - as per switching time test circuit. V_O is the steady state output with switch on. Feedthrough via gate capacitance may result in spikes at leading and trailing edge of output waveform.



NOTE: LOGIC INPUT WAVEFORM IS INVERTED FOR SWITCHES THAT HAVE THE OPPOSITE LOGIC SENSE CONTROL

APPLICATION HINTS*

Switch Family	V+ Positive Supply Voltage (V)	V- Negative Supply Voltage (V)	V _L Logic Supply Voltage (V)	V _R Reference Supply Voltage (V)	V _{IN} Logic Input Voltage V _{INH} Min/ V _{INL} Max (V)	V _S Analog Voltage Range (V)
10 Ω	+15**	-15	+5	Gnd	2.0/0.8	-7.5 to +15
and	+10	-20	+5	Gnd	2.0/0.8	-12.5 to +10
30 Ω	+12	-12	+5	Gnd	2.0/0.8	-4.5 to +12
75 Ω	+15**	-15	+5	Gnd	2.0/0.8	-10 to +15
	+10	-20	+5	Gnd	2.0/0.8	-15 to +10
	+12	-12	+5	Gnd	2.0/0.8	-7 to +12

*Application Hints are for DESIGN AID ONLY, not guaranteed and not subject to production testing.

**Electrical Parameter Chart based on V+ = +15 V, V- = -15 V, V_L = 5 V, V_R = Gnd.

DG189/DG190/DG191

High-Speed Driver with Dual SPDT JFET Switches

FEATURES

- Constant ON Resistance over Entire Analog Range
- Low Leakage
- Low Crosstalk

BENEFITS

- Low Distortion
- Eliminates Large Signal Errors
- High Bandwidth Capability

APPLICATIONS

- Video Switching
- Audio Switching
- Sample/Hold
- D/A Ladder Switches

DESCRIPTION

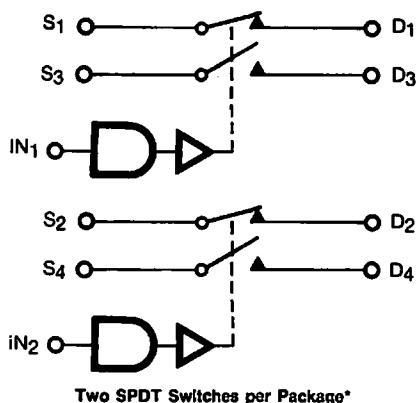
The DG189-191 are precision 2-channel single-pole, double-throw analog switches designed for applications where constant ON resistance over the entire analog range is an important consideration. The major design difference is in ON resistance, being 10, 30 and 75 Ω for the DG189, DG190 and DG191 respectively.

Each device comprises four N-channel JFET transistors and a CMOS driver (TTL compatible) to achieve state of the art performance. The JFET switches provide constant ON resistance, independent of the analog input, insuring

low distortion in precision audio and process control applications. The driver is designed to achieve Break-Before-Make action. In the ON state each switch conducts current equally well in either direction. In the OFF condition the switches will block up to 20 V peak-to-peak, with feedthrough less than -60 dB at 10 MHz.

DG189-191 are available in the 16-lead sidebraze and flat-pack packages, specified over the industrial (-25 to 85°C), and military (-55 to 125°C) temperature ranges.

FUNCTIONAL BLOCK DIAGRAM



Truth Table

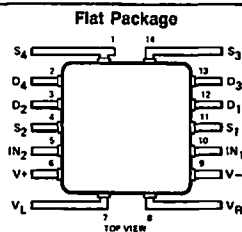
LOGIC	SW 1 SW 2	SW 3 SW 4
0	OFF	ON
1	ON	OFF

Logic "0" ≤ 0.8 V

Logic "1" ≥ 2.4 V

*Switches Shown for Logic "1" Input

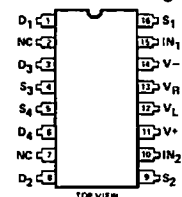
PIN CONFIGURATION



Order Numbers:
DG190AL or DG191AL
See Package 5

*Common to Substrate and Base of Package

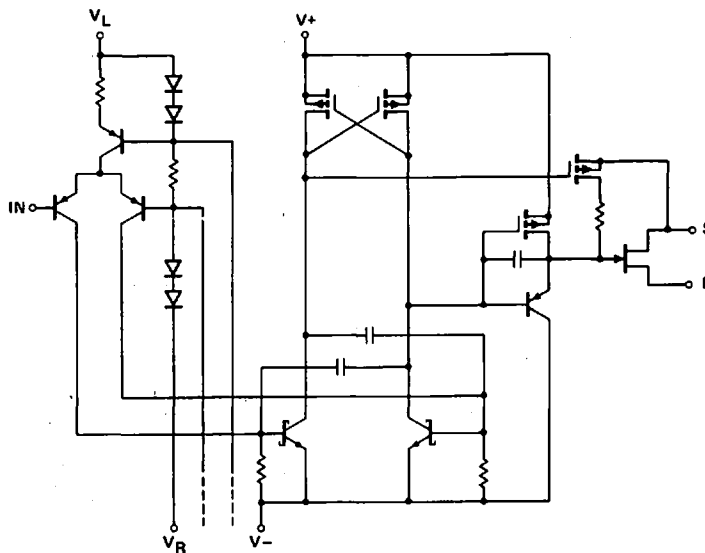
Dual-In-Line Package



Order Numbers:
DG189AP or DG189BP
DG190AP or DG190BP
DG191AP or DG191BP
See Package 12

ABSOLUTE MAXIMUM RATINGS

V_+ to V_-	36 V	Current (All Other Pins)	30 mA
V_+ to V_D	33 V	Storage Temperature	-65 to 150°C
V_D to V_-	33 V	Operating Temperature	
V_D to V_S	± 35 V	A Suffix.....	-55 to 125°C
V_L to V_-	8 V	B Suffix.....	-25 to 85°C
V_L to V_{in}	8 V	Power Dissipation*	
V_L to V_R	8 V	16 Pin DIP**.....	900 mW
V_{in} to V_R	8 V	Flat Pack***.....	900 mW
V_R to V_-	27 V		
V_R to V_{in}	8 V		
Current (S or D)		*All leads welded or soldered to PC board	
DG189	200 mA	**Derate 12 mW/°C above 75°C	
DG190, DG191	30 mA	***Derate 10 mW/°C above 75°C	

SCHEMATIC DIAGRAM (Typical Channel)


ELECTRICAL CHARACTERISTICS¹
 $T_A = 25^\circ\text{C}$

	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: V+ = 15 V, V- = -15 V, VL = 5 V, VR = 0 V	LIMITS						UNIT	
				DG189A			OG189B				
				MIN ²	TYP ³	MAX	MIN ²	TYP ³	MAX		
SWITCH	Analog Signal Range	VANALOG		-7.5		15	-7.5		15	V	
	Drain-Source ON Resistance	rDS(on)	IS = -1 mA, VD = 7.5 V, VIN = 0.8 V or 2.0 V ⁴		7.5	10			15	Ω	
	Source OFF Leakage Current	IS(off)	VIN = 0.8 V or 2.0 V ⁴	VS = 10 V, VD = -10 V V+ = 10 V, V- = -20 V		0.05	10		15	nA	
		VS = 7.5 V, VD = -7.5 V			0.05	10		15			
	Drain OFF Leakage Current	ID(off)		VS = 10 V, VD = -10 V V+ = 10 V, V- = -20 V		0.04	10		15		
		VS = 7.5 V, VD = -7.5 V			0.03	10		15			
	Channel ON Leakage Current	ID(on)+ IS(on)	VD = VS = 7.5 V, VIN = 0.8 V or 2.0 V ⁴	-2	-0.1		-10				
Saturation Drain Current	IDSS	2 ms Pulse Duration		300		300			mA		
INPUT	Input Current With Input Voltage High	IINH	VIN = 5 V		<0.01	10			10	μA	
	Input Current With Input Voltage Low	IINL	VIN = 0	-250	-30		-250				
DYNAMIC	Turn-ON Time	ton	See Switching Time Test Circuit		240	300			300	ns	
	Turn-OFF Time	toff			140	250			300		
	Source OFF Capacitance	CS(off)	f = 1 MHz	VS = -5 V, ID = 0		21		21		pF	
	Drain OFF Capacitance	CD(off)		VD = -5 V, IS = 0		17		17			
	Channel ON Capacitance	CD + S (on)		VD = VS = 0		17		17			
	OFF Isolation			f = 1 MHz, RL = 75 Ω		>55		>55			dB
	SUPPLY	Positive Supply Current	I+	VIN(all) = 0 V		0.6	1.5		0.6	1.5	mA
Negative Supply Current		I-			-5	-2.7		-5	-2.7		
Logic Supply Current		IL				3.1	4.5		3.1	4.5	
Reference Supply Current		IR			-2	-0.9		-2	-0.9		
Positive Supply Current		I+	VIN(all) = 5 V		0.6	1.5		0.6	1.5		
Negative Supply Current		I-			-5	-2.7		-5	-2.7		
Logic Supply Current		IL				3.0	4.5		3.0	4.5	
Reference Supply Current		IR			-2	-1.0		-2	-1.0		

 $T_A = \text{Over Temperature Range}$

	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: V+ = 15 V, V- = -15 V, VL = 5 V, VR = 0 V	LIMITS						UNIT
				DG189A			DG189B			
				MIN ²	TYP ³	MAX	MIN ²	TYP ³	MAX	
SWITCH	Analog Signal Range	VANALOG		-7.5		15	-7.5		15	V
	Drain-Source ON Resistance	rDS(on)	IS = -1 mA, VD = 7.5 V, VIN = 0.8 V or 2.0 V ⁴			20			25	Ω
	Source OFF Leakage Current	IS(off)	VIN = 0.8 V or 2.0 V ⁴	VS = 10 V, VD = -10 V V+ = 10 V, V- = -20 V		1000			300	nA
		VS = 7.5 V, VD = - 7.5 V			1000			300		
	Drain OFF Leakage Current	ID(off)		VS = 10 V, VD = -10 V V+ = 10 V, V- = -20 V		1000			300	
		VS = 7.5 V, VD = - 7.5 V			1000			300		
Channel ON Leakage Current	ID(on)+ IS(on)	VD = VS = 7.5 V, VIN = 0.8 V or 2.0 V ⁴	-200			-200				
INPUT	Input Current With Input Voltage High	IINH	VIN = 5 V			20			20	μA
	Input Current With Input Voltage Low	IINL	VIN = 0	-250			-250			

NOTES:

1. Refer to PROCESS OPTION FLOWCHART for additional information.
2. The algebraic convention whereby the most negative value is a minimum, and the most positive is a maximum, is used in this data sheet.
3. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
4. V_{in} = input voltage to perform proper function.

ELECTRICAL CHARACTERISTICS 1 (Cont.)
 $T_A = 25^\circ\text{C}$

	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: V+ = 15 V, V- = -15 V, VL = 5 V, VR = 0 V		LIMITS						UNIT
					DG190A			DG190B			
					MIN ²	TYP ³	MAX	MIN ²	TYP ³	MAX	
SWITCH	Analog Signal Range	VANALOG			-7.5		15	-7.5		15	V
	Drain-Source ON Resistance	rDS(on)	IS = -1 mA, VD = 7.5 V, VIN = 0.8 V or 2.0 V ⁴			18	30			50	Ω
	Source OFF Leakage Current	IS(off)	VIN = 0.8 V or 2.0 V ⁴	VS = 10 V, VD = -10 V V+ = 10 V, V- = -20 V		0.08	1			5	nA
		VS = 7.5 V, VD = -7.5 V			0.1	1			5		
	Drain OFF Leakage Current	ID(off)		VS = 10 V, VD = -10 V V+ = 10 V, V- = -20 V		0.5	1			5	
		VS = 7.5 V, VD = -7.5 V			0.6	1			5		
Channel ON Leakage Current	ID(on)+ IS(on)	VD = VS = 7.5 V, VIN = 0.8 V or 2.0 V ⁴		-2	-0.02		-10				
INPUT	Input Current With Input Voltage High	IINH	VIN = 5 V				10			10	μA
	Input Current With Input Voltage Low	IINL	VIN = 0		-250	-30		-250			
DYNAMIC	Turn-ON Time	ton	See Switching Time Test Circuit			85	150			180	ns
	Turn-OFF Time	toff				95	130			150	
	Source OFF Capacitance	CS(off)	f = 1 MHz	VS = -5 V, ID = 0		9			9	pF	
	Drain OFF Capacitance	CD(off)		VD = -5 V, IS = 0		6			6		
	Channel ON Capacitance	CD + S (on)		VD = VS = 0		14			14		
	OFF Isolation		f = 1 MHz, RL = 75 Ω			>50		>50			dB
SUPPLY	Positive Supply Current	I+	VIN(all) = 0 V			0.6	1.5		0.6	1.5	mA
	Negative Supply Current	I-			-5.0	-2.7		-5.0	-2.7		
	Logic Supply Current	IL				3.1	4.5		3.1	4.5	
	Reference Supply Current	IR			-2.0	-1.0		-2.0	-1.0		
	Positive Supply Current	I+	VIN(all) = 5 V			0.6	1.5		0.6	1.5	
	Negative Supply Current	I-			-5.0	-2.7		-5.0	-2.7		
	Logic Supply Current	IL				3.1	4.5		3.1	4.5	
	Reference Supply Current	IR			-2.0	-1.0		-2.0	-1.0		

 $T_A = \text{Over Temperature Range}$

	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: V+ = 15 V, V- = -15 V, VL = 5 V, VR = 0 V	LIMITS						UNIT	
				DG190A			DG190B				
				MIN ²	TYP ³	MAX	MIN ²	TYP ³	MAX		
SWITCH	Analog Signal Range	VANALOG			-7.5		15	-7.5		15	V
	Drain-Source ON Resistance	rDS(on)	IS = -1 mA, VD = 7.5 V, VIN = 0.8 V or 2.0 V ⁴				60			75	Ω
	Source OFF Leakage Current	IS(off)	VIN = 0.8 V or 2.0 V ⁴	VS = 10 V, VD = -10 V V+ = 10 V, V- = -20 V			100			100	nA
		VS = 7.5 V, VD = -7.5 V				100			100		
	Drain OFF Leakage Current	ID(off)		VS = 10 V, VD = -10 V V+ = 10 V, V- = -20 V			100			100	
			VS = 7.5 V, VD = -7.5 V			100			100		
	Channel ON Leakage Current	ID(on)+ IS(on)	VD = VS = 7.5 V, VIN = 0.8 V or 2.0 V ⁴		-200			-200			
INPUT	Input Current With Input Voltage High	IINH	VIN = 5 V				20				μA
	Input Current With Input Voltage Low	IINL	VIN = 0		-250			-250		20	

NOTES:

- Refer to PROCESS OPTION FLOWCHART for additional information.
- The algebraic convention whereby the most negative value is a minimum, and the most positive is a maximum, is used in this data sheet.
- Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- V_{in} = input voltage to perform proper function.

ELECTRICAL CHARACTERISTICS 1 (Cont.)
 $T_A = 25^\circ\text{C}$

	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: V ⁺ = 15 V, V ⁻ = -15 V, V _L = 5 V, V _R = 0 V	LIMITS						UNIT
				DG191A			DG191B			
				MIN ²	TYP ³	MAX	MIN ²	TYP ³	MAX	
SWITCH	Analog Signal Range	V _{ANALOG}		-10		15	-10		15	V
	Drain-Source ON Resistance	r _{DS(on)}	I _S = -1 mA, V _D = 7.5 V, V _{in} = 0.8 V or 2.0 V ⁴		35	75			100	Ω
	Source OFF Leakage Current	I _{S(off)}	V _{in} = 0.8 V or 2.0 V ⁴	V _S = 10 V, V _D = -10 V V ⁺ = 10 V, V ⁻ = -20 V	0.05	1			5	nA
		V _S = 7.5 V, V _D = -7.5 V		0.07	1			5		
	Drain OFF Leakage Current	I _{D(off)}		V _S = 10 V, V _D = -10 V V ⁺ = 10 V, V ⁻ = -20 V	0.04	1			5	
			V _S = 7.5 V, V _D = -7.5 V	0.05	1			5		
Channel ON Leakage Current	I _{D(on)} ⁺ I _{S(on)}	V _D = V _S = 7.5 V, V _{in} = 0.8 V or 2.0 V ⁴	-2	-0.03		-10				
INPUT	Input Current With Input Voltage High	I _{INH}	V _{in} = 5 V			10				μA
	Input Current With Input Voltage Low	I _{INL}	V _{in} = 0	-250	-35		-250			
DYNAMIC	Turn-ON Time	t _{on}	See Switching Time Test Circuit		120	250			300	ns
	Turn-OFF Time	t _{off}			100	130			150	
	Source OFF Capacitance	C _{S(off)}	f = 1 MHz	V _S = -5 V, I _D = 0	9			9		pF
	Drain OFF Capacitance	C _{D(off)}		V _D = -5 V, I _S = 0	6			6		
	Channel ON Capacitance	C _D + S (on)		V _D = V _S = 0	14			14		
SUPPLY	OFF Isolation		f = 1 MHz, R _L = 75 Ω		>50			>50		dB
	Positive Supply Current	I ⁺	V _{in(all)} = 0 V			1.5			1.5	mA
	Negative Supply Current	I ⁻		-5			-5			
	Logic Supply Current	I _L				4.5			4.5	
	Reference Supply Current	I _R		-2			-2			
	Positive Supply Current	I ⁺	V _{in(all)} = 5 V			1.5			1.5	
	Negative Supply Current	I ⁻		-5			-5			
	Logic Supply Current	I _L				4.5			4.5	
	Reference Supply Current	I _R		-2			-2			

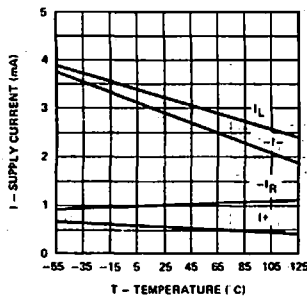
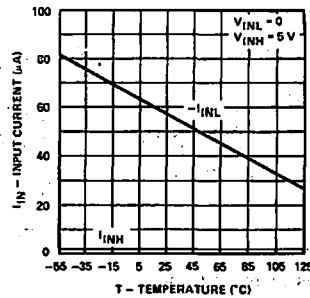
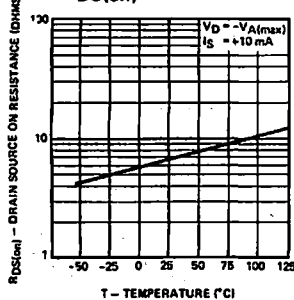
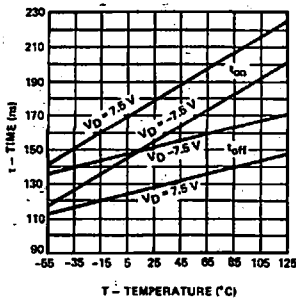
 $T_A = \text{Over Temperature Range}$

	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: V+ = 15 V, V- = -15 V, VL = 5 V, VR = 0 V		LIMITS						UNIT
					DG191A			DG191B			
					MIN ²	TYP ³	MAX	MIN ²	TYP ³	MAX	
SWITCH	Analog Signal Range	VANALOG			-10		15	-10		15	V
	Drain-Source ON Resistance	rDS(on)	IS = -1 mA, VD = 7.5 V, VIN = 0.8 V or 2.0 V ⁴				150			150	Ω
	Source OFF Leakage Current	IS(off)	VIN = 0.8 V or 2.0 V ⁴	VS = 10 V, VD = -10 V V+ = 10 V, V- = -20 V			100			100	nA
		VS = 7.5 V, VD = -7.5 V				100			100		
	Drain OFF Leakage Current	ID(off)		VS = 10 V, VD = -10 V V+ = 10 V, V- = -20 V			100			100	
			VS = 7.5 V, VD = -7.5 V			100			100		
Channel ON Leakage Current	ID(on) ⁺ IS(on)	VD = VS = 7.5 V, VIN = 0.8 V or 2.0 V ⁴		-200			-200				
INPUT	Input Current With Input Voltage High	IINH	VIN = 5 V				20			20	μA
	Input Current With Input Voltage Low	IINL	VIN = 0		-250			-250			

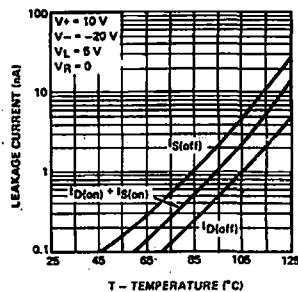
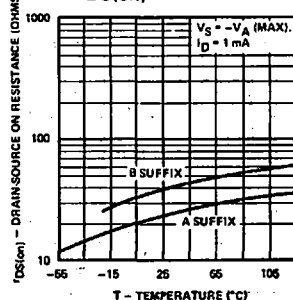
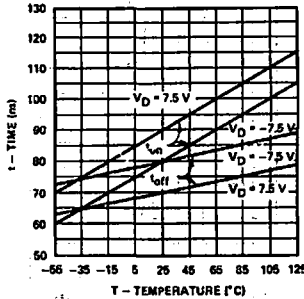
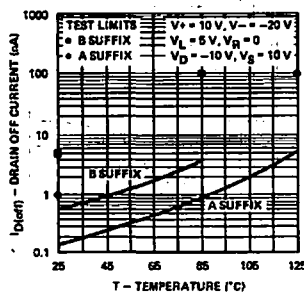
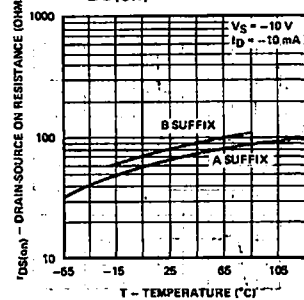
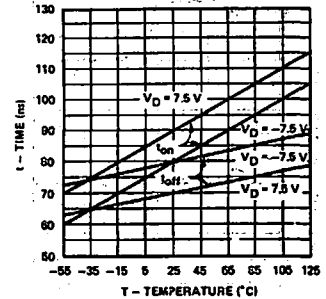
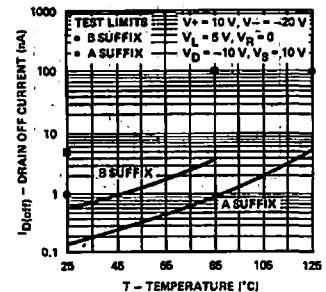
NOTES:

1. Refer to PROCESS OPTION FLOWCHART for additional information.
2. The algebraic convention whereby the most negative value is a minimum, and the most positive is a maximum, is used in this data sheet.
3. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
4. V_{in} = input voltage to perform proper function.

Supply Current vs Temperature

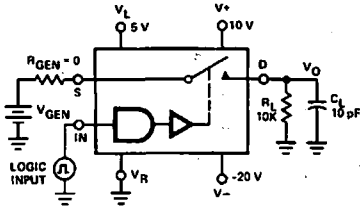
 I_{IN} vs V_{IN} and Temperature10 Ω
DG189 $r_{DS(on)}$ vs TemperatureSwitching Time vs V_D
and Temperature

Leakage vs Temperature

30 Ω
DG190 $r_{DS(on)}$ vs TemperatureSwitching Time vs V_D
and Temperature $I_{D(off)}$ vs Temperature75 Ω
DG191 $r_{DS(on)}$ vs TemperatureSwitching Time vs V_D
and Temperature $I_{D(off)}$ vs Temperature

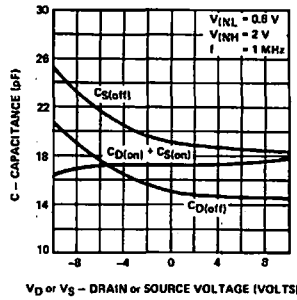
TYPICAL CHARACTERISTICS (Cont.)

Typical delay, rise, fall, settling times, and switching transients in this circuit.

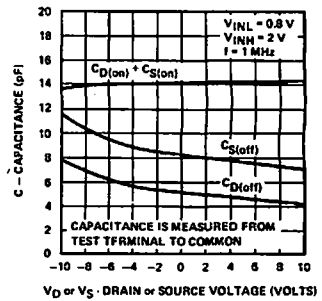


If R_{GEN} , R_L or C_L is increased, there will be proportional increases in rise and/or fall times.

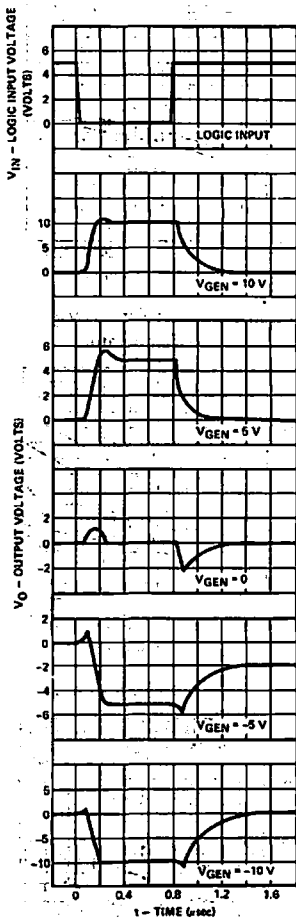
Capacitance vs V_D or V_S
10 Ω FET



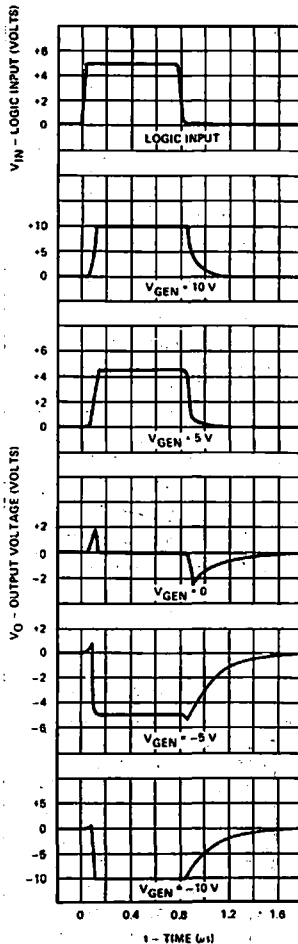
Capacitance vs V_D or V_S
30-75 Ω FET



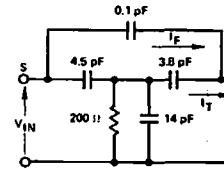
DG189



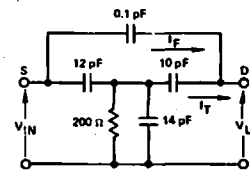
DG190, DG191



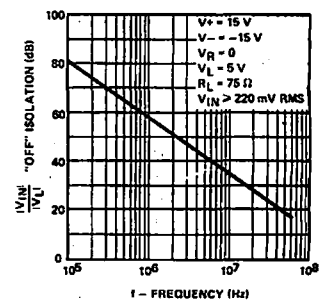
Equivalent "OFF" Circuit 30-75 Ω FET



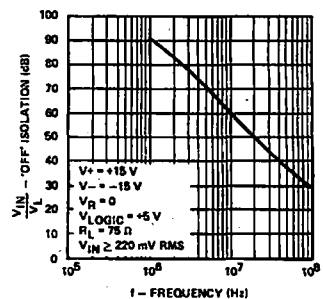
Equivalent "OFF" Circuit 10 Ω FET



"OFF" Isolation vs Frequency 10 Ω FET

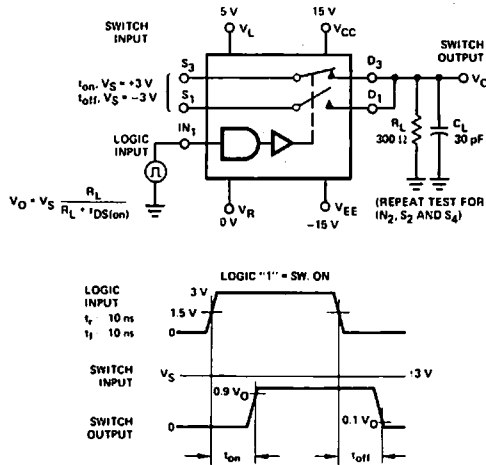


"OFF" Isolation vs Frequency
30-75 Ω FET



SWITCHING TIME TEST CIRCUIT

Switch output waveform shown for V_S = constant with logic input waveform as shown. Note that V_S may be + or - as per switching time test circuit. V_O is the steady state output with switch on. Feedthrough via gate capacitance may result in spikes at leading and trailing edge of output waveform.



APPLICATION HINTS*

Switch Family	V+ Positive Supply Voltage (V)	V- Negative Supply Voltage (V)	V _L Logic Supply Voltage (V)	V _R Reference Supply Voltage (V)	V _{IN} Logic Input Voltage V _{INH} Min/ V _{INL} Max (V)	V _S Analog Voltage Range (V)
10 Ω	+15**	-15	+5	Gnd	2.0/0.8	-7.5 to +15
and	+10	-20	+5	Gnd	2.0/0.8	-12.5 to +10
30 Ω	+12	-12	+5	Gnd	2.0/0.8	-4.5 to +12
75 Ω	+15**	-15	+5	Gnd	2.0/0.8	-10 to +15
	+10	-20	+5	Gnd	2.0/0.8	-15 to +10
	+12	-12	+5	Gnd	2.0/0.8	-7 to +12

*Application Hints are for DESIGN AID ONLY, not guaranteed and not subject to production testing.

**Electrical Parameter Chart based on V+ = +15 V, V- = -15 V, V_L = 5 V, V_R = Gnd.

DG200A

Dual Monolithic SPST CMOS

Analog Switch

FEATURES

- ± 15 V Input Signal Range
- 44 Volt Supply Maximum Ratings
- Low Input Resistance $r_{DS(on)} 70 \Omega$
- Bidirectional Signal Handling
- Static Protected Logic Inputs
- Latch Proof
- TTL and CMOS Compatibility

BENEFITS

- Accurate Signal Switching
- Higher Power Supply Tolerance
- Reduces External Components

APPLICATIONS

- Analog Multiplexing
- Video Signal Switching
- Servo Control Switching
- Programmable Gain Amplifiers

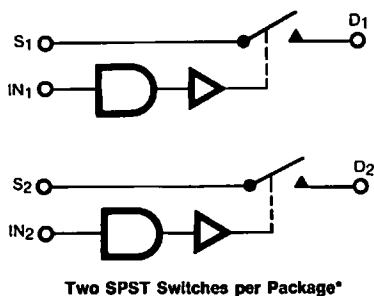
DESCRIPTION

The DG200A is a 2-channel, single-pole, single-throw analog switch designed for general purpose switching applications in communications, instrumentation, and process control. The DG200A is designed on the proprietary PLUS-40 CMOS process to insure low and constant ON resistance over the entire ± 15 V analog range. This bidirectional switch introduces no offset voltage of its own in the ON condition, and will block signals up to 30 V

peak-to-peak in the OFF condition.

Package options are the 14 lead plastic or ceramic DIP, or the 10 pin metal can. The ceramic DIP and metal can versions are characterized for operation over the standard industrial and military temperature ranges while the plastic DIP is specified for commercial temperature range only.

FUNCTIONAL BLOCK DIAGRAM



Truth Table

LOGIC	SWITCH
0	ON
1	OFF

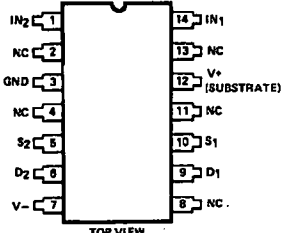
Logic "0" ≤ 0.8 V

Logic "1" ≤ 2.4 V

*Switches shown for Logic "1" Input

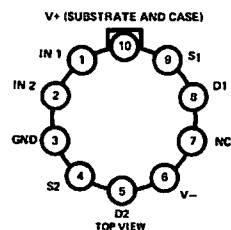
PIN CONFIGURATION

Dual-In-Line Package



Order Numbers:
 DG200AAK or DG200ABK
 or DG200ACK
 See Package 9
 DG200ACJ
 See Package 7

Metal Can Package



Order Numbers:
 DG200AAA, DG200ABA or
 DG200ACA
 See Package 2

ABSOLUTE MAXIMUM RATINGS

Voltages Referenced to V-

V+	44 V
GND	25 V
Digital Inputs ¹ V _S , V _D	-2 V to (V+ +2 V) or 20 mA, whichever occurs first.
Current (Any Terminal Except S or D)	30 mA
Current, S or D	20 mA
Current, S or D	
(Pulsed at 1 msec, 10% Duty Cycle Max)	100 mA
Operating Temperature (A Suffix)	-55 to 125°C
(B Suffix)	-25 to 85°C
(C Suffix)	0 to 70°C

 Storage Temperature (A & B Suffix) -65 to 150°C
 (C Suffix) -65 to 125°C

Power Dissipation (Package)*

Metal Can**	450 mW
14 Pin Ceramic DIP***	825 mW
14 Pin Plastic DIP****	470 mW

*All leads soldered or welded to PC board.

**Derate 6 mW/°C above 75°C.

***Derate 11 mW/°C above 75°C.

****Derate 6.5 mW/°C above 25°C.

ELECTRICAL CHARACTERISTICS²

 T_A = 25°C

	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: V+ = +15 V, V- = -15 V, GND = 0	LIMITS						UNIT	
				DG200A			DG200B/C				
				MIN ³	TYP ⁴	MAX	MIN ³	TYP ⁴	MAX		
SWITCH	Analog Signal Range	V _{ANALOG}		-15		15	-15		15	V	
	Drain-Source ON Resistance	r _{DS(on)}	V _D = ±10 V, V _{in} = 0.8 V, I _S = 1 mA		45	70		45	80	Ω	
	Source OFF Leakage Current	I _{S(off)}	V _{in} = 2.4 V	V _S = 14 V, V _D = -14 V		0.01	2.0	0.01	5.0	nA	
	Drain OFF Leakage Current	I _{D(off)}		V _S = -14 V, V _D = 14 V		-2.0	-0.02	-5.0	-0.02		
				V _D = 14 V, V _S = -14 V		0.01	2.0	0.01	5.0		
				V _D = -14 V, V _S = 14 V		-2.0	-0.02	-5.0	-0.02		
Drain ON Leakage Current ⁵	I _{D(on)}	V _S = V _D = 14 V, V _{in} = 0.8 V, V _S = V _D = -14 V, V _{in} = 0.8 V		0.1	2.0		0.1	5.0			
INPUT	Input Current With Input Voltage High	I _{INH}	V _{in} = 2.4 V, V _{in} = 15 V	-1.0	0.0009		-1.0	0.0009		μA	
	Input Current With Input Voltage Low	I _{INL}	V _{in} = 0 V		0.005	1.0		0.005	1.0		
				-1.0	-0.0015		-1.0	-0.0015			
				Turn-ON Time	t _{on}	See Switching Time Test Circuit		440	1000		440
Turn-OFF Time	t _{off}		370	500			370	500			
DYNAMIC	Charge Injection	O	C _L = 1000 pF, V _{GEN} = 0 V, R _{GEN} = 0 Ω		-10			-10		pC	
	Source OFF Capacitance	C _{S(off)}	V _S = 0 V, V _{in} = 5 V, f = 140 kHz		9.0			9.0		pF	
	Drain OFF Capacitance	C _{D(off)}	V _D = 0 V, V _{in} = 5 V, f = 140 kHz		9.0			9.0			
	Channel ON Capacitance	C _{D(on)} + C _{S(on)}	V _D = V _S = 0 V, V _{in} = 0 V		25			25			
	OFF Isolation ⁶		V _{in} = 5 V, Z _L = 75 Ω V _S = 2.0 V, f = 1 MHz		75			75		dB	
	Crosstalk (Channel To Channel)				90			90			
	SUPPLY	Positive Supply Current	I+	Both Channels ON or OFF V _{in} = 0 and 2.4 V		0.8	2		0.8	2	nA
Negative Supply Current		I-	-1		-0.23		-1	-0.23			

NOTES:

1. Signals on S_X, D_X, or I_{NX}, exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
2. Refer to PROCESS OPTION FLOWCHART for additional information.
3. The algebraic convention whereby the most negative value is a minimum, and the most positive is a maximum, is used in this data sheet.
4. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
5. I_{D(on)} is leakage from driver into "ON" switch.
6. "OFF" isolation = 20 log V_S/V_D, V_S = input to OFF switch, V_D = output.

ELECTRICAL CHARACTERISTICS² (Cont.)
 T_A = Over Temperature Range

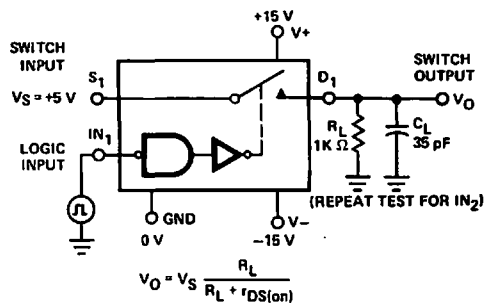
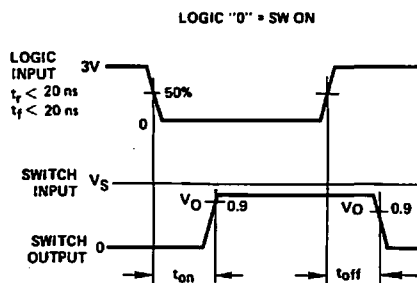
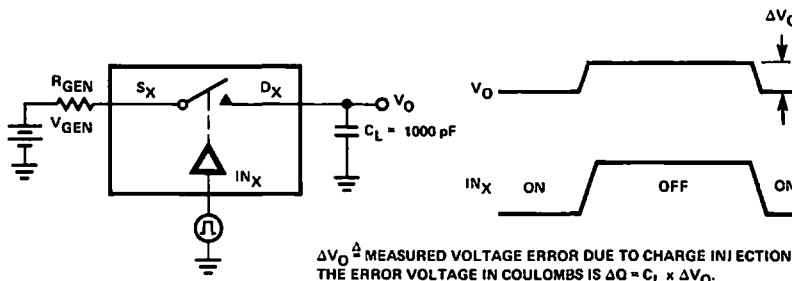
	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: V+ = +15 V, V- = -15 V, GND = 0	LIMITS						UNIT
				DG200A			DG200B/C			
				MIN ³	TYP ⁴	MAX	MIN	TYP ⁴	MAX	
SWITCH	Analog Signal Range	V _{ANALOG}		-15		15	-15		15	V
	Drain-Source ON Resistance	r _{DS(on)}	V _D = ±10 V, V _{in} = 0.8 V, I _S = 1 mA			100			100	Ω
	Source OFF Leakage Current	I _{S(off)}	V _{in} = 2.4 V	V _S = 14 V, V _D = -14 V			100		100	nA
		V _S = -14 V, V _D = 14 V		-100		-100				
		V _D = 14 V, V _S = -14 V				100		100		
	Drain OFF Leakage Current	I _{D(off)}	V _D = -14 V, V _S = 14 V	-100		-100				
Drain ON Leakage Current ⁵	I _{D(on)}	V _S = V _D = 14 V, V _{in} = 0.8 V, V _S = V _D = -14 V, V _{in} = 0.8 V			200		-200	200		
INPUT	Input Current With Input Voltage High	I _{INH}	V _{in} = 2.4 V, V _{in} = 15 V	-10			-10		10	μA
	Input Current With Input Voltage Low	I _{INL}	V _{in} = 0 V	-10			-10			

NOTES:

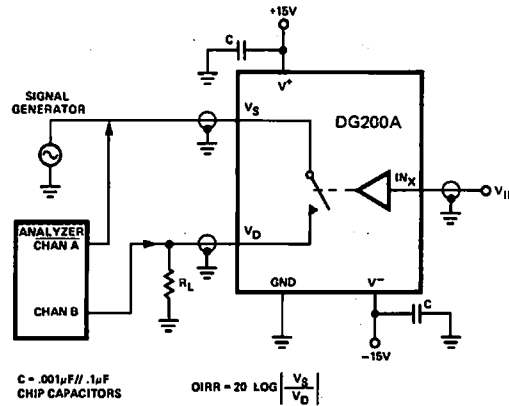
1. Signals on S_X , D_X , or IN_X , exceeding V_+ or V_- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
2. Refer to PROCESS OPTION FLOWCHART for additional information.
3. The algebraic convention whereby the most negative value is a minimum, and the most positive is a maximum, is used in this data sheet.
4. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
5. $I_{D(on)}$ is leakage from driver into "ON" switch.
6. "OFF" isolation $\geq 20\log V_S/V_D$, V_S = input to OFF switch, V_D = output.

SWITCHING TIME TEST CIRCUIT

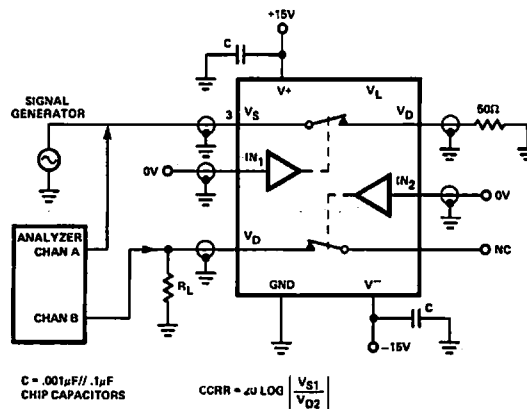
Switch output waveform shown for V_S = constant with logic input waveform as shown. Note that V_S may be + or - as per switching time test circuit. V_O is the steady state output with switch on. Feedthrough via gate capacitance may result in spikes at leading and trailing edge of output waveform.


CHARGE INJECTION TEST CIRCUIT


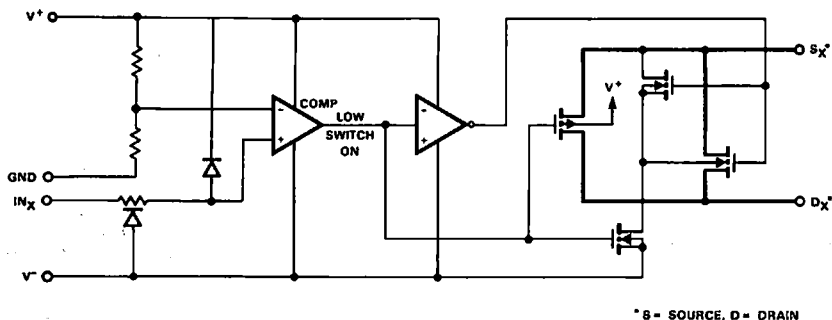
OFF ISOLATION TEST CIRCUIT



CHANNEL TO CHANNEL CROSSTALK TEST CIRCUIT



SCHEMATIC DIAGRAM (TYPICAL CHANNEL)



DG201A/DG202

Quad Monolithic SPST CMOS

Analog Switches



FEATURES

- ± 15 V Input Signal Range
- Low OFF Leakage
- Low ON Resistance
- 44 V Maximum Supply Ratings
- TTL and CMOS Compatible
- Logic Inputs Accept Negative Voltages
- Low Transient Switching

BENEFITS

- No Pull-Up Resistors Required
- Reduced Power Supply Consumption
- Can be Driven from Comparators or Op Amps Without Limiting Resistors
- Multiple Sourced

APPLICATIONS

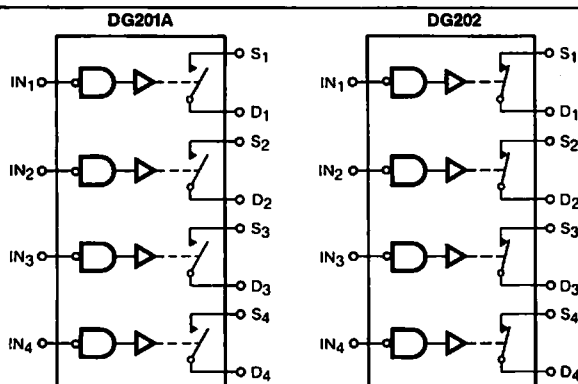
- Disk Drives
- Radar Systems
- Video Terminals
- Low Transient Sample/Holds

DESCRIPTION

The DG201A and DG202 Quad SPST analog switches offer normally open (DG201A) or normally closed (DG202) break-before-make switching for applications where low on resistance [$r_{DS(on)}$], wide signal range (± 15 V), and low charge-transfer are required. In the OFF state, these switches will block up to 30 V peak-to-peak and have a

44 V maximum power supply rating. These switches will conduct current in either direction with no offset in the ON state. ON resistance is nearly constant over the entire analog signal range, thus providing precision signal transfer across the switch. Internal pull-up resistors simplify interface to CMOS or TTL drive circuits.

FUNCTIONAL BLOCK DIAGRAM



Four SPST Switches Per Package*

Truth Table

Logic	DG201A	DG202
0	ON	OFF
1	OFF	ON

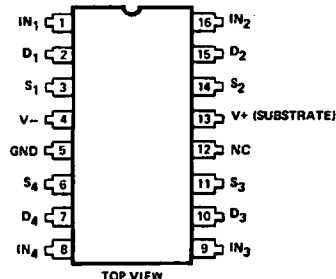
Logic "0" ≤ 0.8 V

Logic "1" ≥ 2.4 V

*Switches Shown For Logic "1" Input

PIN CONFIGURATION

Dual-In-Line Package



Order Numbers:

DG201AAK, DG201ABK or DG201ACK

DG202AK, DG202BK or DG202CK

See Package 10

DG201ACJ or DG202CJ

See Package 8

ABSOLUTE MAXIMUM RATINGS

Voltages Referenced to V-

V+ 44 V

GND 25 V

 Digital Inputs¹ V_S, V_D -2 V to (V+ +2 V) or

20 mA, whichever occurs first.

Current, Any Terminal Except S or D 30 mA

Continuous Current, S or D 20 mA

Peak Current, S or D

(Pulsed at 1 msec, 10% duty cycle max) 70 mA

Storage Temperature (A & B Suffix) -65 to 150°C

(C Suffix) -65 to 125°C

Operating Temperature (A Suffix) -55 to 125°C

(B Suffix) -25 to 85°C

(C Suffix) 0 to 70°C

Power Dissipation (Package)*

16 Pin DIP** 900 mW

16 Pin Plastic DIP*** 470 mW

*Device mounted with all leads soldered or welded to PC board.

**Derate 12 mW/°C above 75°C

***Derate 6.5 mW/°C above 25°C

ELECTRICAL CHARACTERISTICS²

 T_A = 25°C

	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: V = 15 V, V- = -15 V, GND = 0	LIMITS						UNIT
				DG201AA/DG202A			DG201AB,C/DG202B,C			
				MIN ³	TYP ⁴	MAX	MIN ³	TYP ⁴	MAX	
SWITCH	Analog Signal Range	V _{ANALOG}		-15		15	-15		15	V
	Drain-Source ON Resistance	r _{DS(on)}	V _D ±10 V, V _S = 1 mA V _{in} = 0.8 V (DG201A) V _{in} = 2.0 V (DG202)		115	175		115	200	Ω
	Source OFF Leakage Current	I _{S(off)}	V _{in} = 2.4 V (DG201A) V _S = 14 V, V _D = -14 V V _S = -14 V, V _D = 14 V	-1.0	-0.02		-5.0	-0.02		nA
	Drain OFF Leakage Current	I _{D(off)}	V _{in} = 0.8 V (DG202) V _D = 14 V, V _S = -14 V V _D = -14 V, V _S = 14 V	-1.0	-0.02		-5.0	-0.02		
	Drain ON Leakage Current ⁵	I _{D(on)}	V _S = 14 V, V _D = 14 V V _{in} = 0.8 V (DG201A) V _{in} = 2.4 V (DG202)	-1.0	-0.15		-5.0	-0.15		
INPUT	Input Current With Input Voltage High	I _{INH}	V _{in} = 2.4 V V _{in} = 15 V	-1.0	-0.0004		-1.0	-0.0004		μA
	Input Current With Input Voltage Low	I _{INL}	V _{in} = 0 V	-1.0	-0.0004		-1.0	-0.0004		
DYNAMIC	Turn-ON Time	t _{on}	See Switching Time Test Circuit		480	600		480	600	ns
	Turn-OFF Time	t _{off}			370	450		370	450	
	Charge Injection	Q	C _L = 1000 pF, V _{GEN} = 0 V, R _{GEN} = 0 Ω		20			20		pC
	Source OFF Capacitance	C _{S(off)}	V _S = 0 V, V _{in} = 5 V f = 140 kHz		5			5		pF
	Drain OFF Capacitance	C _{D(off)}			5			5		
	Channel ON Capacitance	C _{D(on)} + C _{S(on)}	V _D = V _S = 0 V, V _{in} = 0 V		16			16		
	OFF Isolation		V _{in} = 5 V, Z _L = 75 Ω		70			70		dB
Crosstalk (Channel To Channel)		V _S = 2.0 V, f = 100 kHz		90			90			
SUPPLY	Positive Supply Current	I+	All Channels ON or OFF		0.9	2		0.9	2	mA
	Negative Supply Current	I-		-1	-0.3		-1	-0.3		

NOTES:

1. Signals on S_x, D_x, or I_{Nx}, exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
2. Refer to PROCESS OPTION FLOWCHART for additional information.
3. The algebraic convention whereby the most negative value is a minimum, and the most positive is a maximum, is used in this data sheet.
4. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
5. I_{D(on)} is leakage from driver into "ON" switch.

ELECTRICAL CHARACTERISTICS (Cont.)² T_A = Over Temperature Range

	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: V = 15 V, V- = -15 V, GND = 0		LIMITS						UNIT
					DG201AA/DG202A			DG201AB,C/DG202B,C			
					MIN ³	TYP ⁴	MAX	MIN ³	TYP ⁴	MAX	
SWITCH	Analog Signal Range	V _{ANALOG}			-15		15	-15		15	V
	Drain-Source ON Resistance	r _{DS(on)}	V _D ±10 V, I _S = 1 mA	V _{in} = 0.8 V (DG201A) V _{in} = 2.4 V (DG202)			250			250	Ω
	Source OFF Leakage Current	I _{S(off)}	V _{in} = 2.4 V (DG201A)	V _S = 14 V, V _D = -14 V V _S = -14 V, V _D = 14 V			100			100	nA
	Drain OFF Leakage Current	I _{D(off)}	V _{in} = 0.8 V (DG202)	V _D = 14 V, V _S = -14 V V _D = -14 V, V _S = 14 V	-100		100	-100		100	
	Drain ON Leakage Current ⁵	I _{D(on)}	V _S = 14 V, V _D = 14 V	V _{in} = 0.8 V (DG201A) V _{in} = 2.4 V (DG202)	-200		200	-200		200	
INPUT	Input Current With Input Voltage High	I _{INH}	V _{in} = 2.4 V		-1.0			-10			μA
			V _{in} = 15 v				10			10	
	Input Current With Input Voltage Low	I _{INL}	V _{in} = 0 V		-10			-10			

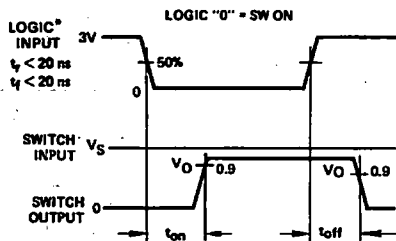
NOTES:

1. Signals on S_X, D_X, or I_{NX}, exceeding V⁺ or V⁻ will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
2. Refer to PROCESS OPTION FLOWCHART for additional information.
3. The algebraic convention whereby the most negative value is a minimum, and the most positive is a maximum, is used in this data sheet.
4. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
5. I_{D(on)} is leakage from driver into "ON" switch.

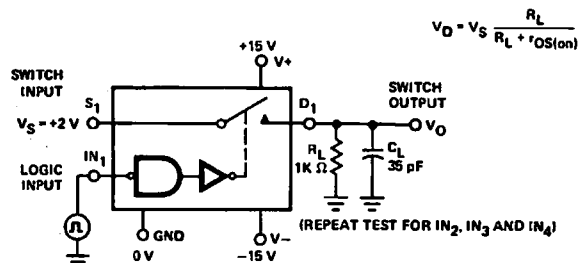
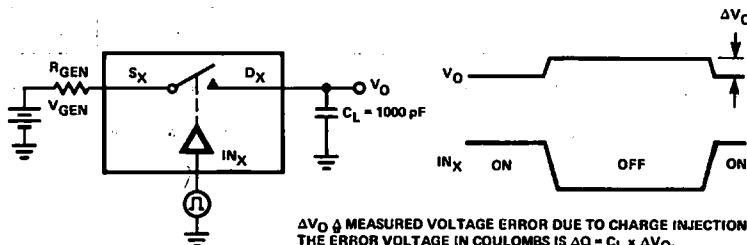
SWITCHING TIME TEST CIRCUIT

Switch output waveform shown for V_S = constant with logic input waveform as shown. Note that V_S may be + or - as per switching time test circuit. V_O is the steady state

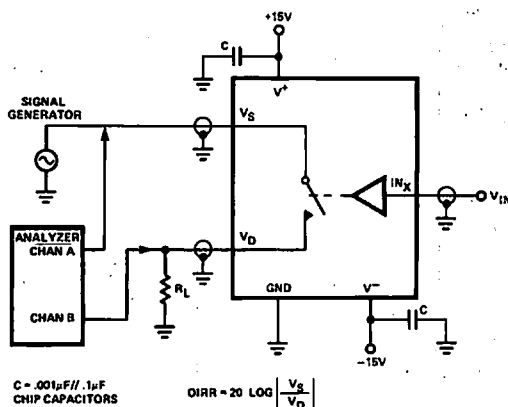
output with switch on. Feedthrough via gate capacitance may result in spikes at leading and trailing edge of output waveform.



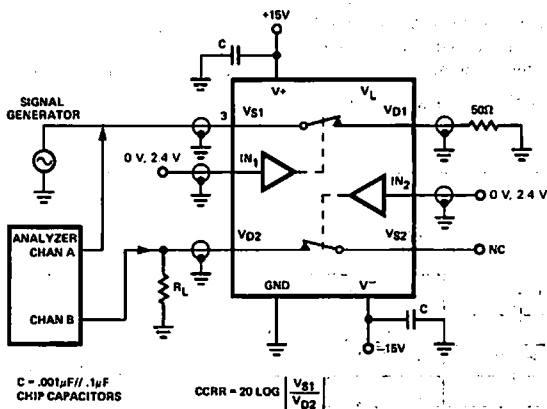
* Logic Shown for DG201A, Invert for DG202.


CHARGE INJECTION TEST CIRCUIT


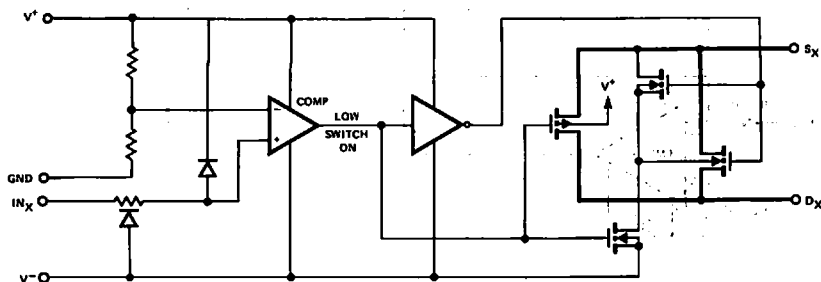
ΔV_O Δ MEASURED VOLTAGE ERROR DUE TO CHARGE INJECTION
THE ERROR VOLTAGE IN COULOMBS IS $\Delta Q = C_L \times \Delta V_O$.



CHANNEL TO CHANNEL CROSSTALK TEST CIRCUIT



SCHEMATIC DIAGRAM (Typical Channel)*



*DG201A Shown

APPLICATIONS

Application Hints*

V+ Positive Supply Voltage (V)	V- Negative Supply Voltage (V)	V _{IN} Logic Input Voltage V _{INH} Min/ V _{INL} Max (V)	V _S or V _O Analog Voltage Range (V)
+15**	-15	2.4/0.8	-15 to +15
+12	-12	2.4/0.8	-12 to +12
+10	-10	2.4/0.8	-10 to +10
+8***	-8	2.4/0.8	-8 to +8

* Application Hints are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

** Electrical Characteristics chart based on V+ = +15 V, V- = -15 V.

*** Operation below ±8 V is not recommended.

DG201A

LOGIC INPUT	SWITCH STATE	LOGIC VOLT LEVEL
0	ON	≤0.8 V
1	OFF	≥2.4 V

DG202

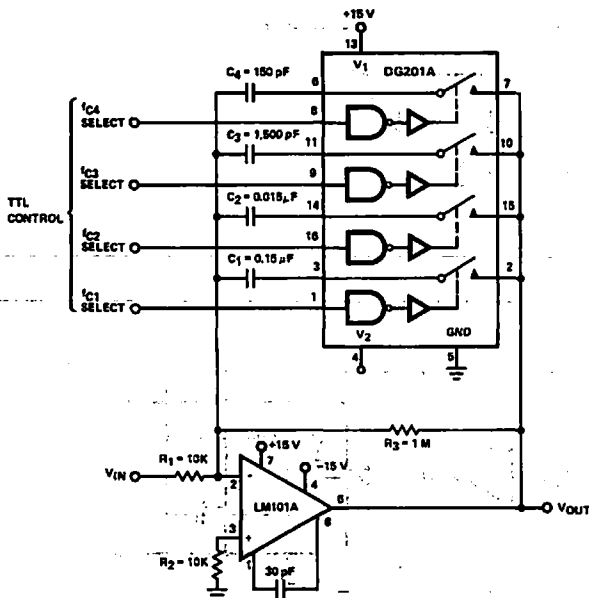
LOGIC INPUT	SWITCH STATE	LOGIC VOLT LEVEL
0	OFF	≤0.8 V
1	ON	≥2.4 V

Logic Inputs

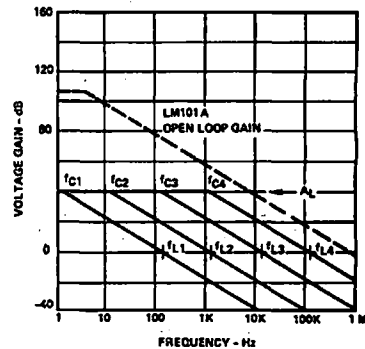
Logic input circuitry protects the input MOS gate from static transients. A series MOS device cuts off when V_{IN} exceeds the positive power supply. Negative transients are clamped to ground by a diode clamp.

The input voltage characteristics have a current spike

occurring at the transition voltage when the logic goes from V_{INH} to V_{INL}. If a series resistor is used for additional static protection, it should be limited to less than 5.6 kΩ to insure switching with worst case current spikes.



Active Low Pass Filter with Digitally Selected Break Frequency



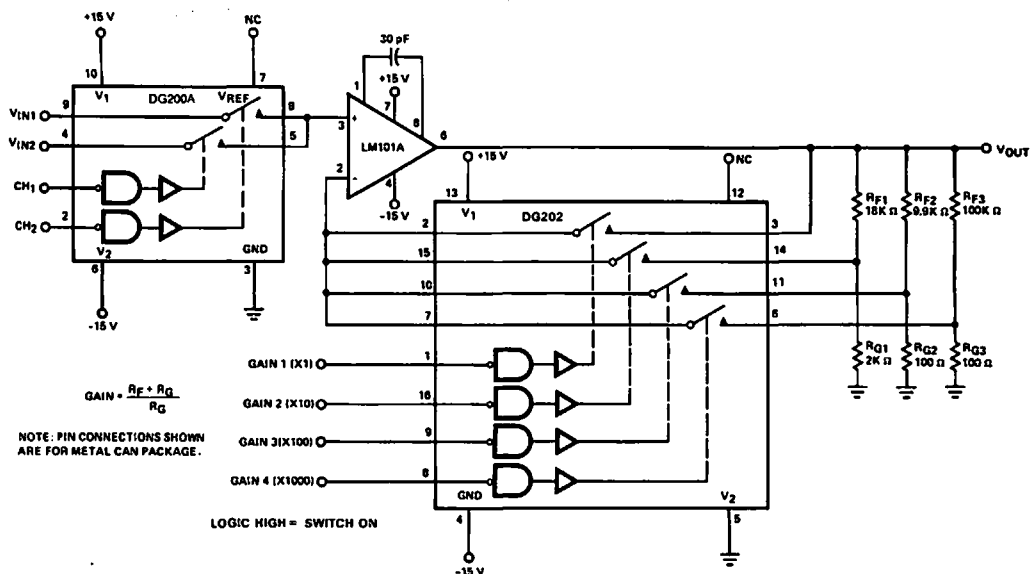
A_L (VOLTAGE GAIN BELOW BREAK FREQUENCY)

$$\frac{R_2}{R_1} = 100 \text{ (40 dB)}$$

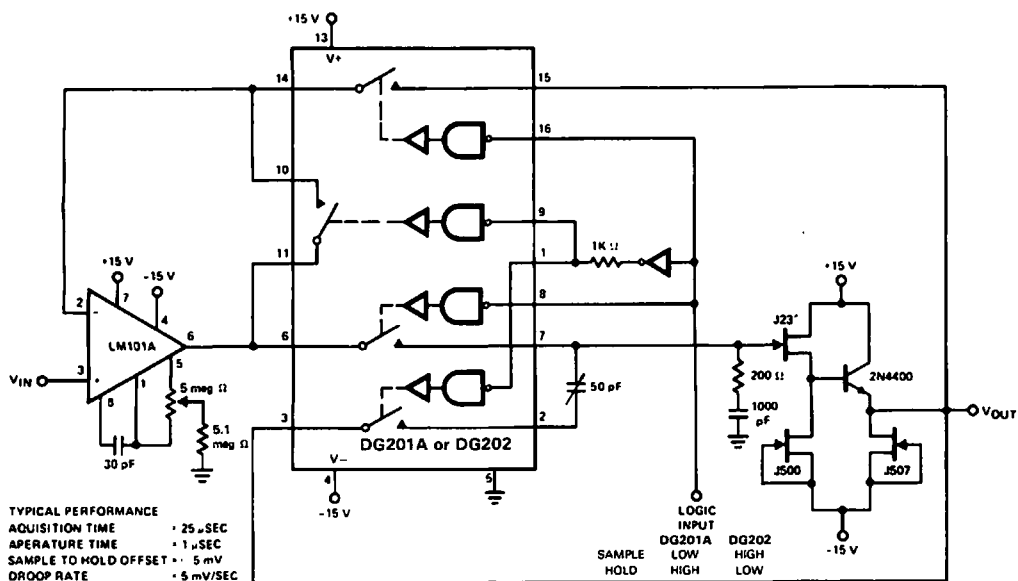
$$f_c \text{ (BREAK FREQUENCY)} = \frac{1}{2\pi R_2 C_X}$$

$$f_L \text{ (UNITY GAIN FREQUENCY)} = \frac{1}{2\pi R_1 C_X}$$

$$\text{MAX ATTENUATION} = \frac{f_{OS(10k)}}{10k} = -40 \text{ dB}$$



A Precision Amplifier with Digitally Programmable Inputs and Gains



Sample and Hold

DG211 / DG212

Low Cost 4-Channel Monolithic SPST CMOS Analog Switches

FEATURES

- Switches ± 15 V Analog Signals
- TTL Compatibility
- PLUS 40 Process
- Logic Inputs accept Negative Voltages
- $R_{ON} \leq 175$ Ohm

BENEFITS

- No Pull-Up Resistors Required
- Reduced Power Supply Consumption
- Can be Driven Directly from Comparators or Op Amps

APPLICATIONS

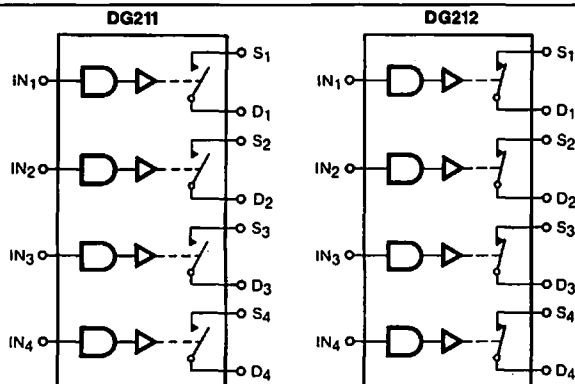
- Disk Drives
- Video Terminals
- Communication Systems

DESCRIPTION

The DG211 and DG212 are low cost 4-channel single-pole-single-throw analog switches for use in general purpose switching applications in communication, instrumentation and process control. Both devices feature true bi-directional performance (with no offset voltage) in the ON condition, and will block signals to 30 V peak-to-peak in the OFF condition. The DG211 and DG212 differ only in that the digital control logic is inverted, as shown in the truth table.

Designed with the proprietary Siliconix PLUS-40 CMOS process to combine low power dissipation with a high breakdown voltage rating of 40 V, both switches will handle ± 15 V input signals with ease, and have a continuous current rating of 20 mA. DG211 and DG212 are supplied in the 16-pin plastic dual-in-line package, and are rated for operation over the 0 to 70°C temperature range.

FUNCTIONAL BLOCK DIAGRAM



Truth Table

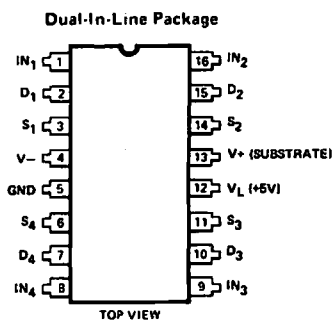
Logic	DG211	DG212
0	ON	OFF
1	OFF	ON

Logic "0" ≤ 0.8 V

Logic "1" ≥ 2.4 V

*Switches Shown for Logic "1" Input

PIN CONFIGURATION



Order Number:
DG211CJ or DG212CJ
See Package 8

ABSOLUTE MAXIMUM RATINGS

V ₊ to V ₋	40 V
V _{IN} to Ground	V ₋ , V ₊
V _L to Ground	-0.3 V, 25 V
V _S or V _D to V ₊	0, -40 V
V _S or V _D to V ₋	0, 40 V
V ₊ to Ground	25 V
V ₋ to Ground	-25 V
Current, Any Terminal Except S or D	30 mA
Continuous Current, S or D	20 mA
Peak Current, S or D (Pulsed at 1 msec, 10% duty cycle max)	70 mA

Storage Temperature	-65 to 125°C
Operating Temperature	0 to 70°C
Power Dissipation (Package)*	
16 Pin Plastic DIP**	470 mW

*Device mounted with all leads soldered or welded to PC board.

**Derate 6.5 mW/°C above 25°C

ELECTRICAL CHARACTERISTICS¹
T_A = 25°C

	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: V ₊ = 15 V, GND = 0	LIMITS			UNIT
				MIN ²	TYP ³	MAX	
SWITCH	Analog Signal Range	V _{ANALOG}		-15		15	V
	Drain-Source ON Resistance	r _{DS (on)}	V _D = ±10 V, V _{IN} = 3.8 V, I _S = 1 mA		115	175	Ω
	Source OFF Leakage Current	I _{S (off)}	V _{IN} = 2.4 V, DG211 V _S = 14 V, V _D = -14 V		0.01	5.0	nA
	Drain OFF Leakage Current	I _{D (off)}	V _{IN} = 0.8 V, DG212 V _S = -14 V, V _D = 14 V	-5.0	-0.02		
			V _D = 14 V, V _S = -14 V		0.01	5.0	
INPUT	Drain ON Leakage Current ⁴	I _{D (on)}	V _S = V _D = -14 V, V _{IN} = 0.8 V, DG211 V _{IN} = 2.4 V, DG212		0.1	5.0	nA
			V _S = V _D = -14 V, V _{IN} = 0.8 V, DG211 V _{IN} = 2.4 V, DG212	-5.0	-0.15		
	Input Current With Input Voltage High	I _{INH}	V _{IN} = 2.4 V	-1.0	-0.0004		μA
	Input Current With Input Voltage Low	I _{INL}	V _{IN} = 15 V		0.003	1.0	
			V _{IN} = 0 V	-1.0	-0.0004		
DYNAMIC	Turn-ON Time	t _{on}	See Switching Time Test Circuit		460	1000	ns
	Turn-OFF Time	t _{off1} t _{off2}	V _S = 2 V, R _L = 1 kΩ, C _L = 35 pF		360 450	500	
	Source OFF Capacitance	C _{S (off)}	V _S = 0 V, V _{IN} = 5 V, f = 1 MHz		5		pF
	Drain OFF Capacitance	C _{D (off)}	V _D = 0 V, V _{IN} = 5 V, f = 1 MHz		5		
	Channel ON Capacitance	C _{D + S (on)}	V _D = V _S = 0 V, V _{IN} = 0 V, f = 1 MHz		16		
	OFF Isolation ⁵	OIRR	V _{IN} = 5 V, R _L = 1 kΩ, C _L = 15 pF, V _S = 1 VRMS, f = 100 kHz		70		dB
	Crosstalk (Channel to Channel)	CCRR			90		
SUPPLY	Positive Supply Current	I ₊	V _{IN} = 0 and 2.4 V		0.35	0.48	mA
	Negative Supply Current	I ₋			0.30	0.48	
	Logic Supply Current	I _L			0.5	1.2	

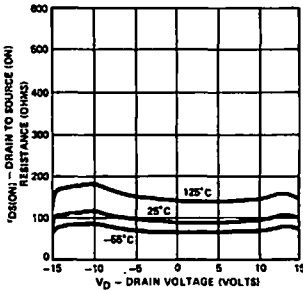
NOTES:

1. Refer to PROCESS OPTION FLOWCHART for additional information.
2. The algebraic convention whereby the most negative value is a minimum, and the most positive is a maximum, is used in this data sheet.
3. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
4. I_{D(on)} is leakage from driver into "ON" switch.
5. OFF Isolation = 20 log $\frac{V_S}{V_D}$, V_S = input to OFF switch, V_D = output.

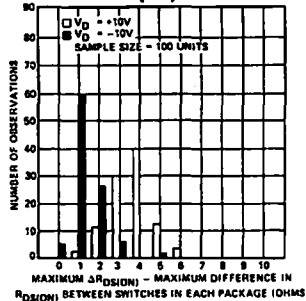
TYPICAL CHARACTERISTICS

The electrical characteristic table guarantees the DG211 and DG212 for operation at ± 15 V, $\pm 10\%$; however, functional operation occurs over the designed range of ± 5 V to ± 20 V power supplies. These characteristic graphs show the effect of device parameters over several parameter permutations including power supply variations. These graphs are for design aid only and are not subject to production testing.

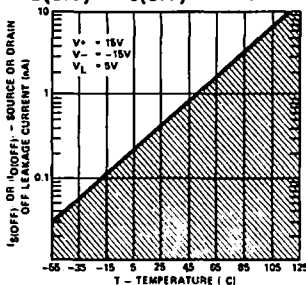
**$r_{DS(ON)}$ vs V_D
Temperature**



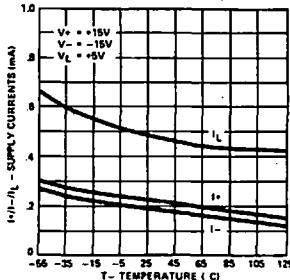
**Maximum Channel To Channel
Variation Of $r_{DS(ON)}$ In Each Device**



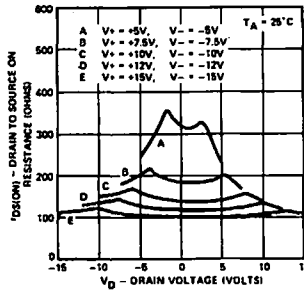
$I_D(OFF)$ Or $I_S(OFF)$ vs Temperature*



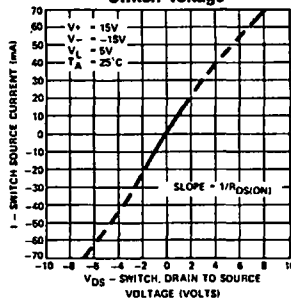
Supply Current vs Temperature



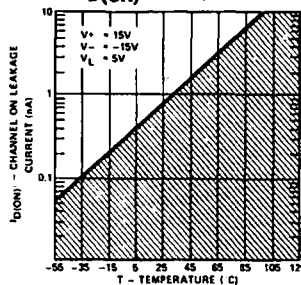
**$r_{DS(ON)}$ vs V_D and
Power Supply Voltage**



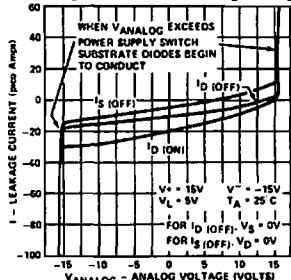
**Switch Current vs
Switch Voltage**



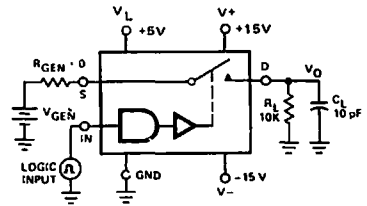
$I_D(ON)$ vs Temperature*



Leakage Current vs Analog Voltage

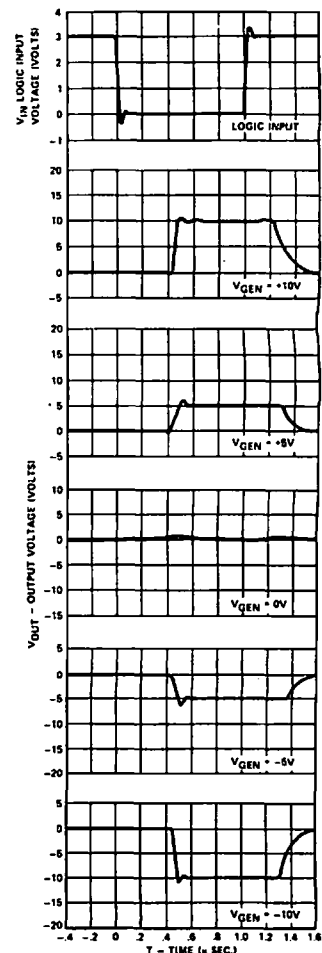


Typical delay, rise, fall, settling times, and switching transients in this circuit.



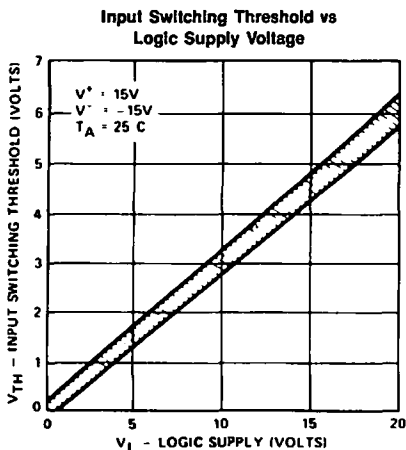
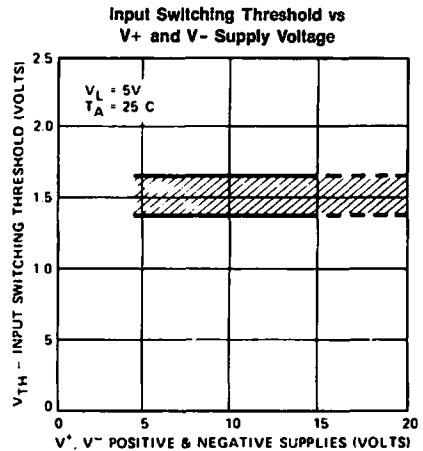
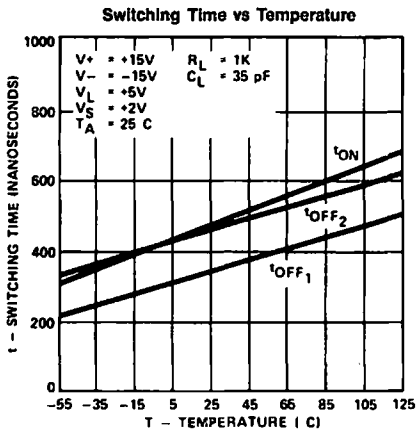
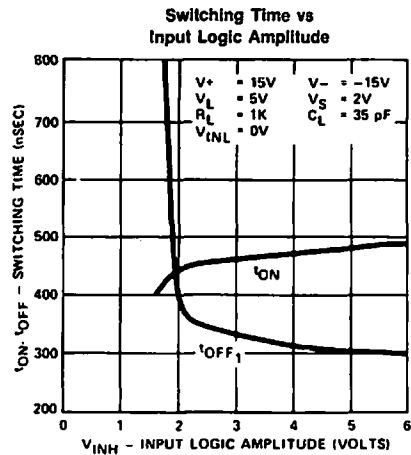
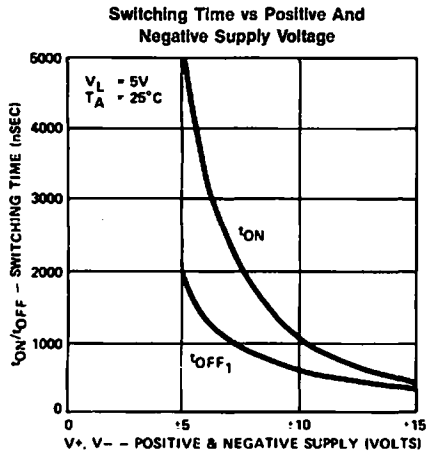
If R_{GEN} , R_L or C_L is increased, in there will be proportional increases rise and/or fall RC times. Applying V_{GEN} to D rather than S results in much greater t_{ON} spikes.

DG211 Shown



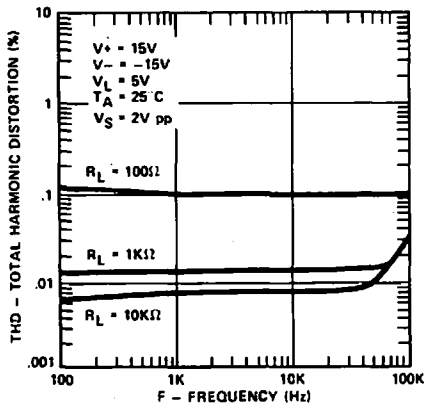
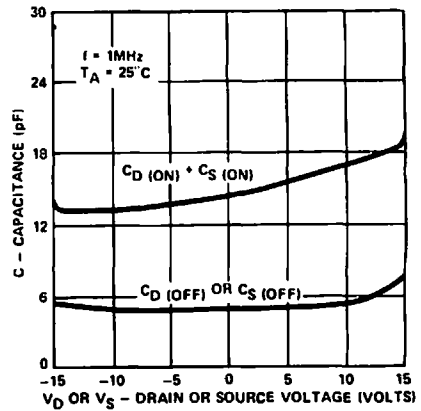
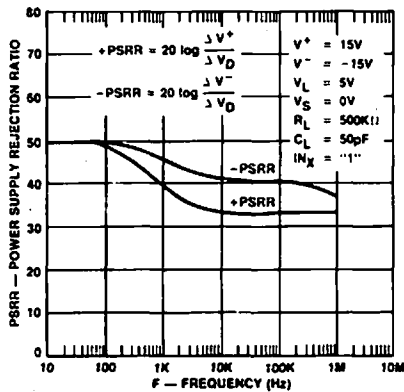
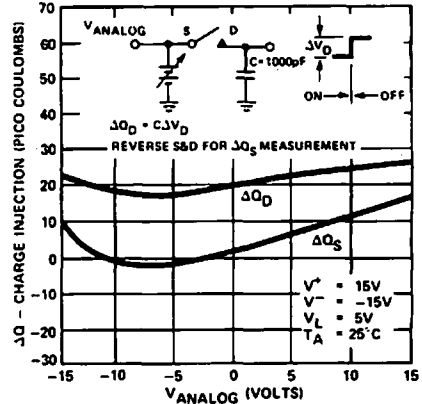
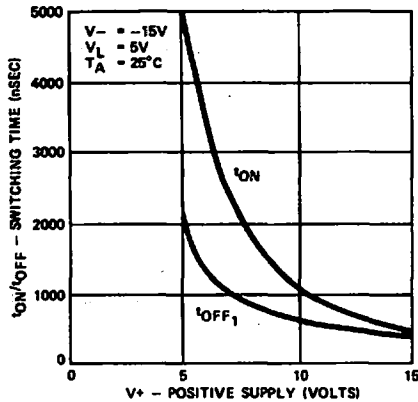
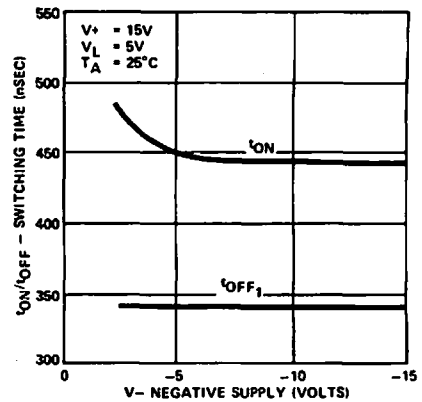
NOTE: Turn-off time is primarily limited here by the RC time constant (50ns) of the load.

* The net leakage into the source or drain is the n-channel leakage minus the p-channel leakage. This difference can be positive, negative, or zero depending on the analog voltage and temperature, and will vary greatly from unit to unit.

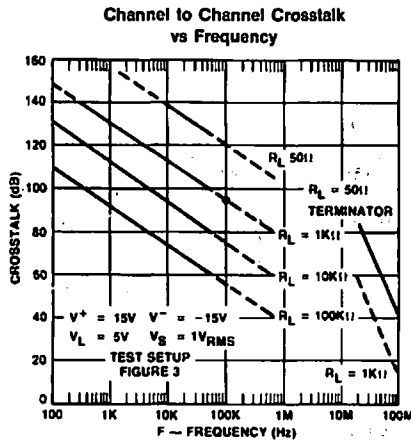
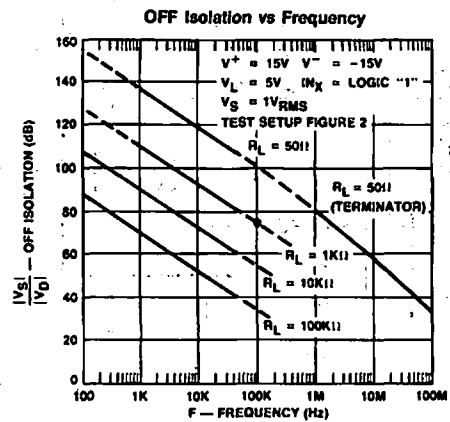
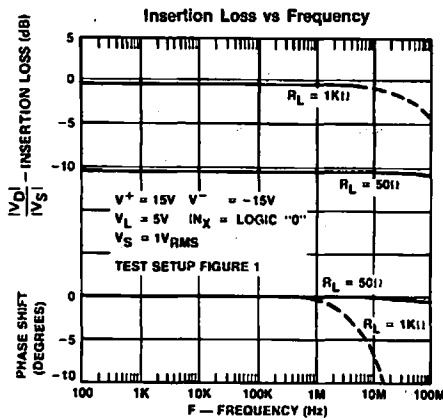
TYPICAL CHARACTERISTICS (Cont.)


Some applications of the DG211 or DG212 will find the logic control inputs (IN_x) driven from the output of comparators or op-amps with nearly plus to minus 15 volt transitions. In these applications the user can shift the input logic transition voltage from the normal 1.6 V of TTL to zero volts by connecting the V_L pin to the GND pin. In this mode of operation the input offset voltage between IN_x and V_L (= GND) measure less than ± 500 mV.

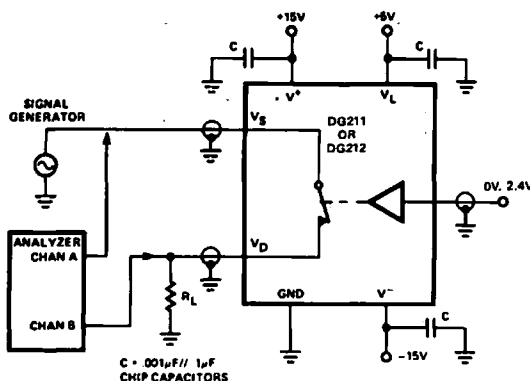
$V_L = 5$ V presets the input threshold voltage for TTL logic compatibility. Improved noise immunity for CMOS logic compatibility results by connecting V_L to the V_{DD} terminal of the CMOS logic.

TYPICAL CHARACTERISTICS (Cont.)
**Total Harmonic Distortion
vs Frequency**

Capacitance vs V_D or V_S

**Power Supply Rejection
vs Frequency**

**Charge Injection
vs Analog Voltage**

**Switching Time vs
Positive Supply Voltage**

**Switching Time vs
Negative Supply Voltage**


TYPICAL CHARACTERISTICS (Cont.)



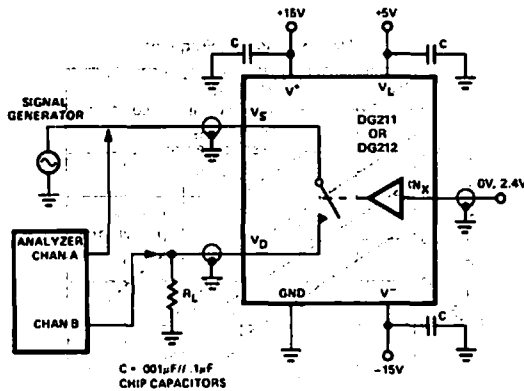
The data plotted in the frequency response graphs are measured in a special coax. The fixture eliminates stray capacitance normally encountered in printed circuit (PC) board layouts and sockets. The OFF isolation versus frequency degrades from the values shown with careless PC board layout. The best layout techniques include good ground planes, guardtraces between signal paths and bypassed power supplies



Testing Insertion Loss vs Frequency
Figure 1

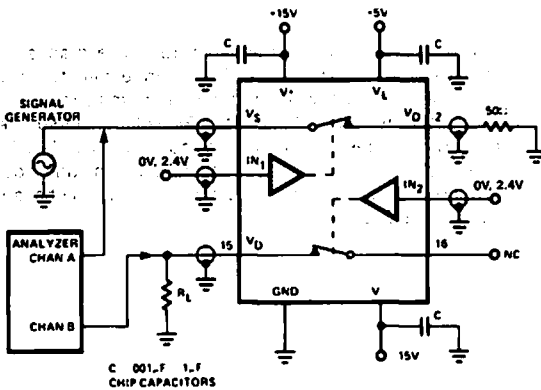
FREQUENCY TESTED	SIGNAL GENERATOR	ANALYZER
100 to 1MHz	WAVETEK MOD 142	HP3575A GAIN-PHASE METER
1M TO 100MHz	TEKTRONIX MOD 191	HP8405A VECTOR VOLT METER

TYPICAL CHARACTERISTICS (Cont.)



Testing OFF Isolation vs Frequency
Figure 2

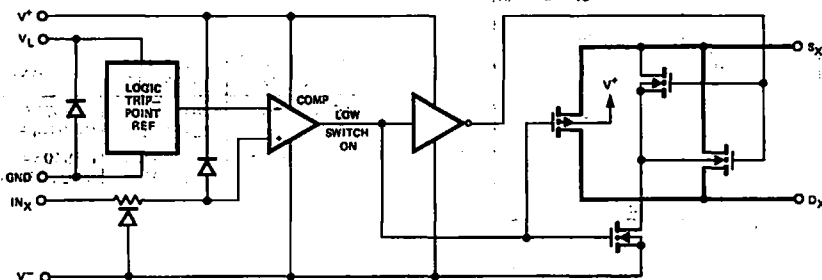
FREQUENCY TESTED	SIGNAL GENERATOR	ANALYZER
100 TO 50KHz	HP3580A TRACKING OSC	HP3580A SPECTRUM ANALYZER
1M TO 100MHz	TEKTRONIX MOD 191	HP8405A VECTOR VOLT METER
100K TO 10MHz	HP8568A TRACKING OSC	HP8568A SPECTRUM ANALYZER



Testing Crosstalk vs Frequency
Figure 3

FREQUENCY TESTED	SIGNAL GENERATOR	ANALYZER
100 TO 50KHz	HP3580A TRACKING OSC	HP3580A SPECTRUM ANALYZER
1M TO 100MHz	TEKTRONIX MOD 191	HP8405A VECTOR VOLT METER
100K TO 10MHz	HP8568A TRACKING OSC	HP8568A SPECTRUM ANALYZER

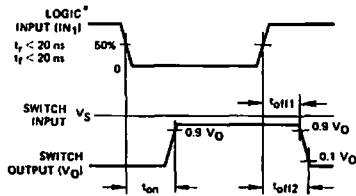
SCHEMATIC DIAGRAM (Typical Channel)



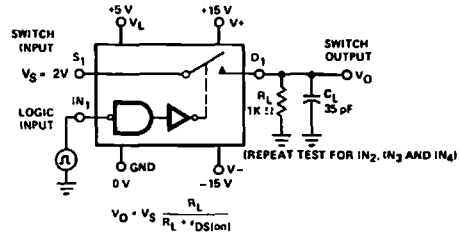
SWITCHING TIME TEST CIRCUIT

Switch output waveform shown for $V_S = \text{constant}$ with logic input waveform as shown. Note the V_S may be + or - as per switching time test circuit. V_O is the steady state

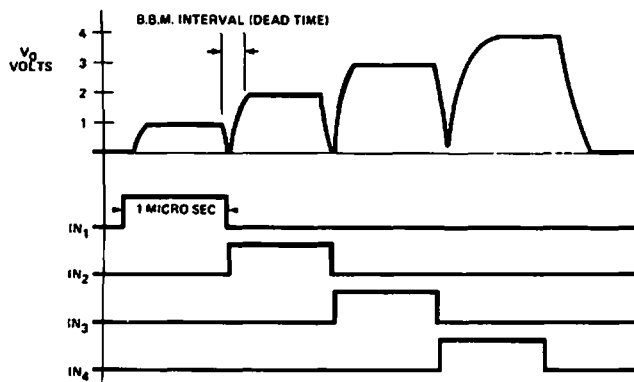
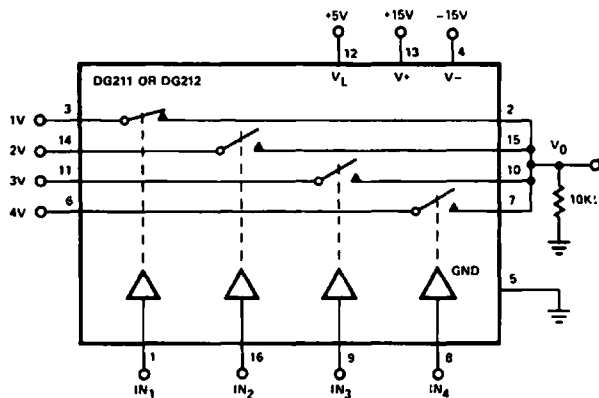
output with switch on. Feedthrough via gate capacitance may result in spikes at leading and trailing edge of output waveform.



*Logic Shown for DG211. Invert for DG212.



APPLICATIONS



Four Channel Analog Multiplexer
Figure 4



DG211 Application Hints*

V+ Positive Supply Voltage (V)	V- Negative Supply Voltage (V)	V _L Logic Supply Voltage (V)	V _{IN} Logic Input Voltage V _{INH} Min/ V _{INL} Max (V)	V _S or V _D Analog Voltage Range (V)
+15**	-15	5	2.4/0.8	-15 to +15
+12	-12	5	2.4/0.8	-12 to +12
+10	-10	5	2.4/0.8	-10 to +10
+8***	-8	5	2.4/0.8	-8 to +8

DG212 Application Hints*

V+ Positive Supply Voltage (V)	V- Negative Supply Voltage (V)	V _L Logic Supply Voltage (V)	V _{IN} Logic Input Voltage V _{INH} Min/ V _{INL} Max (V)	V _S or V _D Analog Voltage Range (V)
+20**	-20	5	2.4/0.8	-20 to +20
+15**	-15	5	2.4/0.8	-15 to +15
+12	-12	5	2.4/0.8	-12 to +12
+10	-10	5	2.4/0.8	-10 to +10
+8***	-8	5	2.4/0.8	-8 to +8
+10	-10	+10	5/2	-10 to +10

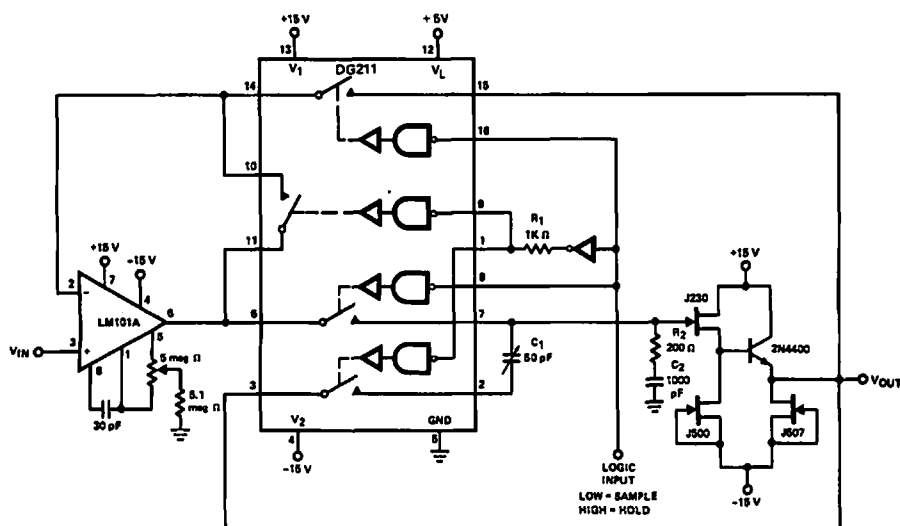
*Application Hints are for DESIGN AID ONLY, not guaranteed and not subject to production testing.

**Electrical Characteristics chart based on V+ = +15 V, V- = -15 V, V_{REF} = Open.

***Operation below ±8 V is not recommended.

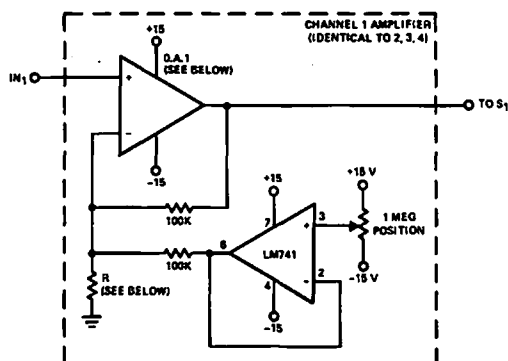
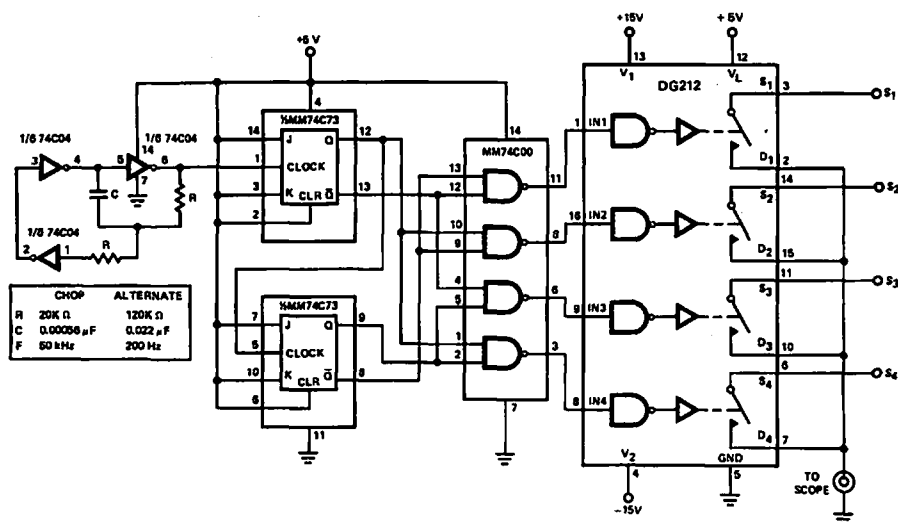
DG211/DG212

LOGIC INPUT	SWITCH STATE	LOGIC VOLT LEVEL
0	ON	≤0.8 V
1	OFF	≥2.4 V



DG211 Sample-and-Hold
Figure 7

APPLICATIONS (Cont.)



O.A.1 IS OP AMP WITH SUITABLE BANDWIDTH, SLEW RATE, ETC., FOR DESIRED SIGNALS
R IS ADDED FOR EXTRA GAIN ACCORDING TO FORMULA VOLTAGE GAIN = $2 + \frac{100K}{R}$

The "Scope Extender" Which Displays 4 Channels Simultaneously
On A Single Trace Scope
Figure 8

DG221

4-Channel Monolithic SPST CMOS Analog Switch with Data Latches



FEATURES

- Accepts 230 nS Write Pulse Width
- On Chip Regulator
- Built on PLUS 40 Process
- Latches are Transparent with WR Low

BENEFITS

- Compatible with Most μ P Bus
- Allows Wide Power Supply Tolerance without affecting TTL Compatibility
- Reduced Power Supply Considerations
- Allows Flexibility of Design

APPLICATIONS

- μ P Based Systems
- Automatic Test Equipment
- Communication Systems
- Data Acquisition Systems

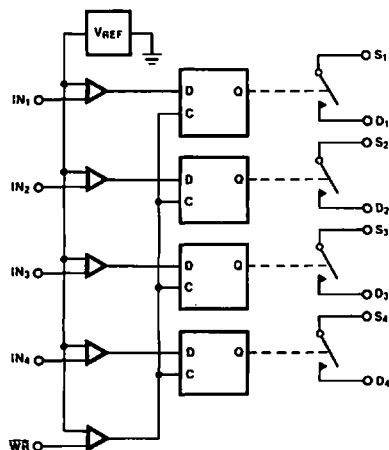
DESCRIPTION

The DG221 is a monolithic 4-channel single-pole, single-throw analog switch designed for precision switching applications in communication, instrumentation and process control systems. Featuring independent on-board latches and a common WR pin, each DG221 can be memory mapped, and addressed as a single data byte for simultaneous switching.

Designed on the Siliconix proprietary PLUS-40 CMOS

process to combine low power dissipation with a high breakdown voltage rating of 40 V, DG221 features true bidirectional switch operation over its rated analog signal range of ± 15 , a low ON resistance of 60 Ω (typ), and handling of continuous loads up to 20 mA. Options include 16-pin dual-in-line ceramic and plastic DIP packages and the three standard operating temperature ranges of 0 to 70°C, -25 to 85°C, and -55 to 125°C.

FUNCTIONAL BLOCK DIAGRAM



Four Latchable SPST Switches Per Package*

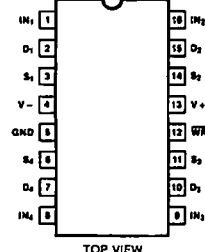
*Switches Shown for Logic "1" Input

Truth Table		
IN _x	WR	SWITCH
0	0	ON
1	0	OFF
X	1	Maintains Previous State

Logic "0" ≤ 0.8 V
 Logic "1" ≥ 2.4 V
 WR input is level sensitive
 (not edge-triggered)

PIN CONFIGURATION

Dual-In-Line Package



Order Numbers:

DG221AK, DG221BK, or DG221CK
 See Package 10
 DG221CJ
 See Package 8

ABSOLUTE MAXIMUM RATINGS

Voltages referenced to V-

V+ 44 V

GND 25 V

 Digital Inputs $\overline{WR}$, V_S , V_D^1 -2 V to ($V^+ + 2$ V) or 20 mA, whichever occurs first

Current, Any Terminal Except S or D 30 mA

Continuous Current, S or D 20 mA

Peak Current S or D

(pulsed at 1 msec, 10% duty cycle max) 70 mA

Storage Temperature (A & B Suffix) -65 to +150°C

(C Suffix) -65 to +125°C

Operating Temperature (A Suffix) -55 to 125°C

(B Suffix) -25 to 85°C

(C Suffix) 0 to 70°C

Power Dissipation (Package)*

16 Pin DIP** 900 mW

16 Pin Plastic DIP*** 470 mW

*Device mounted with all leads soldered or welded to PC board.

**Derate 12 mW/°C above 75°C

***Derate 6.5 mW/°C above 25°C

ELECTRICAL CHARACTERISTICS²

 T_A = 25°C

	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: V+ = 15 V, V- = -15 V, VL = 5 V, GND = 0V		LIMITS						UNIT	
					A SUFFIX			B/C SUFFIX				
					MIN ³	TYP ⁴	MAX	MIN ³	TYP ⁴	MAX		
SWITCH	Minimum Analog Signal Handling Capability	VANALOG			-15		15	-15		15	V	
	Drain-Source ON Resistance ⁵	rDS(on)	Vin = 0.8 V IS = -1 mA	VD = 10 V VD = -10V		60 70	90 90		60 70	90 90	Ω	
	Source OFF Leakage Current	IS(off)	Vin = 2.4 V	VS = 14 V, VD = -14 V VS = -14 V, VD = 14 V VS = -14 V, VD = 14 V		0.01 -1	1		0.01 -5.0	5 -0.02	5	
	Drain OFF Leakage Current	ID(off)		VS = 14 V, VD = -14 V		0.01 -1.0	1		0.01 -0.02	5 -0.02	nA	
	Drain ON Leakage Current ⁶	ID(on)		Vin = 0.8 V	VD = VS = 14 V VD = VS = -14 V		0.1 -1	1		0.1 -0.15	5	
	INPUT	Input Current with Input Voltage High	IINH IWRH	Vin = 2.4 V Vin = 15 V		-1	-0.0004 0.003		1	-1	-0.0004 0.003	1
Input Current with Input Voltage Low		IINL IWRL	Vin = 0 V		-1	-0.0004			-1	-0.0004		
DYNAMIC	Charge Injection	Q	CL = 1000 pF, RGEN = 0 Ω, VGEN = 0 V			20				20		pC
	Source OFF Capacitance	CS(off)	f = 1 MHz	VS = 0, Vin = 5 V		8				8		pF
	Drain OFF Capacitance	CD(off)		VD = 0, Vin = 5 V		9				9		
	Channel ON Capacitance	CD + S (on)		VD = VS = 0, Vin = 0 V		29				29		
	OFF Isolation		Vin = 5 V			70				70		dB
	Interchannel Crosstalk Isolation		VS = 1 Vpp, f = 100 kHz, CL = 15 pF, RL = 1 kΩ			90				90		
	Turn ON Time	ton	See Switching Time Test Circuit Figure 1				550			550	ns	
	Turn OFF Time	toff					340			340		
	Turn ON Time Write	ton, WR	See Switching Time Test Circuit Figure 2				550			550		
Turn OFF Time Write	toff, WR					340			340			
SUPPLY	Positive Supply Current	I+	All Channels ON or OFF Vin = 0 or 2.4 V			0.8	1.5		0.8	1.5	mA	
	Negative Supply Current	I-				-1	-0.4		-1	-0.4		

NOTES:

1. Signals on S_x, D_x, $\overline{WR}$ or I_{Nx} exceeding V₊ or V₋ will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
2. Refer to PROCESS OPTION FLOWCHART for additional information.
3. The algebraic convention whereby the most negative value is a minimum, and the most positive is a maximum, is used in this data sheet.
4. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
5. Δr_{DS(on)} is guaranteed to be within ±5% switch to switch within a package (not a tested parameter).
6. I_{D(on)} is leakage from driver into "ON" switch.

ELECTRICAL CHARACTERISTICS²(Cont.)

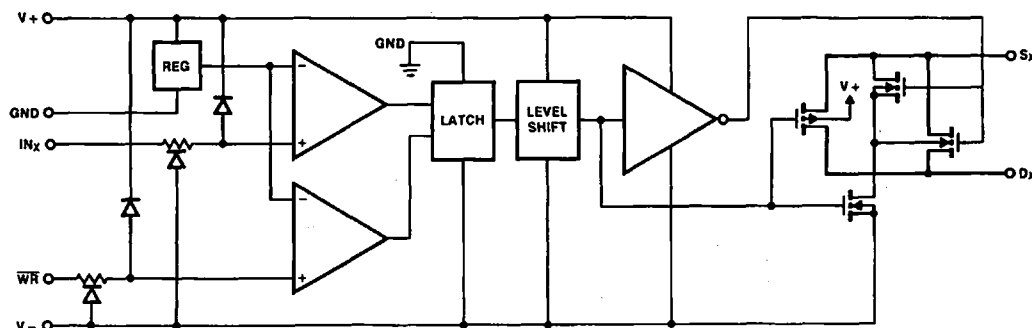
T_A = Over Temperature Range

	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: V _I = 15 V, V ₋ = -15 V, V _L = 5 V, GND = 0V	LIMITS						UNIT
				A SUFFIX			B/C SUFFIX			
				MIN ³	TYP ⁴	MAX	MIN ³	TYP ⁴	MAX	
SWITCH	Minimum Analog Signal Handling Capability	V _{ANALOG}		-15		15	-15		15	V
	Drain-Source ON Resistance ⁵	r _{DS(on)}	V _{in} = 0.8 V I _S = -1 mA			135			135	Ω
			V _D = 10 V						135	
			V _D = -10V			135			135	
	Source OFF Leakage Current	I _{S(off)}	V _{in} = 2.4 V			100			100	nA
				V _S = 14 V, V _D = -14 V						
		V _S = -14 V, V _D = 14 V		-100		-100				
	Drain OFF Leakage Current	I _{D(off)}			100			100		
			V _S = -14 V, V _D = 14 V			100			100	
			V _S = 14 V, V _D = -14 V	-100			-100			
	Drain ON Leakage Current	I _{D(on)}	V _{in} = 0.8 V			200			200	
			V _D = V _S = 14 V							
			V _D = V _S = -14 V	-200			-200			
INPUT	Input Current with Input Voltage High	I _{INH} I _{WRH}	V _{in} = 2.4 V	-10			-10			μA
			V _{in} = 15 V			10			10	
	Input Current with Input Voltage Low	I _{INL} I _{WRL}		V _{in} = 0 V	-10			-10		

NOTES:

1. Signals on S_x, D_x, WR or IN_x, exceeding V₊ or V₋ will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
2. Refer to PROCESS OPTION FLOWCHART for additional information.
3. The algebraic convention whereby the most negative value is a minimum, and the most positive is a maximum, is used in this data sheet.
4. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
5. Δr_{DS(on)} is guaranteed to be within ±5% switch to switch within a package (not a tested parameter).
6. I_{D(on)} is leakage from driver into "ON" switch.

FUNCTIONAL SCHEMATIC (Single Channel Shown)



SWITCHING TIME TEST CIRCUIT

Switch output waveform shown for V_S = constant with logic input waveform as shown. Note that V_S may be + or - as per switching time test circuit. V_O is the steady state

output with switch on. Feedthrough via gate capacitance has been minimized by design.

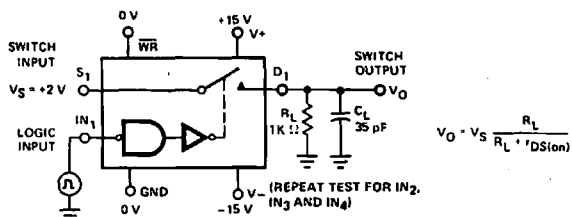
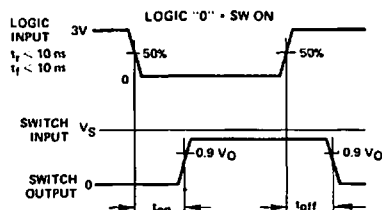


Figure 1

WR SWITCHING TIME TEST CIRCUIT

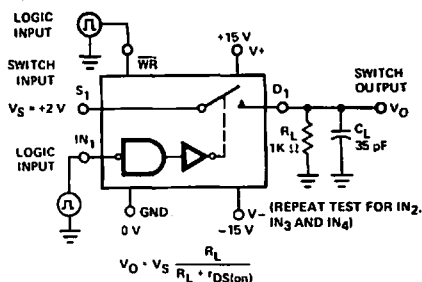
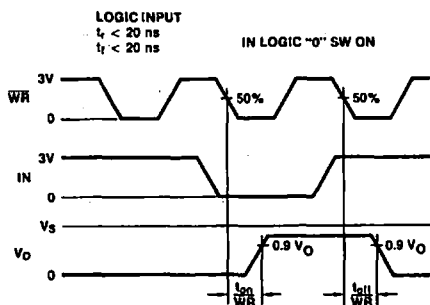
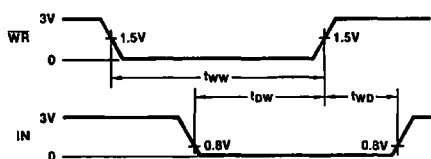


Figure 2

WR SETUP CONDITIONS

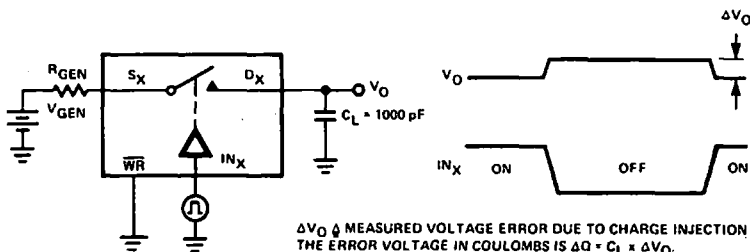


WR/INPUT MINIMUM TIMING REQUIREMENTS

PARAMETER	MIN LIMIT	UNIT
t_{WW} Write Pulse Width	230	ns
t_{DW} Data Valid to Write	180	
t_{WD} Data Valid After Write	30	

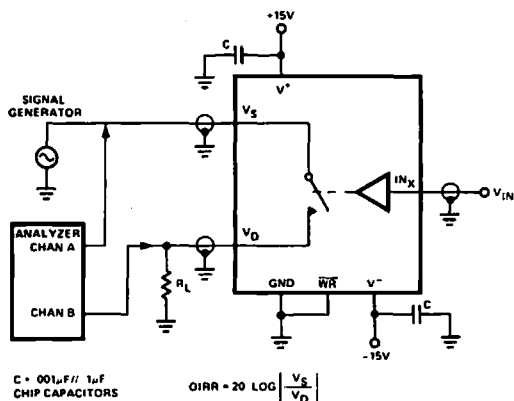
Figure 3

CHARGE INJECTION TEST CIRCUIT



ΔV_O MEASURED VOLTAGE ERROR DUE TO CHARGE INJECTION
THE ERROR VOLTAGE IN COULOMBS IS $\Delta Q = C_L \times \Delta V_O$

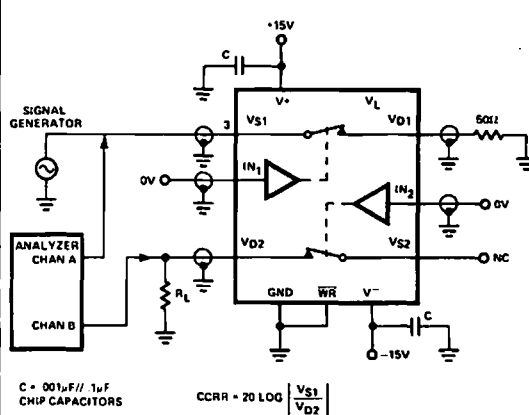
OFF ISOLATION TEST CIRCUIT



$C = 001\mu F // 1\mu F$
CHIP CAPACITORS

$OIRR = 20 \text{ LOG } \left| \frac{V_S}{V_O} \right|$

CHANNEL TO CHANNEL CROSSTALK TEST CIRCUIT



$C = 001\mu F // 1\mu F$
CHIP CAPACITORS

$CCRR = 20 \text{ LOG } \left| \frac{V_{S1}}{V_{D2}} \right|$

Application Hints

V+ Positive Power Supply	V- Negative Power Supply	GND	WR	Input	Analog Signal
+15 V	-15 V	0	0.8/2.4	0.8/2.4 V	±15 V
+20 V	-20 V	0	0.8/2.4	0.8/2.4 V	±20
+10 V	-10 V	0	0.8/2.4	0.8/2.4 V	±10 V
+10 V	-5 V	0	0.8/2.4	0.8/2.4 V	±10/-5 V

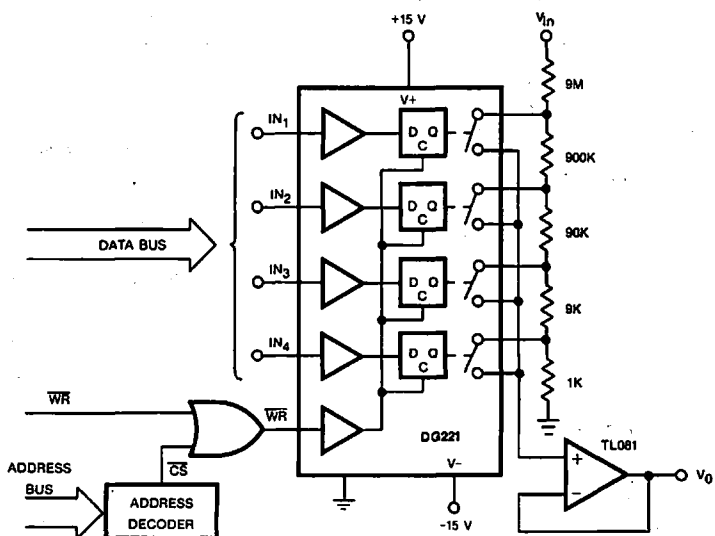
Truth Table

IN ₁	IN ₂	IN ₃	IN ₄	WR*	Switch
0	0	0	0	0	None
1	1	1	1	0	All
1	0	0	0	0	1
0	1	0	0	0	2
0	0	1	0	0	3
0	0	0	1	0	4
1*	0	0	0	0*	1*

Truth Table

WR	IN ₁	IN ₂	IN ₃	IN ₄	Gain
0	1	0	0	0	.1
0	0	1	0	0	.01
0	0	0	1	0	.001
0	0	0	0	1	.0001

*WR may be held at "0" for switch operation in accord with DG201A. With WR at "0" SW 1 will remain ON as long as "IN₁" is held at "1".



μP Controlled Analog Signal Attenuator
Figure 4

The TL081 is used as unity gain buffer while DG221 selected voltage divider provides attenuation.

DG243

Monolithic General Purpose CMOS Analog Switch



FEATURES

- PLUS-40 Process
- Make-Before-Break Operation
- Full Rail-to-Rail Analog Signal Range
- True TTL Compatibility
- Pin Compatible with Intersil IH5043, Harris HI5043, Siliconix DG5043, DG191, DG390

BENEFITS

- Reduced Power Supply Considerations
- Reduced Switching Noise
- Reduced Need for Buffers
- Pull-Up Resistors not Required
- Multiple Sourced

APPLICATIONS

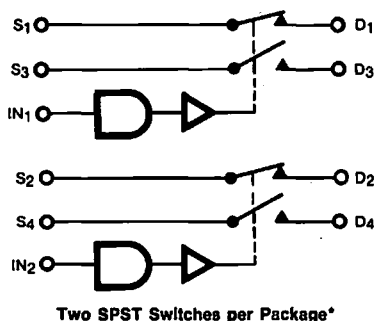
- Programmable Gain Amplifiers
- Analog Multiplexing
- Servo Control Systems

DESCRIPTION

The DG243 is a monolithic 2-channel SPDT analog switch designed for precision switching applications in communication, instrumentation, and process control systems. Featuring make-before-break action, the DG243 can be used in closed loop systems to switch gain or bandwidth determining networks without opening the loop. Designed on the Siliconix proprietary PLUS-40 CMOS process to

combine low power dissipation with a high breakdown voltage rating of 40 V, The DG243 features true bidirectional switch operation over its rated analog signal range of ± 15 V, a low ON resistance (30 ohms), and can handle continuous loads up to 30 mA. Options include 16 pin CERDIP and plastic DIP, and operating temperature ranges of 0°C to 70°C and -55°C to 125°C.

FUNCTIONAL BLOCK DIAGRAM



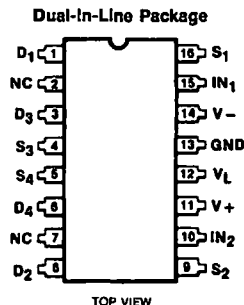
Truth Table

LOGIC	SW 1 SW 2	SW 3 SW 4
0	OFF	ON
1	ON	OFF

Logic "0" ≤ 0.8 V
Logic "1" ≥ 2.0 V

*Switches shown for Logic "1" Input

PIN CONFIGURATION



Order Number:
DG243AK or DG243CK
See Package 10
DG243CJ
See Package 8

ABSOLUTE MAXIMUM RATINGS

Voltages Referenced to V-

V+ 44 V

V_L (GND -0.3 V) to 44 V

GND 25 V

Digital Inputs¹ V_S, V_D -2 V to (V+ +2 V) or
30 mA, whichever occurs first.

Current, Any Terminal Except S or D 30 mA

Continuous Current, S or D 30 mA

Peak Current, S or D

(Pulsed at 1 msec, 10% duty cycle max) 100 mA

Storage Temperature (A Suffix) -65 to 150°C

Storage Temperature (C Suffix) -65 to 125°C

Operating Temperature (A Suffix) -55 to 125°C

(C Suffix) 0 to 70°C

Power Dissipation*

Metal Can and Plastic DIP** 450 mW

16 Pin DIP*** 900 mW

Flat Pack**** 900 mW

*All leads soldered or welded to PC board.

**Derate 6 mW/°C above 75°C

***Derate 12 mW/°C above 75°C

****Derate 10 mW/°C above 75°C

ELECTRICAL CHARACTERISTICS²T_A = 25°C

	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: V+ = 15 V, V- = -15 V, GND = 0, V _L = 5 V	LIMITS						UNIT
				DG243A			DG243C			
				MIN ³	TYP ⁴	MAX	MIN ³	TYP ⁴	MAX	
SWITCH	Analog Signal Range	V _{ANALOG}		-15		15	-15		15	V
	Drain-Source ON Resistance ⁵	r _{DS(on)}	V _D = ±10 V, I _S = 10 mA		30	50		30	50	Ω
	Source OFF Leakage Current ⁵	I _{S(off)}	V _S = 14 V, V _D = -14 V		0.2	1.0		0.2	1.0	nA
	Leakage Current ⁵		V _S = -14 V, V _D = 14 V	-1.0	-0.3		-1.0	-0.3		
	Drain OFF Leakage Current ⁵	I _{D(off)}	V _S = -14 V, V _D = 14 V		0.17	1.0		0.17	1.0	
			V _S = 14 V, V _D = -14 V	-1.0	-0.35		-1.0	-0.35		
Drain ON Leakage Current ⁵	I _{D(on)}	V _S = V _D = 14 V		0.05	2.0		0.05	2.0		
		V _S = V _D = -14 V	-2.0	-0.4		-2.0	-0.4			
INPUT	Input Current With Input Voltage High ⁵	I _{INH}	V _{in} = 2.0 V	-1.0	-0.01	1.0	-1.0	-0.01	1.0	μA
	Input Current With Input Voltage Low ⁵	I _{INL}	V _{in} = 0.8 V	-1.0	-0.005	1.0	-1.0	-0.005	1.0	
DYNAMIC	Turn-ON Time	t _{on}	See Switching Time Test Circuit		250	500		250	700	ns
	Turn-OFF Time	t _{off}			390	1000		390	1200	
	Charge Injection	Q	C _L = 1000 pF, V _{GEN} = 0 V, R _{GEN} = 0 Ω		60			60		pC
	Source OFF Capacitance ⁵	C _{S(off)}	V _D = V _S = 0 V, V _{in} = 0 V, f = 1 MHz		15			15		pF
	Drain OFF Capacitance ⁵	C _{D(off)}			17			17		
	Channel ON Capacitance ⁵	C _D + S _(on)			45			45		
	OFF Isolation ⁵		V _{in} = 5 V, Z _L = 75 Ω		75			75		dB
	Crosstalk (Channel To Channel) ⁵		V _S = 2.0 V, f = 1 MHz		89			89		
SUPPLY	Positive Supply Current	I+	All Channels ON or OFF		180	300		180	300	μA
	Negative Supply Current	I-		-300	-150		-300	-150		
	Logic Supply Current	I _L			100	300		100	300	
	Ground Supply Current	I _{GND}		-300	-140		-300	-140		

NOTES:

1. Signals on S_X, D_X, or I_{NX}, exceeding V+ or V- will be clamped by internal diodes. Limit forward current to maximum current ratings.

2. Refer to PROCESS OPTION FLOWCHART for additional information.

3. The algebraic convention whereby the most negative value is a minimum, and the most positive value is a maximum, is used in this data sheet.

4. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

5. V_{in} = Input voltage to perform the proper function.For Logic "1" - V_{INH} = 2.0 VFor Logic "0" - V_{INL} = 0.8 V

ELECTRICAL CHARACTERISTICS (Cont.)²
 T_A = Over Temperature Range

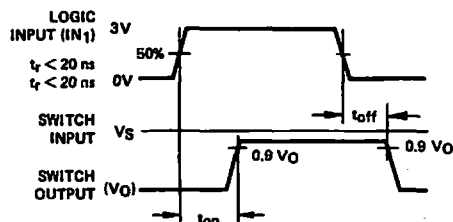
	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: V+ = 15 V, V- = -15 V, GND = 0, V _L = 5 V	LIMITS						UNIT
				DG243A			DG243C			
				MIN ³	TYP ⁴	MAX	MIN ³	TYP ⁴	MAX	
SWITCH	Analog Signal Range	V _{ANALOG}		-15		15	-15		15	V
	Drain-Source ON Resistance ⁵	r _{DS(on)}	V _D = ±10 V, I _S = 10 mA			75			75	Ω
	Source OFF Leakage Current ⁵	I _{S(off)}	V _S = 14 V, V _D = -14 V			100			100	nA
			V _S = -14 V, V _D = 14 V	-100			-100			
	Drain OFF Leakage Current ⁵	I _{D(off)}	V _S = -14 V, V _D = 14 V			100			100	
			V _S = 14 V, V _D = -14 V	-100			-100			
Drain ON Leakage Current ⁵	I _{D(on)}	V _S = V _D = 14 V			200			200		
		V _S = V _D = -14 V	-200			-200				
INPUT	Input Current With Input Voltage High ⁵	I _{INH}	V _{INH} = 2.0 V	-1.0		1.0	-1.0		1.0	μA
	Input Current With Input Voltage Low ⁵	I _{INL}	V _{INL} = 0.8 V	-1.0		1.0	-1.0		1.0	

NOTES:

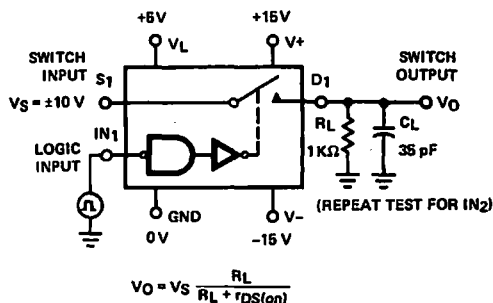
1. Signals on S_X , D_X , or IN_X , exceeding V_+ or V_- will be clamped by internal diodes. Limit forward current to maximum current ratings.
2. Refer to PROCESS OPTION FLOWCHART for additional information.
3. The algebraic convention whereby the most negative value is a minimum, and the most positive value is a maximum, is used in this data sheet.
4. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
5. V_{IN} = Input voltage to perform the proper function.
For Logic "1" - $V_{INH} = 2.0\text{ V}$
For Logic "0" - $V_{INL} = 0.8\text{ V}$

SWITCHING TIME TEST CIRCUIT

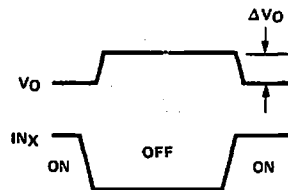
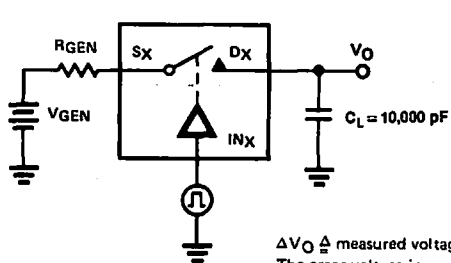
Switch output waveform shown for $V_S = \text{constant}$ with logic input waveform as shown. Note that V_S may be + or - as per switching time test circuit. V_O is the steady state output with switch on. Feedthrough via gate capacitance may result in spikes at leading and trailing edge of output waveform.



Note: Logic input waveform is inverted for switches that have the opposite logic sense control.

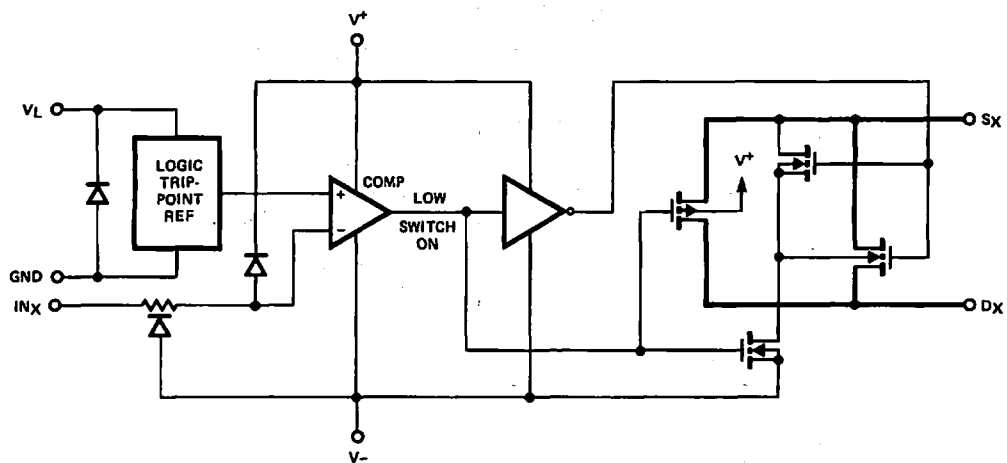


CHARGE INJECTION TEST CIRCUIT



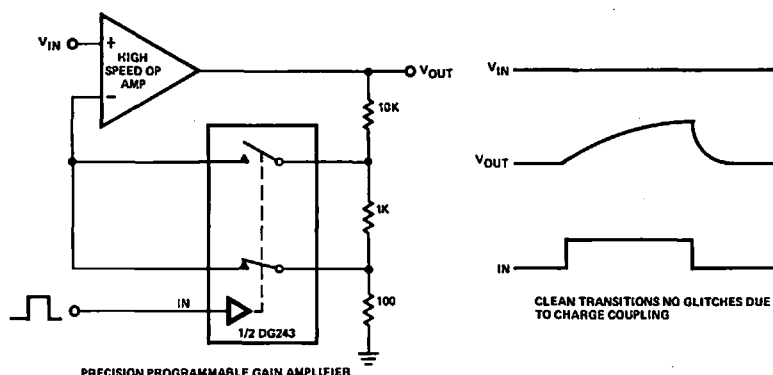
$\Delta V_O \triangleq$ measured voltage error due to charge injection.
The error voltage in coulombs is $\Delta Q = C_L \times \Delta V_O$.

SCHEMATIC DIAGRAM (Typical Channel)



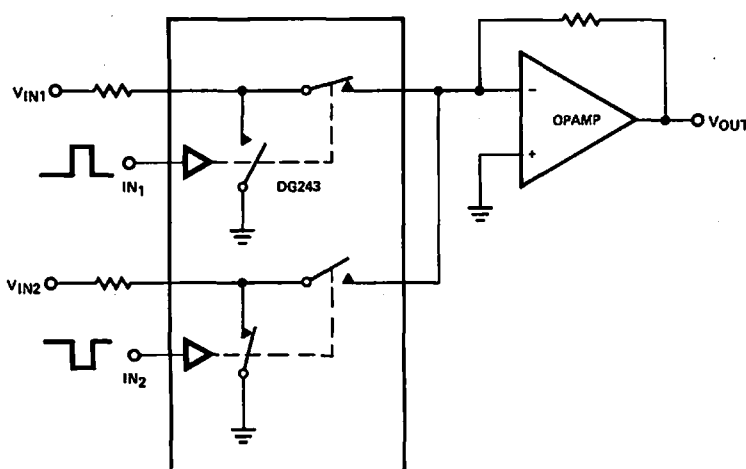
APPLICATIONS

The Make-Before-Break operation of the DG243 provides simple transient suppression in these two important applications.



Improving Transient Response in Programmable Gain Amplifiers. "Getting Rid of Glitches".
Figure 1

Figure 1 shows a minimum amount of glitching during changes of gain states. The relatively low impedance of the gain setting resistors 10K, 1K, 100Ω shunt the injected charge to ground minimizing transient effects occurring at the inverting input of the op amp. Consequently, these transients are not amplified to V_{OUT}.



Minimizing Glitches in Audio Switching
Figure 2

Figure 2 takes advantage of the Make-Before-Break operation of the DG243 by shorting transition current to real ground instead of virtual ground. The proper offset voltage specification for op amp selection gives the best results.

The circuit outperforms its Break-Before-Make cousin, the DG5043 in this application.



DG271

High Speed Quad Monolithic SPST CMOS Analog Switch

FEATURES

- Fast Switching Times <75 ns
- Power Dissipation <157 mW
- Charge Injection <9.0 pC
- $r_{DS(on)} < 50 \Omega$
- TTL Compatible

BENEFITS

- Faster System Operation
- Reduced Power Supply Requirements
- Reduced System Error
- Pull-up Resistors not Required

APPLICATIONS

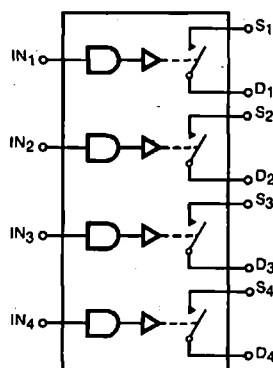
- High Speed Switching
- Sample/Hold
- Digital Filters
- Op Amp Gain Switching
- Winchester Disk Drives

DESCRIPTION

The DG271 Quad SPST analog switch offers normally open, high speed break-before-make switching for applications where low ON resistance (32 Ω typ), wide signal range (± 15 V), and low charge-transfer are required. In the OFF state, the switch will block up to 30 V peak-to-peak, and has a 44 V maximum power supply rating. The DG271 will conduct current in either direction with no offset in

the ON state. ON resistance is nearly constant over the entire analog signal range, thus providing precision signal transfer across the switch. Internal pull-up resistors simplify interface to CMOS or TTL drive circuits. Package options are 16 pin plastic or ceramic DIP, with performance rated over the 0 to 70°C and -25 to 85°C temperature ranges.

FUNCTIONAL BLOCK DIAGRAM



Four SPST Switches per Package*

Truth Table

LOGIC	SWITCH
0	ON
1	OFF

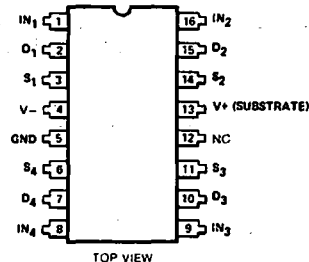
Logic "0" ≤ 0.8 V

Logic "1" ≥ 2.0 V

*Switches Shown for Logic "1" Input

PIN CONFIGURATION

Dual-In-Line Package



Order Numbers:
DG271BK or DG271CK
See Package 10

DG271CJ
See Package 8

ABSOLUTE MAXIMUM RATINGS

Voltages Referenced to V-

V+ 44 V

GND 25 V

 Digital Inputs¹ V_S, V_D -2 V to (V+ +2 V) or
20 mA, whichever occurs first.

Current, Any Terminal Except S or D 30 mA

Continuous Current, S or D 20 mA

Peak Current, S or D

(Pulsed at 1 msec. 10% duty cycle max) 100 mA

Storage Temperature (B Suffix) -65 to 150°C

(C Suffix) -65 to 125°C

Operating Temperature (B Suffix) -25 to 85°C

(C Suffix) 0 to 70°C

Power Dissipation (Package)*

16 Pin DIP** 900 mW

16 Pin Plastic DIP*** 470 mW

 *Device mounted with all leads soldered or welded to
PC board

**Derate 12 mW/°C above 75°C

***Derate 6.5 mW/°C above 25°C

ELECTRICAL CHARACTERISTICS²

 T_A = 25°C

	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: V+ = 15 V, V- = -15 V, GND = 0	LIMITS			UNIT
				MIN ³	TYP ⁴	MAX	
SWITCH	Analog Signal Range	V _{ANALOG}	V _D = ±10 V, I _S = 1 mA, V _{IN} = 0.8 V	-15		15	V
	Drain-Source ON Resistance	r _{DS(on)}	V _D = ±10 V, I _S = 1 mA, V _{IN} = 0.8 V		32	50	Ω
	Source OFF Leakage Current	I _{S(off)}	V _{IN} = 2.0 V	V _S = 14 V, V _D = -14 V		1	nA
				V _S = -14 V, V _D = 14 V		-1	
	Drain OFF Leakage Current	I _{D(off)}	V _{IN} = 0.8 V	V _S = -14 V, V _D = 14 V		1	
INPUT				V _S = 14 V, V _D = -14 V		-1	
	Drain ON Leakage Current ⁵	I _{D(on)}	V _{IN} = 0.8 V	V _S = V _D = 14 V		1	μA
				V _S = V _D = -14 V		-1	
	Input Current with Input Voltage High	I _{INH}	V _{IN} = 2.0 V	-1	0.22		
			V _{IN} = 15 V		0.035	1	
DYN	Input Current with Input Voltage Low	I _{INL}	V _{IN} = 0 V	-1	0.010		ns
	Turn-ON Time	t _{on}	See Switching Time Test Circuit		53.0	75	
	Turn-OFF Time	t _{off}			50.6	75	
	Charge Injection ⁶	Q	C _L = 1000pF, V _{gen} = 0 V, R _{gen} = 0 Ω		9.0		pC
SUPPLY	Positive Supply Current	I+	All Channels "ON" or "OFF" V _{IN} = 0 or 2 V		4.3	6.0	mA
	Negative Supply Current	I-		-4.5	-3.4		

 T_A = Over Temperature Range

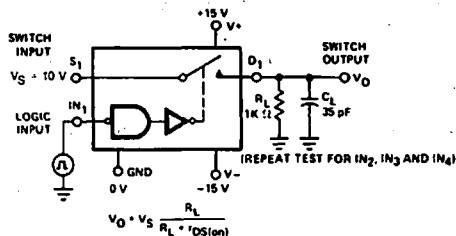
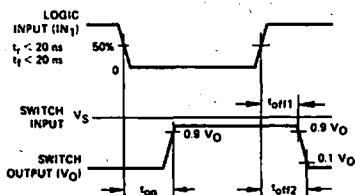
	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: V+ = 15 V, V- = -15 V, GND = 0	LIMITS			UNIT
				MIN ³	TYP ⁴	MAX	
SWITCH	Analog Signal Range	V _{ANALOG}	V _D = ±10 V, I _S = 1 mA, V _{IN} = 0.8 V	-15		15	V
	Drain-Source ON Resistance	r _{DS(on)}	V _D = ±10 V, I _S = 1 mA, V _{IN} = 0.8 V			75	Ω
	Source OFF Leakage Current	I _{S(off)}	V _{IN} = 2.0 V	V _S = 14 V, V _D = -14 V		100	nA
				V _S = -14 V, V _D = 14 V		-100	
	Drain OFF Leakage Current	I _{D(off)}	V _{IN} = 0.8 V	V _S = -14 V, V _D = 14 V		100	
INPUT				V _S = 14 V, V _D = -14 V		-100	
	Drain ON Leakage Current ⁵	I _{D(on)}	V _{IN} = 0.8 V	V _S = V _D = 14 V		200	μA
				V _S = V _D = -14 V		-200	
	Input Current with Input Voltage High	I _{INH}	V _{IN} = 2.0 V	-10			
			V _{IN} = 15 V			10	
INPUT	Input Current with Input Voltage Low	I _{INL}	V _{IN} = 0 V	-10			

NOTES:

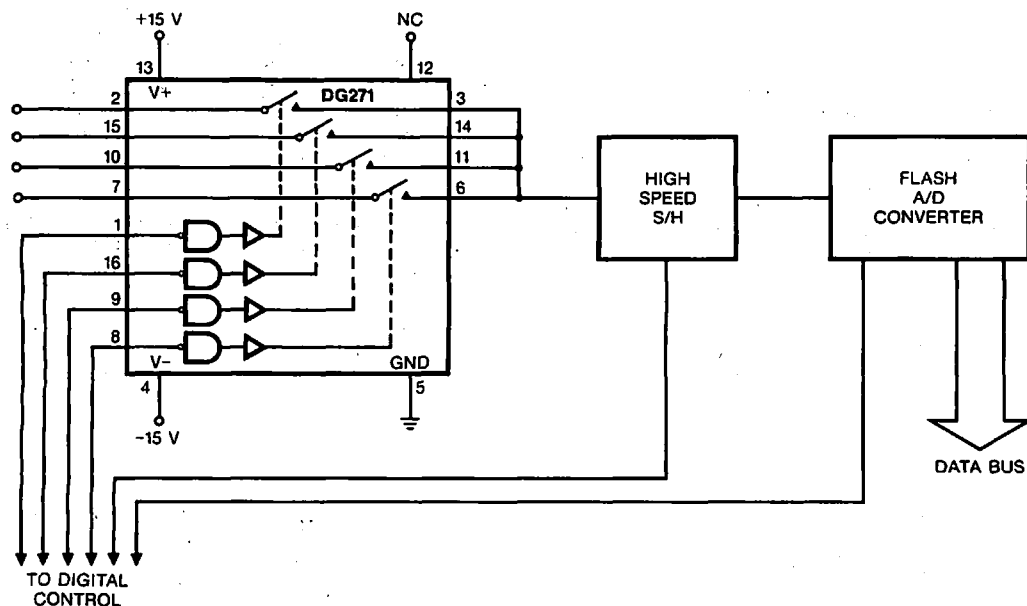
1. Signals on S_X, D_X, or I_{NX} exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
2. Refer to PROCESS OPTION FLOWCHART For additional information.
3. The algebraic convention whereby the most negative value is minimum, and the most positive is maximum is used in this data sheet.
4. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
5. I_{D(on)} is leakage from driver into "ON" switch.

SWITCHING TIME TEST CIRCUIT

Switch output waveform shown for $V_S = \text{constant}$ with logic input waveform as shown. Note that V_S may be + or - as per switching time test circuit. V_O is the steady state output with switch on. Feedthrough via gate capacitance may result in spikes at leading and trailing edge of output waveform.



TYPICAL APPLICATION



DG271 in a High Speed Data Acquisition System
Figure 1

DG300A/DG301A/ DG302A/DG303A TTL Compatible CMOS Analog Switch Family



FEATURES

- Latchproof CMOS
- Fast Switching (<250 ns)
- Low $r_{DS(ON)}$ (<50 Ω)
- Single Supply Capability

BENEFITS

- Full Rail to Rail Analog Signal Range
- Low Signal Error
- Low Power Dissipation

APPLICATIONS

- Low Level Switching Circuits
- Programmable Gain Amplifiers
- Portable Battery Operation

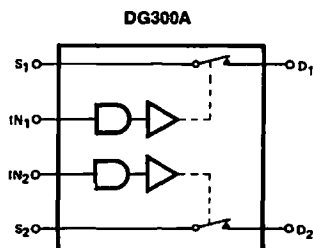
DESCRIPTION

The DG300A-DG303A family of monolithic CMOS switches feature three switch configuration options (SPST, SPDT, and DPST) for precision applications in communications, instrumentation and process control, where low leakage switching combined with low power requirements are required. Designed on the Siliconix PLUS-40 CMOS process, the switches are latch proof, and are designed to block up to 30 Volts peak-to-peak when OFF. In the ON condition the switches conduct equally well in both directions (with no offset voltage), and minimize error conditions with their almost flat ON resistance of 50 Ω , max.

Featuring low power consumption, a few milliwatts, these switches are ideal for battery powered applications, without sacrificing switching speed. Designed for break-before-make switching action, the switches are TTL and CMOS input compatible. Single supply operation (for positive switch voltages) is afforded by connecting the V- rail to 0 Volts.

The DG300A-DG303A family is offered in 14 or 16-pin plastic and ceramic DIP's, or the 10-pin metal can. Temperature options are 0 to 70°C, -25 to 85°C, and -55 to 125°C.

FUNCTIONAL BLOCK DIAGRAM



Two SPST Switches per Package*

Truth Table

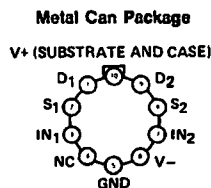
LOGIC	SWITCH
0	OFF
1	ON

Logic "0" $\leq$ 0.8 V

Logic "1" $\geq$ 4.0 V

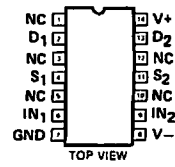
*Switches Shown for Logic "1" Input

PIN CONFIGURATION



Order Numbers:
DG300AAA or DG300ABA
See Package 2

Dual-In-Line Package

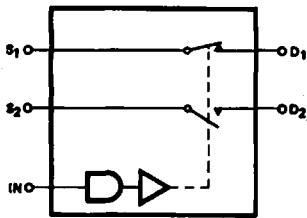


Order Numbers:
DG300AAK, DG300ABK,
DG300ACK
See Package 9
DG300ACJ
See Package 7

FUNCTIONAL BLOCK DIAGRAM

PIN CONFIGURATION

DG301A

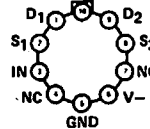


One SPDT Switch per Package*

Truth Table**

LOGIC	SW1	SW2
0	OFF	ON
1	ON	OFF

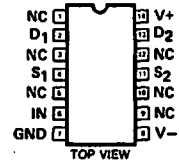
Metal Can Package
V+ (SUBSTRATE AND CASE)



TOP VIEW

Order Numbers:
DG301AAA or DG301ABA
See Package 2

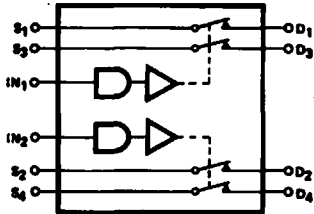
Dual-In-Line Package



TOP VIEW

Order Numbers:
DG301AAK, DG301ABK,
DG301ACK
See Package 9
DG301ACJ
See Package 7

DG302A

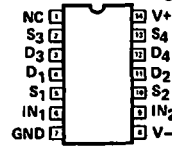


Two DPST Switches per Package*

Truth Table**

LOGIC	SWITCH
0	OFF
1	ON

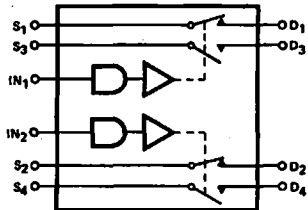
Dual-In-Line Package



TOP VIEW

Order Numbers:
DG302AAK, DG302ABK,
DG302ACK
See Package 9
DG302ACJ
See Package 7

DG303A

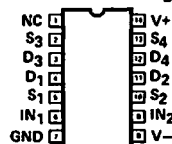


Two SPDT Switches per Package*

Truth Table**

LOGIC	SW1	SW2
0	OFF	ON
1	ON	OFF

Dual-In-Line Package



TOP VIEW

Order Numbers:
DG303AAK, DG303ABK,
DG303ACK
See Package 9
DG303ACJ
See Package 7

*Switches Shown for Logic "1" Input

**Logic "0" ≤ 0.8 V, Logic "1" ≥ 4.0 V

ABSOLUTE MAXIMUM RATINGS

Voltages Referenced to V-

V+ 44 V

GND 25 V

 Digital Inputs¹ V_S, V_D -2 V to (V⁺ +2 V) or
30 mA, whichever occurs first.

Current, Any Terminal Except S or D 30 mA

Continuous Current, S or D 30 mA

(Pulsed at 1 msec, 10% duty cycle max) 100 mA

 Storage Temperature (A & B Suffix) -65 to 150°C
(C Suffix) -65 to 125°C

Operating Temperature (A Suffix) -55 to 125°C

(B Suffix) -25 to 85°C

(C Suffix) 0 to 70°C

Power Dissipation*

Cerdip (K)** 825 mW

Plastic DIP (J)*** 470 mW

Metal Can (A)**** 450 mW

 *Device mounted with all leads soldered or welded to
PC board.

**Derate 11 mW/°C above 75°C

***Derate 6.5 mW/°C above 25°C

****Derate 6 mW/°C above 75°C

ELECTRICAL CHARACTERISTICS²

 T_A = 25°C

	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: V+ = 15 V, V- = -15 V, GND = 0 V	LIMITS						UNIT
				DG300A-DG303AA			DG300A-DG303AB/C			
				MIN ³	TYP ⁴	MAX	MIN ³	TYP ⁴	MAX	
SWITCH	Analog Signal Range	V _{ANALOG}	I _S = 10 mA, V _{IN} = 0.8 V or 4.0 V ⁵	-15		15	-15		15	V
	Drain-Source ON Resistance	r _{DS(on)}	I _S = -10 mA, V _D = 10 V I _S = 10 mA, V _D = -10 V		30	50		30	50	Ω
	Source OFF Leakage Current	I _{S(off)}	V _{IN} = 0.8 V or V _{IN} = 4.0 V ⁵ V _S = 14 V, V _D = -14 V		0.1	1		0.1	5	nA
	Drain OFF Leakage Current	I _{D(off)}	V _S = -14 V, V _D = 14 V V _S = -14 V, V _D = 14 V	-1	-0.1		-5	-0.1		
	Drain ON Leakage Current	I _{D(on)}	V _S = 14 V, V _D = -14 V V _D = V _S = 14 V	-1	-0.1	1	-5	-0.1	5	
			V _D = V _S = -14 V	-2	-0.1		-5	-0.1		
INPUT	Input Current/Voltage High	I _{INH}	V _{IN} = 5.0 V V _{IN} = 15 V	-1	-0.001		-1	-0.001		μA
					0.001	1		0.001	1	
	Input Current/Voltage Low	I _{INL}	V _{IN} = 0 V	-1	-0.001		-1	-0.001		
DYNAMIC	Turn-ON Time	t _{on}	See Switching Time Test Circuit		150	250		150		ns
	Turn-OFF Time	t _{off}			130			130		
	Break-Before-Make Interval	t _{on} t _{off}	See Break-Before-Make Time Test Circuit DG301A/DG303A Only		50			50		
	Charge Injection	O	C _L = 1 μF, R _{gen} = 0 Ω, V _{gen} = 0 V	3			3			mV
	Source OFF Capacitance	C _{S(off)}	f = 1 MHz, V _S = 0		14			14		pF
	Drain OFF Capacitance	C _{D(off)}	V _{IN} = 0.8 V or V _{IN} = 4.0 V ⁵ V _S = V _D = 0		14			14		
	Channel ON Capacitance	C _{D(on)} + C _{S(on)}			40			40		
	Input Capacitance	C _{in}	f = 1 MHz, V _{IN} = 0 V _{IN} = 15 V		6			6		
					7			7		
	Off Isolation		V _{IN} = 0, R _L = 1 kΩ V _S = 1 V _{RMS} , f = 500 kHz		62			62		dB
Crosstalk (Channel to Channel)				74			74			
SUPPLY	Positive Supply Current	I ⁺	V _{IN} = 4 V (One Input) (All Others = 0)		0.23	0.5		0.23	0.5	mA
	Negative Supply Current	I ⁻		-10	-0.001		-10	-0.001		μA
	Positive Supply Current	I ⁺	V _{IN} = 0.8 V (All Inputs)		0.001	10		0.001	10	
	Negative Supply Current	I ⁻		-10	-0.001		-10	-0.001		

NOTES:

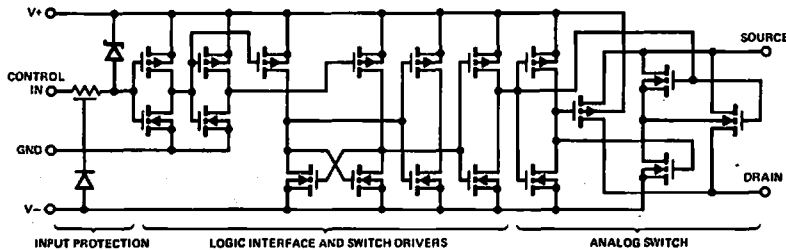
1. Signals on S_X, D_X, or I_{NX} exceeding V⁻ or V⁺ will be clamped by internal diodes. Limit diode forward current to maximum current ratings.
2. Refer to PROCESS OPTION FLOWCHART for additional information.
3. The algebraic convention whereby the most negative value is a minimum, and the most positive value is a maximum is used in this data sheet.
4. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
5. OFF isolation = 20 log $\frac{V_S}{V_D}$, V_S = input to OFF switch, V_D = Output.

ELECTRICAL CHARACTERISTICS² (Cont.)
 T_A = Over Temperature Range

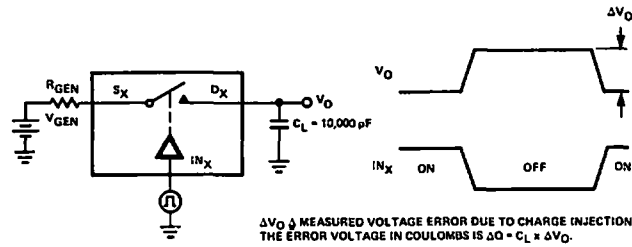
	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: V+ = 15 V, V- = -15 V, GND = 0 V	LIMITS						UNIT
				DG300A-DG303AA			DG300A-DG303AB/C			
				MIN ³	TYP ⁴	MAX	MIN ³	TYP ⁴	MAX	
SWITCH	Analog Signal Range	V _{ANALOG}	I _S = 10 mA, V _{in} = 0.8 V or 4.0 V ⁵	-15		15	-15		15	V
	Drain-Source ON Resistance	r _{DS(on)}	V _{in} = 0.8 V or V _{in} = 4.0 V ⁵	I _S = -10 mA, V _D = 10 V			75		75	Ω
		I _S = 10 mA, V _D = -10 V				75		75		
	Source OFF Leakage Current	I _{S(off)}		V _S = 14 V, V _D = -14 V			100		100	
		V _S = -14 V, V _D = 14 V		-100			-100			
	Drain OFF Leakage Current	I _{D(off)}		V _S = -14 V, V _D = 14 V			100		100	nA
		V _S = 14 V, V _D = -14 V		-100			-100			
Drain ON Leakage Current	I _{D(on)}	V _D = V _S = 14 V			100			100		
		V _D = V _S = -14 V	-200			-200				
INPUT	Input Current/Voltage High	I _{INH}	V _{in} = 5.0 V	-1						μA
			V _{in} = 15 V			1				
	Input Current/Voltage Low	I _{INL}	V _{in} = 0 V	-1						
SUPPLY	Positive Supply Current	I ₊	V _{in} = 4 V (One Input) (All Others = 0)			1				mA
	Negative Supply Current	I ₋		-100						
	Positive Supply Current	I ₊	V _{in} = 0.8 V (All Inputs)			100				μA
	Negative Supply Current	I ₋		-100						

NOTES:

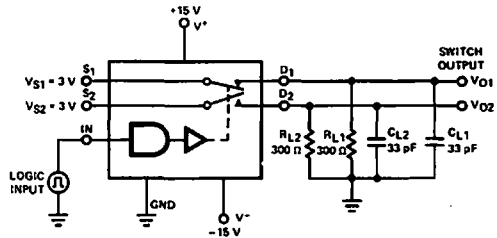
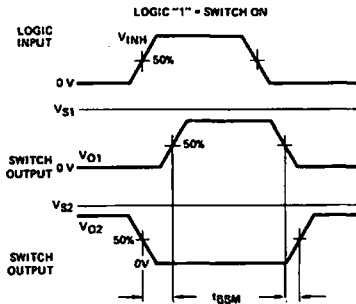
1. Signals on S_X , D_X , or IN_X exceeding V_+ or V_- will be clamped by internal diodes. Limit diode forward current to maximum current ratings.
2. Refer to PROCESS OPTION FLOWCHART for additional information.
3. The algebraic convention whereby the most negative value is a minimum, and the most positive value is a maximum is used in this data sheet.
4. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
5. OFF isolation = $20 \log \frac{V_S}{V_D}$, = input to OFF switch, V_D = Output.

SCHEMATIC DIAGRAM (Typical Channel)


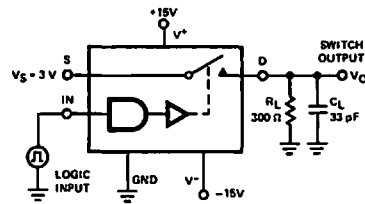
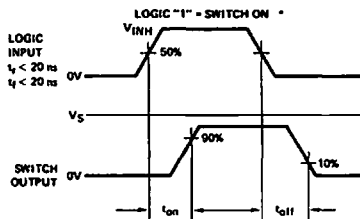
TEST CIRCUITS



Charge Injection Test Circuit



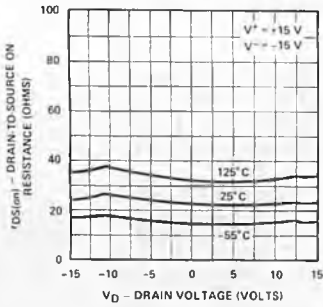
Break-Before-Make Time Test Circuit SPDT (DG301A, DG303A)



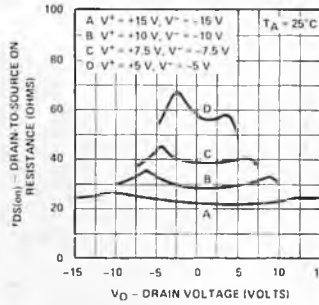
Switching Time Test Circuit

TYPICAL CHARACTERISTICS

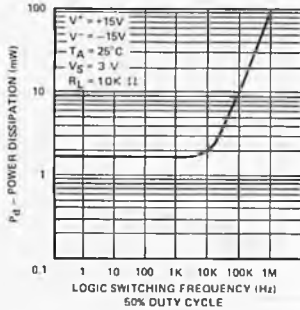
$r_{DS(on)}$ vs V_D and Temperature



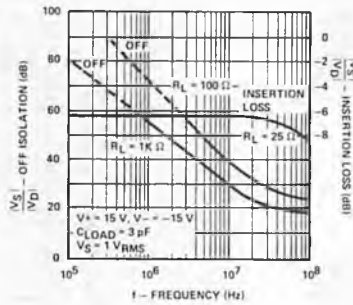
$r_{DS(on)}$ vs V_D and Power Supply Voltage



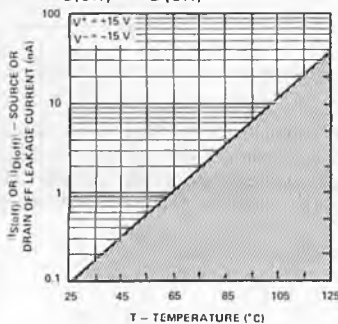
Device Power Dissipation vs Switching Frequency
Single Logic Input



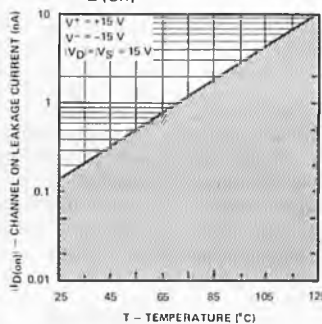
OFF Isolation Insertion Loss vs Frequency



$I_S(off)$ or $I_D(off)$ vs Temperature*

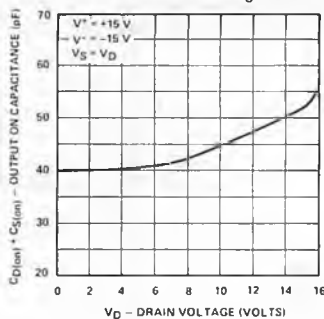


$I_D(on)$ vs Temperature*

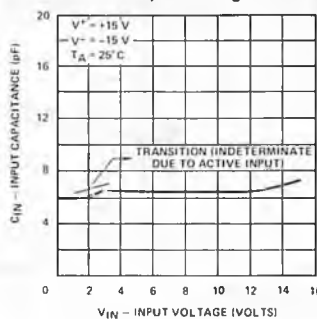


*The net leakage into the source or drain is the n-channel leakage minus the p-channel leakage. This difference can be positive, negative, or zero depending on the analog voltage and temperature, and will vary greatly from unit to unit.

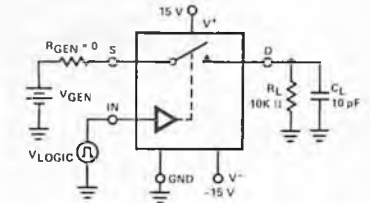
Output ON Capacitance vs Drain Voltage



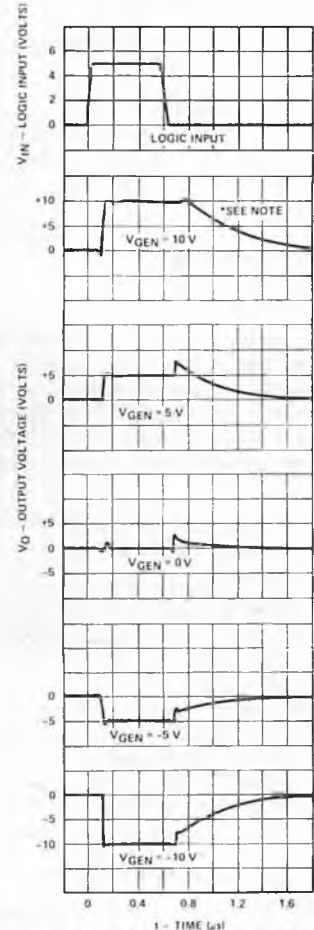
Input Capacitance vs Input Voltage



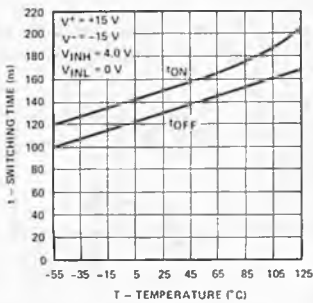
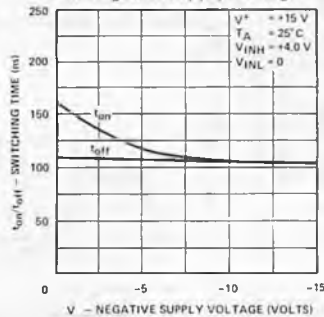
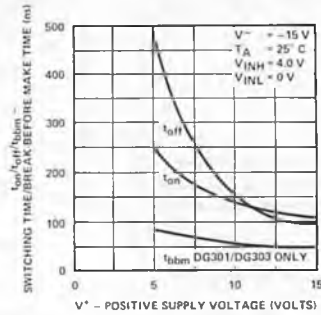
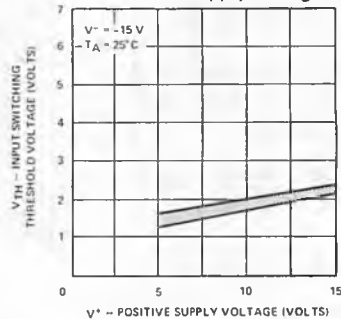
Typical delay, rise, fall, settling times, and switching transients in this circuit.



If R_{GEN} , R_L or C_L is increased, there will be proportional increases in rise and/or fall RC times. Applying V_{GEN} to D rather than S results in much greater spikes.

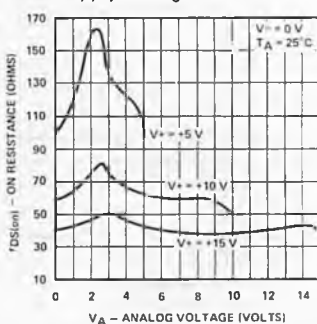
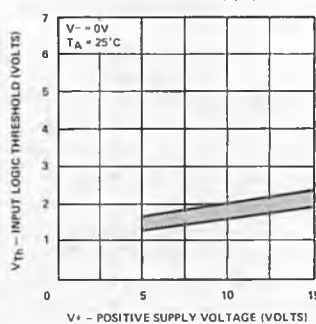
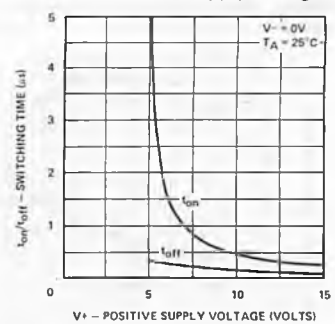


*Note: The turn off time is primarily limited here by the RC time constant (100 ns) of the load.

TYPICAL CHARACTERISTICS (Cont.)
Switching Time vs Temperature

Switching Time vs Negative Supply Voltage

Switching Time and Break-Before-Make Time vs Positive Supply Voltage

Input Switching Threshold vs Positive Supply Voltage

APPLICATIONS

The DG300A series of analog switches will switch positive analog signals while using a single positive supply. This will allow use in many applications where only one supply is available. The trade-offs or performance given up while using single supplies are: 1) Increased $r_{DS(ON)}$; 2) slower switching speed. Typical curves for aid in designing with

single supplies are supplied in the Figures below. As stated in the absolute maximum ratings section of the data sheet, the analog voltage should not go above or below the supply voltages which in single operation are $V+$ and 0 volts.

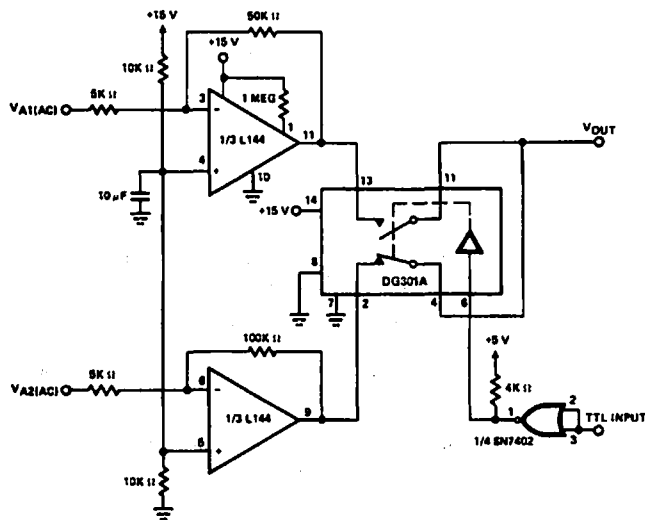
 $R_{DS(on)}$ vs Analog and Positive Supply Voltage With $V- = 0V$

Input Threshold Voltage vs Positive Supply

Switching Time vs $V+$ - Positive Supply Voltage

Single Supply Range:
 $V-$ and GND Tied Together
 $V+$: +5 V to +25 V

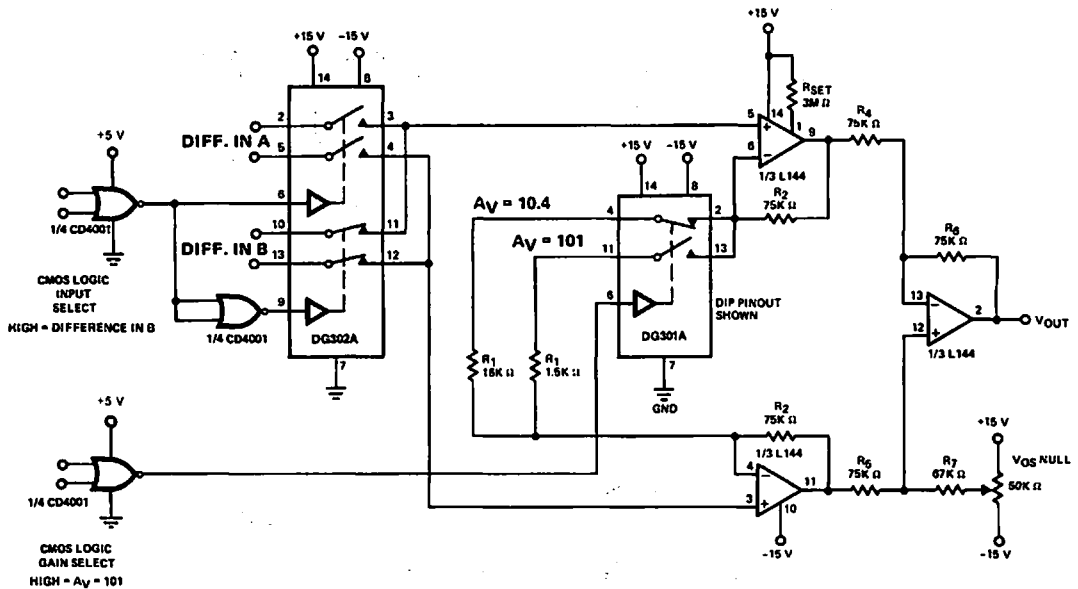
Analog Signal Range:
 $V- \leq V_{ANALOG} \leq V+$

APPLICATIONS (Cont.)

V+ Positive Supply Voltage (V)	V- Negative Supply Voltage (V)	GND	V _{in} Logic Inputs V _{INH} /V _{INL} (V)	V _S Analog Voltage Range (V)
15 V	-15 V	0	4.0 V/0.8 V	-15 to 15
20 V	-20 V	0	4.0 V/0.8 V	-20 to 20 V
15 V	0 V	0	4.0 V/0.8 V	0 to 15 V



Single Supply OP Amp Switching

APPLICATIONS (Cont.)


R_{SET} programs L144 power dissipation, gain-bandwidth product. Refer to AN73-6 and the L144 data sheet.

Voltage gain of the instrumentation amplifier is:

$$A_V = 1 + \frac{2R_2}{R_1} \quad (\text{In the circuit shown, } A_{V1} = 10.4, A_{V2} = 101)$$

**Low Power Instrumentation Amplifier with
Digitally Selectable Inputs and Gain**

DG304A/DG305A/ DG306A/DG307A CMOS Analog Switch Family



FEATURES

- Latchproof CMOS
- Fast Switching (<250 ns)
- Low $r_{DS(ON)}$ (<50 Ω)
- Single Supply Capability
- CMOS Switching Levels

BENEFITS

- Full Rail to Rail Analog Signal Range
- Low Signal Error
- Low Power Dissipation

APPLICATIONS

- Low Level Switching Circuits
- Programmable Gain Amplifiers
- Portable Battery Operation

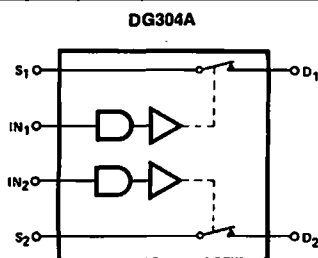
DESCRIPTION

The DG304A to DG307A family of monolithic CMOS switches feature four switch configuration options (SPST, SPDT, DPST, and SPDT) for precision applications in communications, instrumentation and process control, where low leakage switching combined with low power requirements are required. Designed on the Siliconix PLUS-40 CMOS process, the switches are latch proof, and are designed to block up to 30 Volts peak-to-peak when OFF. In the ON condition the switches conduct equally well in both directions (with no offset voltage) and minimize error conditions with their almost flat ON resistance of 50 Ω , max.

Featuring low power consumption, (a few milliwatts), these switches are ideal for battery powered applications, without sacrificing switching speed. Break-before-make switching action is guaranteed, and the switches are CMOS input compatible. Single supply operation (for positive switch voltages) is afforded by connecting the V- rail to 0 Volts.

The DG304A to DG307A family is offered in 14 or 16-pin plastic and ceramic DIP's, or the 10-pin metal can. Temperature options are 0 to 70°C, -25 to 85°C, and -55 to 125°C.

FUNCTIONAL BLOCK DIAGRAM



Two SPST Switches per Package*

Truth Table

LOGIC	SWITCH
0	OFF
1	ON

Logic "0" $\leq$ 3.5 V

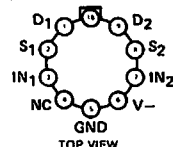
Logic "1" $\geq$ 11 V

*Switches Shown for Logic "1" Input

PIN CONFIGURATION

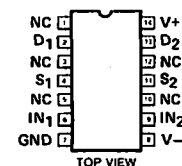
Metal Can Package

V+ (SUBSTRATE AND CASE)

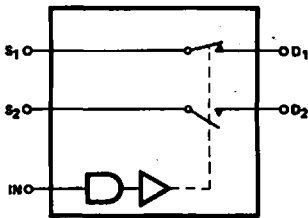


Order Numbers:
DG304AAA or DG304ABA
See Package 2

Dual-In-Line Package



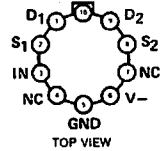
Order Numbers:
DG304AAK, DG304ABK,
DG304ACK
See Package 9
DG304ACJ
See Package 7

FUNCTIONAL BLOCK DIAGRAM
PIN CONFIGURATION
DG305A


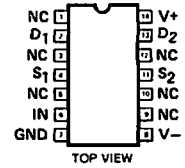
One SPDT Switch per Package*

Truth Table**

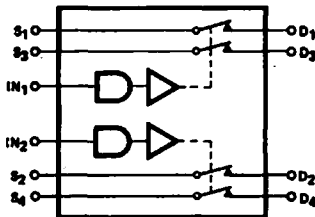
LOGIC	SW1	SW2
0	OFF	ON
1	ON	OFF

Metal Can Package
V+ (SUBSTRATE AND CASE)


Order Numbers:
DG305AAA or DG305ABA
See Package 2

Dual-In-Line Package


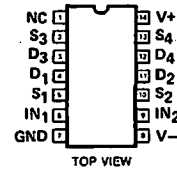
Order Numbers:
DG305AAK, DG305ABK,
DG305ACK
See Package 9
DG305ACJ
See Package 7

DG306A


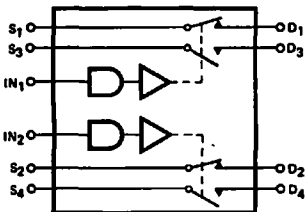
Two DPST Switches per Package*

Truth Table**

LOGIC	SWITCH
0	OFF
1	ON

Dual-In-Line Package


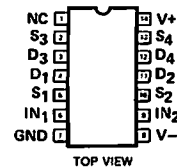
Order Numbers:
DG306AAK, DG306ABK,
DG306ACK
See Package 9
DG306ACJ
See Package 7

DG307A


Two SPDT Switches per Package*

Truth Table

LOGIC	SW1 SW2	SW3 SW4
0	OFF	ON
1	ON	OFF

Dual-In-Line Package


Order Numbers:
DG307AAK, DG307ABK,
DG307ACK
See Package 9
DG307ACJ
See Package 7

*Switches Shown for Logic "1" Input

**Logic "0" ≤ 3.5 V, Logic "1" ≥ 11 V

ABSOLUTE MAXIMUM RATINGS

Voltages Referenced to V-

V+	44 V
GND	25 V
Digital Inputs ¹ V _S , V _D	-2 V to (V+ +2 V) or 30 mA, whichever occurs first.
Current, Any Terminal Except S or D	30 mA
Continuous Current, S or D	30 mA
(Pulsed at 1 msec, 10% duty cycle max)	100 mA
Storage Temperature (A & B Suffix)	-65 to 150°C
(C Suffix)	-65 to 125°C
Operating Temperature (A Suffix)	-55 to 125°C
(B Suffix)	-25 to 85°C
(C Suffix)	0 to 70°C

Power Dissipation*

Cerdip (K)**	825 mW
Plastic DIP (J)***	470 mW
Metal Can (A)****	450 mW

*Device mounted with all leads soldered or welded to PC board.

**Derate 11 mW/°C above 75°C

***Derate 6.5 mW/°C above 25°C

****Derate 6 mW/°C above 75°C

ELECTRICAL CHARACTERISTICS²

 T_A = 25°C

	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: V+ = 15 V, V- = -15 V, GND = 0 V		LIMITS						UNIT
					DG304A to DG307AA			DG304A to DG307AB/C			
					MIN ³	TYP ⁴	MAX	MIN ³	TYP ⁴	MAX	
SWITCH	Analog Signal Range	V _{ANALOG}	I _S = 10 mA, V _{in} = 3.5 V or 11 V ⁵		-15		15	-15		15	V
	Drain-Source ON Resistance	r _{DS(on)}	V _{in} = 3.5 V or V _{in} = 11 V ⁵	I _S = -10 mA, V _D = 10 V		30	50		30	50	Ω
		I _S = 10 mA, V _D = -10 V			30	50		30	50		
	Source OFF Leakage Current	I _{S(off)}		V _S = 14 V, V _D = -14 V		0.1	1		0.1	5	
		V _S = -14 V, V _D = 14 V		-1	-0.1		-5	-0.1			
	Drain OFF Leakage Current	I _{D(off)}		V _S = -14 V, V _D = 14 V		0.1	1		0.1	5	nA
	V _S = 14 V, V _D = -14 V	-1		-0.1		-5	-0.1				
	Drain ON Leakage Current	I _{D(on)}	V _D = V _S = 14 V		0.1	1		0.1	5		
			V _D = V _S = -14 V	-2	-0.1		-5	-0.1			
INPUT	Input Current/Voltage High	I _{I(H)}	V _{in} = 5.0 V		-1	-0.001		-1	-0.001		μA
			V _{in} = 15 V			0.001	1		0.001	1	
	Input Current/Voltage Low	I _{I(L)}	V _{in} = 0 V		-1	-0.001		-1	-0.001		
DYNAMIC	Turn-ON Time	t _{on}	See Switching Time Test Circuit			110	250		110		ns
	Turn-OFF Time	t _{off}				70	150		70		
	Break-Before-Make Interval	t _{on} t _{off}	See Break-Before-Make Time Test Circuit DG305A/DG307A Only			50			50		
	Charge Injection	Q	C _L = 1 μF, R _{gen} = 0 Ω, V _{gen} = 0 V		3			3		mV	
	Source OFF Capacitance	C _{S(off)}	f = 1 MHz, V _{in} = 3.5 V or V _{in} = 11 V ⁵	V _S = 0		14			14		pF
	Drain OFF Capacitance	C _{D(off)}		V _D = 0		14			14		
	Channel ON Capacitance	C _{D(on)} + C _{S(on)}		V _S = V _D = 0		40			40		
	Input Capacitance	C _{in}		V _{in} = 0		6			6		
				V _{in} = 15 V		7			7		
	Off Isolation		V _{in} = 0, R _L = 1 kΩ V _S = 1 V _{RMS} , f = 500 kHz			62			62	dB	
	Crosstalk (Channel to Channel)				74			74			
SUPPLY	Positive Supply Current	I+	V _{in} = 15 (All inputs)			0.001	10		0.001	10	μA
	Negative Supply Current	I-			-10	-0.001		-10	-0.001		
	Positive Supply Current	I+	V _{in} = 0 (All inputs)			0.001	10		0.001	10	
	Negative Supply Current	I-			-10	-0.001		-10	-0.001		

NOTES:

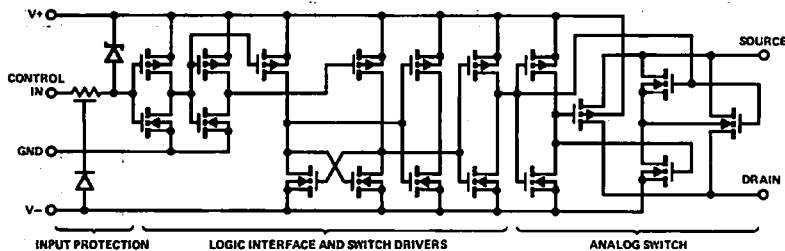
1. Signals on S_X, D_X, or I_{NX} exceeding V+ or V- will be clamped by internal diodes. Limit diode forward current to maximum current ratings.
2. Refer to PROCESS OPTION FLOWCHART for additional information.
3. The algebraic convention whereby the most negative value is a minimum, and the most positive value is a maximum is used in this data sheet.
4. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
5. OFF isolation = 20 log $\frac{V_S}{V_D}$, = input to OFF switch, V_D = Output.

ELECTRICAL CHARACTERISTICS² (Cont.)
 T_A = Over Temperature Range

	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: V+ = 15 V, V- = -15 V, GND = 0 V	LIMITS						UNIT	
				DG304A to DG307AA			DG304A to DG307AB/C				
				MIN ³	TYP ⁴	MAX	MIN ³	TYP ⁴	MAX		
SWITCH	Analog Signal Range	V _{ANALOG}	I _S = 10 mA, V _{in} = 3.5 V or 11 V ⁵	-15		15	-15		15	V	
	Drain-Source ON Resistance	r _{DS(on)}	V _{in} = 3.5 V or V _{in} = 11 V ⁵	I _S = -10 mA, V _D = 10 V				75		75	Ω
		I _S = 10 mA, V _D = -10 V				75		75			
	Source OFF Leakage Current	I _{S(off)}		V _S = 14 V, V _D = -14 V				100		100	nA
		V _S = -14 V, V _D = 14 V		-100			-100				
	Drain OFF Leakage Current	I _{D(off)}		V _S = -14 V, V _D = 14 V				100		100	
		V _S = 14 V, V _D = -14 V		-100			-100				
Drain ON Leakage Current	I _{D(on)}	V _D = V _S = 14 V				100		100			
		V _D = V _S = -14 V		-200			-200				
INPUT	Input Current/Voltage High	I _{INH}	V _{in} = 5.0 V	-1						μA	
			V _{in} = 15 V			1					
	Input Current/Voltage Low	I _{INL}	V _{in} = 0 V	-1							
SUPPLY	Positive Supply Current	I ₊	V _{in} = 15 (All inputs)			100				μA	
	Negative Supply Current	I ₋		-100							
	Positive Supply Current	I ₊	V _{in} = 0 (All inputs)			100					
	Negative Supply Current	I ₋		-100							

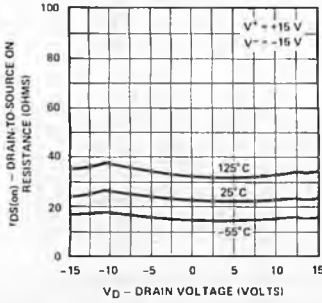
NOTES:

1. Signals on S_X , D_X , or IN_X exceeding V_+ or V_- will be clamped by internal diodes. Limit diode forward current to maximum current ratings.
2. Refer to PROCESS OPTION FLOWCHART for additional information.
3. The algebraic convention whereby the most negative value is a minimum, and the most positive value is a maximum is used in this data sheet.
4. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
5. OFF isolation = $20 \log \frac{V_S}{V_D}$, V_S = input to OFF switch, V_D = Output.

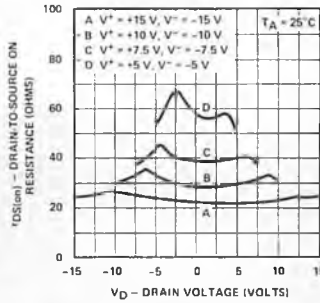
SCHEMATIC DIAGRAM (Typical Channel)


TYPICAL CHARACTERISTICS

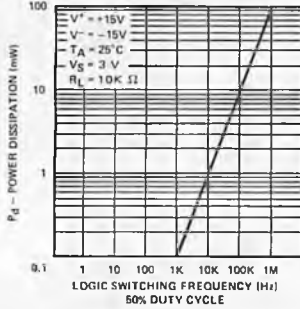
$r_{DS(on)}$ vs V_D and Temperature



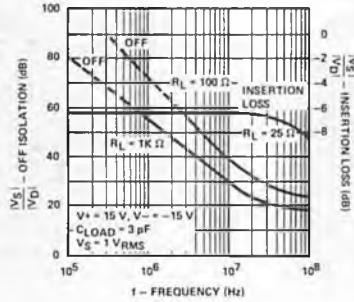
$r_{DS(on)}$ vs V_D and Power Supply Voltage



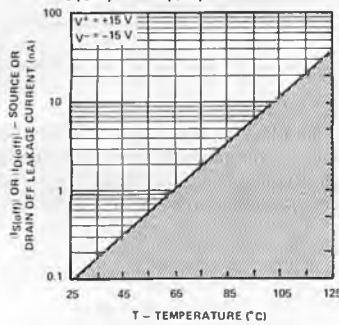
Device Power Dissipation vs Switching Frequency
Single Logic Input



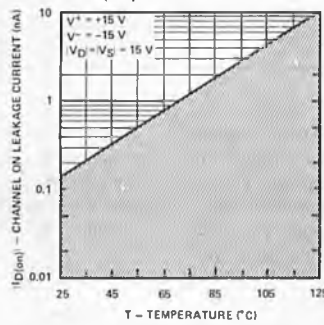
OFF Isolation Insertion Loss vs Frequency



$I_{S(off)}$ or $I_{D(off)}$ vs Temperature*

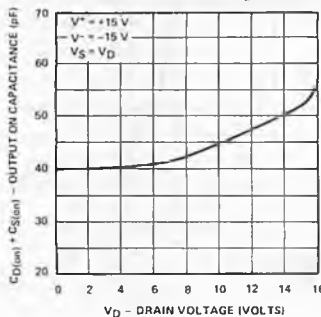


$I_{D(on)}$ vs Temperature*

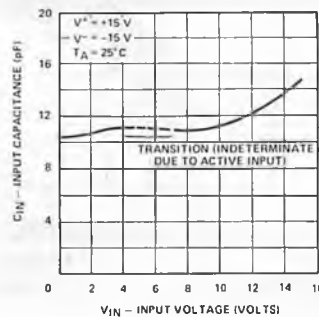


*The net leakage into the source or drain is the n-channel leakage minus the p-channel leakage. This difference can be positive, negative, or zero depending on the analog voltage and temperature, and will vary greatly from unit to unit.

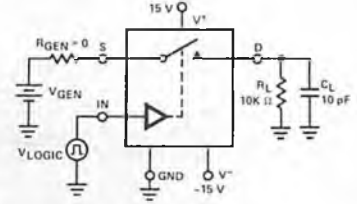
Output ON Capacitance vs Drain Voltage



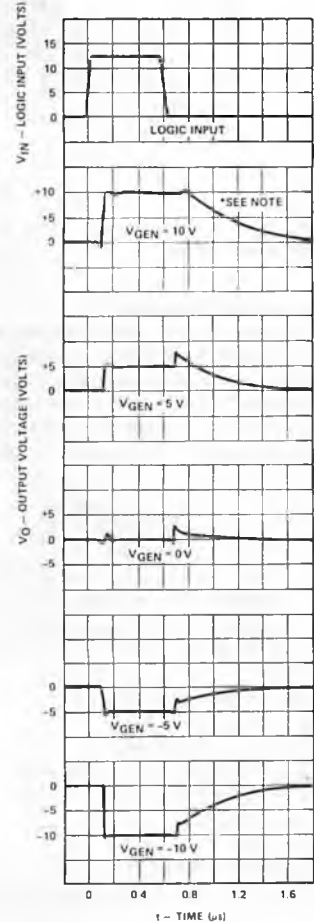
Input Capacitance vs Input Voltage



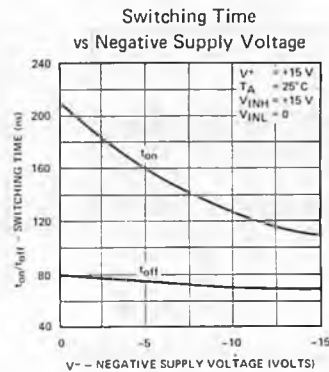
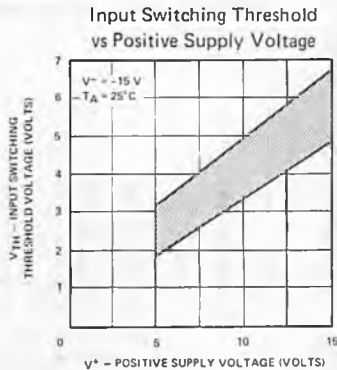
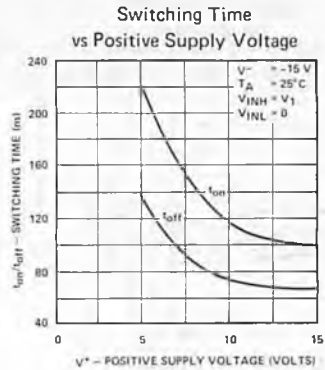
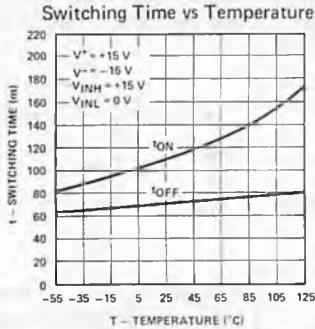
Typical delay, rise, fall, settling times, and switching transients in this circuit.



If R_{GEN} , R_L or C_L is increased, there will be proportional increases in rise and/or fall RC times. Applying V_{GEN} to D than S results in much greater spikes.

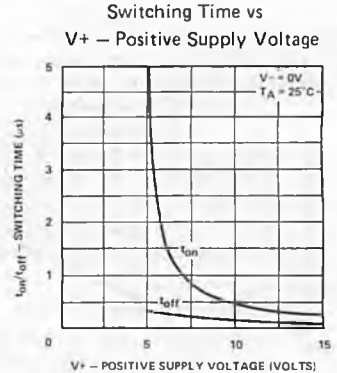
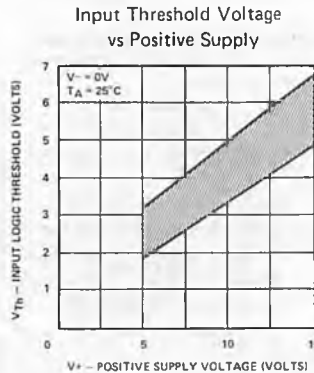
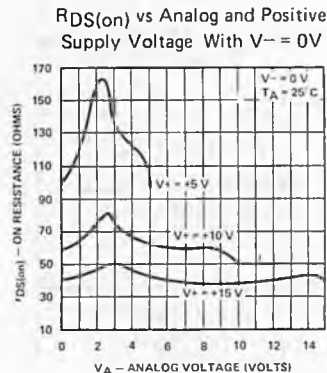


*Note: The turn off time is primarily limited here by the RC time constant (100 ns) of the load.

TYPICAL CHARACTERISTICS (Cont.)

APPLICATIONS
Single Supply Operation

The DG300 series of analog switches will switch positive analog signals while using a single positive supply. This will allow use in many applications where only one supply is available. The trade-offs or performance given up while using single supplies are: 1) Increased $r_{\text{DS(ON)}}$; 2) slower switching speed. Typical curves for aid in designing with

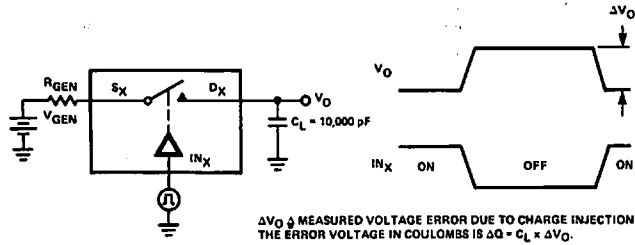
single supplies are supplied in the Figures below. As stated in the absolute maximum ratings section of the data sheet, the analog voltage should not go above or below the supply voltages which in single operation are V^{+} and 0 volts.



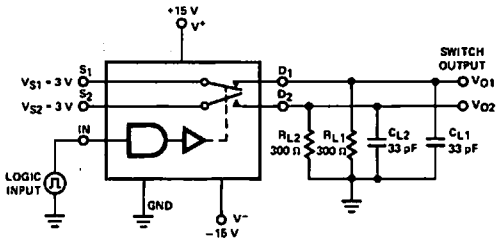
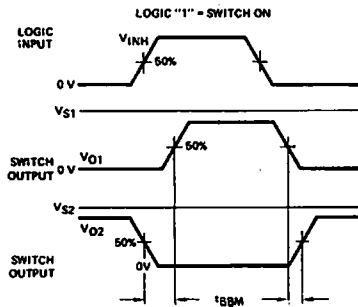
Single Supply Range:
 $(V^{-} \text{ and GND Tied Together})$
 $V^{+}: +5\text{ V to }+25\text{ V}$

Analog Signal Range:
 $V^{-} < V_{\text{ANALOG}} < V^{+}$

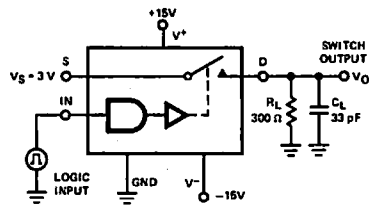
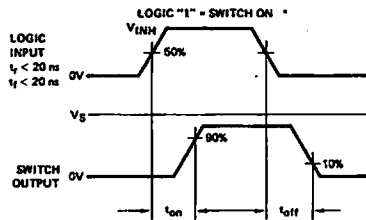
TEST CIRCUITS



Charge Injection Test Circuit



Break-Before-Make Time Test Circuit SPDT (DG305A, DG307A)



Switching Time Test Circuit

DG308A/DG309

Quad Monolithic SPST CMOS

Analog Switches



FEATURES

- ± 15 V Input Range
- Fast $t_{on} < 130$ ns, typ
- $r_{DS(on)} < 60 \Omega$, typ
- Low Power $< 30 \mu W$, typ
- CMOS Logic Compatible

BENEFITS

- Static Protected Logic Inputs
- Latchproof
- Rail-to-Rail Analog Signal Range
- Single or Dual Supply Capability

APPLICATIONS

- Portable, Battery Instrumentation
- Communication Systems
- Computer Peripherals
- High Speed Multiplexing

DESCRIPTION

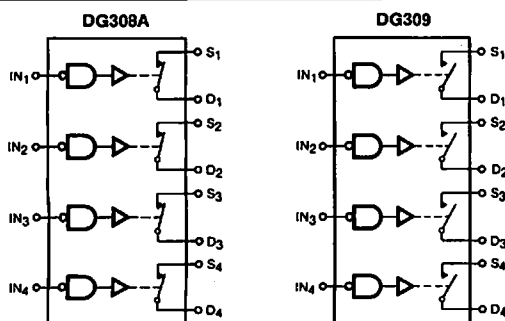
The DG308A and DG309 are quad single-pole-single-throw analog switches designed for high speed switching applications in communications, instrumentation and process control. Featuring low 60Ω ON resistance and 130 ns turn-on time, DG308A is supplied in the "normally-closed" configuration (logic 1) while DG309 is supplied "normally-open" (logic 1). Input thresholds are CMOS compatible.

Designed with the proprietary Siliconix PLUS-40 CMOS process to combine low power dissipation with a

high breakdown voltage rating of 40 V, both switches feature true bi-directional performance, (with no offset voltage) and will block signals to 30 V peak-to-peak in the OFF condition. Rated analog signal range is ± 15 V at 20mA continuous.

DG308A and DG309 are supplied in the 16-pin plastic and ceramic dual-in-line packages, and are optionally specified over the temperature ranges -55 to $125^\circ C$, -25 to $85^\circ C$ and 0 to $70^\circ C$.

FUNCTIONAL BLOCK DIAGRAM



Four SPST Switches Per Package*

Truth Table

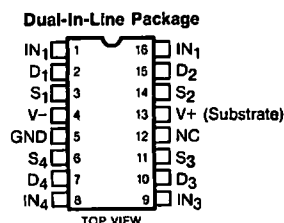
LOGIC	DG308A	DG309
0	OFF	ON
1	ON	OFF

Logic "0" ≤ 3.5 V

Logic "1" ≥ 11 V

*Switches Shown For Logic "1" Input

PIN CONFIGURATION



Order Numbers:

DG308AAK, DG308ABK or DG308ACK

DG309AK, DG309BK or DG309CK

See Package 10

DG308ACJ or DG309CJ

See Package 8

ABSOLUTE MAXIMUM RATINGS

Voltages Referenced to V-

V+ 44 V

GND 25 V

 Digital Inputs, V_S, V_D -2 V to (V⁺ + 2 V) or
20 mA, whichever occurs first.

Current, Any Terminal Except S or D 30 mA

Continuous Current, S or D 20 mA

Peak Current S or D 70 mA

(Pulsed at 1 msec, 10% duty cycle max)

Storage Temperature (A & B Suffix) -65 to 150°C

(C Suffix) -65 to 125°C

Operating Temperature (A Suffix) -55 to 125°C

(B Suffix) -25 to 85°C

(C Suffix) 0 to 70°C

Power Dissipation (Package)*

16-Pin DIP** 900 mW

16-Pin Plastic DIP*** 470 mW

 *Device mounted with all leads soldered or welded to
PC board.

**Derate 12 mW/°C above 75°C

***Derate 6.5 mW/°C above 25°C

ELECTRICAL CHARACTERISTICS²

 T_A = 25°C

	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: V ₊ = 15 V, V ₋ = -15 V, GND = 0 V	LIMITS						UNIT
				DG308AA			DG308AB/C			
				MIN ³	TYP ⁴	MAX	MIN ³	TYP ⁴	MAX	
SWITCH	Analog Signal Range	V _{ANALOG}		-15		15	-15		15	V
	Drain-Source ON Resistance	r _{DS(on)}	V _{in} = 11 V (DG308A) V _D = 10 V, I _S = -1 mA V _D = -10 V, I _S = 1 mA		60	100		60	100	Ω
	Drain ON Leakage Current	I _{D(on)}	V _{in} = 3.5 V (DG309) V _D = V _S = 14 V V _D = V _S = -14 V		0.1	1		0.1	5	
	Source OFF Leakage Current	I _{S(off)}	V _{in} = 3.5 V (DG308A) V _S = 14 V, V _D = -14 V V _S = -14 V, V _D = 14 V		0.1	1		0.1	5	nA
	Drain OFF Leakage Current	I _{D(off)}	V _{in} = 11 V (DG309) V _D = 14 V, V _S = -14 V V _D = -14 V, V _S = 14 V		0.1	1		0.1	5	
INPUT	Input Current with Input Voltage High	I _{INH}	V _{in} = 15 V		0.001	1		0.001	1	μA
	Input Current with Input Voltage Low	I _{INL}	V _{in} = 0 V	-1	-0.001		-1	-0.001		
DYNAMIC	Turn-ON Time	t _{on}	See Switching Time Test Circuit		130	200		130	200	ns
	Turn-OFF Time	t _{off}			90	150		90	150	
	Charge Injection	Q	C _L = 1 μF, R _{gen} = 0 Ω, V _{gen} = 0 V		-10			-10		pC
	Source OFF Capacitance	C _{S(off)}	V _S = 0, V _{in} = 0 V (DG308A) V _{in} = 15 V (DG309)		11			11		pF
	Drain OFF Capacitance	C _{D(off)}	V _D = 0, V _{in} = 0 V (DG308A) V _{in} = 15 V (DG309)		8			8		
	Channel ON Capacitance	C _{D(on)} + C _{S(on)}	V _D = V _S = 0, V _{in} = 15 V (DG308A) V _{in} = 0 V (DG309)		27			27		
	Off Isolation ⁵		V _{in} = 0 V (DG308A) or 15 V (DG309), Z _L = 75 Ω, V _S = 2 Vp-p, f = 500 kHz		78			78		
SUPPLY	Positive Supply Current	I ₊	All Channels "ON" or "OFF" V _{in} = 0 or 15 V		0.001	10		0.001	100	μA
	Negative Supply Current	I ₋			-10	-0.001		-100	-0.001	

NOTES:

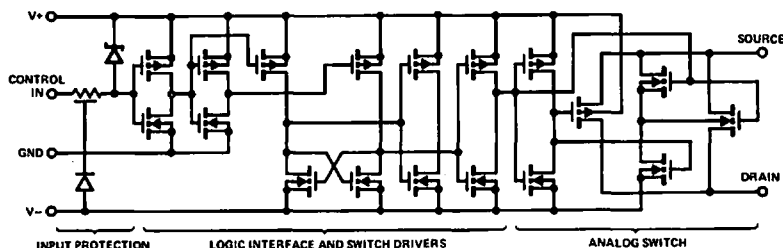
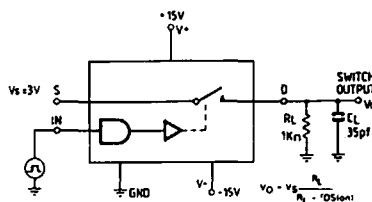
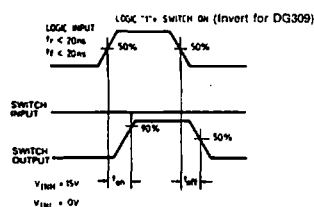
1. Signals on S_X, D_X, or I_{NX} exceeding V⁺ or V⁻ will be clamped by internal diodes. Limit forward diode current to maximum current rating.
2. Refer to PROCESS OPTION FLOWCHART for additional information.
3. The algebraic convention whereby the most negative value is a minimum, and the most positive is a maximum is used in this data sheet.
4. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
5. OFF Isolation = 20 log₁₀ $\frac{V_D}{V_S}$, V_D = Output, V_S = Input to OFF Switch.

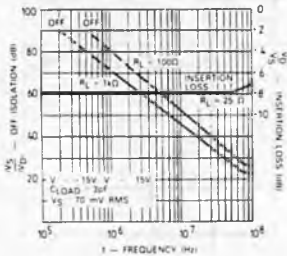
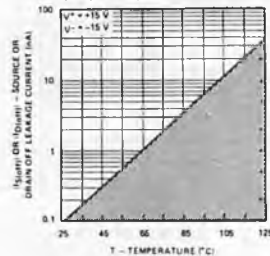
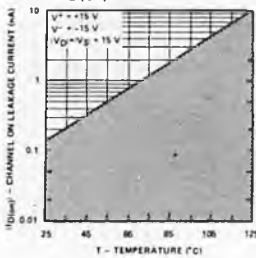
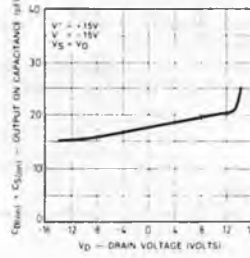
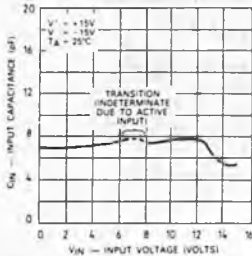
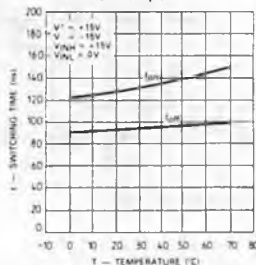
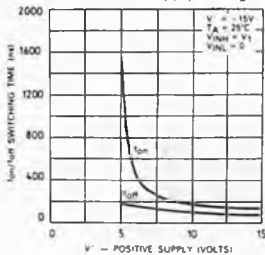
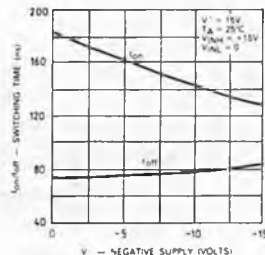
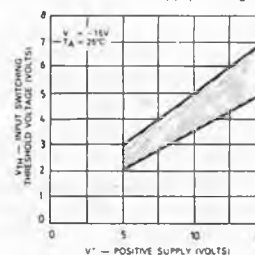
ELECTRICAL CHARACTERISTICS² (Cont.) T_A = Over Temperature Range

	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: V+ = 15 V, V- = -15 V, GND = 0 V		LIMITS						UNIT
					DG308AA			DG308AB/C			
					MIN ³	TYP ⁴	MAX	MIN ³	TYP ⁴	MAX	
SWITCH	Analog Signal Range	V _{ANALOG}			-15		15	-15		15	V
	Drain-Source ON Resistance	r _{DS(on)}	V _{in} = 11 V (DG308A)	V _D = 10 V, I _S = 1 mA V _D = -10 V, I _S = 1 mA			150			125	Ω
	Drain ON Leakage Current	I _{D(on)}	V _{in} = 3.5 V (DG309)	V _D = V _S = 14 V V _D = V _S = -14 V			100			200	
	Source OFF Leakage Current	I _{S(off)}	V _{in} = 3.5 V (DG308A)	V _S = 14 V, V _D = -14 V V _S = -14 V, V _D = 14 V			100		-100	100	nA
	Drain OFF Leakage Current	I _{D(off)}	V _{in} = 11 V (DG309)	V _D = 14 V, V _S = -14 V V _D = -14 V, V _S = 14 V			100		-100	100	
	INPUT	Input Current with Input Voltage High	I _{INH}	V _{in} = 15 V			1				μA
	Input Current with Input Voltage Low	I _{INL}	V _{in} = 0 V	-1							
SUPPLY	Positive Supply Current	I+	V _{in} = 0 or 15 V				100				μA
	Negative Supply Current	I-			-100						

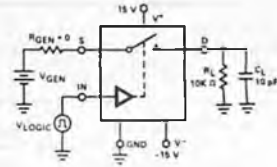
NOTES:

1. Signals on S_X , D_X , or I_NX exceeding V^+ or V^- will be clamped by internal diodes. Limit forward diode current to maximum current rating.
2. Refer to **PROCESS OPTION FLOWCHART** for additional information.
3. The algebraic convention whereby the most negative value is a minimum, and the most positive is a maximum is used in this data sheet.
4. Typical values are for **DESIGN AID ONLY**, not guaranteed nor subject to production testing.
5. OFF isolation = $20 \log_{10} \frac{V_D}{V_S}$, V_D = Output, V_S = Input to OFF Switch.

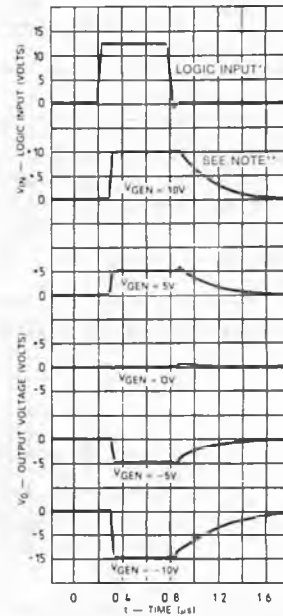
SCHEMATIC DIAGRAM (Typical Channel)

SWITCHING TIME TEST CIRCUIT


TYPICAL CHARACTERISTICS
OFF-Isolation, Insertion Loss vs Frequency

 $I_S(\text{off})$ or $I_D(\text{off})$ vs Temperature*

 $I_D(\text{on})$ vs Temperature*

Output ON Capacitance vs Drain Voltage

Input Capacitance vs Input Voltage

Switching Time vs Temperature

Switching Time vs Positive Supply Voltage

Switching Time vs Negative Supply Voltage

Input Switching Threshold vs Positive Supply Voltage


Typical delay, rise, fall, settling times, and switching transients in this circuit.



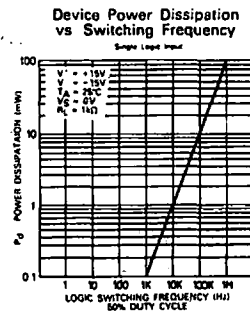
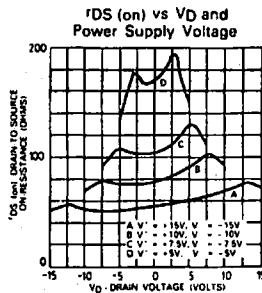
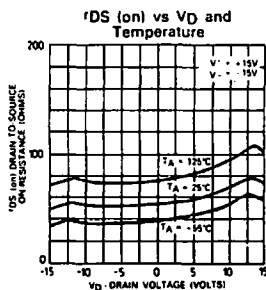
If R_{GEN} , R_L or C_L is increased, there will be proportional increases in rise and/or fall RC times. Applying V_{GEN} to D rather than S results in much greater spikes.



*Logic Input inverted for DG309.

**The turn-off time is primarily limited here by the RC time constant (100 ns) of the load.

*The net leakage into the source or drain is the n-channel leakage minus the p-channel leakage. This difference can be positive, negative, or zero depending on the analog voltage and temperature, and will vary greatly from unit to unit.

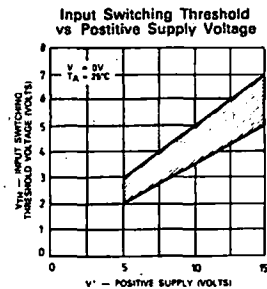
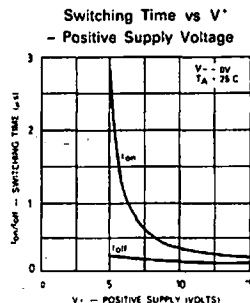
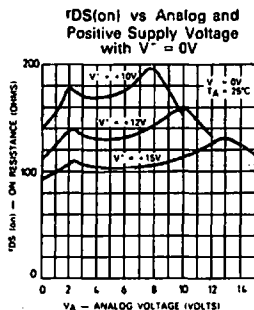


APPLICATIONS

Single Supply Operation

The DG308A and DG309 will switch positive analog signals while using a single positive supply. This will allow use in many applications where only one supply is available. The trade-offs or performance given up while using single supplies are: 1) Increased $r_{DS(ON)}$; 2) slower switching speed. Typical curves for aid in designing with

single supplies are supplied in the Figures below. As stated in the absolute maximum ratings section of the data sheet, the analog voltage should not go above or below the supply voltages which in single operation are $V+$ and 0 volts.



Single Supply Range: (V^- and GND Tied Together) V^+ : +5 V to +25 V
Analog Signal Range: $V^- < V_{ANALOG} < V^+$

DG381A/DG384A/ DG387A/DG390A

General Purpose CMOS Analog Switches



FEATURES

- Latchproof CMOS
- Pin and Functional Replacement for the DG181 Family
- Low $r_{DS(ON)}$ ($<75 \Omega$)
- Single Supply Capability

BENEFITS

- Full Rail to Rail Analog Signal Range
- Minimizes Signal Error
- Low Power Dissipation

APPLICATIONS

- Low Level Switching Circuits
- Programmable Gain Amplifiers
- Portable Battery Operation

DESCRIPTION

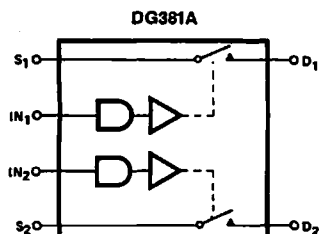
The DG381A-DG390A family of switches were designed on the Siliconix PLUS-40 CMOS process to be functionally comparable in performance to the multi-chip DG181 family, but with the reliability and low power consumption obtainable with monolithic CMOS technology. The family features three different switching options (SPST, SPDT, DPST) with low and nearly constant ON resistance ($<75 \Omega$) over their entire operating range of ± 15 Volts. In the ON condition the switches will conduct current in either direction with no offset voltage, while in the OFF condition the switches block up to 30 V p-p.

Featuring low power consumption, (3 mW typical) these

switches are ideal for battery powered applications, without sacrificing switching speed. Designed for break-before-make switching action, the switches are TTL and CMOS input compatible. Single supply operation (for positive switch voltages) is afforded by connecting the V-rail to 0 Volts.

The DG381A-DG390A family is offered in 14 or 16-pin plastic and ceramic DIP's, or the 10-pin metal can. Temperature options are 0 to 70°C, -25 to 85°C, and -55 to 125°C.

FUNCTIONAL BLOCK DIAGRAM



Two SPST Switches per Package*

Truth Table

LOGIC	SW1 SW2
0	ON
1	OFF

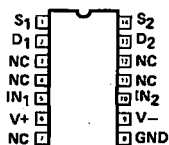
Logic "0" ≤ 0.8 V

Logic "1" ≥ 4.0 V

*Switches Shown for Logic "1" Input

PIN CONFIGURATION

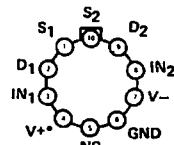
Dual-In-Line Package



TOP VIEW

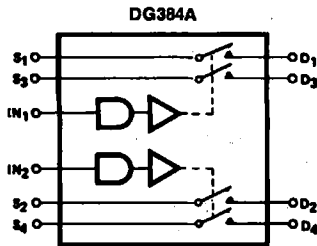
Order Numbers:
DG381AAK, DG381ABK,
or DG381ACK
See Package 9
DG381ACJ
See Package 7

Metal Can Package



TOP VIEW

Order Numbers:
DG381AAA, DG381ABA,
or DG381ACA
See Package 2

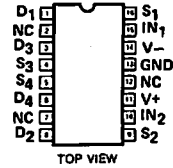
FUNCTIONAL BLOCK DIAGRAM
PIN CONFIGURATION


Two DPST Switches per Package*

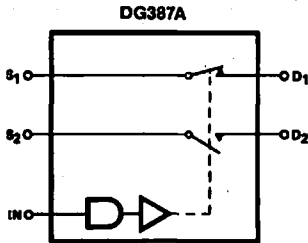
Truth Table**

LOGIC	SW1-4
0	OFF
1	ON

Dual-In-Line Package



Order Numbers:
DG384AAK, DG384ABK,
 or **DG384ACK**
 See Package 10
DG384ACJ
 See Package 8

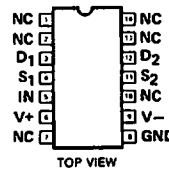


One SPDT Switch per Package*

Truth Table**

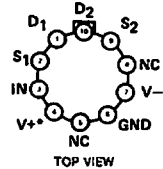
LOGIC	SW1	SW2
0	OFF	ON
1	ON	OFF

Dual-In-Line Package

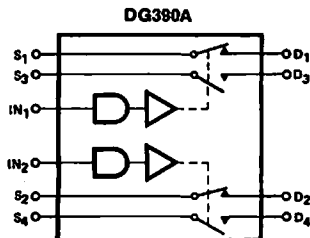


Order Numbers:
DG387AAK, DG387ABK,
 or **DG387ACK**
 See Package 9
DG387ACJ
 See Package 7

Metal Can Package



Order Numbers:
DG387AAA, DG387ABA,
 or **DG387ACA**
 See Package 2

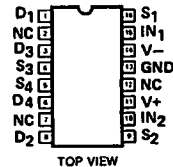


Two SPDT Switches per Package*

Truth Table**

LOGIC	SW1 SW2	SW3 SW4
0	OFF	ON
1	ON	OFF

Dual-In-Line Package



Order Numbers:
DG390AAK, DG390ABK,
 or **DG390ACK**
 See Package 10
DG390ACJ
 See Package 8

*Switches Shown for Logic "1" Input
 **Logic "0" ≤ 0.8 V, Logic "1" ≥ 4.0 V

ABSOLUTE MAXIMUM RATINGS

Voltages Referenced to V-

 V+ 44 V
 GND 25 V
 Digital Inputs¹ V_S, V_D -2 V to (V+ + 2 V) or
 30 mA, whichever occurs first.

Current, Any Terminal Except S or D 30 mA

 Continuous Current, S or D 30 mA
 (Pulsed at 1 msec, 10% duty cycle max) 100 mA

 Storage Temperature (A & B Suffix) -65 to 150°C
 (C Suffix) -65 to 125°C

 Operating Temperature (A Suffix) -55 to 125°C
 (B Suffix) -25 to 85°C
 (C Suffix) 0 to 70°C

Power Dissipation*

Cerdip (K)** 825 mW

Plastic DIP (J)*** 470 mW

Metal Can (A)**** 450 mW

*Device mounted with all leads soldered or welded to PC board.

**Derate 11 mW/°C above 75°C

***Derate 6.5 mW/°C above 25°C

****Derate 6 mW/°C above 75°C

ELECTRICAL CHARACTERISTICS²

 T_A = 25°C

	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: V+ = 15 V, V- = -15 V, GND = 0 V	LIMITS						UNIT	
				DG381A-DG390AA			DG381A-DG390AA				
				MIN ³	TYP ⁴	MAX	MIN ³	TYP ⁴	MAX		
SWITCH	Analog Signal Range	V _{ANALOG}	I _S = 10 mA, V _{IN} = 0.8 V or 4.0 V ⁵	-15		15	-15		15	V	
	Drain-Source ON Resistance	r _{DS(on)}	V _{IN} = 0.8 V or V _{IN} = 4.0 V ⁵	I _S = -10 mA, V _D = 10 V		30	50		30	50	Ω
		I _S = 10 mA, V _D = -10 V			30	50		30	50		
	Source OFF Leakage Current	I _{S(off)}		V _S = 14 V, V _D = -14 V		0.1	1		0.1	5	
		V _S = -14 V, V _D = 14 V		-1	-0.1		-5	-0.1			
	Drain OFF Leakage Current	I _{D(off)}		V _S = -14 V, V _D = 14 V		0.1	1		0.1	5	
		V _S = 14 V, V _D = -14 V	-1	-0.1		-5	-0.1				
		V _D = V _S = 14 V		0.1	1		0.1	5			
		V _D = V _S = -14 V	-2	-0.1		-5	-0.1				
INPUT	Input Current/Voltage, High	I _{INH}	V _{IN} = 5.0 V	-1	-0.001		-1	-0.001		μA	
			V _{IN} = 15 V		0.001	1		0.001	1		
	Input Current/Voltage Low	I _{INL}	V _{IN} = 0 V	-1	-0.001		-1	-0.001			
DYNAMIC	Turn-ON Time	t _{on}	See Switching Time Test Circuit		150	300		150		ns	
	Turn-OFF Time	t _{off}			130	250		130			
	Break-Before-Make Interval	t _{on} - t _{off}	See Break-Before-Make Time Test Circuit DG387A/DG390A Only		50			50			
	Charge Injection	O	See Charge Injection Test Circuit		3			3		mV	
	Source OFF Capacitance	C _{S(off)}	f = 1 MHz, V _{IN} = 0.8 V or V _{IN} = 4.0 V ⁵	V _S = 0		14			14	pF	
	Drain OFF Capacitance	C _{D(off)}		V _D = 0		14			14		
	Channel ON Capacitance	C _{D(on)} + C _{S(on)}		V _S = V _D = 0		40			40		
	Input Capacitance	C _{in}		V _{IN} = 0		6			6		
				V _{IN} = 15 V		7			7		
	Off Isolation		V _{IN} = 0, R _L = 1 kΩ V _S = 1 V _{RMS} , f = 500 kHz		62			62		dB	
Crosstalk (Channel to Channel)				74			74				
SUPPLY	Positive Supply Current	I+	V _{IN} = 4 V (One Input, All Others = 0)		0.23	0.5		0.23	1	mA	
	Negative Supply Current	I-		-10	-0.001		-100	-0.001			
	Positive Supply Current	I+	V _{IN} = 0.8 V (All inputs)		0.001	10		0.001	100	μA	
	Negative Supply Current	I-		-10	-0.001		-100	-0.001			

NOTES:

1. Signals on S_x, D_x, or I_{Nx} exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
2. Refer to PROCESS OPTION FLOWCHART for additional information.
3. The algebraic convention whereby the most negative value is a minimum, and the most positive is a maximum is used in this data sheet.
4. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
5. V_{IN} = Input voltage to perform proper function.
6. "OFF" isolation = 20 log V_S/V_D, V_S = input to OFF switch, V_D = Output.

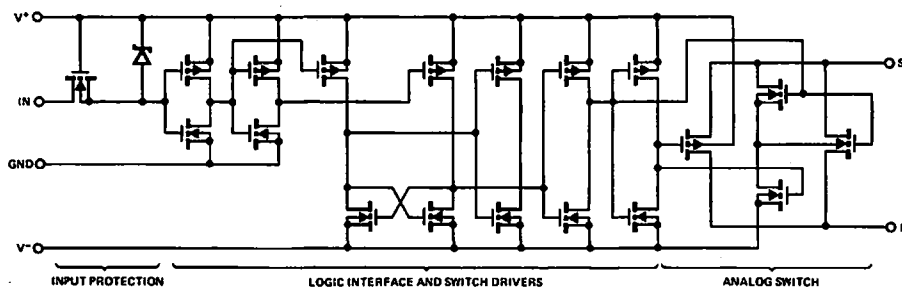
ELECTRICAL CHARACTERISTICS² (Cont.)
 T_A = Over Temperature Range

	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: V+ = 15 V, V- = -15 V, GND = 0 V	LIMITS						UNIT
				DG381A-DG390AA			DG381A-DG390AA			
				MIN ³	TYP ⁴	MAX	MIN ³	TYP ⁴	MAX	
SWITCH	Analog Signal Range	V _{ANALOG}	I _S = 10 mA, V _{in} = 0.8 V or 4.0V ⁵	-15		15	-15		15	V
	Drain-Source ON Resistance	r _{DS(on)}	V _{in} = 0.8 V or V _{in} = 4.0V ⁵	I _S = -10 mA, V _D = 10 V		75			75	Ω
		I _S = 10 mA, V _D = -10 V			75			75		
		V _S = 14 V, V _D = -14 V			100			100		
	Source OFF Leakage Current	I _{S(off)}		V _S = -14 V, V _D = 14 V	-100		-100			nA
		V _S = -14 V, V _D = 14 V			100			100		
		V _S = 14 V, V _D = -14 V		-100		-100				
	Drain OFF Leakage Current	I _{D(off)}	V _D = V _S = 14 V		100			100		
		V _D = V _S = -14 V	-200		-200					
INPUT	Input Current/Voltage High	I _{INH}	V _{in} = 5.0 V	-1						μA
			V _{in} = 15 V			1				
	Input Current/Voltage Low	I _{INL}	V _{in} = 0 V	-1						
SUPPLY	Positive Supply Current	I ₊	V _{in} = 4 V (One Input, All Others = 0)			0.5				mA
	Negative Supply Current	I ₋		-100						
	Positive Supply Current	I ₊	V _{in} = 0.8 V (All inputs)			100				μA
	Negative Supply Current	I ₋		-100						

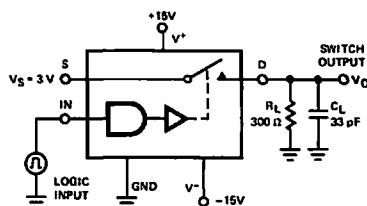
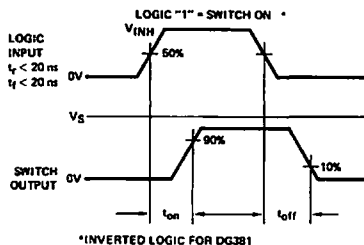
NOTES:

1. Signals on S_X , D_X , or IN_X exceeding V_+ or V_- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
2. Refer to PROCESS OPTION FLOWCHART for additional information.
3. The algebraic convention whereby the most negative value is a minimum, and the most positive is a maximum is used in this data sheet.
4. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
5. V_{in} = Input voltage to perform proper function.
6. "OFF" isolation = $20 \log V_S/V_D$. V_S = Input to OFF switch, V_D = Output.

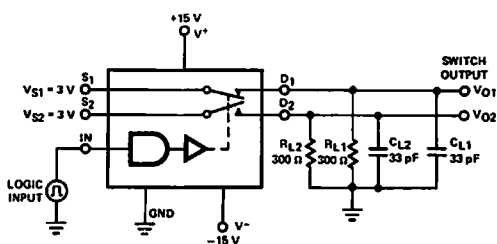
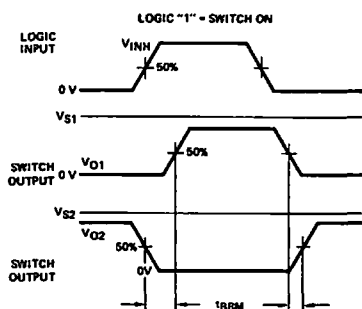
PARTIAL SCHEMATIC OF TYPICAL SWITCH



TEST CIRCUITS



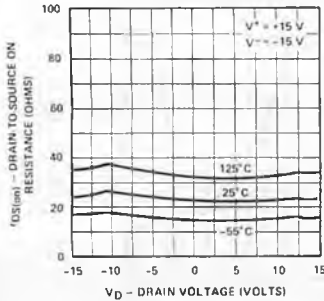
Switching Time Test Circuit



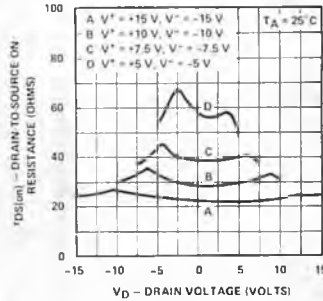
Break-Before-Make Time Test Circuit SPDT (DG387A, DG390A)

TYPICAL CHARACTERISTICS

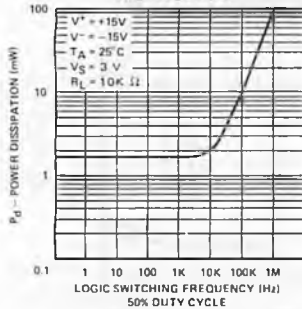
$r_{DS(on)}$ vs V_D and Temperature



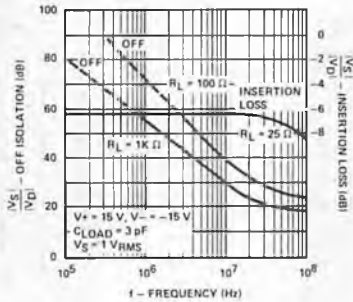
$r_{DS(on)}$ vs V_D and Power Supply Voltage



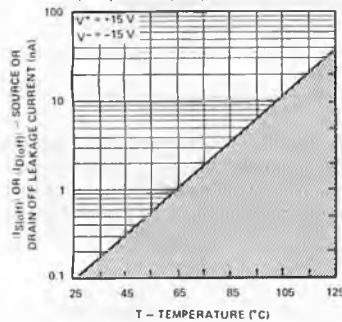
Device Power Dissipation vs Switching Frequency
Single Logic Input



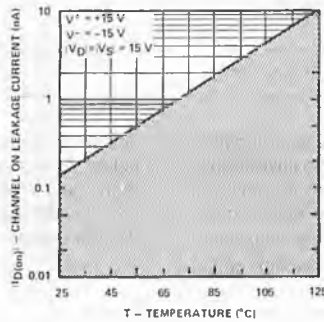
OFF Isolation Insertion Loss vs Frequency



$I_{S(off)}$ or $I_{D(off)}$ vs Temperature*

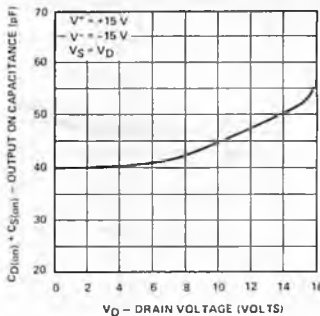


$I_{D(on)}$ vs Temperature*

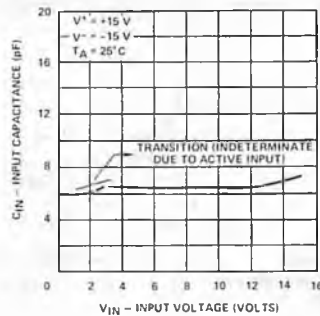


*The net leakage into the source or drain is the n-channel leakage minus the p-channel leakage. This difference can be positive, negative, or zero depending on the analog voltage and temperature, and will vary greatly from unit to unit.

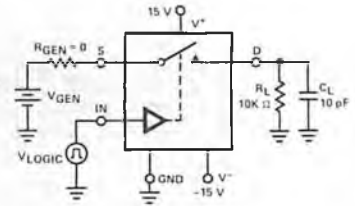
Output ON Capacitance vs Drain Voltage



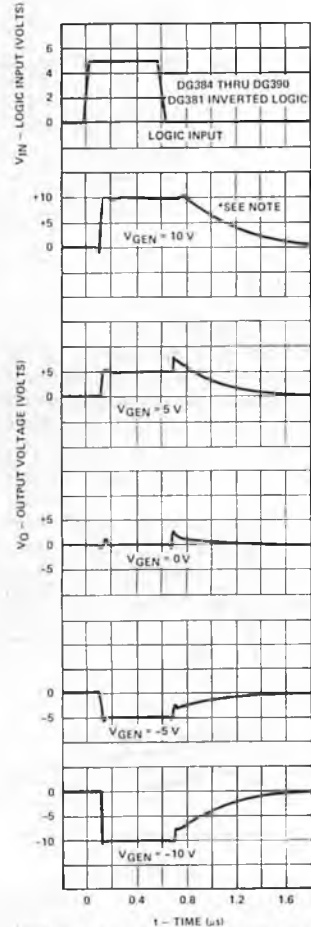
Input Capacitance vs Input Voltage



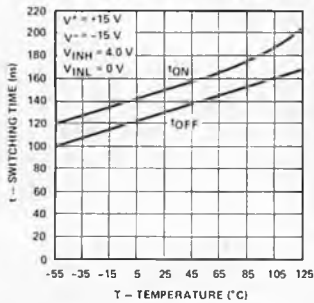
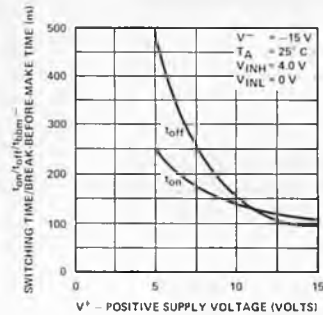
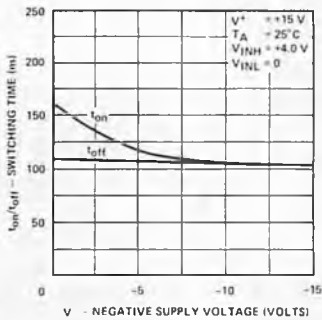
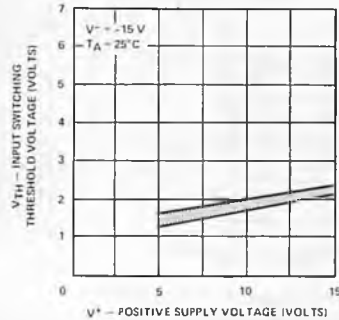
Typical delay, rise, fall, settling times, and switching transients in this circuit.



If R_{GEN} , R_L or C_L is increased, there will be proportional increases in rise and/or fall RC times. Applying V_{GEN} to D rather than S results in much greater spikes.

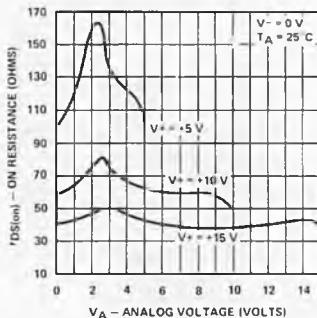
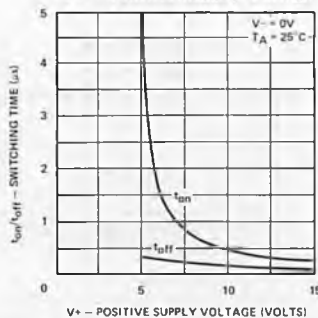
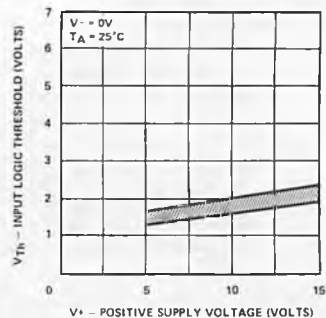


*Note: The turn off time is primarily limited here by the RC time constant (100 ns) of the load.

TYPICAL CHARACTERISTICS (Cont.)
Switching Time vs Temperature

Switching Time and Break-Before-Make Time vs Positive Supply Voltage

Switching Time vs Negative Supply Voltage

Input Switching Threshold vs Positive Supply Voltage

APPLICATIONS
Single Supply Operation

The DG381A-DG390A series of analog switches will switch positive analog signals while using a single positive supply. This will allow use in many applications where only one supply is available. The trade-offs or performance given up while using single supplies are: 1) Increased $R_{DS(ON)}$; 2) slower switching speed. Typical curves for aid in

designing with single supplies are supplied in the Figures below. As stated in the absolute maximum ratings section of the data sheet, the analog voltage should not go above or below the supply voltages which in single operation are $V+$ and 0 volts.

 $R_{DS(on)}$ vs Analog and Positive Supply Voltage With $V- = 0V$

Switching Time vs $V+$ - Positive Supply Voltage
Input Threshold Voltage vs Positive Supply

Single Supply Range:
($V-$ and GND Tied Together)
 $V+$: +5 V to +25 V

Analog Signal Range:
 $V- < V_{ANALOG} < V+$

DG5040-DG5045

Monolithic General Purpose CMOS Analog Switches



FEATURES

- ± 15 Volt Input Range
- ON Resistance $< 35 \Omega$
- High Current Capacity, to 100 mA (pulse)
- Break-Before-Make Switching
- TTL, CMOS, PMOS Compatible

BENEFITS

- Available Normally Open or Closed
- Low Signal Errors
- No Shorting of Inputs
- Simple Interfacing

APPLICATIONS

- High Performance Switching
- Sample and Hold Circuits
- Digital Filters

DESCRIPTION

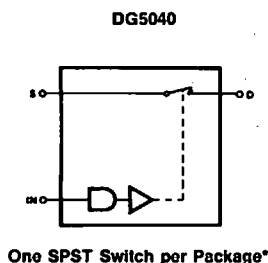
The DG5040 family of solid state analog switches are recommended for general purpose applications in instrumentation, and process control. Built on the Siliconix PLUS 40 high voltage CMOS monolithic process, these devices provide ease-of-use and performance advantages to the system designer. Key performance features of the 5040 series are $1 \mu s$ switching, low power supply requirements, and break-before-make switching which guarantees that an ON channel will be turned OFF before an OFF channel can turn ON. Each switch conducts equally in either direction, when ON, and blocks up to 30

volts peak-to-peak when OFF. OFF leakage current is less than 1 nA.

There are six devices in this series, which are differentiated by the type of switch action as shown in the functional block diagrams. In all cases the switches are bidirectional and maintain almost constant ON resistance throughout their operating range.

Package options include the 16-pin plastic and ceramic DIP. Performance grades include 0 to $70^\circ C$, and -55 to $125^\circ C$.

FUNCTIONAL BLOCK DIAGRAM



Truth Table

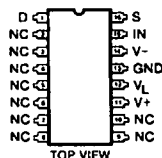
LOGIC	SWITCH
0	OFF
1	ON

Logic "0" $\leq 0.8 V$
Logic "1" $\geq 2.0 V$

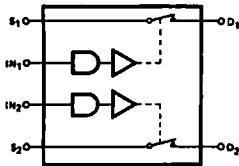
*Switches Shown for Logic "1" Input

PIN CONFIGURATION

Dual-In-Line Package



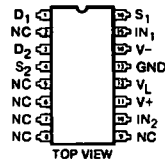
Order Numbers:
DG5040AK, DG5040CK,
DG5040CJ
See Package 8 or 10

FUNCTIONAL BLOCK DIAGRAM
PIN CONFIGURATION
DG5041


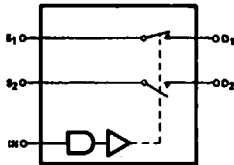
Two SPST Switches per Package*

Truth Table**

LOGIC	SWITCH
0	OFF
1	ON

Dual-In-Line Package


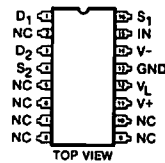
Order Numbers:
DG5041AK, DG5041CK,
DG5041CJ
See Package 8 or 10

DG5042


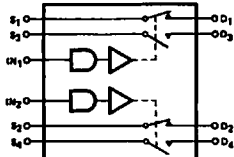
One SPDT Switch per Package*

Truth Table**

LOGIC	SW1	SW2
0	OFF	ON
1	ON	OFF

Dual-In-Line Package


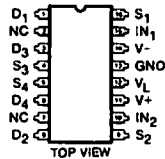
Order Numbers:
DG5042AK, DG5042CK,
DG5042CJ
See Package 8 or 10

DG5043


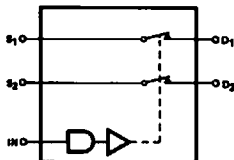
Two SPDT Switches per Package*

Truth Table**

LOGIC	SW1 SW2	SW3 SW4
0	OFF	ON
1	ON	OFF

Dual-In-Line Package


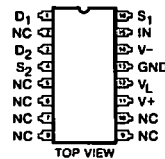
Order Numbers:
DG5043AK, DG5043CK,
DG5043CJ
See Package 8 or 10

DG5044


One DPST Switch per Package*

Truth Table**

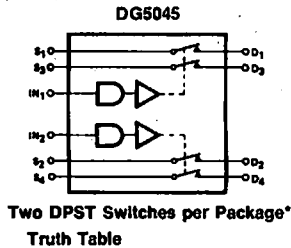
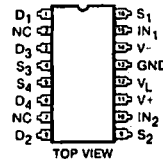
LOGIC	SWITCH
0	OFF
1	ON

Dual-In-Line Package


Order Numbers:
DG5044AK, DG5044CK,
DG5044CJ
See Package 8 or 10

*Switches Shown for Logic "1" Input

**Logic "0" ≤ 0.8 V, Logic "1" ≥ 2.0 V

FUNCTIONAL BLOCK DIAGRAM
PIN CONFIGURATION

Dual-In-Line Package


Order Numbers:
DG5045AK, DG5045CK,
DG5045CJ
See Package 8 or 10

*Switches Shown for Logic "1" Input

ABSOLUTE MAXIMUM RATINGS

Voltages Referenced to V-
V+ 44 V
V_L (GND -0.3 V) to 44 V
GND 25 V
Digital Inputs¹, V_S, V_D -2 V to (V+ +2 V) or 30 mA, whichever occurs first.
Current, Any Terminal Except S or D 30 mA
Continuous Current, S or D 30 mA
Peak Current, S or D 100 mA
(Pulsed at 1 msec, 10% duty cycle max)
Storage Temperature (A Suffix) -65 to 150°C
(C Suffix) -65 to 125°C

Operating Temperature (A Suffix) -55 to 125°C
(C Suffix) 0 to 70°C
Power Dissipation* 450 mW
Plastic DIP** 900 mW
16 Pin DIP***

*All leads welded or soldered to PC board.

**Derate 6 mW/°C above 75°C

***Derate 12 mW/°C above 75°C

ELECTRICAL CHARACTERISTICS²

T_A = 25°C

	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: V+ = 15 V, V- = -15 V, V _L = 5 V	LIMITS						UNIT
				DG5040-DG5045A			DG5040-DG5045C			
				MIN ³	TYP ⁴	MAX	MIN ³	TYP ⁴	MAX	
SWITCH	Analog Signal Range	V _{ANALOG}		-15		15	-15		15	V
	Drain-Source ON Resistance	r _{DS(on)}	V _D = 10 V, I _S = -10 mA			50			50	Ω
			V _D = -10 V, I _S = -10 mA			50			50	
	Source OFF Leakage Current	I _{S(off)}	V _{in} = 2.0 V or 0.8 V ⁵ V _S = 14 V, V _D = -14 V			1			1	
			V _S = -14 V, V _D = 14 V	-1		-1				
			V _S = -14 V, V _D = 14 V			1			1	
SWITCH	Drain OFF Leakage Current	I _{D(off)}	V _S = 14 V, V _D = -14 V	-1		-1				nA
			V _S = V _D = 14 V			2			2	
			V _S = V _D = -14 V	-2		-2				
INPUT	Input Current with Input Voltage High	I _{INH}	V _{in} = 2.0 V	-1		1	-1		1	μA
	Input Current with Input Voltage Low	I _{INL}	V _{in} = 0.8 V	-1		1	-1		1	
DYNAMIC	Turn-ON Time	t _{on}	V _S = ±10 V, R _L = 1 kΩ, C _L = 35 pF			1000			1200	ns
	Turn-OFF Time	t _{off}				500			700	
	Charge Injection	Q	C _L = 10,000 pF, V _{gen} = 0 V, R _{gen} = 0 Ω		3			3		pC
	Source OFF Capacitance	C _{S(off)}	V _S = V _D = 0 V, f = 1 MHz		15			15		pF
	Drain OFF Capacitance	C _{D(off)}			17			17		
	Channel ON Capacitance	C _D + S(on)			45			45		
	OFF Isolation		Z _L = 75 Ω, V _S = 2 V _{pp} , f = 1 MHz		75			75		dB
DYNAMIC	Crosstalk (Channel to Channel)				89			89		
SUPPLY	Positive Supply Current	I+	V _{in} = 0 V or 2.0 V			300			300	μA
	Negative Supply Current	I-		-300			-300			
	Logic Supply Current	I _L				300			300	
	Ground Current	I _{GND}		-300			-300			

NOTES:

(See next page)

ELECTRICAL CHARACTERISTICS² (Cont.)
 T_A = Over Temperature Range

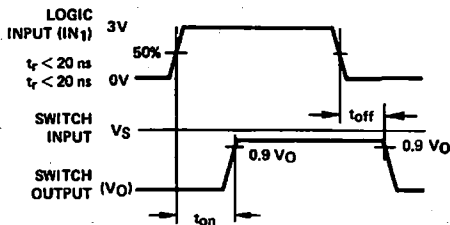
	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: V+ = 15 V, V- = -15 V, VL = 5 V	LIMITS						UNIT
				DG5040-DG5045A			DG5040-DG5045C			
				MIN ³	TYP ⁴	MAX	MIN ³	TYP ⁴	MAX	
SWITCH	Analog Signal Range	VANALOG		-15		15	-15		15	V
	Drain-Source ON Resistance	rOS(on)	VIN = 2.0 V or 0.8 V ⁵	VD = 10 V, IS = -10 mA		50		50	Ω	
		VD = -10 V, IS = -10 mA			50		50			
	Source OFF Leakage Current	IS(off)		VS = 14 V, VD = -14 V		1		1	nA	
		VS = -14 V, VD = 14 V		-1		-1				
	Drain OFF Leakage Current	ID(off)		VS = -14 V, VD = 14 V		1		1		
		VS = 14 V, VD = -14 V		-1		-1				
Drain ON Leakage Current ⁶	ID(on)	VS = VD = 14 V		2		2				
		VS = VD = -14 V	-2		-2					
INPUT	Input Current with Input Voltage High	IINH	VINH = 2.0 V	-1		1	-1		1	μA
	Input Current with Input Voltage Low	IINL	VINL = 0.8 V	-1		1	-1		1	

NOTES:

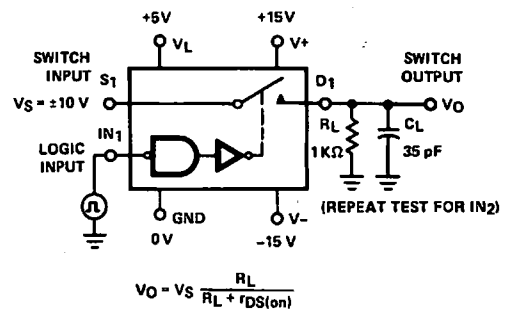
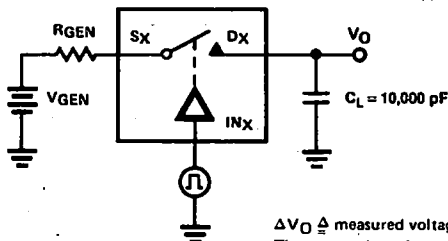
1. Signals on S_X , D_X , or IN_X exceeding V_+ or V_- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
2. Refer to PROCESS OPTION FLOWCHART for additional information.
3. The algebraic convention whereby the most negative value is a minimum, and the most positive is a maximum is used in this data sheet.
4. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
5. V_{in} = Input voltage to perform proper function.
6. $I_D(on)$ is leakage from driver into "ON" switch.

SWITCHING TIME TEST CIRCUIT

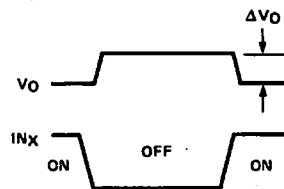
Switch output waveform shown for $V_S = \text{constant}$ with logic input waveform as shown. Note that V_S may be + or - as per switching time test circuit. V_O is the steady state output with switch on. Feedthrough via gate capacitance may result in spikes at leading and trailing edge of output waveform.



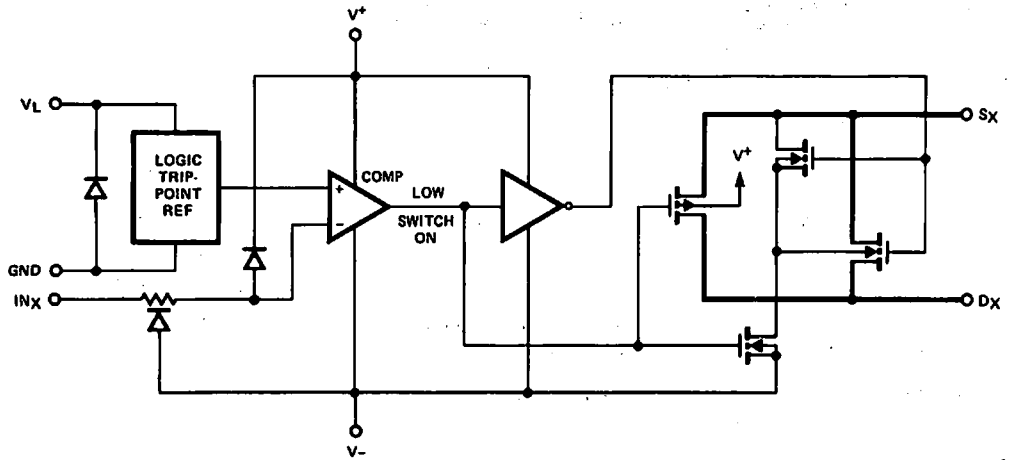
Note: Logic input waveform is inverted for switches that have the opposite logic sense control.


CHARGE INJECTION TEST CIRCUIT


$\Delta V_O \triangleq$ measured voltage error due to charge injection.
The error voltage in coulombs is $\Delta Q = C_L \times \Delta V_O$.



SCHEMATIC DIAGRAM (Typical Channel)





DG5140-DG5145

Low Power-High Speed CMOS Analog Switches

FEATURES

- ± 15 Volt Input Range
- ON Resistance $< 30 \Omega$
- Very Fast Switching Action
($t_{ON} < 100\text{ns}$)
($t_{OFF} < 75\text{ns}$)
- Ultra Low Power Requirements ($I_S \leq 1 \mu\text{A}$)
- TTL, CMOS Compatible

BENEFITS

- Available Normally Open or Closed
- Low Signal Errors
- Break-Before-Make Switching Action
- Battery Operation
- Simple Interfacing

APPLICATIONS

- High Performance Switching
- Sample and Hold Circuits
- Digital Filters

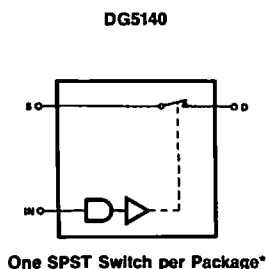
DESCRIPTION

The DG5140 family of solid state analog switches are built on the Siliconix proprietary high voltage silicon gate process to achieve high voltage rating and superior switch time ON/OFF performance. Key performance features of the 5140 series are break-before-make switching action to guarantee that an ON channel will be turned OFF before the OFF channel can turn on, ultra-low power supply requirements, and TTL and CMOS compatibility. Each switch conducts equally well in both directions when on and blocks up to 30 volts peak-to-peak when off. With switch OFF leakage less than 100pA and maximum power supply current of 1 μA (A Suffix), these switches are ideal for battery powered industrial and military applications.

There are six devices in this series, which are differentiated by the type of switch action as shown in the functional block diagrams. In all cases the switches are bidirectional and maintain almost constant ON resistance throughout their operating range.

Package options include the 16-pin plastic and ceramic DIP. Performance grades include 0 to 70°C, and -55 to 125°C.

FUNCTIONAL BLOCK DIAGRAM



Truth Table

LOGIC	SWITCH
0	OFF
1	ON

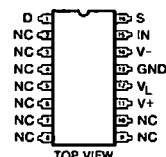
Logic "0" $\leq 0.8 \text{ V}$

Logic "1" $\geq 2.4 \text{ V}$

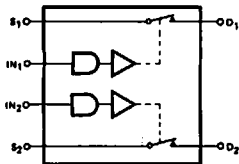
*Switches Shown for Logic "1" Input

PIN CONFIGURATION

Dual-In-Line Package



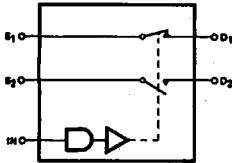
Order Numbers:
DG5140AK, DG5140CK,
DG5140CJ
See Package 8 or 10

FUNCTIONAL BLOCK DIAGRAM
PIN CONFIGURATION
DG5141


Two SPST Switches per Package*

Truth Table**

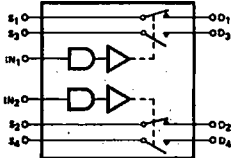
LOGIC	SWITCH
0	OFF
1	ON

DG5142


One SPDT Switch per Package*

Truth Table**

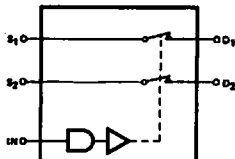
LOGIC	SW1	SW2
0	OFF	ON
1	ON	OFF

DG5143


Two SPDT Switches per Package*

Truth Table**

LOGIC	SW1 SW2	SW3 SW4
0	OFF	ON
1	ON	OFF

DG5144


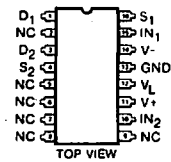
One DPST Switch per Package*

Truth Table**

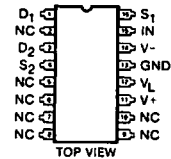
LOGIC	SWITCH
0	OFF
1	ON

*Switches Shown for Logic "1" Input

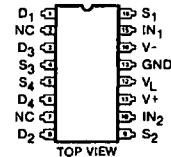
**Logic "0" ≤ 0.8 V, Logic "1" ≥ 2.4 V

Dual-In-Line Package


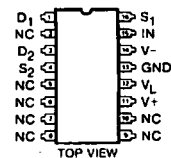
Order Numbers:
DG5141AK, DG5141CK,
DG5141CJ
See Package 8 or 10

Dual-In-Line Package


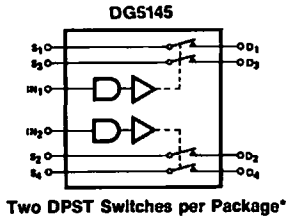
Order Numbers:
DG5142AK, DG5142CK,
DG5142CJ
See Package 8 or 10

Dual-In-Line Package


Order Numbers:
DG5143AK, DG5143CK,
DG5143CJ
See Package 8 or 10

Dual-In-Line Package


Order Numbers:
DG5144AK, DG5144CK,
DG5144CJ
See Package 8 or 10

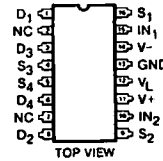
FUNCTIONAL BLOCK DIAGRAM

Truth Table

LOGIC	SWITCH
0	OFF
1	ON

Logic "0" ≤ 0.8 V

Logic "1" ≥ 2.4 V

*Switches Shown for Logic "1" Input

PIN CONFIGURATION
Dual-In-Line Package


Order Numbers:
DG5145AK, DG5145CK,
DG5145CJ
 See Package 8 or 10

ABSOLUTE MAXIMUM RATINGS

Voltages Referenced to V-

V+ 44 V

V_L (GND -0.3 V) to 44 V

GND 25 V

Digital Inputs¹ V_S, V_D -2 V to (V+ +2 V) or 30 mA, whichever occurs first.

Current, Any Terminal Except S or D 30 mA

Continuous Current, S or D 30 mA

Peak Current, S or D

(Pulsed at 1 msec, 10% duty cycle max) 100 mA

Storage Temperature (A Suffix) -65 to 150°C

(C Suffix) -65 to 125°C

Operating Temperature (A Suffix) -55 to 125°C

(C Suffix) 0 to 70°C

Power Dissipation (Package)*

Plastic DIP** 450 mW

16 Pin DIP*** 900 mW

*All leads welded or soldered to PC board.

**Derate 6 mW/°C above 75°C

***Derate 12 mW/°C above 75°C

ELECTRICAL CHARACTERISTICS²

T_A = 25°C

	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: V+ = 15 V, V- = -15 V, V _L = 5 V	LIMITS						UNIT
				DG5140-DG5145A			DG5140-DG5145C			
				MIN ³	TYP ⁴	MAX	MIN ³	TYP ⁴	MAX	
SWITCH	Analog Signal Range	V _{ANALOG}		-14		14	-14		14	V
	Drain-Source ON Resistance	r _{DS(on)}	I _S = -10 mA, V _{IN} = 0.8 V or 2.0 V ⁵			30			50	Ω
	Switch OFF Leakage Current	I _{S(off)} ⁺ I _{D(off)}	V _{IN} = 0.8 V or 2.0 V ⁵ V _S = 10 V, V _D = -10 V V _S = -10 V, V _D = 10 V			0.1			0.5	nA
	Switch ON Leakage Current	I _{D(on)} ⁺ I _{S(on)}	V _D = V _S = -10 V to 10 V V _{IN} = 0.8 V or V _{IN} = 2.0 V ⁵			0.1			0.5	
INPUT	Input Current with Input Voltage High	I _{INH}	V _{IN} = 2.4 V			1			1	μA
	Input Current with Input Voltage Low	I _{INL}	V _{IN} = 0.8 V			1			1	
DYNAMIC	Turn-ON Time	t _{on}	See Switching Time Test Circuit		100	200		150	300	ns
	Turn-OFF Time	t _{off}			75	125		125	150	
	Charge Injection	Q	C _L = 10,000 pF, V _{gen} = 0 V, R _{gen} = 0 Ω			100			150	pC
	OFF Isolation		R _L = 100 Ω, C _L ≤ 5 pF, f = 1 MHz			54			50	dB
	Crosstalk (Channel to Channel)		One Channel Off; Any Other Channel Switches			54			50	
SUPPLY	Positive Supply Current	I ₊	Switch Duty Cycle < 10%			1.0			10	μA
	Negative Supply Current	I ₋		-1.0			-1.0			
	Logic Supply Current	I _L				1.0			10	
	Ground Current	I _{GND}		-1.0			-10			

NOTES:

1. Signals on S_x, D_x, or IN_x exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
2. Refer to PROCESS OPTION FLOWCHART for additional information.
3. The algebraic convention whereby the most negative value is a minimum, and the most positive is a maximum is used in this data sheet.
4. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
5. V_{IN} = Input voltage to perform proper function.

ELECTRICAL CHARACTERISTICS² (Cont.) $T_A = \text{Over Temperature Range}$

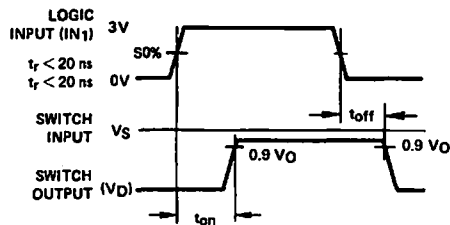
	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: V+ = 15 V, V- = -15 V, VL = 5 V	LIMITS						UNIT
				DG5140-DG5145A			DG5140-DG5145C			
				MIN ³	TYP ⁴	MAX	MIN ³	TYP ⁴	MAX	
SWITCH	Analog Signal Range	VANALOG		-14		14	-14		14	V
	Drain-Source ON Resistance	rDS(on)	IS = -10 mA, VIN = 0.8 V or 2.0 V ⁵			60			75	Ω
	Switch OFF Leakage Current	IS(off)+ ID(off)	VIN = 0.8 V or 2.0 V ⁵ VS = 10 V, VD = -10 V VS = -10 V, VD = 10 V			20			20	nA
	Switch ON Leakage Current	ID(on)+ IS(on)	VD = VS = -10 V to 10 V VIN = 0.8 V or VIN = 2.0 V ⁵			40			40	
INPUT	Input Current with Input Voltage High	IINH	VIN = 2.4 V			1			1	μA
	Input Current with Input Voltage Low	IINL	VIN = 0.8 V			1			1	

NOTES:

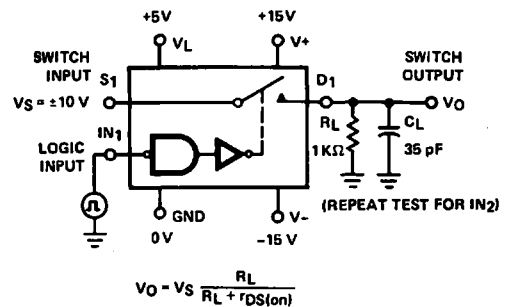
1. Signals on S_X , O_X , or IN_X exceeding V_+ or V_- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
2. Refer to **PROCESS OPTION FLOWCHART** for additional information.
3. The algebraic convention whereby the most negative value is a minimum, and the most positive is a maximum is used in this data sheet.
4. Typical values are for **DESIGN AID ONLY**, not guaranteed nor subject to production testing.
5. V_{IN} = Input voltage to perform proper function.

SWITCHING TIME TEST CIRCUIT

Switch output waveform shown for $V_S = \text{constant}$ with logic input waveform as shown. Note that V_S may be + or - as per switching time test circuit. V_O is the steady state output with switch on. Feedthrough via gate capacitance may result in spikes at leading and trailing edge of output waveform.



Note: Logic input waveform is inverted for switches that have the opposite logic sense control.





DG5240-DG5245

Low Power-High Speed Latched CMOS Analog Switches

FEATURES

- Latched Inputs
- Very Fast Switching Action
($t_{ON} < 100$ ns)
($t_{OFF} < 75$ ns)
- ON Resistance $< 30 \Omega$
- ± 15 Volt Input Range
- Ultra Low Power Requirements ($I_S \leq 1 \mu A$)

BENEFITS

- Microprocessor Compatible
- Break-Before-Make Switching Action
- Low Signal Error
- Options Include Normally Open or Closed Switches
- Battery Operation

APPLICATIONS

- High Performance Switching
- Sample and Hold Circuits
- Digital Filters

DESCRIPTION

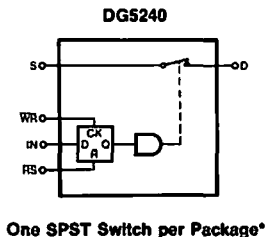
The DG5240 family of solid state analog switches feature latched inputs (to simplify interfacing with microprocessors), very fast switching action ($t_{ON} < 100$ ns), and less than $1 \mu A$ power supply current (A Suffix), making them ideally suited to precision applications in military and industrial control. Built on the Siliconix proprietary high voltage silicon gate process to achieve high voltage rating and superior switch time ON/OFF performance, the DG5240 series also features fast break-before-make switching action to guarantee that an ON channel will be turned OFF before the OFF channel can turn on, ON resistance less than 30Ω , and TTL and CMOS compatibility. Each switch conducts equally well in either direction when ON, and blocks up to 30 volts peak-to-peak when off.

The input data latches are updated when $\overline{WR}$ is set low. The $\overline{RS}$ pin is used to reset all switches in the circuit to the default value (all inputs low) when it is set low.

There are six devices in this series, which are differentiated by the type of switch action as shown in the configuration diagrams. In all cases the switches are bidirectional and maintain almost constant ON resistance throughout their operating range.

Package options include the 16-pin plastic and ceramic DIP, 16-lead flatpack, and the 10-pin metal can. Performance grades include 0 to $70^\circ C$, and -55 to $125^\circ C$.

FUNCTIONAL BLOCK DIAGRAM



Truth Table

LOGIC	SWITCH
0	OFF
1	ON

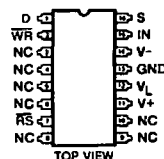
Logic "0" ≤ 0.8 V

Logic "1" ≥ 2.4 V

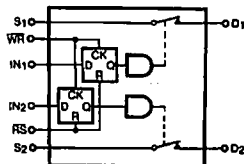
*Switches Shown for Logic "1" Input

PIN CONFIGURATION

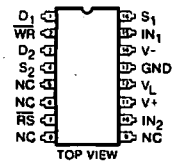
Dual-In-Line Package



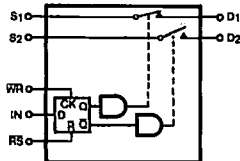
Order Numbers:
DG5240AK, DG5240CK,
DG5240CJ
See Package 8 or 10

FUNCTIONAL BLOCK DIAGRAM
PIN CONFIGURATION
DG5241

Two SPST Switches per Package*
Truth Table**

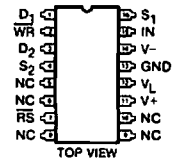
LOGIC	SWITCH
0	OFF
1	ON

Dual-In-Line Package


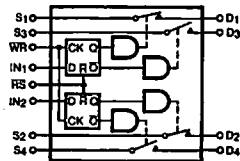
Order Numbers:
**DG5241AK, DG5241CK,
 DG5241CJ**
 See Package 8 or 10

DG5242

One SPDT Switch per Package*
Truth Table**

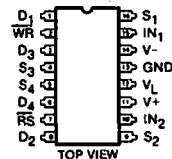
LOGIC	SW1	SW2
0	OFF	ON
1	ON	OFF

Dual-In-Line Package


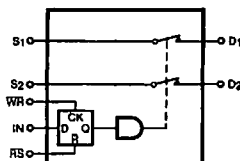
Order Numbers:
**DG5242AK, DG5242CK,
 DG5242CJ**
 See Package 8 or 10

DG5243

Two SPDT Switches per Package*
Truth Table**

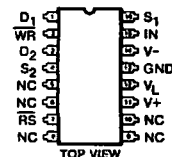
LOGIC	SW1 SW2	SW3 SW4
0	OFF	ON
1	ON	OFF

Dual-In-Line Package


Order Numbers:
**DG5243AK, DG5243CK,
 DG5243CJ**
 See Package 8 or 10

DG5244

One DPST Switch per Package*
Truth Table**

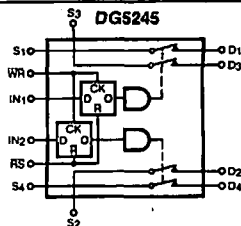
LOGIC	SWITCH
0	OFF
1	ON

Dual-In-Line Package


Order Numbers:
**DG5244AK, DG5244CK,
 DG5244CJ**
 See Package 8 or 10

*Switches Shown for Logic "1" Input

**Logic "0" ≤ 0.8 V, Logic "1" ≥ 2.4 V

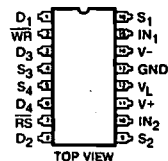
FUNCTIONAL BLOCK DIAGRAM

Two DPST Switches per Package*
Truth Table

LOGIC	SWITCH
0	OFF
1	ON

 Logic "0" ≤ 0.8 V

 Logic "1" ≥ 2.4 V

*Switches Shown for Logic "1" Input

PIN CONFIGURATION
Dual-In-Line Package


Order Numbers:
 DG5245AK, DG5245CK,
 DG5245CJ
 See Package 8 or 10

ABSOLUTE MAXIMUM RATINGS

Voltages Referenced to V-

V+ 44 V

V_L (GND -0.3 V) to 44 V

GND 25 V

 Digital Inputs¹ V_S, V_D -2 V to (V+ +2 V) or
 30 mA, whichever occurs first.

Current, Any Terminal Except S or D 30 mA

Continuous Current, S or D 30 mA

Peak Current, S or D

(Pulsed at 1 msec, 10% duty cycle max) 100 mA

Storage Temperature (A Suffix) -65 to 150°C

(C Suffix) -65 to 125°C

 Operating Temperature (A Suffix) -55 to 125°C
 (C Suffix) 0 to 70°C

Power Dissipation*

Plastic DIP** 450 mW

16 Pin DIP*** 900 mW

*All leads welded or soldered to PC board.

**Derate 6 mW/°C above 75°C

***Derate 12 mW/°C above 75°C

ELECTRICAL CHARACTERISTICS²

 T_A = 25°C

	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: V+ = 15 V, V- = -15 V, V _L = 5 V, V _{RS} = 5 V, V _{WR} = 0	LIMITS						UNIT
				DG5240-DG5245A			DG5240-DG5245C			
				MIN ³	TYP ⁴	MAX	MIN ³	TYP ⁴	MAX	
SWITCH	Analog Signal Range	V _{ANALOG}		-14		14	-14		14	V
	Drain-Source ON Resistance	r _{DS(on)}	I _S = -10 mA, V _{IN} = 0.8 V or 2.4 V ⁵			30			50	Ω
	Switch OFF Leakage Current	I _{S(off)} + I _{D(off)}	V _{IN} = 0.8 V or 2.4 V ⁵ V _S = 10 V, V _D = -10 V V _S = -10 V, V _D = 10 V			0.1 0.1			0.5 0.5	nA
	Switch ON Leakage Current	I _{D(on)} + I _{S(on)}	V _D = V _S = -10 V to 10 V			0.2			1	
INPUT	Input Current with Input Voltage High	I _{INH}	V _{IN} = 2.4 V			1			1	μA
	Input Current with Input Voltage Low	I _{INL}	V _{IN} = 0.8 V			1			1	
DYNAMIC	Turn-ON Time	t _{on}	See Switching Time Test Circuit		100	200		150	300	ns
	Turn-OFF Time	t _{off}			75	125		125	150	
	Charge Injection	Q	C _L = 10,000 pF, V _{gen} = 0 V, R _{gen} = 0 Ω			100			150	pC
	OFF Isolation		R _L = 100 Ω, C _L ≤ 5 pF, f = 1 MHz			54			50	dB
	Crosstalk (Channel to Channel)		One Channel Off; Any Other Channel Switches			54			50	
SUPPLY	Positive Supply Current	I+	Switch Duty Cycle < 10%			1.0			10	μA
	Negative Supply Current	I-		1.0			10			
	Logic Supply Current	I _L				1.0			10	
	Ground Current	I _{GND}		1.0			10			

NOTES:

1. Signals on S_x, D_x, or I_{Nx} exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
2. Refer to PROCESS OPTION FLOWCHART for additional information.
3. The algebraic convention whereby the most negative value is a minimum, and the most positive is a maximum is used in this data sheet.
4. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
5. V_{in} = Input voltage to perform proper function.

ELECTRICAL CHARACTERISTICS² (Cont.) $T_A = \text{Over Temperature Range}$

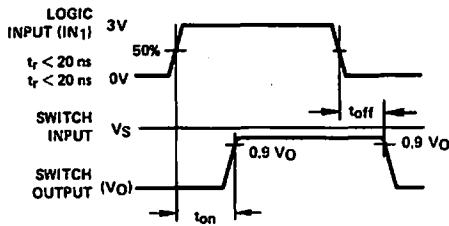
	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: V+ = 15 V, V- = -15 V, VL = 5 V, VRS = 5 V, VWR = 0	LIMITS						UNIT	
				DG5240-DG5245A			DG5240-DG5245C				
				MIN ³	TYP ⁴	MAX	MIN ³	TYP ⁴	MAX		
SWITCH	Analog Signal Range	VANALOG		-14		14	-14		14	V	
	Drain-Source ON Resistance	rDS(on)	IS = -10 mA, VIN = 0.8 V or 2.4 V ⁵	-55		80	75		125	Ω	
	Switch OFF Leakage Current	IS(off)+ ID(off)	VIN = 0.8 V or 2.4 V ⁵	VS = 10 V, VD = -10 V	0.1		20	0.5		20	nA
			VS = -10 V, VD = 10 V	0.1		20	0.5		20		
	Switch ON Leakage Current	IO(on)+ IS(on)	VD = VS = -10 V to 10 V	0.2		40	1		40		
INPUT	Input Current with Input Voltage High	IINH	Vin = 2.4 V			1			1	μA	
	Input Current with Input Voltage Low	IINL	Vin = 0.8 V			1			1		

NOTES:

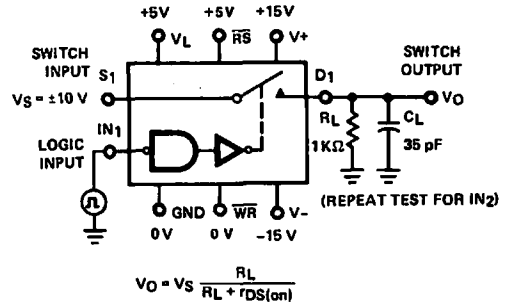
1. Signals on S_X , D_X , or IN_X exceeding V_+ or V_- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
2. Refer to PROCESS OPTION FLOWCHART for additional information.
3. The algebraic convention whereby the most negative value is a minimum, and the most positive is a maximum is used in this data sheet.
4. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
5. V_{in} = Input voltage to perform proper function.

SWITCHING TIME TEST CIRCUIT

Switch output waveform shown for $V_S = \text{constant}$ with logic input waveform as shown. Note that V_S may be + or - as per switching time test circuit. V_O is the steady state output with switch on. Feedthrough via gate capacitance may result in spikes at leading and trailing edge of output waveform.



Note: Logic input waveform is inverted for switches that have the opposite logic sense control.



Si3002

Monolithic SPDT MOS

Switch with Driver



FEATURES

- Internal Gate Protection Zener Diodes
- TTL and DTL Compatible Input

BENEFITS

- Reduces External Component Requirements
- Easily Interfaced

APPLICATIONS

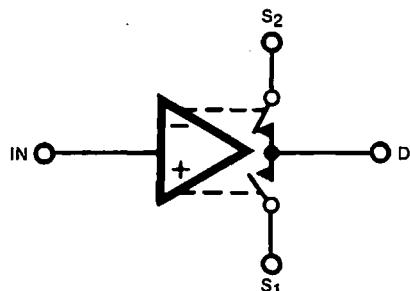
- Switching Analog Signals

DESCRIPTION

The Si3002 contains two P-channel MOS field-effect transistors designed to function as single-pole double-throw electronic switches. A level-shifting driver enables a low-level input (0.8 to 2 V) to control the ON-OFF state of the switches. In the ON state, each switch will conduct current equally well in either direction. In the OFF state the

switches will block voltages up to 20 V peak-to-peak. With logic "0" at the driver input, a common drain (D) is connected through an ON switch to source (S_1). With logic "1" at the input, "D" is connected to S_2 . Switch action is make-before-break.

FUNCTIONAL BLOCK DIAGRAM



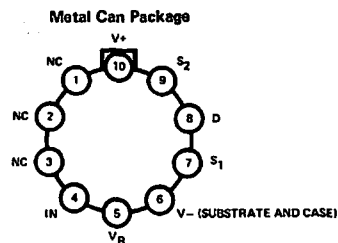
One SPDT Switch per Package*

Truth Table

LOGIC	SW 1	SW 2
0	ON	OFF
1	OFF	ON

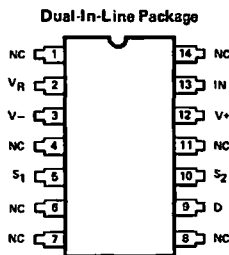
*Switch Shown for Logic "1" Input

PIN CONFIGURATION



TOP VIEW

Order Number:
SI3002AA
See Package 2



TOP VIEW

Order Numbers:
SI3002AP or SI3002BP
See Package 11

ABSOLUTE MAXIMUM RATINGS

V+ to V-	36 V
V+ to VS or VD	25 V
V+ to VR or VIN	12 V
VD to V-	36 V
VS to V-	36 V
VD to VS	±25 V
VIN to VR	±6 V
Current (Any Terminal)	30 mA
Storage Temperature	-65 to 150°C

Operating Temperature (A Suffix)	-55 to 125°C
(B Suffix)	-25 to 85°C
Power Dissipation (Package)*	
Metal Can**	450 mW
14 Pin DIP***	825 mW
*Device mounted with all leads soldered or welded to PC board.	
**Derate 6 mW/°C above 75°C	
***Derate 11 mW/°C above 75°C	

ELECTRICAL CHARACTERISTICS¹

TA = 25°C

	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: V+ = 10 V, V- = -20 V, VR = 0		LIMITS						UNIT
					SI3002A			SI3002B			
					MIN ²	TYP ³	MAX	MIN ²	TYP ³	MAX	
SWITCH	Analog Signal Range	VANALOG			-10		10	-10		10	V
	Drain-Source ON Resistance	rDS(on)	VD = 10 V	IS = -1 mA VINL = 0.8 V (Sw1 ON) VINH = 2.0 V (Sw2 ON)			100			100	Ω
			VD = 0 V				150			150	
			VD = -10 V				400			400	
	Source OFF Leakage Current	IS(off)	VS = -10 V, VD = 10 V	VINL = 0.8 V (Sw1 ON) VINH = 2.0 V (Sw2 ON)	-1			-5			nA
Channel ON Leakage Current	ID(on) + IS(on)	VD = -10 V, IS = 0	-2				-10				
INPUT	Input Current Voltage Low	IINL	VIN = 0 (Sw1 ON)		-0.8			-0.8			mA
	Input Current Voltage High	IINH	VIN = 5.5 (Sw2 ON)				0.1			0.1	μA
DYNAMIC	Turn-ON Time	ton	See Switching Time Test Circuit				1.0			1.0	μs
	Turn-OFF Time	toff					1.5			1.5	
	Source OFF Capacitance	CS(off)	VS = 0, f = 1 MHz			6			6		pF
SUPPLY	Positive Supply Current	I+	VIN = 0				3.0			3.5	mA
	Negative Supply Current	I-			-3.0			-3.0			
	Reference Supply Current	IR			-0.1			-0.1			
	Positive Supply Current	I+	VIN = 5 V				3.0			3.5	
	Negative Supply Current	I-			-3.0			-3.0			
	Reference Supply Current	IR			-1.5			-1.5			

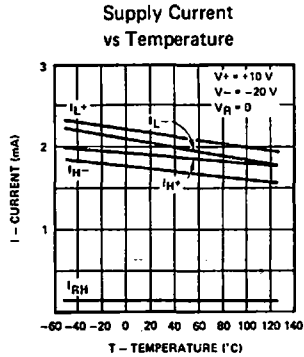
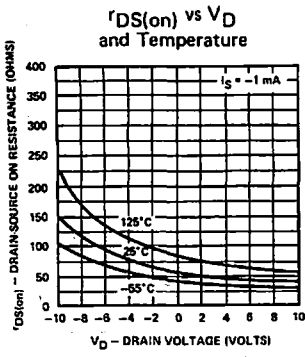
TA = Over Temperature Range

		SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: V+ = 10 V, V- = -20 V, VR = 0		LIMITS						UNIT
					SI3002A			SI3002B			
					MIN ²	TYP ³	MAX	MIN ²	TYP ³	MAX	
SWITCH	Analog Signal Range	V _{ANALOG}			-10		10	-10		10	V
	Drain-Source ON Resistance	r _{DS(on)}	V _D = 10 V	I _S = -1 mA			150			150	Ω
			V _D = 0 V	V _{INL} = 0.8 V (Sw ₁ ON)			250		250		
			V _D = -10 V	V _{INH} = 2.0 V (Sw ₂ ON)			500		500		
	Source OFF Leakage Current	I _{S(off)}	V _S = -10 V, V _D = 10 V	V _{INL} = 0.8 V (Sw ₁ ON)	-1000			-100			nA
Channel ON Leakage Current	I _{D(on)} + I _{S(on)}	V _D = -10 V, I _S = 0	V _{INH} = 2.0 V (Sw ₂ ON)	-2000			-200				
INPUT	Input Current Voltage Low	I _{iNL}	V _{IN} = 0 (Sw ₁ ON)		-1.0			-1.0			mA
	Input Current Voltage High	I _{iNH}	V _{IN} = 5.5 (Sw ₂ ON)				10			10	μA

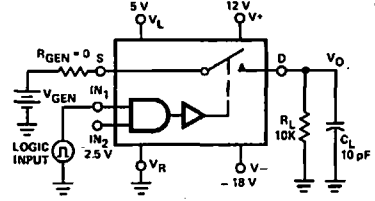
NOTES:

1. Refer to PROCESS OPTION FLOWCHART for additional information.
2. The algebraic convention whereby the most negative value is a minimum, and the most positive is a maximum, is used in this data sheet.
3. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

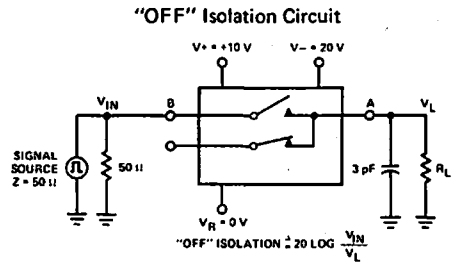
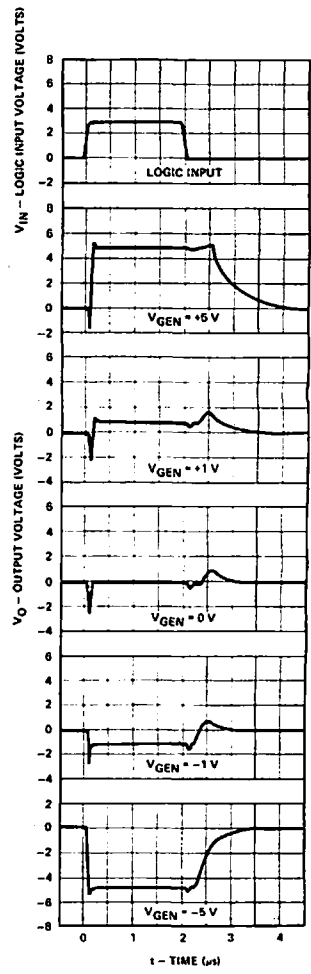
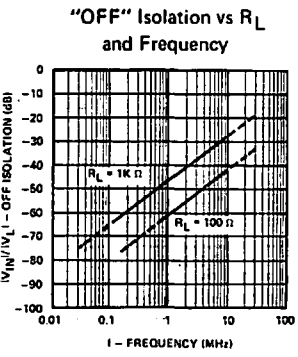
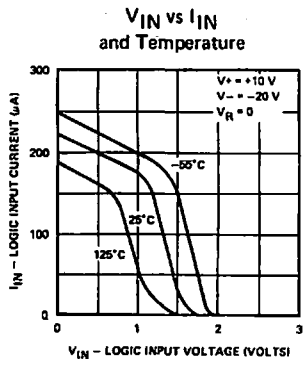
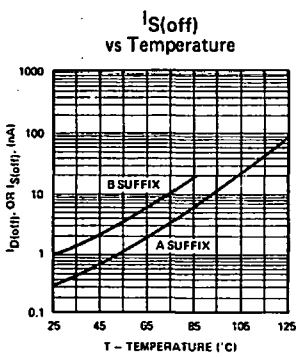
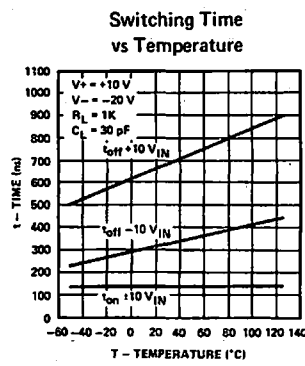
TYPICAL CHARACTERISTICS



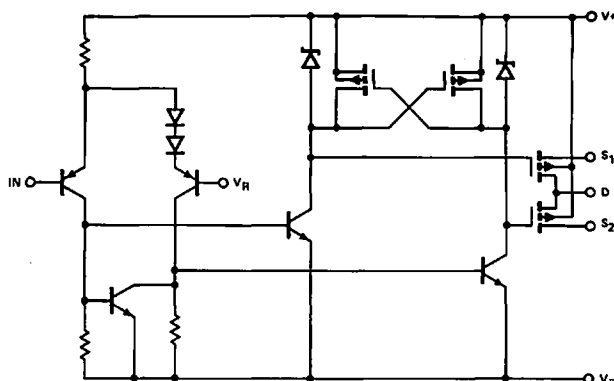
Typical delay, rise, fall, settling times, and switching transients in this circuit.



If R_{GEN} , R_L or C_L is increased, there will be proportional increases in rise and/or fall RC times.



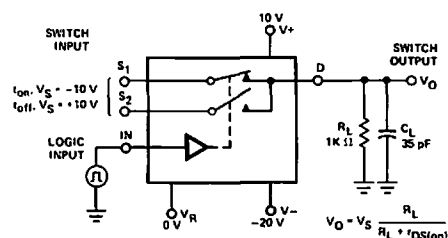
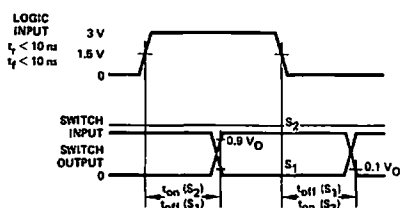
SCHEMATIC DIAGRAM



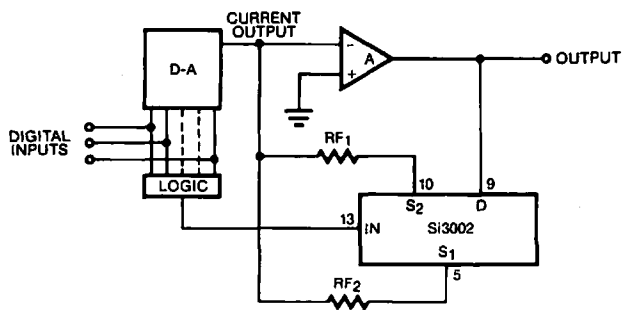
SWITCHING TIME TEST CIRCUIT

Switch output waveform shown for $V_S = \text{constant}$ with logic input waveform as shown. Note that V_S may be + or - as per switching time test circuit. V_O is the steady state

output with switch on. Feedthrough via gate capacitance may result in spikes at leading and trailing edge of output waveform.



APPLICATION



Inverting Auto-Ranging System

D125

Monolithic 6-Channel

FET Switch Drivers



FEATURES

- TTL Compatible
- DC Level Shifting to $>19\text{ V}$
- Fast Switching ($1.5\text{ }\mu\text{s}$) Turn Off Time

BENEFITS

- Reduces System Component Requirements

APPLICATIONS

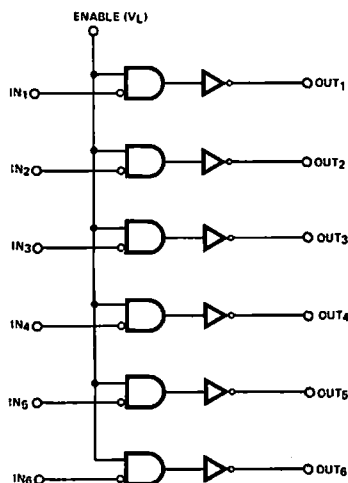
- Interfacing Low Level Logic to MOSFETs or JFETs
- Designed to Interface with G118 and G119 6-Channel Analog Switches

DESCRIPTION

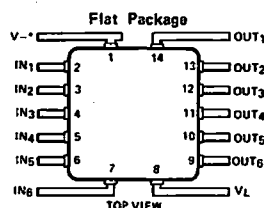
The D125 contains six drivers, designed to perform the level-shifting and amplification needed to interface low-level logic outputs and field-effect transistor switches (MOSFET or JFET). With the input logic supply, V_L , at 5 V, the driver output reference, V_- may be set between -1 and -25 V . Each output is designed to sink 5 mA of current in

the ON condition, and to hold off up to 30 V in the OFF condition. The input stage is a base-input PNP transistor, with the emitter returned to the V_L supply through a resistor. To turn the driver ON, the logic stage driving it must be capable of sinking 0.7 mA.

FUNCTIONAL BLOCK DIAGRAM

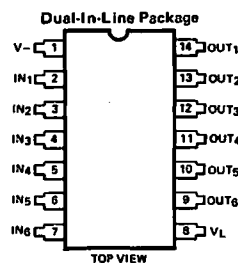


PIN CONFIGURATION



Order Number: D125AL
See Package 5

*Common to Substrate and Base of Package



Order Numbers:
D125AP Or D125BP
See Package 11

ABSOLUTE MAXIMUM RATINGS

V _O to V-	36 V	Power Dissipation*	
V _L to V-	30 V	Flat Package**	750 mW
V _{IN} to V-	30 V	14 Pin DIP***	825 mW
V _{IN} to V _L	±6 V		
Current (Any Terminal)	30 mA	*All leads soldered or welded to PC board.	
Storage Temperature	-65 to 150°C	**Derate 10 mW/°C above 75°C	
Operating Temperature (A Suffix)	-55 to 125°C	***Derate 11 mW/°C above 75°C	
(B Suffix)	-25 to 85°C		

ELECTRICAL CHARACTERISTICS¹

$$T_A = 25^\circ\text{C}$$

	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: V ⁻ = -20 V, V _L = 5 V	LIMITS						UNIT
				D125A			D125B			
				MIN ²	TYP ³	MAX	MIN ²	TYP ³	MAX	
OUTPUT	Output Voltage, Low	V _{OL}	I _O = 5 mA, V _L = 4.5 V V _{IN} = 0.5 V		-19.8	-19.6		-19.8	-19.6	V
	Output Current, High	I _{OH}	V _O = 10 V V _{IN} = 4.6 V		0.005	0.1		0.005	0.1	
INPUT	Input Current, Voltage High	I _{INH}	V _{IN} = 4.6 V	-1	0.001	1	-1	0.001	1	μA
	Input Current, Voltage Low	I _{INL}	V _{IN} = 0	-0.7	-0.15		-1	-0.2		
DYNAMIC	Turn-ON Time	t _{on}	See Switching Time Test Circuit		0.11	0.5		0.11	0.5	μs
	Turn-OFF Time	t _{off}			1.05	1.2		1.05	1.5	
SUPPLY	Negative Supply Current	I ⁻	V _{IN1} = 0 All Other V _{IN} = 4.6 V	-2.5	-1.5		-2.5	-1.5		mA
	Logic Supply Current	I _L			1.6	2.5		1.6	2.5	
	Negative Supply Current	I ⁻	All V _{IN} = 4.6 V	-2	-0.09		-2	-0.09		μA
	Logic Supply Current	I _L			0.09	1		0.09	2	

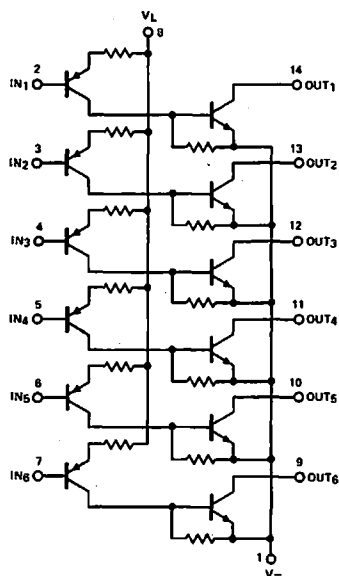
T_A = Over Temperature Range

	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: V- = -20 V, V _L = 5 V	LIMITS						UNIT
				D125A			D125B			
				MIN ²	TYP ³	MAX	MIN ²	TYP ³	MAX	
OUTPUT	Output Voltage, Low	V _{OL}	I _O = 5 mA, V _L = 4.5 V V _{IN} = 0.5 V			-19.6			-19.6	V
	Output Current, High	I _{OH}	V _O = 10 V V _{IN} = 4.6 V			10			10	μA
INPUT	Input Current, Voltage High	I _{INH}	V _{IN} = 4.6 V	-10		10	-20		20	μA
	Input Current, Voltage Low	I _{INL}	V _{IN} = 0	-0.7			-1			μA
SUPPLY	Negative Supply Current	I ₋	I _O = 0, V _{IN1} = 0 All Other V _{IN} = 4.6 V	-2.5			-2.5			mA
	Logic Supply Current	I _L				2.5			2.5	mA
	Negative Supply Current	I ₋	V _O = 10 V All V _{IN} = 4.6 V	-200			-100			μA
	Logic Supply Current	I _L				100			100	μA

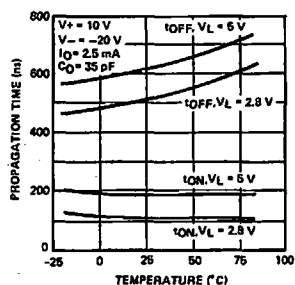
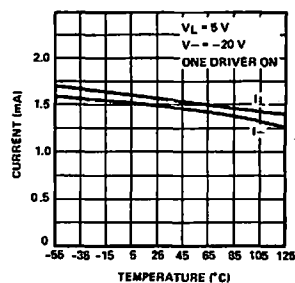
NOTES:

1. Refer to PROCESS OPTION FLOWCHART for additional information.
2. The algebraic convention whereby the most negative value is a minimum, and the most positive is a maximum, is used in this data sheet.
3. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

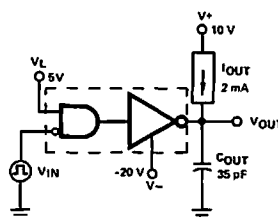
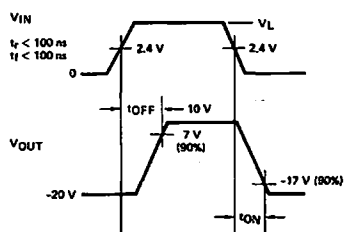
SCHEMATIC DIAGRAM



TYPICAL CHARACTERISTICS

Propagation vs
TemperatureSupply Current vs
Temperature

SWITCHING TIME TEST CIRCUIT



D129

4-Channel MOSFET Switch Driver with Decode



FEATURES

- TTL Compatible
- 4 Circuits on Chip
- Output Sink Current to 10 mA
- DC Level Shifts to >19 V

BENEFITS

- Reduces System Component Requirements

APPLICATIONS

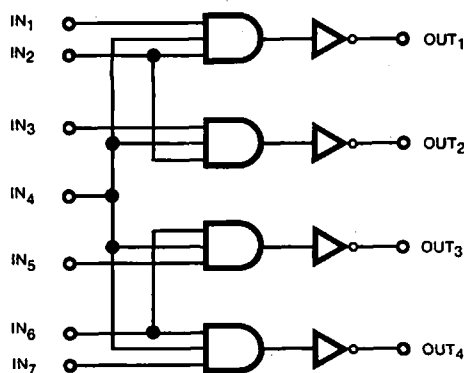
- Interfacing Low Level Logic to MOSFETs or JFETs
- Designed to Interface with G118 and G119

DESCRIPTION

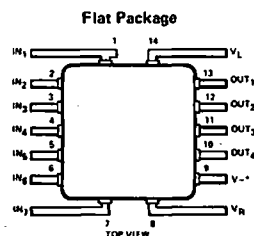
The D129 is a four-channel driver designed to provide the DC level-shifting and amplification functions needed to interface low-level logic outputs (0.7 to 2.2 V) and field-effect transistor switch inputs (up to 50 V peak-to-peak). With an input logic supply of 5 V, the output transistor emitter, V_- , may be set at any voltage between -5 and -30 V. In the ON state, the output collector will sink up to 10 mA of current, and in the OFF state will hold off voltages

up to 50 V above V_- . Each of the four drivers has a 3-input logic gate, with each of the inputs either open or at positive logic "1", the driver will be ON. With any of the inputs either grounded or at positive logic "0", the driver will be OFF. Some of the logic inputs to the four gates are internally connected to facilitate decoding from a binary counter; however, one input to each gate provides a means for independent operation of each driver, if desired.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION

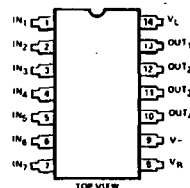


Order Number: D129AL

See Package 5

*Common to Substrate and Base of Package

Dual-In-Line Package



Order Numbers:

D129AP or D129BP

See Package 11

ABSOLUTE MAXIMUM RATINGS

V_O to V-(A Suffix)	50 V
V_O to V-(B Suffix)	36 V
V_R to V-(A Suffix)	33 V
V_R to V-(B Suffix)	24 V
V_L to V_R	8 V
V_{IN} to V_R	± 6 V
V_{IN} to V_{IN} (Any Other V_{IN} Terminals)	6 V
Current (Any Terminal)	30 mA
Storage Temperature	-65 to 150°C

Operating Temperature (A Suffix) -55 to 125°C
(B Suffix) -25 to 85°C

Power Dissipation*

Flat Package** 750 mW

14 Pin DIP*** 825 mW

*All leads soldered or welded to PC board.

**Derate 10 mW/°C above 75°C

***Derate 11 mW/°C above 75°C

ELECTRICAL CHARACTERISTICS¹ $T_A = 25^\circ\text{C}$

	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: $V_L = 5\text{ V}$, $V_- = -20\text{ V}$, $V_R = 0$		LIMITS						UNIT
					D129A			D129B			
					MIN ²	TYP ³	MAX	MIN ²	TYP ³	MAX	
OUTPUT	Output Voltage, Low	V_{OL}	$V_{IN} = 2.2\text{ V}$ $V_L = 4.5\text{ V}$	$I_{OUT} = 10\text{ mA}$ $I_{OUT} = 1\text{ mA}$		-19.8 -19.95	-19.3 -19.8		-19.7 	-19.25	V
	Output Current, High	I_{OH}	$V_O = 10\text{ V}$ $V_{IN} = 0.7\text{ V}$			0.005	0.1			0.2	
INPUT	Input Current, Voltage High	I_{INH}	$V_{IN} = 5\text{ V}$, Input Under Test $V_{IN} = 0$, All Other Inputs				0.25			1	μA
	Input Current, Voltage Low	I_{INL}	$V_{IN} = 0$, $V_L = 5.5\text{ V}$		-200	-0.2		-225			
DYNAMIC	Turn-ON Time	t_{on}	See Switching Time Test Circuit ($C_L = 35\text{ pF}$)			0.22	0.3			0.3	μs
	Turn-OFF Time	t_{off}				1.16	1.5			1.5	
SUPPLY	Negative Supply Current	I_-	$V_- = -20\text{ V}$ $V_L = 5.5\text{ V}$	One Channel "ON"	-2	-1.5		-2.25			mA
	Logic Supply Current	I_L				2.2	3			3.3	
	Negative Supply Current	I_-		All $V_{IN} = 0$ All Channels "OFF"	-10	-0.01		-25			μA
	Logic Supply Current	I_L				0.46	0.75			1	mA

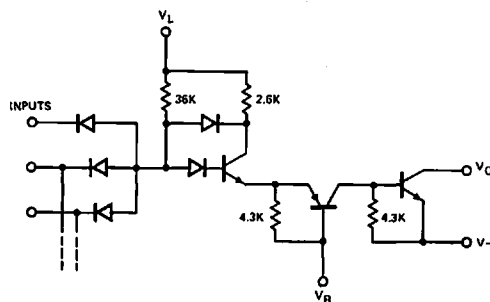
 $T_A = \text{Over Temperature Range}$

	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: $V_L = 5\text{ V}$, $V_- = -20\text{ V}$, $V_R = 0$		LIMITS						UNIT
					D129A			D129B			
					MIN ²	TYP ³	MAX	MIN ²	TYP ³	MAX	
OUTPUT	Output Voltage, Low	V_{OL}	$V_{IN} = 2.2\text{ V}$ $V_L = 4.5\text{ V}$	$I_{OUT} = 10\text{ mA}$ $I_{OUT} = 1\text{ mA}$	-19.3 -19.8			-19.25			V
	Output Current, High	I_{OH}	$V_O = 10\text{ V}$ $V_{IN} = 0.7\text{ V}$				20			10	
INPUT	Input Current, Voltage High	I_{INH}	$V_{IN} = 5\text{ V}$				5			5	μA
	Input Current, Voltage Low	I_{INL}	$V_{IN} = 0$, $V_L = 5.5\text{ V}$		-250			-250			
	Negative Supply Current	I_-			-1						mA

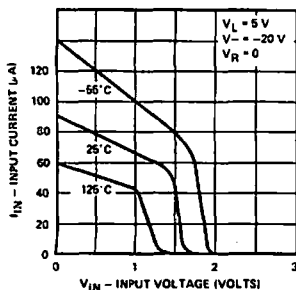
NOTES:

1. Refer to PROCESS OPTION FLOWCHART for additional information.
2. The algebraic convention whereby the most negative value is a minimum, and the most positive value is a maximum, is used in this data sheet.
3. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

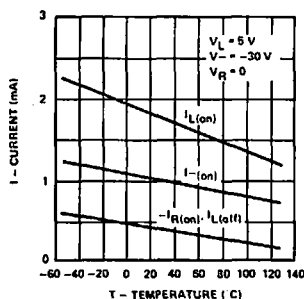
SCHEMATIC DIAGRAM



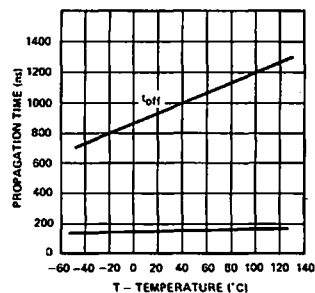
TYPICAL CHARACTERISTICS

 I_{IN} vs V_{IN} 

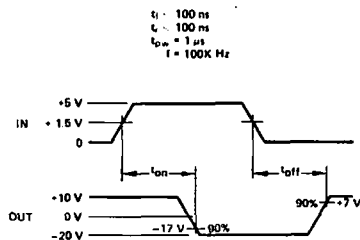
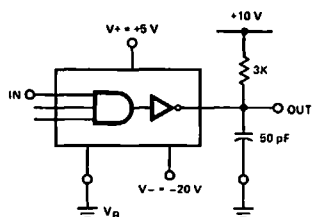
Current vs Temperature



Propagation Time vs Temperature



SWITCHING TIME AND TEST CIRCUIT



D139

Monolithic 2-Channel FET Switch Driver



FEATURES

- Complementary Outputs
- 150ns Propagation Time
- 30V Output Swing
- TTL, DTL, & RTL Compatible

BENEFITS

- Versatile
- Minimizes Switching Time
- Easily Interfaced

APPLICATIONS

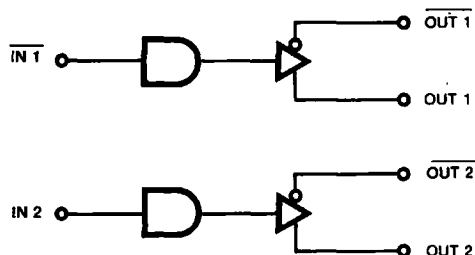
- Interfaces Low Level Signal to FET Switches
- TTL to CMOS
- TTL to PROM Logic Levels

DESCRIPTION

The D139 is a dual low level to high level voltage translator with complementary outputs. Uses include bipolar to MOS logic interface and bipolar logic to FET analog switch control. The following characteristics of the input circuit provide an ideal interface to the common logic forms TTL, CMOS, and DTL: light loading ($\approx 1/3$ TTL load) to "0" inputs, a 1.2 V trip point, and high input impedance with high breakdown to "1" inputs. The output can

drive up to 30 V peak-to-peak into pure capacitive loads or moderate resistive loads. Current source coupling between the input and output and split power supplies allow wide flexibility in the actual output voltage levels. Complementary outputs permit maximum application versatility, allowing functions such as double-throw analog switch control. A positive logic "1" at the input provides a "1" at OUT and a "0" at $\overline{\text{OUT}}$.

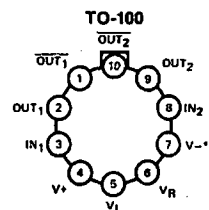
FUNCTIONAL BLOCK DIAGRAM



LOGIC	OUT	$\overline{\text{OUT}}$
0	V-	V+
1	V+	V-

Logic "0" ≤ 0.8 V
Logic "1" ≥ 2.0 V

PIN CONFIGURATION

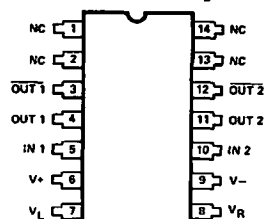


TOP VIEW

*COMMON TO SUBSTRATE AND CASE

Order Numbers
D139AA Or D139BA
See Package 2

Dual-In-Line Package



TOP VIEW

Order Numbers:
D139AP or D139BP
See Package 11
D139CJ
See Package 7

ABSOLUTE MAXIMUM RATINGS

V+ to V-	36 V
V+ to V _R	36 V
V+ to V _O	36 V
V _L to V _R	8 V
V _{IN} to V _R	8 V
V _R to V-	36 V
V _L to V-	36 V
V _O to V-	36 V
V _L to V _{IN}	8 V
Current (Any Terminal) DC	12 mA
Peak (Any Terminal)	100 mA
(200 μ s pulse width, 100 pps)	

Operating Temperature

(A Suffix)	-55 to 125°C
(B Suffix)	-25 to 85°C
(C Suffix)	0 to 70°C

Storage Temperature

(A & B Suffix)	-65 to 150°C
(C Suffix)	-65 to 125°C
Power Dissipation* (L Package)**	750 mW
(P Package)***	825 mW
(J Package)****	470 mW
Thermal Resistance (θ_{JA} , J Package)	0.16°C/mW

*All leads soldered or welded to PC board.

**Derate L package 10 mW/°C above 75°C

***Derate P package 11 mW/°C above 75°C

****Derate J package 6.5 mW/°C above 25°C

ELECTRICAL CHARACTERISTICS¹T_A = 25°C

	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: V ₊ = 10 V, V _L = 5 V, V ₋ = -20 V, V _R = 0		LIMITS						UNIT		
					D139A			D139B/C					
					MIN ²	TYP ³	MAX	MIN ²	TYP ³	MAX			
OUTPUT	Output Voltage, High (V ₊ to V _O)	V _{OH} /V _{OH}	V _{IH} = 2 V for V _{OH} /V _{OL} , V _{IL} = 0.8 V for V _{OH} /V _{OL}	I _{OUT} = -10 μA		0.6	0.9		0.6	0.9	V		
				I _{OUT} = -2 mA		0.82	1.5		0.82	1.5			
	Output Voltage, Low (V _O to V ₋)	V _{OL} /V _{OL}				I _{OUT} = 10 μA		0.52	1.1			0.52	1.1
				I _{OUT} = 2 mA		0.73	1.5		0.73	1.5			
INPUT	Input Current, Voltage High	I _{INH}	V _{IN} = 5 V			0.003	10		0.003	10	μA		
	Input Current, Voltage Low	I _{INL}	V _{IN} = 0		-500	-18.0		-500	-0.02				
DYNAMIC	Switching Time, Low To High, Delay Plus Rise Time	t ₍₊₎	See Switching Time Test Circuit (C _L = 35 pF)			65	170		65	170	ns		
	Switching Time, High To Low, Delay Plus Fall Time	t ₍₋₎				90	200		90	200			
SUPPLY	Positive Supply Current	I ₊	Input Voltage High Or Input Voltage Low			0.01	0.1		0.01	0.1	mA		
	Logic Supply Current	I _L				2.2	4		2.2	4			
	Negative Supply Current	I ₋			-3	-1.6		-3	-1.6				
	Reference Supply Current, Input Voltage High	I _{RH}	V _{IN1} = V _{IN2} = 5 V		-1.6	-0.66		-1.6	-0.66				
	Reference Supply Current, Input Voltage Low	I _{RL}	V _{IN1} = V _{IN2} = 0 V		1.1	-0.63		-1.1	-0.63				

NOTES

(See next page)

ELECTRICAL CHARACTERISTICS¹ (Cont.) T_A = Over Temperature Range

	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: V+ = 10 V, VL = 5 V, V- = -20 V, VR = 0		LIMITS						UNIT
					D139A			D139B/C			
					MIN ²	TYP ³	MAX	MIN ²	TYP ³	MAX	
OUTPUT	Output Voltage, High (V+ to VO)	VOH/VOH	VIH = 2 V for VOH/VOL, VIL = 0.8 V for VOH/VOL	IOUT = -10 μA			1.1			1.1	V
				IOUT = -2 mA			1.5			1.5	
	Output Voltage, Low (VO to V-)	VOL/VOL					1.3			1.3	
							1.5			1.5	
INPUT	Input Current, Voltage High	IINH	VIN = 5 V				20			20	μA
	Input Current, Voltage Low	IINL	VIN = 0		-600			-600			

NOTES:

1. All DC parameters are 100% tested at 25°C. Lots are sample-tested for AC parameters and high and low temperature limits to assure conformance with specifications.
2. The algebraic convention whereby the most negative value is a minimum, and the most positive value is a maximum, is used in this data sheet.
3. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

DRIVING PMOS ANALOG SWITCHES

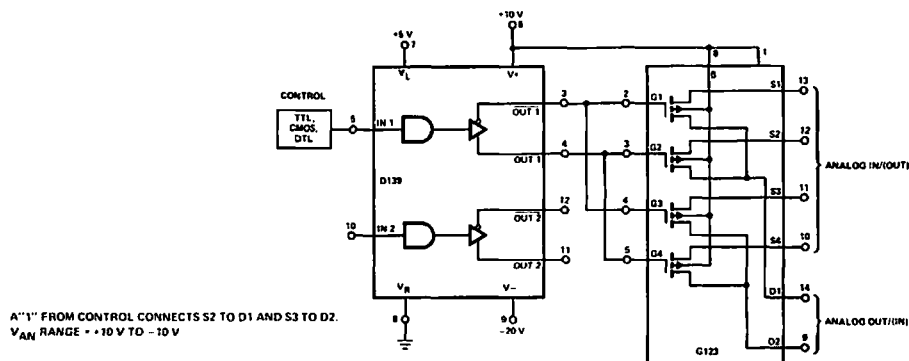


Figure 1
PMOS Interface Circuit

Driving PMOS Analog Switches. The D139 output swing is dictated by the analog signal range. V_{OH} is the PMOS "OFF" level and must equal the most positive analog voltage. V_{OL} is the PMOS "ON" level and must be 10 V more negative than the most negative analog voltage. Therefore for $V_{AN} = \pm 10\text{ V} \rightarrow +10\text{ V}$ and $V_- = -20\text{ V}$, PMOS control is make-before-break.

SCHEMATIC DIAGRAM

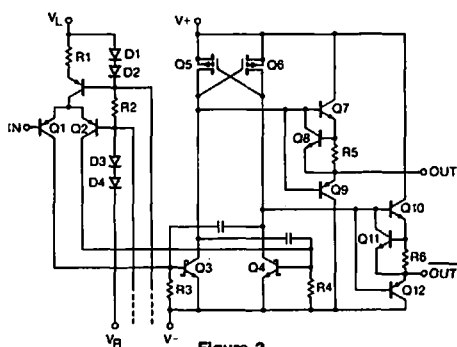


Figure 2

PMOS LOGIC INTERFACE

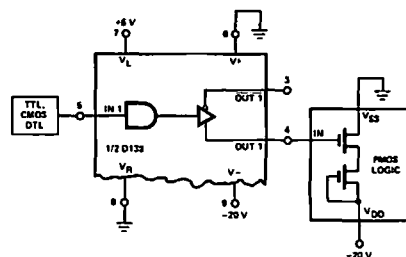
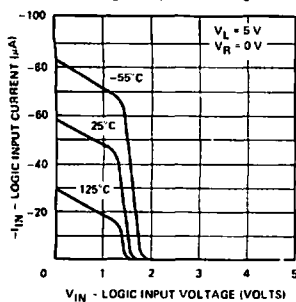
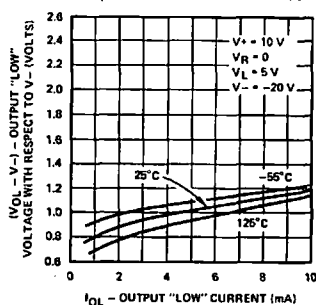


Figure 3

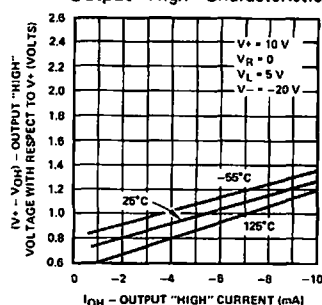
TYPICAL CHARACTERISTICS

Logic Input Current vs
Logic Input Voltage

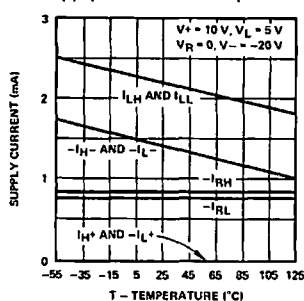
Output "Low" Characteristic



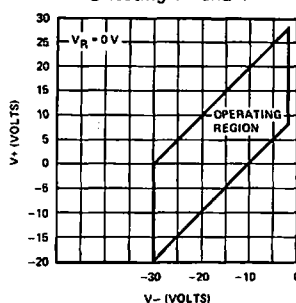
Output "High" Characteristic



Supply Current vs Temperature

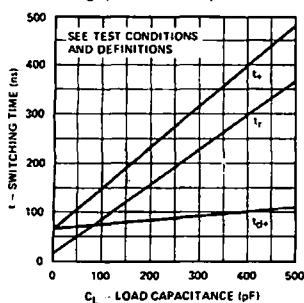
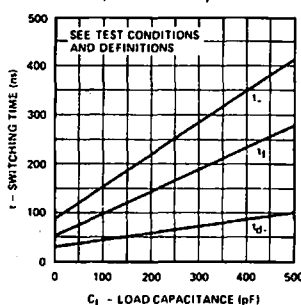


Selecting V+ and V-

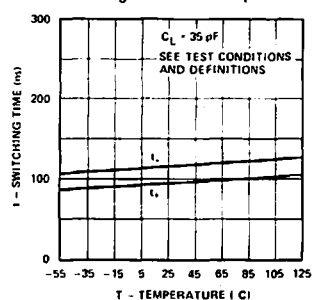


Selecting V+ and V-

The output swings between V_+ and V_- ($V_{OH} \cong V_+$ and $V_{OL} \cong V_-$). Select V_+ and V_- , within the operating region of curve at left, to provide the desired output swing. Note that V_- can be -2.0 V to -30 V and $V_+ - V_-$ must be at least 10 V.

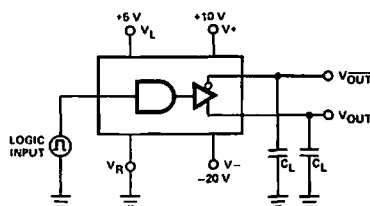
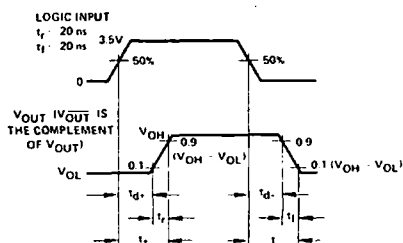
Switching Time, Low to
High, vs Load CapacitanceSwitching Time, High to
Low, vs Load Capacitance

Switching Time vs Temperature

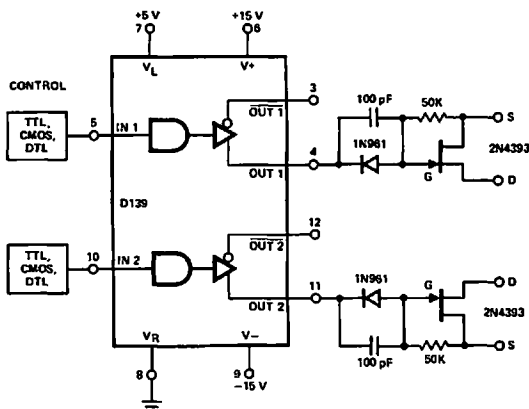


TEST CONDITIONS AND DEFINITIONS

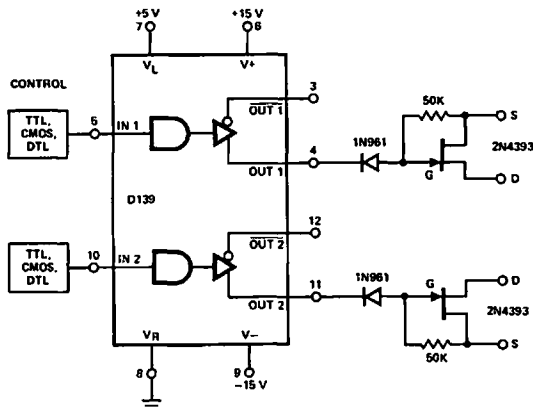
Switching Time Test Circuit



DRIVING NJFET ANALOG SWITCHES

Fast Dual SPST, NJFET, for
Low Frequency Signals (1)

THE 2N4393 WILL BE "ON" FOR A "1" FROM CONTROL.
 V_{AN} RANGE = +10 V TO -10 V.

Dual SPST, NJFET for High
Frequency Signals (1)

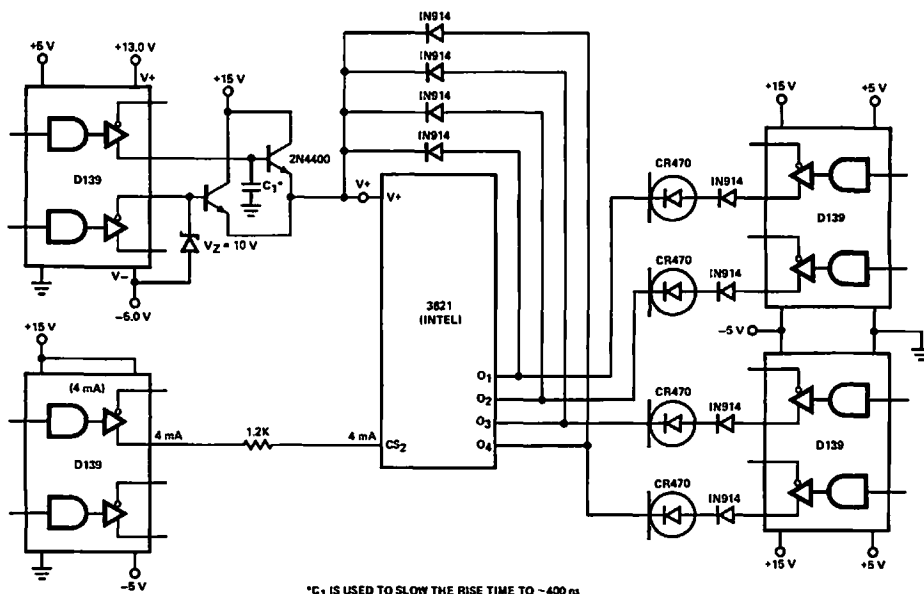
THE 2N4393 WILL BE "ON" FOR A "1" FROM CONTROL.
 V_{AN} RANGE = +10 V TO -10 V.

Figure 4

Driving NJFET Analog Switches. V_{OH} is the "ON" NJFET level and must be isolated from the gate by a series diode as shown above to prevent forward gate current. V_{OL} is the "OFF" NJFET level and must be more negative than the most negative analog signal voltage by $(|V_{GS(off)}| + 2 \text{ V})$. NJFET control is break-before-make.

(1) See Siliconix Application Note "Driver Circuits for the J-FET Analog Switch" AN73-5, August 1973.

APPLICATIONS



* C_1 IS USED TO SLOW THE RISE TIME TO ~400 ns

Figure 5
 D139 Used In Programming The Intel 3621 PROM

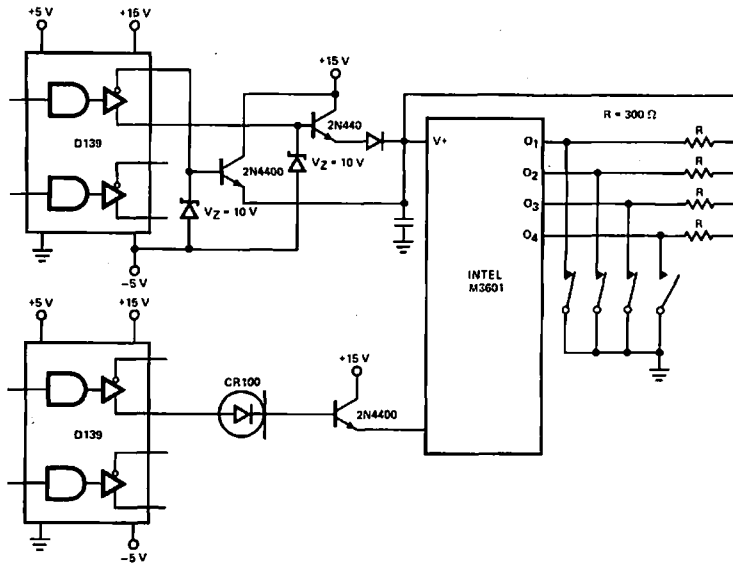


Figure 6
D139 Used In Programming The Intel 3601 PROM

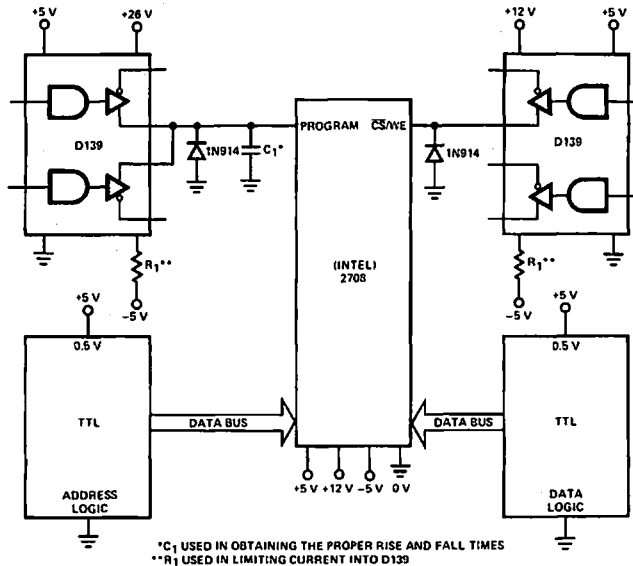


Figure 7
D139 Used In Programming The Intel 2708 PROM

D139 2-Channel Interface. The D139 may be used to interface 0.5 V TTL to CMOS Logic by setting V_L , V_R , $V+$ and $V-$ to the proper levels. If 0 to 5 V TTL levels are to be used to control the switch, V_L should be set to 5 V and V_R grounded.

$V+$ and $V-$ may be set to whatever levels are needed. The operating region of the D139 is determined by the graph of $V+$ vs $V-$.

Note. $V-$ must be at least 2 V below V_R in order for the D139 to operate. See the $V+$ vs $V-$ graph for selecting the supply voltages within the operating region.

G118

Monolithic 6-Channel Enhancement-Type MOSFET Switch



FEATURES

- Internal Zener Diode Protects the Gate
- Six Switches Per Chip

BENEFITS

- Reduces External Component Requirements

APPLICATIONS

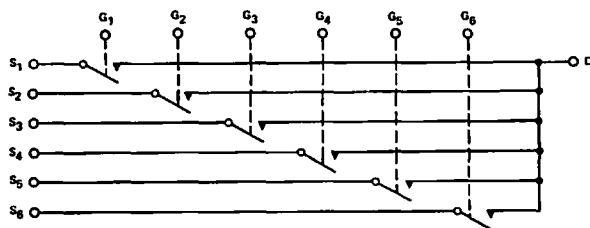
- Switching Analog Signals
- Multiplexing
- Designed to Operate with D125, D129 and D139

DESCRIPTION

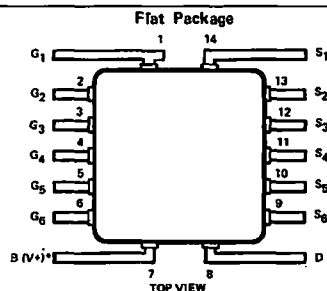
The G118 contains six enhancement-mode P-channel MOSFETs designed to function as analog switches. In the ON state each switch will conduct current equally well in either direction, and in the OFF state each switch will block voltages up to 20 V peak-to-peak. The switches are

integrated on a common substrate (body). They have a common drain terminal (D) which will function equally well as a common source; likewise, the source terminals will function as drains.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



TOP VIEW

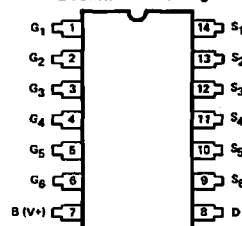
Order Number:

G118AL

See Package 5

*Common to Substrate and Base of Package

Dual-In-Line Package



TOP VIEW

Order Numbers:

G118AP or G118BP

See Package 11

ABSOLUTE MAXIMUM RATINGS

V_B to V_S	-2 to 30 V
V_B to V_D	-2 to 30 V
V_D to V_S	± 30 V
V_B to V_G	35 V
I_S , I_D	100 mA
I_G	5 mA
Storage Temperature	-65 to 150°C

Operating Temperature (A Suffix) -55 to 125°C
(B Suffix) -25 to 85°C

Power Dissipation*

Fiat Package** 750 mW
14 Pin DIP*** 825 mW

*All leads soldered or welded to PC board.

**Derate 10 mW/°C above 75°C.

***Derate 11 mW/°C above 75°C.

ELECTRICAL CHARACTERISTICS1

 $T_A = 25^\circ\text{C}$

	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: $V_{DB} = 0, V_{PB} = 0$			LIMITS						UNIT
						G118A			G118B			
STATIC	Drain-Source ON Resistance	$r_{DS(on)}$	$I_S = -1 \text{ mA}$	$V_{DB} = 0, V_{GD} = -30 \text{ V}$	MIN ²	TYP ³	MAX	MIN ²	TYP ³	MAX	Ω	
				$V_{DB} = -10 \text{ V}, V_{GD} = -20 \text{ V}$			100			125		
				$V_{DB} = -20 \text{ V}, V_{GD} = -10 \text{ V}$			200			250		
							450			500		
	Source OFF Leakage Currents	$I_S(off)$	$V_{SD} = -20 \text{ V}, V_{GD} = 0$	0.5			-5			nA		
	Drain OFF Leakage Currents	$I_D(off)$	$V_{DS} = -20 \text{ V}, V_{GD} = 0, V_{SB} = 0$	-3			-10					
	Gate-Channel Leakage Currents	I_{GSS}	$V_{GB} = -20 \text{ V}$	-0.5			-5					
	Gate-Source Threshold Voltage	$V_{GS(th)}$	$I_D = -10 \mu\text{A}, V_{DG} = 0, V_{SB} = 0$	-4		-1.5	-4		1.5			
	Drain-Source Breakdown Voltage	BV_{DSS}	$I_D = -50 \mu\text{A}, V_{GS} = 0, V_{SB} = 0$				-30			-30	V	
	Source-Drain Breakdown Voltage	BV_{SDS}	$I_S = -10 \mu\text{A}, V_{GD} = 0$				-30			-30		
Gate-Body Breakdown Voltage	BV_{GBS}	$I_G = -10 \mu\text{A}$	-90		-35	-90		-35				
DYNAMIC	Gate-Source Capacitance	C_{gs}	$V_{GB} = 0$ $f = 1 \text{ MHz}$	$V_{DB} = V_{SB} = 0,$ Body Guarded	Drain Guarded		0.9			0.9	pF	
	Gate-Drain Capacitance	C_{gd}			Source Guarded		0.9			0.9		
	Drain-Source OFF Capacitance	$C_{ds(off)}$			Gate Guarded		0.4			0.4		
	Source-Body Capacitance	C_{sb}			$V_{DB} = 0, V_{SB} = -5 \text{ V}$	Drain And Gate Guarded		2				2
	Drain-Body Capacitance	C_{db}			$V_{SB} = 0, V_{DB} = -5 \text{ V}$	Gate And Source Guarded		12				12

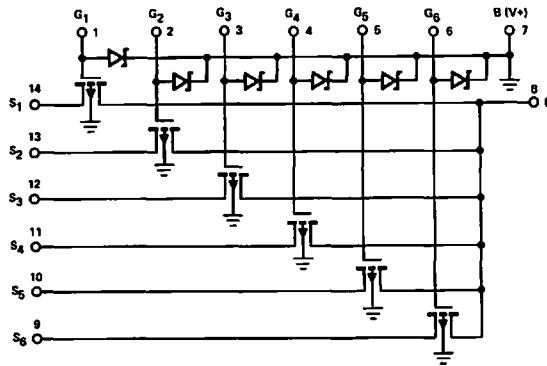
 $T_A = \text{Over Temperature Range}$

	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: $V_{DB} = 0, V_{PB} = 0$	LIMITS						UNIT
				G118A			G118B			
				MIN ²	TYP ³	MAX	MIN ²	TYP ³	MAX	
STATIC	Drain-Source ON Resistance	$r_{DS(on)}$	$I_S = -1 \text{ mA}$ $V_{DB} = 0, V_{GD} = -30 \text{ V}$$V_{DB} = -10 \text{ V}, V_{GD} = -20 \text{ V}$$V_{DB} = -20 \text{ V}, V_{GD} = -10 \text{ V}$			125			150	Ω
	Source OFF Leakage Current	$I_{S(off)}$	$V_{SD} = -20 \text{ V}, V_{GD} = 0$	-500			-500			nA
	Drain OFF Leakage Currents	$I_{D(off)}$	$V_{DS} = -20 \text{ V}, V_{GS} = 0, V_{SB} = 0$	-3000			-1000			nA
	Gate-Channel Leakage Currents	I_{GSS}	$V_{GB} = -20 \text{ V}$	-500			-500			nA
	Gate-Source Threshold Voltage	$V_{GS(th)}$	$I_D = -10 \mu\text{A}, V_{DG} = 0, V_{SB} = 0$	-4		-1.5	-4		1.5	V
	Drain-Source Breakdown Voltage	BV_{DSS}	$I_D = -50 \mu\text{A}, V_{GS} = 0, V_{SB} = 0$			-30			-30	V
	Source-Drain Breakdown Voltage	BV_{SDS}	$I_S = -10 \mu\text{A}, V_{GD} = 0$			-30			-30	V
	Gate-Body Breakdown Voltage	BV_{GBS}	$I_G = -10 \mu\text{A}$	-90		-35	-90		-35	V

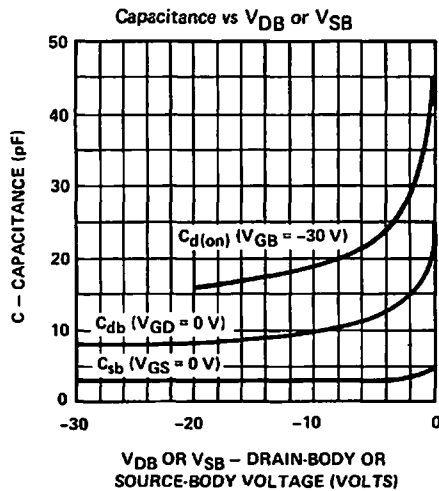
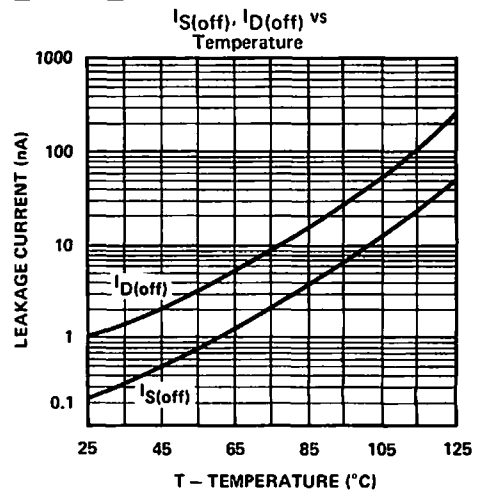
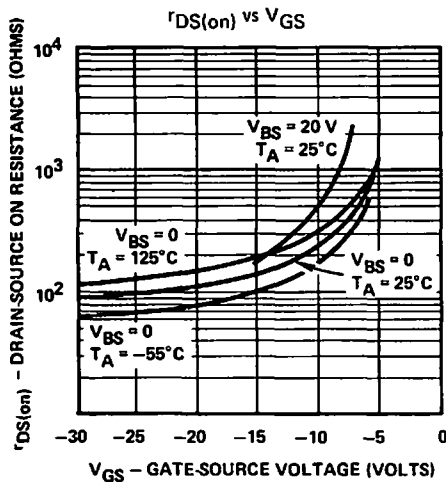
NOTES:

1. Refer to PROCESS OPTION FLOWCHART for additional information.
2. The algebraic convention whereby the most negative value is a minimum, and the most positive value is a maximum, is used in this data sheet.
3. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

SCHEMATIC DIAGRAM



TYPICAL CHARACTERISTICS



G119

Monolithic 6-Channel Enhancement-Type MOSFET Switch



FEATURES

- Integrated MOSFET for Each Gate to Provide "Pull-Up" Current for Gate-Driver Circuit
- Internal Zener Diode Protects the Gate
- Six Switches Per Chip
- Low $R_{DS(on)}$ (100 Ω)

BENEFITS

- Reduces External Component Requirements

APPLICATIONS

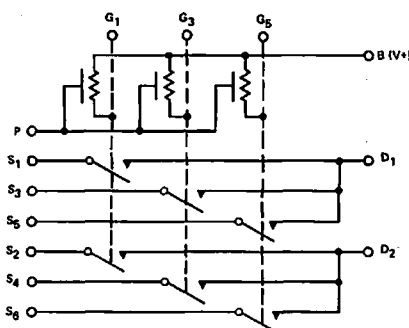
- Differential Input Analog Signal Switching
- Multiplexing
- Designed to Operate with D125, D129 and D139

DESCRIPTION

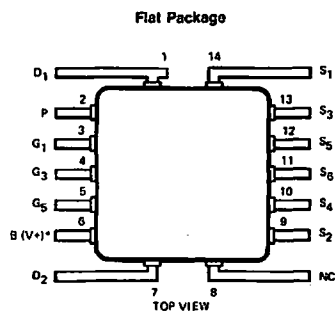
The G119 contains six enhancement-mode P-channel MOSFETs designed to function as analog switches. In the ON state each switch will conduct current equally well in either direction, and in the OFF state each switch will block voltages up to 30 V peak-to-peak. The switches are integrated onto a silicon substrate (body) and are internally connected into two groups of three switches per group. This arrangement facilitates the switching or multiplexing of differential analog signals. Each group has a

common drain terminal (D_1 and D_2) which will function equally well as a common source. Each gate terminal (G) controls a pair of switches and is provided with a normally-OFF "pull-up" MOSFET which may be turned ON to provide a current source to the gate-driving circuit. The pull-ups are turned ON or OFF by connecting the "P" terminal to a negative supply or to the "B" terminal respectively.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



Order Numbers:
G119AL or G119BL
See Package 5

*Common to Substrate and Base of Package

ABSOLUTE MAXIMUM RATINGS

V_B to V_S	-2 to 30 V
V_B to V_D	-2 to 30 V
V_D to V_S	± 30 V
V_B to V_G , V_B to V_P	35 V
I_S , I_D	100 mA
I_G	5 mA
I_P	100 μ A

Storage Temperature	-65 to 150°C
Operating Temperature (A Suffix)	-55 to 125°C
(B Suffix)	-25 to 85°C
Power Dissipation*	750 mW
*All leads soldered or welded to PC board. Derate 10 mW/°C above 75°C.	

ELECTRICAL CHARACTERISTICS¹ $T_A = 25^\circ\text{C}$

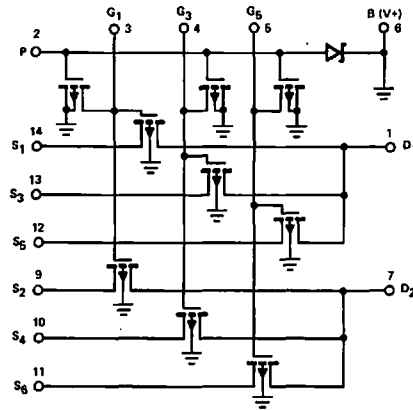
			TEST CONDITIONS UNLESS OTHERWISE NOTED: $V_{DB} = 0, V_{PB} = 0$		LIMITS						UNIT
PARAMETER	SYMBOL				G119A			G119B			
					MIN ²	TYP ³	MAX	MIN ²	TYP ³	MAX	
STATIC	Drain-Source ON Resistance	$r_{DS(on)}$	$I_S = -1 \text{ mA}$	$V_{DB} = 0, V_{GD} = -30 \text{ V}$ $V_{DB} = -10 \text{ V}, V_{GD} = -20 \text{ V}$ $V_{DB} = -20 \text{ V}, V_{GD} = -10 \text{ V}$			100 200 450			125 250 500	Ω
	Source OFF Leakage Currents	$I_{S(off)}$	$V_{SD} = -20 \text{ V}, V_{GD} = 0$		-0.5			-5			nA
	Drain OFF Leakage Currents	$I_{D(off)}$	$V_{DS} = -20 \text{ V}, V_{GD} = 0, V_{SB} = 0$		-1.5			-10			nA
	Gate ON Currents	$I_{G(on)}$	$V_{GB} = -30 \text{ V}, V_{PB} = -30 \text{ V}$		-2.4		-0.8	-2.4		-0.8	mA
	Gate-Channel Leakage Currents	I_{GSS}	$V_{GB} = -20 \text{ V}$		-0.5			-5			nA
	Gate-Source Threshold Voltage	$V_{GS(th)}$	$I_D = -10 \mu\text{A}, V_{DG} = 0, V_{SB} = 0$		-4		-1.5	-4		-1.5	V
	Drain-Source Breakdown Voltage	BV_{DSS}	$I_D = -50 \mu\text{A}, V_{GS} = 0, V_{SB} = 0$				-30			-30	V
	Source-Drain Breakdown Voltage	BV_{SDS}	$I_S = -10 \mu\text{A}, V_{GD} = 0$				-30			-30	V
	Gate-Body Breakdown Voltage	BV_{GBS}	$I_G = -10 \mu\text{A}$		-90		-35	-90		-35	V
	Pull-Up Gate-Body Breakdown Voltage	BV_{PBS}	$I_P = -10 \mu\text{A}, V_{GB} = 0$		-90		-35	-90		-35	V
DYNAMIC	Gate-Source Capacitance	C_{gs}	$V_{GB} = 0$ $f = 1 \text{ MHz}$	$V_{DB} = V_{SB} = 0$, Body Guarded	Drain Guarded		1.8			1.8	pF
	Gate-Drain Capacitance	C_{gd}			Source Guarded		1.8			1.8	
	Drain-Source OFF Capacitance	$C_{ds(off)}$			Gate Guarded		0.4			0.4	
	Source-Body Capacitance	C_{sb}	$V_{DB} = 0, V_{SB} = -5 \text{ V}$	Drain And Gate Guarded		2			2		
	Drain-Body Capacitance	C_{db}	$V_{SB} = 0, V_{DB} = -5 \text{ V}$	Gate And Source Guarded		6			6		

 $T_A = \text{Over Temperature Range}$

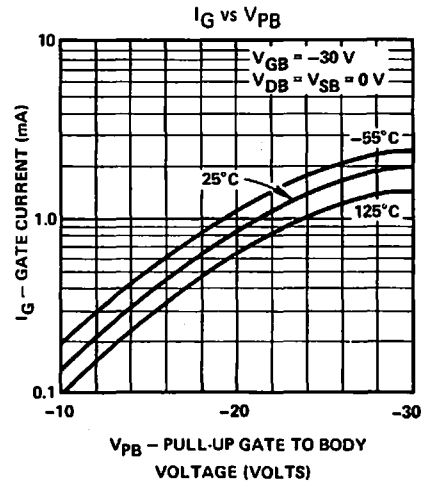
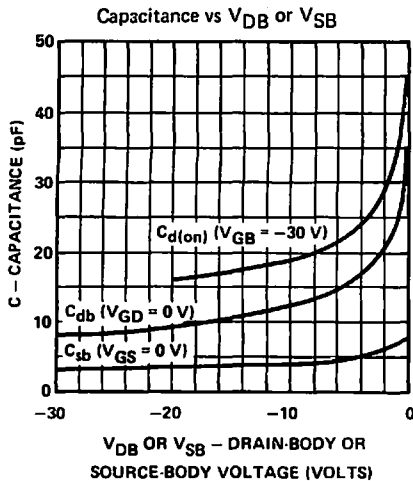
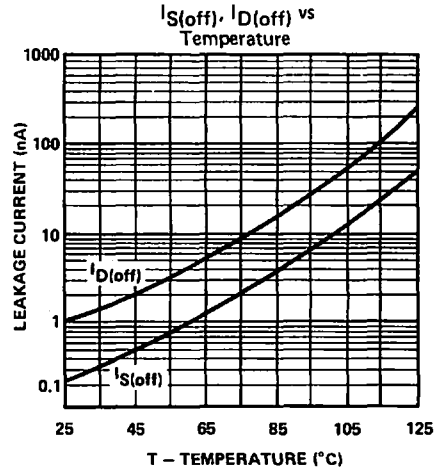
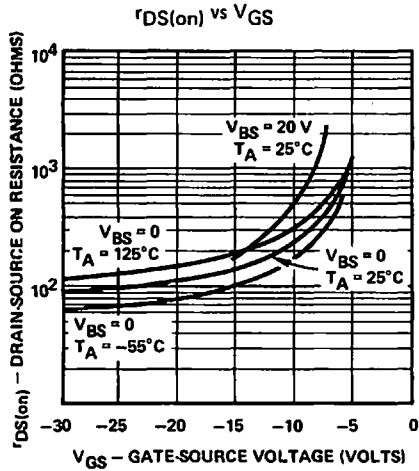
	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: $V_{DB} = 0, V_{PB} = 0$	LIMITS						UNIT
				G119A			G119B			
				MIN ²	TYP ³	MAX	MIN ²	TYP ³	MAX	
STATIC	Drain-Source ON Resistance	$r_{DS(on)}$	$I_S = -1\text{ mA}$ $V_{DB} = 0, V_{GD} = -30\text{ V}$ $V_{DB} = -10\text{ V}, V_{GD} = -20\text{ V}$ $V_{DB} = -20\text{ V}, V_{GD} = -10\text{ V}$			125 250 600			150 300 600	Ω
	Source OFF Leakage Currents	$I_{S(off)}$	$V_{SD} = -20\text{ V}, V_{GD} = 0$	-500			-500			nA
	Drain OFF Leakage Currents	$I_{D(off)}$	$V_{DS} = -20\text{ V}, V_{GS} = 0, V_{SB} = 0$	-150u			-1000			nA
	Gate-Channel Leakage Currents	I_{GSS}	$V_{GB} = -20\text{ V}$	-500			-500			nA
	Gate-Source Threshold Voltage	$V_{GS(th)}$	$I_D = -10\text{ }\mu\text{A}, V_{DG} = 0, V_{SB} = 0$	-4		-1.5	-4		-1.5	V
	Drain-Source Breakdown Voltage	BV_{DSS}	$I_D = -50\text{ }\mu\text{A}, V_{GS} = 0, V_{SB} = 0$			-30			-30	V
	Source-Drain Breakdown Voltage	BV_{SDS}	$I_S = -10\text{ }\mu\text{A}, V_{GD} = 0$			-30			-30	V
	Gate-Body Breakdown Voltage	BV_{GBS}	$I_G = -10\text{ }\mu\text{A}$	-90		-35	-90		-35	V
	Pull-Up Gate-Body Breakdown Voltage	BV_{PBS}	$I_P = -10\text{ }\mu\text{A}, V_{GB} = 0$	-90		-35	-90		-35	V

NOTES:

1. Refer to PROCESS OPTION FLOWCHART for additional information
2. The algebraic convention whereby the most negative value is a minimum, and the most positive value is a maximum, is used in this data sheet.
3. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.



TYPICAL CHARACTERISTICS



SD5000/SD5001/SD5002

DMOS FET Quad

Analog Switch Arrays



FEATURES

- Low "ON" Resistance
- Low Input Capacitance
- Low Output Capacitance
- Low Feedback Capacitance
- High Channel-to-Channel Isolation

BENEFITS

- "OFF" Isolation of -107 dB
- Low Insertion Loss
- Glitch Free Signals
- Fast Switching

APPLICATIONS

- Audio Switching
- Video Switching
- Sample/Hold
- Choppers
- Crosspoint Switches

DESCRIPTION

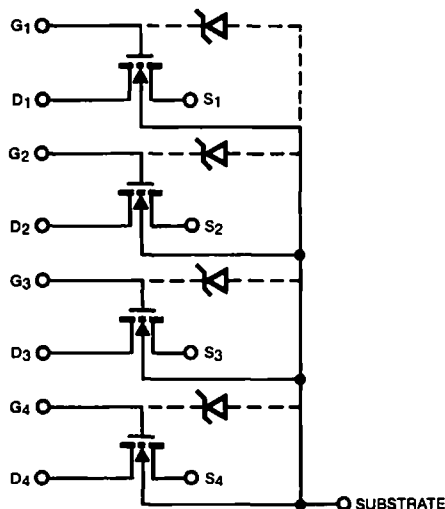
The Siliconix SD5000 series is a monolithic array of single-pole, single-throw analog switches designed for high speed switching in audio, video, and high frequency applications in communications, instrumentation, and process control. Designed on the Siliconix DMOS process, the SD5000 is rated for analog signals of ± 10 V, while the SD5001 and SD5002 are rated for ± 5 V and ± 7.5 V respectively.

These bidirectional switches feature very low interelectrode capacitance and ON resistance to achieve low

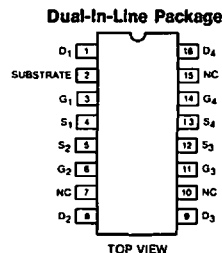
insertion loss, crosstalk, and feedthrough performance. The threshold voltage for all switches is 2 V maximum, simplifying driver requirements for low level signal applications.

The SD5000 family is available in 16-pin plastic and side braze dual-in-line packages, and is rated for operation over the 0 to 85°C temperature range.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



Order Part Numbers:
SD5000I, SD5001I, SD5002I
See Package 8
SD5000N, SD5001N, SD5002N
See Package 12

ABSOLUTE MAXIMUM RATINGS

	SD5000	SD5001	SD5002	I_D	50 mA
V_{DS}	20 V	10 V	15 V	Operating Temperature	0 to 85°C
V_{SD}^1	20 V	10 V	15 V	Storage Temperature	-55 to 150°C
V_{DB}	25 V	15 V	22.5 V	Power Dissipation (Package) ²	640 mW
V_{SB}	25 V	15 V	22.5 V	(Each Device)	300 mW
V_{GS}	30/-25 V	25/-15 V	30/-22.5 V		
V_{GB}	30/-0.3 V	25/-0.3 V	30/-0.3 V		
V_{GD}	30/-25 V	25/-15 V	30/-22.5 V		

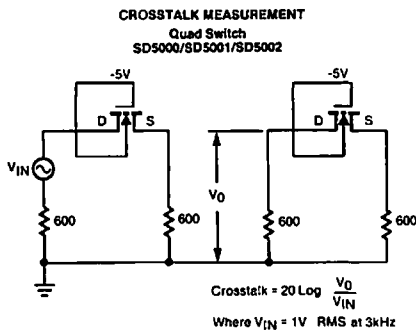
ELECTRICAL CHARACTERISTICS³ $T_A = 25^\circ\text{C}$

PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED:	LIMITS									UNIT
			SD5000			SD5001			SD5002			
			MIN ⁴	TYP ⁵	MAX	MIN ⁴	TYP ⁵	MAX	MIN ⁴	TYP ⁵	MAX	
Analog Signal Range	V _{ANALOG}		-10		10	-5		5	-7.5		7.5	
Drain-Source Breakdown Voltage	BV _{DS}	V _{GS} = V _{BS} = -5 V, I _D = 10 nA	20	25		10	25		15	25		V
Source-Drain Breakdown Voltage	BV _{SD}	V _{GD} = V _{BD} = -5 V, I _S = 10 nA	20			10			15			
Drain-Substrate Breakdown Voltage	BV _{DB}	V _{GB} = 0 V, I _D = 10 nA, Source Open	25			15			22.5			
Source-Substrate Breakdown Voltage	BV _{SB}	V _{GB} = 0 V, I _S = 10 μA, Drain Open	25			15			22.5			
Drain-Source Leakage Current	I _{DS(off)}	V _{GS} = V _{BS} = -5 V	V _{DS} = 20 V		1	10						
			V _{DS} = 10 V				1	10				
			V _{DS} = 15 V						1	10		
Source-Drain Leakage Current	I _{SD(off)}	V _{GD} = V _{BD} = -5 V	V _{SD} = 20 V		1	10						
			V _{SD} = 10 V				1	10				
			V _{SD} = 15 V							1	10	
Gate Leakage Current	I _{GBS}	V _{DB} = V _{SB} = 0 V	V _{GB} = 30 V		1							
			V _{GB} = 25 V					1				
			V _{GB} = 30 V									1
Threshold Voltage	V _T	V _{DS} = V _{GS} = V _T , I _D = 1 μA, V _{SB} = 0 V	0.1	1.0	2.0	0.1	1.0	2.0	0.1	1.0	2.0	V
Drain-Source ON Resistance	r _{DS(on)}	I _D = 1 mA, V _{SB} = 0 V	V _{GS} = 5 V		50	70		50	70		50	70
			V _{GS} = 10 V		30		30		30			
			V _{GS} = 15 V		23		23		23			
			V _{GS} = 20 V		19		19		19			
Resistance Match ⁶	r _{DS(on)}	I _D = 1 mA, V _{SB} = 0 V, V _{GS} = 5 V	1	5		1	5		1	5		
Forward Transconductance	g _{fs}	V _{DS} = 10 V, I _D = 20 mA, V _{SB} = 0 V, f = 1 kHz	10	15		10	15		10	15		mS ⁷
Gate Node Capacitance	C _G	V _{DS} = 10 V, V _{GD} = V _{BS} = -15 V, f = 1 MHz See Capacitance Model Figure 1	2.4	3.5		2.4	3.5		2.4	3.5		pF
Drain Node Capacitance	C _D		1.3	1.6		1.3	1.6		1.3	1.6		
Source Node Capacitance	C _S		3.5	5		3.5	5		3.5	5		
Reverse Transfer Capacitance	C _{DG}		0.3	.5		0.3	.5		0.3	.5		
Crosstalk		See Test Circuits 1 and 2 f = 3 kHz	-107			-107			-107			dB

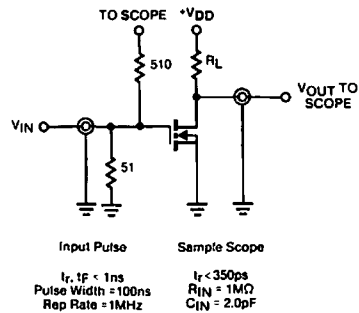
NOTES:

- Refer to test conditions specified in Electrical Characteristics Tables.
- Derate 5 mW/°C above 25°C.
- Refer to PROCESS OPTION FLOWCHART for additional information.
- The algebraic convention whereby the most negative value is a minimum, and the most positive value is a maximum, is used in this data sheet.
- Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- This untested parameter is guaranteed by design.
- 1 mS = 1 m-mho (Ω)

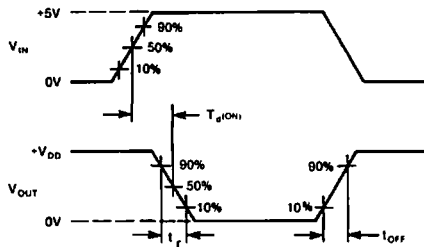
TEST CIRCUIT



SWITCHING TEST CIRCUIT



SWITCHING WAVEFORMS

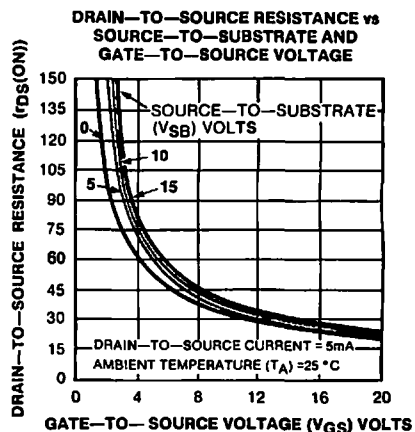
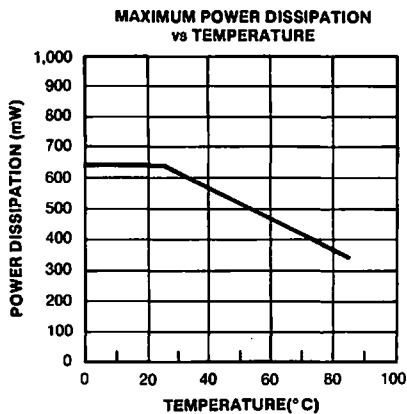


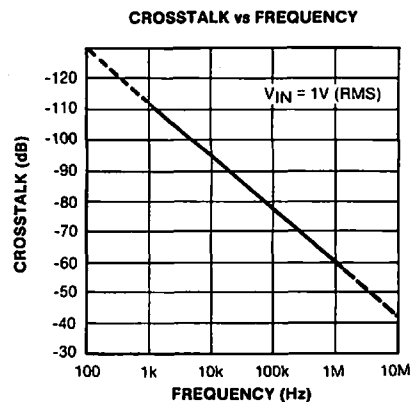
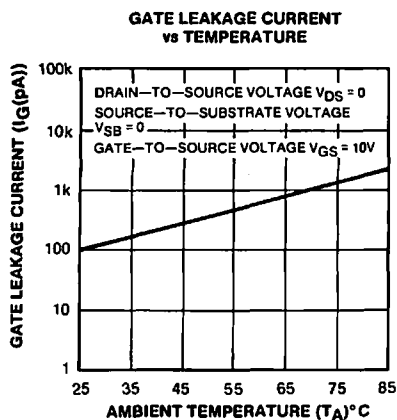
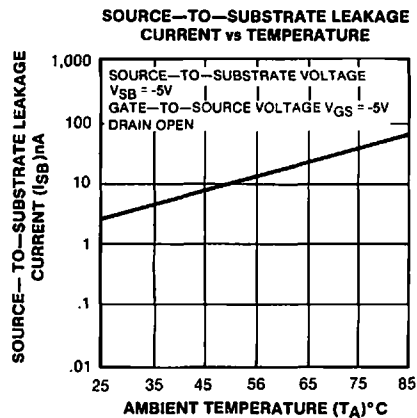
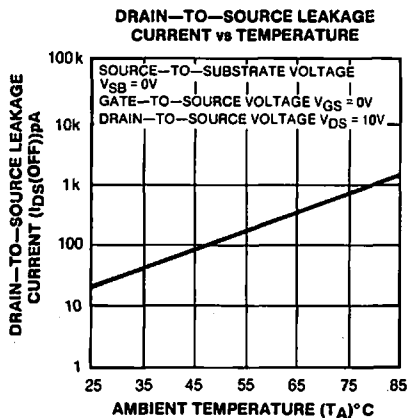
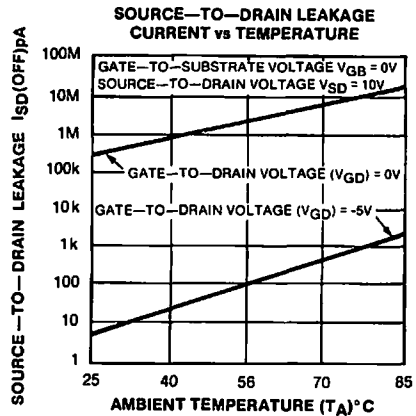
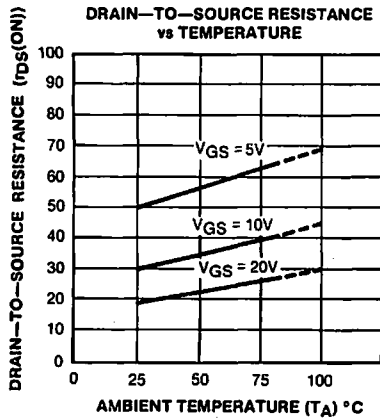
SWITCHING CHARACTERISTICS

		$t_{d(ON)}(\text{ns})$		$t_r(\text{ns})$		$t_{OFF}(\text{ns})$	
V_{DD}	R_L	TYP	MAX	TYP	MAX	TYP	MAX
5	680	0.6	1.0	0.7	1.0	9.0	
10	680	0.7		0.8		9.0	
15	1k	0.9		1.0		14.0	

* t_{OFF} is dependent on R_L and does not depend on the device characteristics.

TYPICAL CHARACTERISTICS





THEORY OF OPERATION

The SD5000 series consists of four SPST switches with analog signal capability of ± 10 volts for the SD5000, ± 5 volts for the SD5001 and ± 7.5 volts for the SD5002. Each switch of the array is a DMOS N-channel field-effect transistor of the enhancement-mode type; that is, the device is normally off when gate-to-source voltage (V_{GS}) is zero volts. When V_{GS} exceeds the threshold voltage, V_T , the FET switch starts to turn ON with V_{GS} in excess of $+10$ volts, a low resistance path (typically $30\ \Omega$) exists between input and output of the switch. Figure 1 shows the normal mode of operation of a single switch of the array for ± 5 volt analog signal processing. Note that the source is recommended for the input since feedback or reverse transfer capacitance is lower when drain is used as the output. When analog signals are routed from one point to another the important factors are isolation, crosstalk between switches, feedthrough and feedback transients, insertion loss and speed of operation. The SD5000 series offers superior performance in all these areas (Figure 1).

Isolation. ON resistance is typically $30\ \Omega$ and OFF resistance is typically $10^{10}\ \Omega$, which results in an OFF to ON resistance ratio in excess of 10^9 . Isolation from output to input from 3 kHz analog signals is typically $-107\ \text{dB}$.

Feedback and feedthrough transients are kept to a minimum because of the very low feedback and feedthrough capacitances. This means that "glitches" or "clean" signals appear at the output.

Insertion loss depends upon the source and load impedances involved. As an example, for $600\ \Omega$ source impedance the insertion loss for voice signals (1 V RMS at 3 kHz) is less than 0.3 dB. Thus the SD5000 series makes good telephone cross-point switches.

Speed. Because of the low ON resistance and low input capacitance, the SD5000 switches turn ON at subnanosecond speeds. They are also capable of handling very high frequency analog signals and still maintain excellent isolation (20-30 dB at 1 GHz).

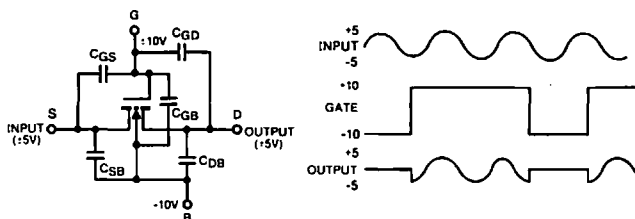
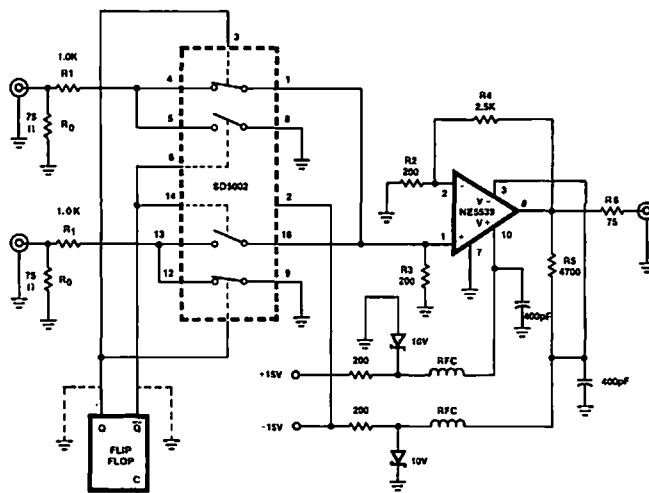


Figure 1

TYPICAL APPLICATION

Figure 2 shows an SD5002 configured for operation as a one of two channel video switch. The "L" switches of the two channels are terminated at the input by the two R_0 resistors, allowing impedance matching to various transmis-

sion line impedances. The switches can be directly controlled by standard CMOS or TTL logic gates. For more detailed information on this application, see AN83-15.



High Performance Video Switch

Figure 2

SD5400/SD5401/SD5402

DMOS FET Quad

Analog Switch Arrays



FEATURES

- Low "ON" Resistance ($<30\ \Omega$)
- Low Input Capacitance (6 pF)
- Low Output Capacitance (2 pF)
- Low Feedback Capacitance (0.5 pF)
- High Channel-to-Channel Isolation ($\sim 107\ \text{dB}$)
- Small Outline Package

BENEFITS

- Low Crosstalk
- Low Insertion Loss
- Glitch Free Signals
- Fast Switching
- Reduced Board Space Requirements

APPLICATIONS

- Audio Switching
- Video Switching
- Sample/Hold
- Choppers
- Crosspoint Switches

DESCRIPTION

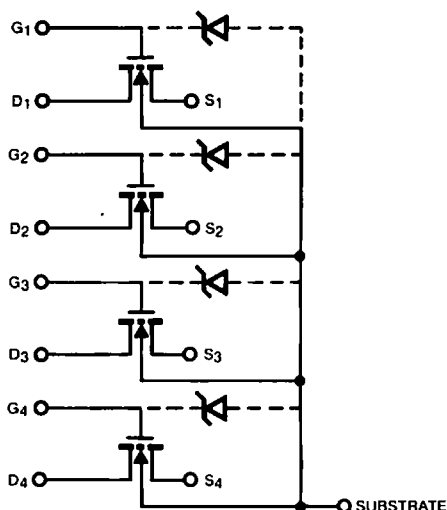
The Siliconix SD5400 series is a monolithic array of single-pole, single-throw analog switches designed for high speed switching in audio, video, and high frequency applications in communications, instrumentation, and process control. Designed on the Siliconix DMOS process, the SD5400 is rated for analog signals of $\pm 10\ \text{V}$, while the SD5401 and SD5402 are rated for $\pm 5\ \text{V}$ and $\pm 7.5\ \text{V}$ respectively.

These bidirectional switches feature very low interelectrode capacitance and ON resistance to achieve low

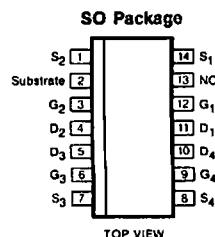
insertion loss, crosstalk, and feedthrough performance. The threshold voltage for all switches is 2 V maximum, simplifying driver requirements for low level signal applications.

The SD5400 family is available in a 14-pin plastic Small Outline (SO) package, and is rated for operation over the 0 to 70°C commercial temperature range.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



Order Numbers:
SD5400CY, SD5401CY,
or SD5402CY
See Package 30

ABSOLUTE MAXIMUM RATINGS

	SD5400	SD5401	SD5402	I_D	50 mA
V_{DS}	20 V	10 V	15 V	Operating Temperature	0 to 70°C
V_{SD}^1	20 V	10 V	15 V	Storage Temperature	-55 to 125°C
V_{DB}	25 V	15 V	22.5 V	Power Dissipation (Package) ²	640 mW
V_{SB}	25 V	15 V	22.5 V	(Each Device)	300 mW
V_{GS}	30/-25 V	25/-15 V	30/-22.5 V		
V_{GB}	30/-0.3 V	25/-0.3 V	30/-0.3 V		
V_{GD}	30/-25 V	25/-15 V	30/-22.5 V		

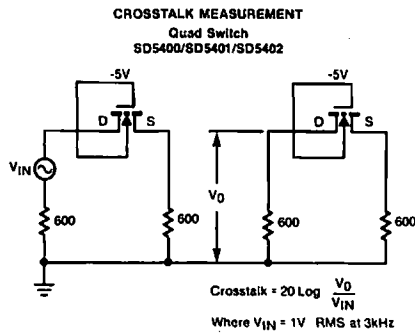
ELECTRICAL CHARACTERISTICS³ $T_A = 25^\circ\text{C}$

PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED:	LIMITS									UNIT	
			SD5400			SD5401			SD5402				
			MIN ⁴	TYP ⁵	MAX	MIN ⁴	TYP ⁵	MAX	MIN ⁴	TYP ⁵	MAX		
Analog Signal Range	V _{ANALOG}		-10		10	-5		5	-7.5		7.5		
Drain-Source Breakdown Voltage	BV _{DS}	V _{GS} = V _{BS} = -5 V, I _D = 10 nA	20	25		10	25		15	25		V	
Source-Drain Breakdown Voltage	BV _{SD}	V _{GD} = V _{BD} = -5 V, I _S = 10 nA	20			10			15				
Drain-Substrate Breakdown Voltage	BV _{DB}	V _{GB} = 0 V, I _D = 10 nA, Source Open	25			15			22.5				
Source-Substrate Breakdown Voltage	BV _{SB}	V _{GB} = 0 V, I _S = 10 μA, Drain Open	25			15			22.5				
Drain-Source Leakage Current	I _{DS(off)}	V _{GS} = V _{BS} = -5 V	V _{DS} = 20 V			1	10						
			V _{DS} = 10 V					1	10				
			V _{DS} = 15 V								1	10	
Source-Drain Leakage Current	I _{SD(off)}	V _{GD} = V _{BD} = -5 V	V _{SD} = 20 V			1	10						
			V _{SD} = 10 V					1	10				
			V _{SD} = 15 V								1	10	
Gate Leakage Current	I _{GBS}	V _{DB} = V _{SB} = 0 V	V _{GB} = 30 V			1							
			V _{GB} = 25 V						1				
			V _{GB} = 30 V									1	
Threshold Voltage	V _T	V _{DS} = V _{GS} = V _T , I _D = 1 μA, V _{SB} = 0 V	0.1	1.0	2.0	0.1	1.0	2.0	0.1	1.0	2.0	V	
Drain-Source ON Resistance	r _{DS(on)}	I _D = 1 mA, V _{SB} = 0 V	V _{GS} = 5 V			50	70		50	70		50	70
			V _{GS} = 10 V			30		30		30		30	
			V _{GS} = 15 V			23		23		23		23	
			V _{GS} = 20 V			19		19		19		19	
Resistance Match ⁶	r _{DS(on)}	I _D = 1 mA, V _{SB} = 0 V, V _{GS} = 5 V		1	5		1	5		1	5		
Forward Transconductance	g _{fs}	V _{DS} = 10 V, I _D = 20 mA, V _{SB} = 0 V, f = 1 kHz	10	15		10	15		10	15		mS ⁷	
Gate Node Capacitance	C _G	V _{DS} = 10 V, V _{GD} = V _{BS} = -15 V, f = 1 MHz See Capacitance Model Figure 1		2.4	3.5		2.4	3.5		2.4	3.5		
Drain Node Capacitance	C _D			1.3	2		1.3	2		1.3	2		
Source Node Capacitance	C _S			3.5	6		3.5	6		3.5	6		
Reverse Transfer Capacitance	C _{DG}			0.3	.5		0.3	.5		0.3	.5		
Crosstalk		See Test Circuits 1 and 2 f = 3 kHz		-107			-107			-107		dB	

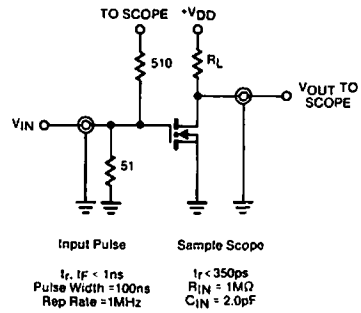
NOTES:

- Refer to test conditions specified in Electrical Characteristics Tables.
- Derate 5 mW/°C above 25°C.
- Refer to PROCESS OPTION FLOWCHART for additional information.
- The algebraic convention whereby the most negative value is a minimum, and the most positive value is a maximum, is used in this data sheet.
- Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- This untested parameter is guaranteed by design.
- 1 mS = 1 m-mho (U)

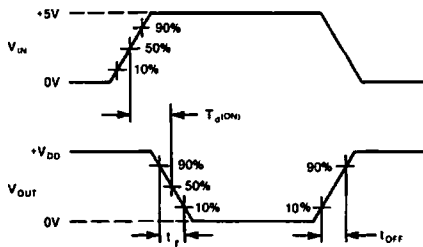
TEST CIRCUIT



SWITCHING TEST CIRCUIT



SWITCHING WAVEFORMS

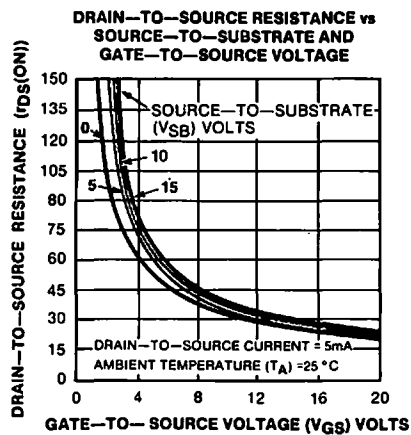


SWITCHING CHARACTERISTICS

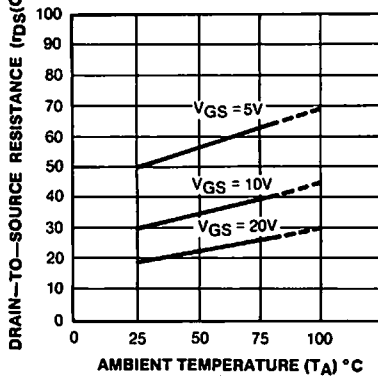
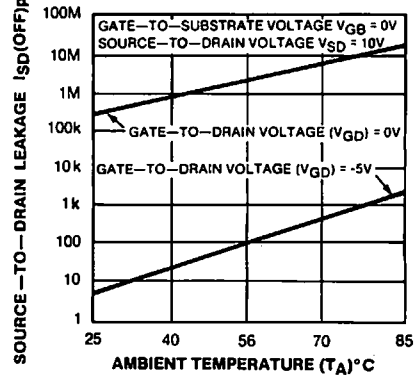
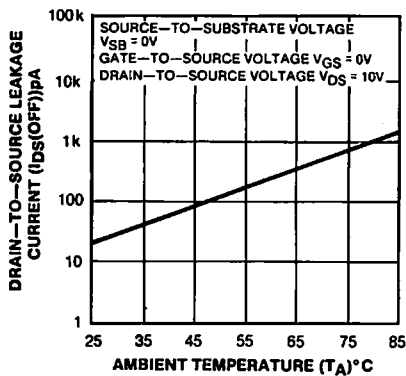
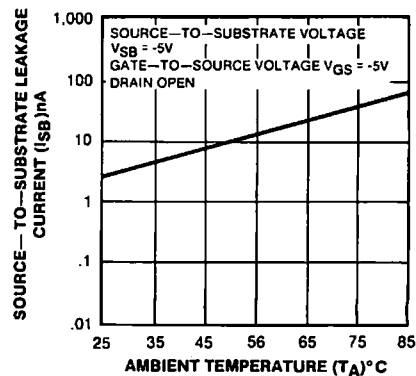
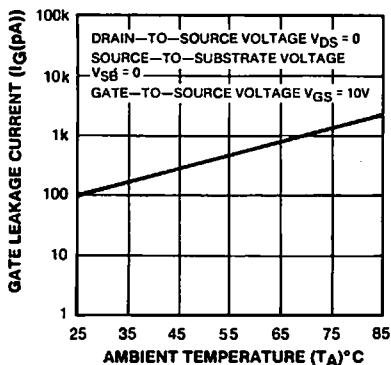
V _{DD}	R _L	t _{d(ON)} (ns)		t _r (ns)		* t _{OFF} (ns)	
		TYP	MAX	TYP	MAX	TYP	MAX
5	680	0.8	1.0	0.7	1.0	9.0	
10	680	0.7		0.8		9.0	
15	1k	0.9		1.0		14.0	

*t_{OFF} is dependent on R_L and does not depend on the device characteristics.

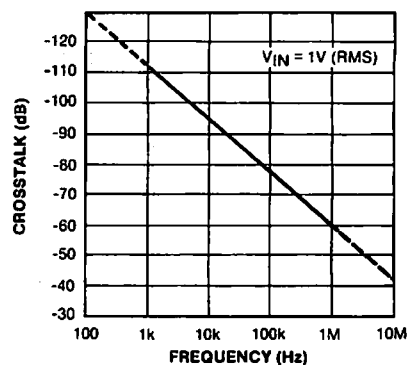
TYPICAL CHARACTERISTICS



TYPICAL CHARACTERISTICS (Cont.)

DRAIN-TO-SOURCE RESISTANCE
vs TEMPERATURESOURCE-TO-DRAIN LEAKAGE
CURRENT vs TEMPERATUREDRAIN-TO-SOURCE LEAKAGE
CURRENT vs TEMPERATURESOURCE-TO-SUBSTRATE LEAKAGE
CURRENT vs TEMPERATUREGATE LEAKAGE CURRENT
vs TEMPERATURE

CROSSTALK vs FREQUENCY



The SD5400 series consists of four SPST switches with analog signal capability of ± 10 volts for the SD5400, ± 5 volts for the SD5401 and ± 7.5 volts for the SD5402. Each switch of the array is a DMOS N-channel field-effect transistor of the enhancement-mode type; that is, the device is normally off when gate-to-source voltage (V_{GS}) is zero volts. When V_{GS} exceeds the threshold voltage, V_T , the FET switch starts to turn ON with V_{GS} in excess of $+10$ volts, a low resistance path (typically $30\ \Omega$) exists between input and output of the switch. Figure 1 shows the normal mode of operation of a single switch of the array for ± 5 volt analog signal processing. Note that the source is recommended for the input since feedback or reverse transfer capacitance is lower when drain is used as the output. When analog signals are routed from one point to another the important factors are isolation, crosstalk between switches, feedthrough and feedback transients, insertion loss and speed of operation. The SD5400 series offers superior performance in all these areas (Figure 1).

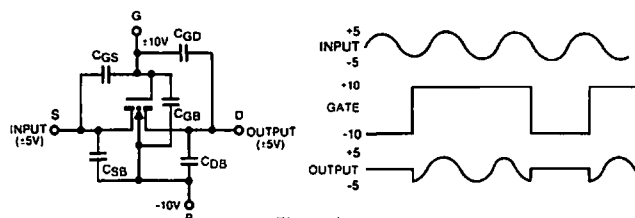
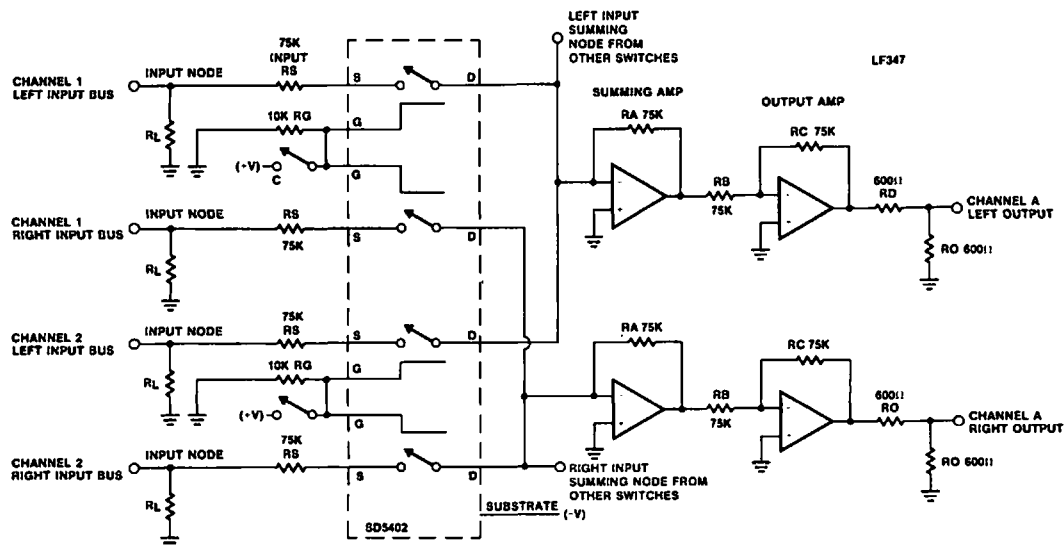


Figure 1

TYPICAL APPLICATION

Figure 2 shows the SD5402 used as an audio crosspoint switch. Each SD5402 provides switching for 2 stereo channels. Additional channels can be added by connect-

ing each output to its respective summing node. For additional information on this application refer to AN83-7.

Audio Crosspoint Switch
Figure 2

DG501

8-Channel Multiplex Switch with Decode

FEATURES

- Break-Before-Make Switching
- Pull-Up Resistors on Inputs
- Bi-Directional Signal Handling

BENEFITS

- Reduced System Cross-Talk
- Easily Interfaced to TTL

APPLICATIONS

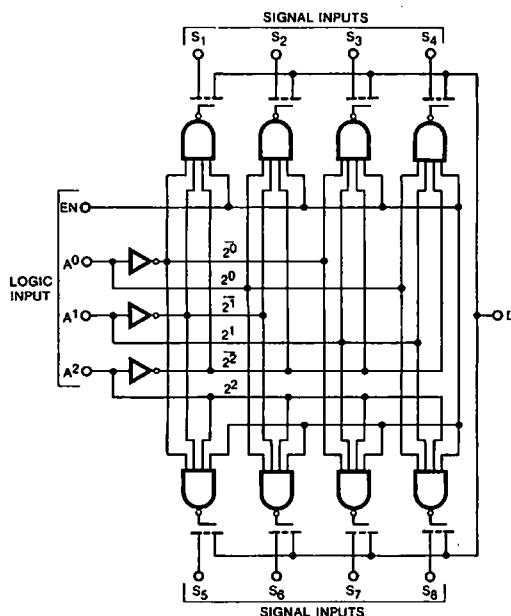
- Multiplexing ± 5 V Analog Signals
- Data Acquisition Systems

DESCRIPTION

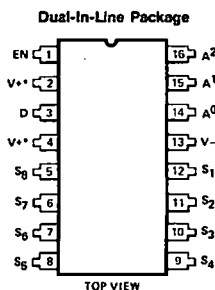
Designed for applications where single-ended, break-before-make switching action is required, the DG501 is an 8-channel analog multiplexer that is capable of handling bi-directional signals up to ± 5 V. In addition, an "OFF" state can be activated by using a chip enable signal. In the OFF state, this device can block up to 10 V peak-to-peak signals. An on-chip decoder accepts a 3 bit binary word

which enables the selection of any one of the eight analog switches to be turned on individually. Pull-up resistors are provided at each logic input to simplify TTL interface compatibility. This device is available in either a 16 pin plastic or ceramic DIP and is available in commercial, industrial and military temperature ranges.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



Order Numbers:
DG501AP or DG501BP
See Package 12

DG501CJ
See Package 8

* Both V+ lines are internally connected, either one or both may be used. V+ common to substrate.

ABSOLUTE MAXIMUM RATINGS

V+ to V-	-0.3 to +30 V
V+ to V _A , V _{EN}	-0.3 to +30 V
V+ to V _D or V _S	-0.3 to +30 V
V _D to V _S	±25 V
V _A , V _{EN} to V-	30 V
V _D or V _S to V-	30 V
Current (Any Terminal)	-20 mA
Storage Temperature (A & B Suffix)	-65 to 150°C
(C Suffix)	-65 to 125°C

Operating Temperature (A Suffix)	-55 to 125°C
(B Suffix)	-25 to 85°C
(C Suffix)	0 to 70°C

Power Dissipation*

16 Pin Ceramic DIP**	900 mW
16 Pin Plastic DIP***	470 mW

*Device mounted with all leads welded or soldered to PC board.

**Derate 12 mW/°C above 75°C.

***Derate 6.5 mW/°C above 25°C.

ELECTRICAL CHARACTERISTICS¹T_A = 25°C

	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: V ₊ = 5 V, V ₋ = -20 V, V _{EN} = 3.5 V, V _{AL} = 0.6 V, V _{AH} = 3.5 V		LIMITS						UNIT
					DG501A			DG501B/C			
					MIN ²	TYP ³	MAX	MIN ²	TYP ³	MAX	
SWITCH	Analog Signal Range	V _{ANALOG}			-5		5	-5		5	V
	Drain-Source ON Resistance	r _{DS(on)}	I _S = -100 μA V ₋ = -15 V	V _D = 5 V		75	200		75	200	Ω
				V _D = 0		97	250		97	250	
				V _D = -5 V		140	600		140	800	
			I _S = -1 μA V ₋ = -20 V	V _D = 5 V		65	150		65	150	
				V _D = 0		80	200		80	200	
				V _D = -5 V		100	250		100	250	
	Source OFF Leakage Current	I _{S(off)}	V _S = -5 V, V _D = 5 V V _{EN} = 0.6 V		-1	-0.005		-3	-0.015		
Drain OFF Leakage Current	I _{D(off)}	V _D = -5 V, V _S = 5 V V _{EN} = 0.6 V		-8	-0.07		-10	-0.1	nA		
Channel ON Leakage Current	I _{D(on)} + I _{S(on)}	V _D = V _S = 5 V			0.1	8		0.12	10		
INPUT	Logic Input Current, Input Voltage Low	I _{INL}	V _{AL} = 0		-1.2	-1		-1.2	-0.8	mA	
	Logic Input Current, Input Voltage High	I _{INH}	V _{AH} = 3.5 V		-150			-150		μA	
DYNAMIC	Switching Time	t _{transition}	See Switching Time Test Circuit V _{S1} = ±1 V, V _{S6} = ±1 V, V _{S2} - 7 = gnd	V ₋ = -20 V		0.8	1.5		1	2	μs
			V ₋ = -15 V		1.25	2.5		1.5	3		
	Break-Before-Make Interval	t _{open}	See Switching Time Test Circuit V _{S(all)} = 1 V			0.05			0.05		
	Turn-ON Time	t _{on}				1.2			1.2		
	Turn-OFF Time	t _{off}				0.8			0.8		
	Turn-ON Time	t _{on}	Same As Above, Except V ₋ = -15 V			2			2		
	Turn-OFF Time	t _{off}				0.8			0.8		
	Source OFF Capacitance	C _{S(off)}	V _S = V _D = 5 V, V _{EN} = 0.6 V, f = 1 MHz			10			10		pF
Drain OFF Capacitance	C _{D(off)}				20			20			
SUPPLY	Drain Supply Current	I ₋	V _{EN} = 0, V _{AL(all)} = 0		-6	-2.6		-6	-2.6		mA
	Source Supply Current	I ₊				5.6	8		5.6	8	
	Drain Supply Current	I ₋	V _{EN} = 3.5 V, V _{AL(all)} = 0		-6	-2.4		-6	-2.4		
	Source Supply Current	I ₊				4.9	7		4.9	7	

NOTES

(See next page)

ELECTRICAL CHARACTERISTICS¹ (Cont.)
 T_A = Over Temperature Range

	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: V+ = 5 V, V- = -20 V, VEN = 3.5 V, VAL = 0.6 V, VAH = 3.5 V		LIMITS						UNIT
					DG501A			DG501B/C			
					MIN ²	TYP ³	MAX	MIN ²	TYP ³	MAX	
SWITCH	Analog Signal Range	VANALOG			-5		5	-5		5	V
	Drain-Source ON Resistance	rDS(on)	IS = -100 μA V- = -15 V	VD = 5 V			300			300	Ω
				VD = 0			375			350	
				VD = -5 V			900			900	
			IS = -1 μA V- = -20 V	VD = 5 V			225			200	
				VD = 0			300			300	
				VD = -5 V			375			350	
	Source OFF Leakage Current	IS(off)	VS = -5 V, VD = 5 V VEN = 0.6 V		-1000			-150			nA
	Drain OFF Leakage Current	ID(off)	VD = -10 V, VS = 10 V VEN = 0.6 V		-4000			-500			
	Channel ON Leakage Current	ID(on) + IS(on)	VD = VS = 5 V				4000			500	

NOTES:

1. All DC parameters are 100% tested at 25°C. Lots are sample-tested for AC parameters and high and low temperature limits to assure conformance with specifications.
2. The algebraic convention whereby the most negative value is a minimum, and the most positive value is a maximum, is used in this data sheet.
3. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

TRUTH TABLE

LOGIC INPUTS				CHANNEL
A^0	A^1	A^2	EN	'ON'
L	L	L	H	S_1
H	L	L	H	S_2
L	H	L	H	S_3
H	H	L	H	S_4
L	L	H	H	S_5
H	L	H	H	S_6
L	H	H	H	S_7
H	H	H	H	S_8
X	X	X	L	OFF

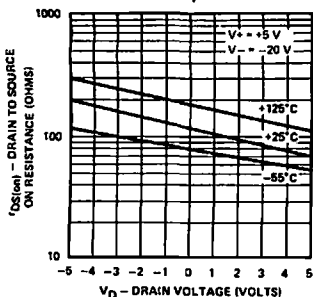
Logic Levels*

LOW: $V_L = V_{LOW} \leq 0.6\text{ V}$

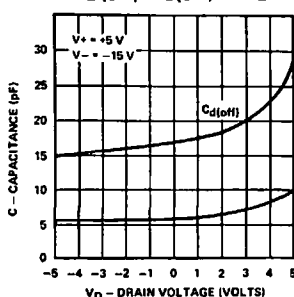
HIGH: $V_H = V_{HIGH} \geq 3.5\text{ V}$

*For supply voltages of +5 V and -20 V

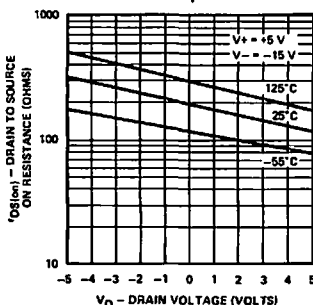
$r_{DS(on)}$ vs V_D and Temperature



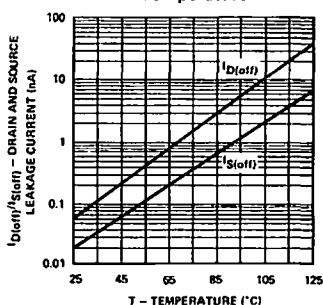
$C_D(off)$, $C_S(off)$ vs V_D



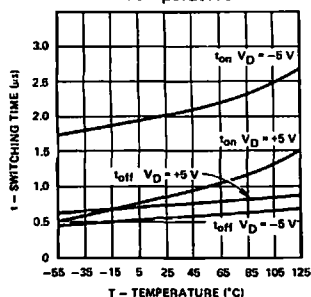
$r_{DS(on)}$ vs V_D and Temperature



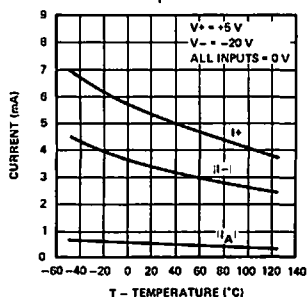
$I_D(off)$, $I_S(off)$ vs Temperature



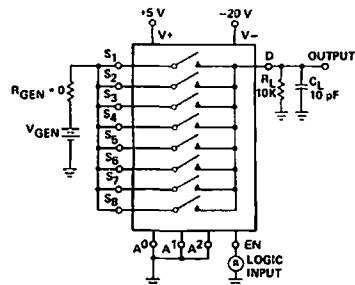
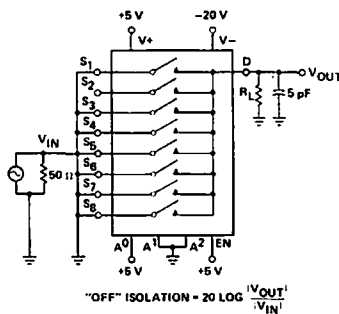
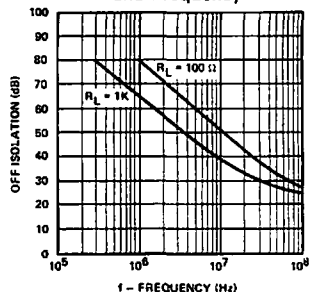
Switching Time vs Temperature



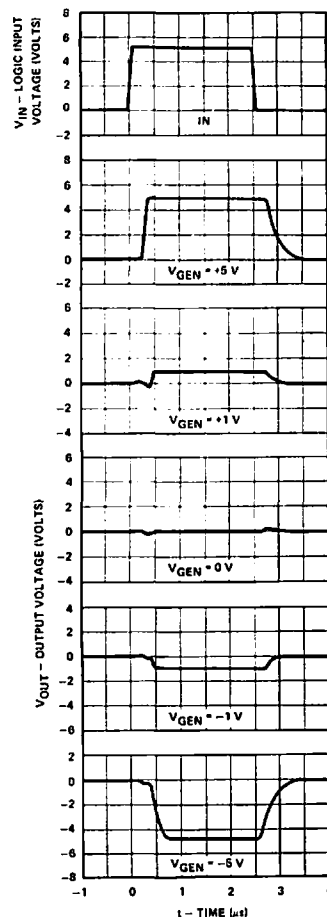
Supply Current vs Temperature



"OFF" Isolation vs R_L and Frequency



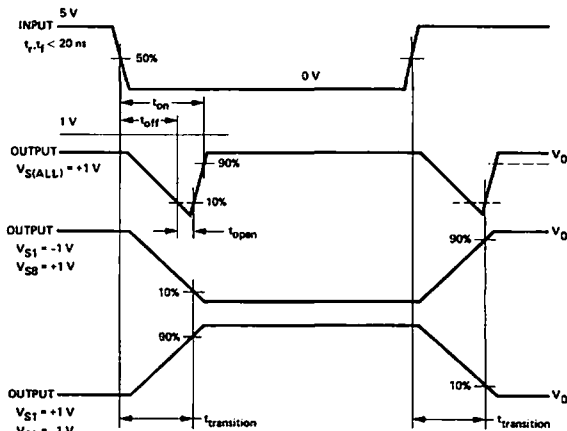
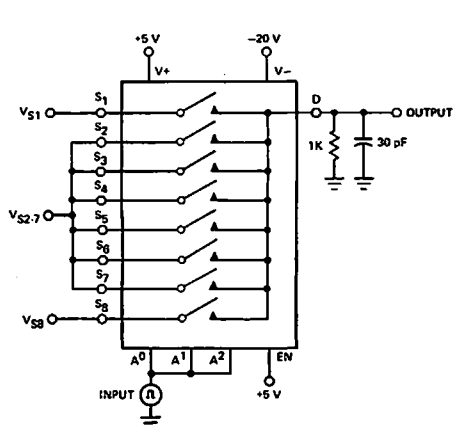
If R_{GEN} , R_L or C_L is increased, there will be proportional increases in rise and/or fall RC times.



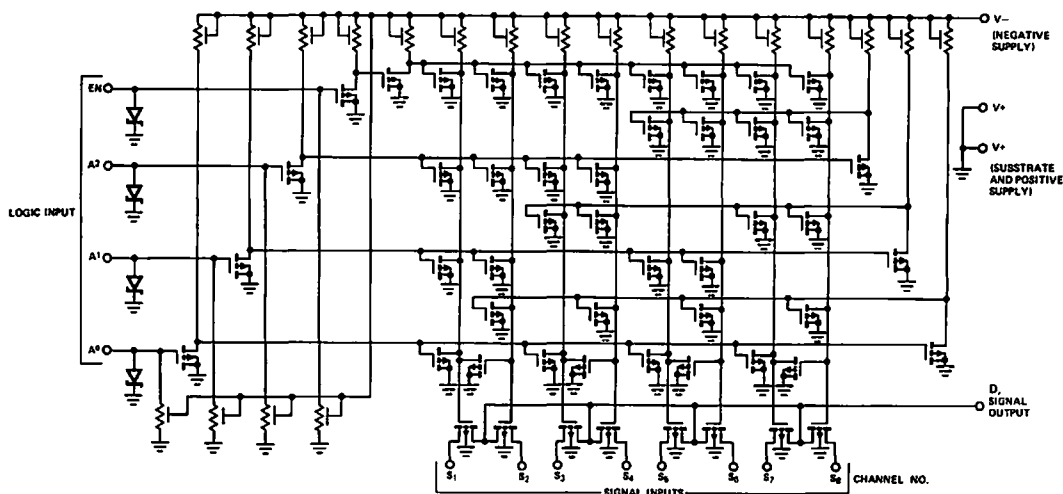
SWITCHING TIME TEST CIRCUIT

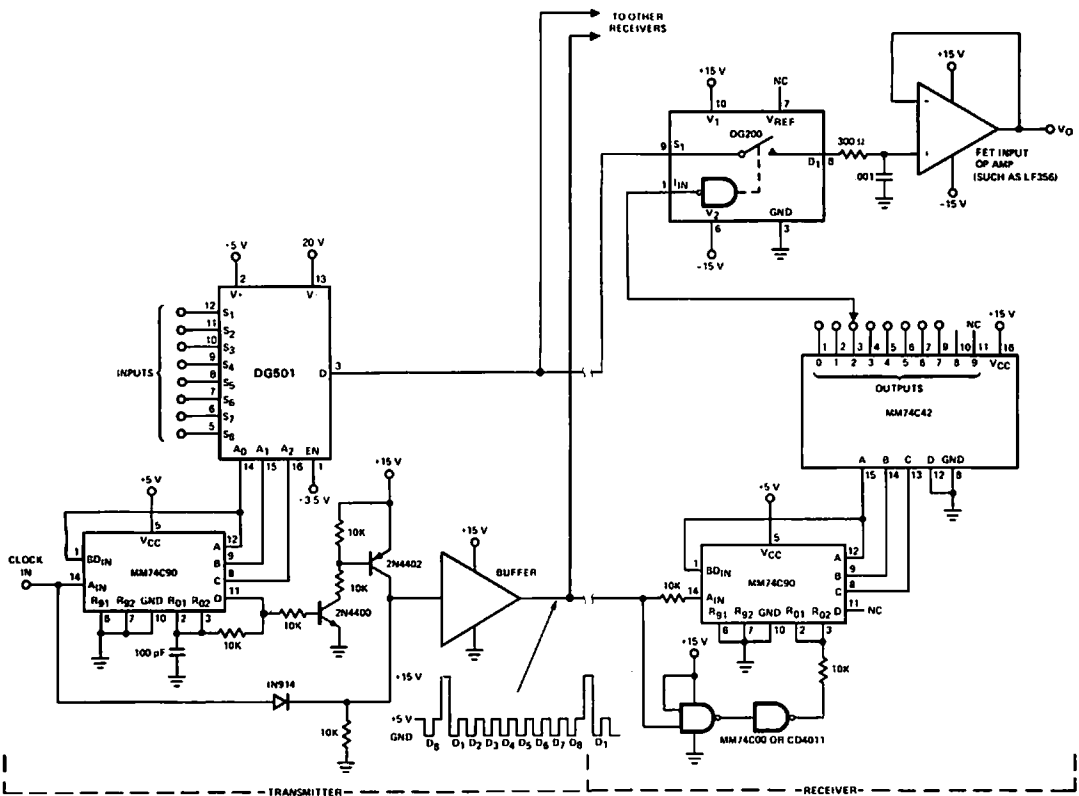
Switch output waveform shown for V_S = constant with logic input waveform as shown. Note that V_S may be + or - as per switching time test circuit. V_O is the steady state

output with switch on. Feedthrough via gate capacitance may result in spikes at leading and trailing edge of output waveform.



SCHEMATIC DIAGRAM





A One Of 8-channel Transmission System

APPLICATION HINTS*

V+ Positive Supply Voltage (V)	V- Negative Supply Voltage (V)	V _{EN} Enable Input Voltage Min High/ Max Low (V)	V _{IN} Logic Input Voltage V _{INH} Min/ V _{INL} Max (V)	V _S or V _D Analog Signal Range (V)
+5**	-20	3.5/0.6	3.5/0.6	-5 to +5
+5	-15	3.5/0.6	3.5/0.6	-5 to +5

*Application Hints are for DESIGN AID ONLY, not guaranteed and not subject to production testing.

****Electrical parameters chart based on $V+ = 5\text{ V}$, $V- = -20\text{ V}$.**

DG503

8-Channel Multiplex Switch with Decode



FEATURES

- ± 10 V Input Signal Range
- Break-Before-Make Switching
- Bidirectional Signal Handling

BENEFITS

- Reduced System Cross-Talk

APPLICATIONS

- Data Acquisition
- Multiplexing Signals

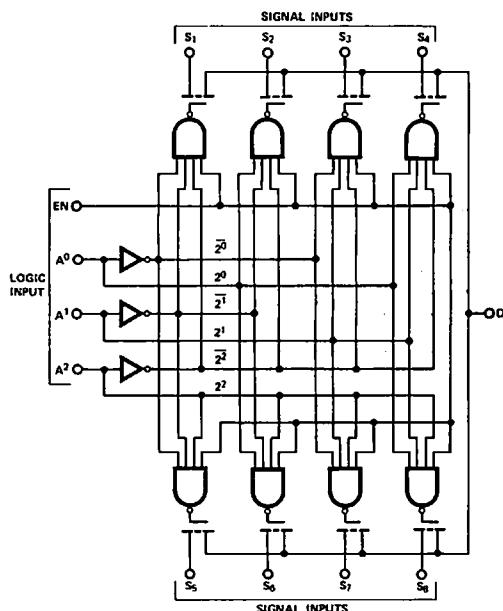
DESCRIPTION

Designed for applications where single-ended, Break-Before-Make switching action is required, the DG503 is an 8-channel analog multiplexer that is capable of handling bi-directional signals up to ± 10 V. In addition, an "OFF" state can be activated by using a chip-enable signal. In the OFF state the device can block up to 20 V peak-to-peak signals. An on-chip decoder accepts a 3-bit binary word

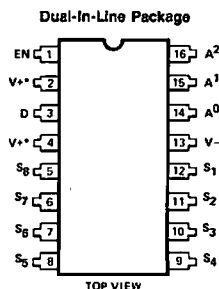
which enables the selection of any one of eight analog switches to be turned on individually. Pull-up resistors are provided at each logic input to simplify TTL compatibility.

DG503 is available in a 16-pin plastic or ceramic DIP, and in the standard commercial, industrial and military temperature ranges.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



Order Numbers: DG503AP or DG503BP
See Package 12
DG503CJ
See Package 8

*Both V+ lines are internally connected, either one or both may be used. V+ common to substrate.

ABSOLUTE MAXIMUM RATINGS

$V+$ to $V-$ -0.3, 33 V
 $V+$ to V_A , V_{EN} -0.3, 33 V
 $V+$ to V_D or V_S -0.3, 33 V
 V_D to V_S ± 25 V
 V_A , V_{EN} to $V-$ 33 V
 V_D or V_S to $V-$ 33 V
 Current (Any Terminal) -20 mA

Storage Temperature (A & B Suffix) -65 to 150°C
 (C Suffix) -65 to 125°C
 Operating Temperature (A Suffix) -55 to 125°C
 (B Suffix) -25 to 85°C
 (C Suffix) 0 to 70°C
 Power Dissipation* 900 mW
 *All leads soldered or welded to PC board. Derate
 12 mW/°C above 75°C.

ELECTRICAL CHARACTERISTICS¹
 $T_A = 25^\circ\text{C}$

	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: V+ = +10 V, V- = -20 V, VEN = 8.5 V, VAL = +0.6 V, VAH = +8.5 V		LIMITS						UNIT
					DG503A			DG503B/C			
					MIN ²	TYP ³	MAX	MIN ²	TYP ³	MAX	
SWITCH	Analog Signal Range	VANALOG			-10		10	-10		10	V
	Drain-Source ON Resistance	rDS(on)	IS = -100 μA	VD = -10 V			800			800	Ω
			IS = -1 μA	VD = 10 V			150		150		
							250			250	
	Source OFF Leakage Current	IS(off)	VS = -10 V, VD = 10 V, VEN = 0.6 V		2			-3			nA
Drain OFF Leakage Current	ID(off)	VD = -10 V, VS = 10 V, VEN = 0.6 V		-8			-10				
Channel ON Leakage Current	ID(on) + IS(on)	VD = VS = 10 V				8			10		
IN	Logic Input Current, Input Voltage High	IINL	VA(all) = 0		-1			-1			μA
DYNAMIC	Switching Time	ttransition	See Switching Time Test Circuit VS1 = ±1 V, VS2 = ∓1 V, VS2 - 7 = GND				1.5			2	μs
	Break-Before-Make Interval	topen				0.05		0.05			
	Turn-ON Time	ton	See Switching Time Test Circuit VS(all) = ±1 V			1.2		1.2			
	Turn-OFF Time	toff				0.8		0.8			
	Source OFF Capacitance	CS(off)	VS = VD = 0 V, VEN = 0.5 V, f = 1 MHz			5		5		pF	
	Drain OFF Capacitance	CD(off)				20		20			
SUPPLY	Drain Supply Current	I-	VEN = 0		-6			-6			mA
	Source Supply Current	I+					8		8		
	Drain Supply Current	I-	VEN = 8.5 V, VA(all) = 0		-6			-6			
	Source Supply Current	I+					7		7		

NOTES:

- All DC parameters are 100% tested at 25°C. Lots are sample-tested for AC parameters and high and low temperature limits to assure conformance with specifications.
- The algebraic convention whereby the most negative value is a minimum, and the most positive value is a maximum, is used in this data sheet.
- Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

ELECTRICAL CHARACTERISTICS¹ (Cont.)
 $T_A = \text{Over Temperature Range}$

	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: V+ = +10 V, V- = -20 V, VEN = 8.5 V, VAL = +0.6 V, VAH = +8.5 V		LIMITS						UNIT
					DG503A			DG503B/C			
					MIN ²	TYP ³	MAX	MIN ²	TYP ³	MAX	
SWITCH	Drain-Source ON Resistance	rDS(on)	IS = -100 μA	VD = -10 V			1250			1000	Ω
			IS = -1 μA	VD = 10 V			225			200	
				VD = 0			375			350	
	Source OFF Leakage Current	IS(off)	VS = -10 V, VD = 10 V, VEN = 0.6 V	-2000			-150			nA	
	Drain OFF Leakage Current	ID(off)	VD = -10 V, VS = 10 V, VEN = 0.6 V	-4000			-500				
Channel ON Leakage Current	ID(on) + IS(on)	VD = VS = 10 V			4000			500			

NOTES:

1. All DC parameters are 100% tested at 25° C. Lots are sample-tested for AC parameters and high and low temperature limits to assure conformance with specifications.
2. The algebraic convention whereby the most negative value is a minimum, and the most positive value is a maximum, is used in this data sheet.
3. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

TRUTH TABLE

LOGIC INPUTS				CHANNEL
A^0	A^1	A^2	EN	'ON'
L	L	L	H	S ₁
H	L	L	H	S ₂
L	H	L	H	S ₃
H	H	L	H	S ₄
L	L	H	H	S ₅
H	L	H	H	S ₆
L	H	H	H	S ₇
H	H	H	H	S ₈
X	X	X	L	OFF

Logic Levels*

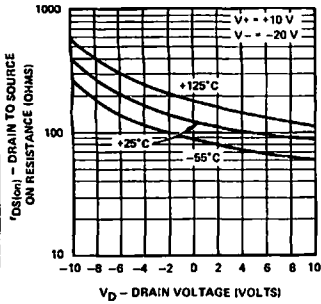
$$V_L = V_{LOW} \leq 0.6\text{ V}$$

$$V_H = V_{HIGH} \geq 8.5\text{ V}$$

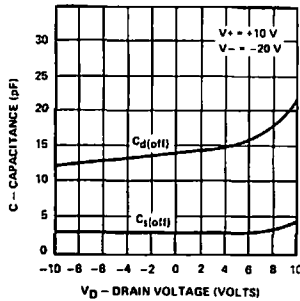
*For Supply Voltages of 10 V and -20 V

TYPICAL CHARACTERISTICS

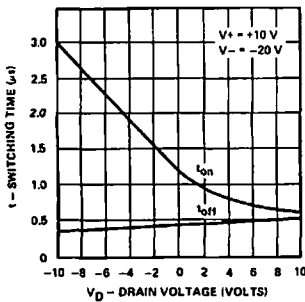
$r_{DS(on)}$ vs V_D and Temperature



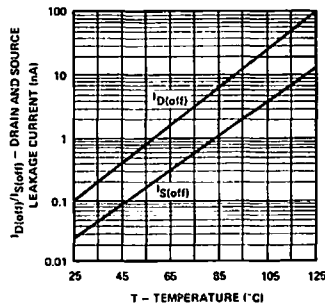
$C_D(off)$, $C_S(off)$ vs V_D



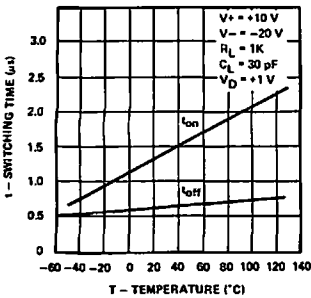
Switching Time vs V_D



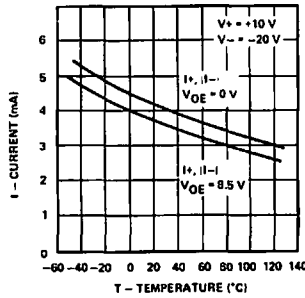
$I_D(off)$, $I_S(off)$ vs Temperature



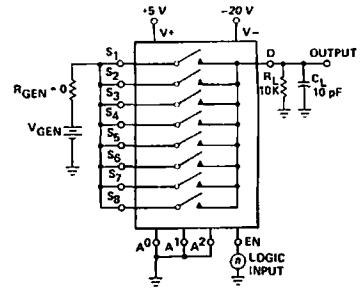
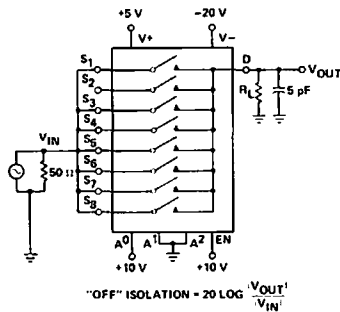
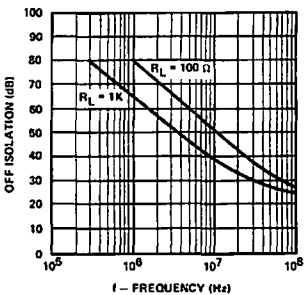
Switching Time vs Temperature



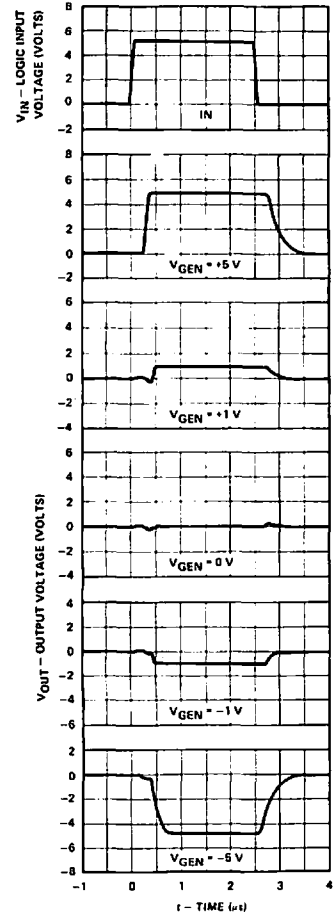
Supply Current vs Temperature



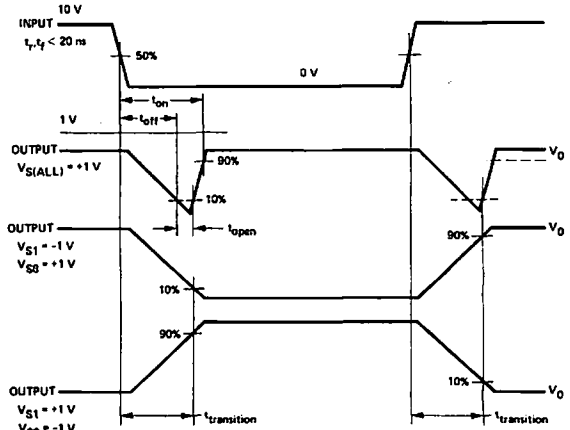
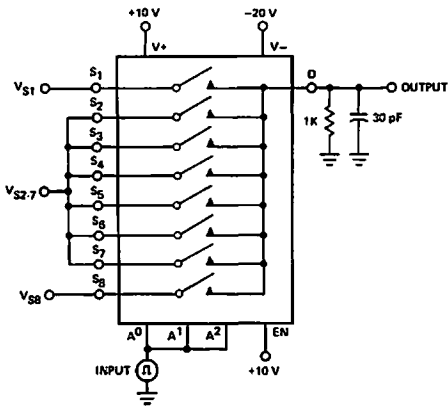
"OFF" Isolation vs R_L and Frequency



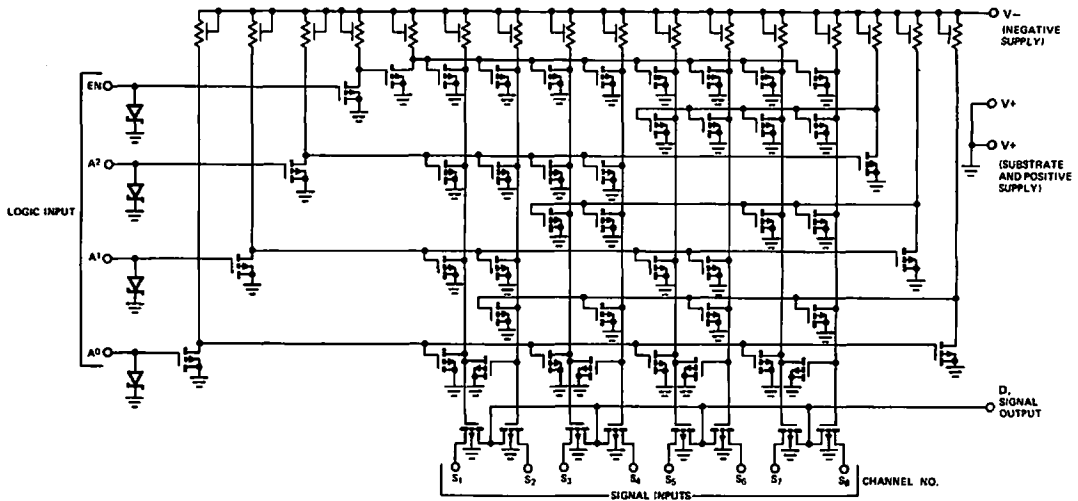
If R_{GEN} , R_L or C_L is increased, there will be proportional increases in rise and/or fall RC times.



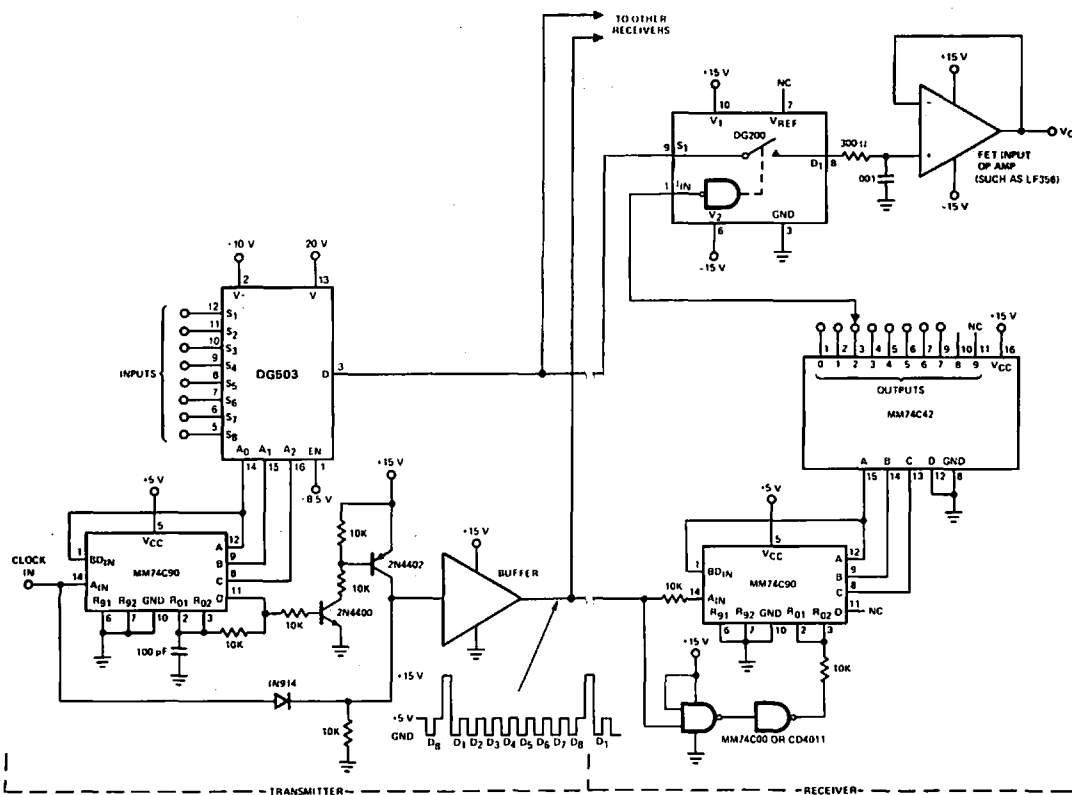
SWITCHING TIME TEST CIRCUIT



SCHEMATIC DIAGRAM



TYPICAL APPLICATION



A One Of 8-channel Transmission System

APPLICATION HINTS*

V ₊ Positive Supply Voltage (V)	V ₋ Negative Supply Voltage (V)	V _{EN} Enable Input Voltage Min High/ Max Low (V)	V _{IN} Logic Input Voltage V _{INH} Min/ V _{INL} Max (V)	V _S or V _D Analog Signal Range (V)
+10**	-20	8.5/0.6	8.5/0.6	-10 to +10
+5	-20	3.5/0.6	3.5/0.6	-10 to +5
+10	-15	8.5/0.6	8.5/0.6	-5 to +10
+5	-15	3.5/0.6	3.5/0.6	-5 to +5

* Application Hints are for DESIGN AID ONLY, not guaranteed and not subject to production testing.

** Electrical parameters chart based on V₊ = +10 V, V₋ = -20 V.

DG506A/DG507A

16-Channel and Dual 8-Channel Analog Multiplexers



FEATURES

- 40 V Power Supply Rating
- Latch Proof
- TTL Compatible
- $rDS(on) < 400 \Omega$
- $\Delta rDS(on) < 6\%$

BENEFITS

- Environmentally Rugged
- Easily Interfaced
- Improved System Accuracy
- Pin Compatible with Harris HI506 Analog Devices AD7506

APPLICATIONS

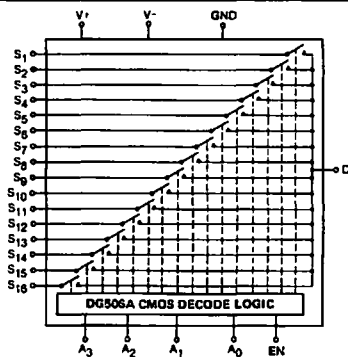
- Data Acquisition Systems
- Communication Systems
- Multiplexing Reference Signals

DESCRIPTION

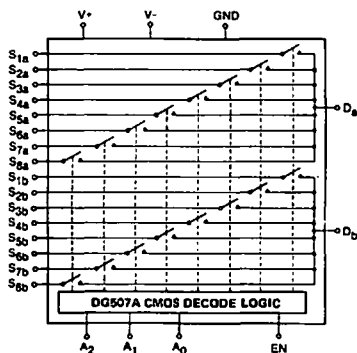
The DG506A and DG507A designed on the Siliconix PLUS-40 CMOS process provide solid state switch action with 400 ohms contact (ON) resistance and very high OFF resistance. True bidirectional switch action takes place over the full analog signal range of ± 15 volts, with Break-Before-Make operation to prevent momentary shorting of signal input. The DG506A provides 16-channel single

ended multiplexing and demultiplexing of ± 15 volt analog signals. The DG507A provides 8-channel differential multiplexing and multiplexing of ± 15 volt common mode plus differential signals. Both devices include on-chip CMOS/TTL compatible binary channel address decoders and chip enable to simplify channel selection and tiering structure.

FUNCTIONAL BLOCK DIAGRAM

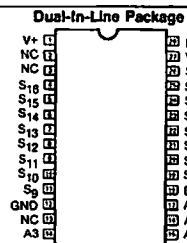


DG506A
16-Channel Single Ended Multiplexer



DG507A
Differential 8-Channel Multiplexer

PIN CONFIGURATION



Order Numbers:

DG506AAR, DG506ABR, or DG506ACR

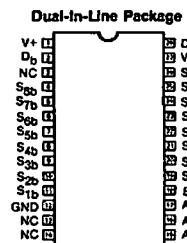
See Package 13

DG506ACK, DG506ABK, or DG506ACK

See Package 24

DG506ACJ

See Package 14



Order Numbers:

DG507AAR, DG507ABR, or DG507ACR

See Package 13

DG507AAK, DG507ABK, or DG507ACK

See Package 24

DG507ACJ

See Package 14

ABSOLUTE MAXIMUM RATINGS

DG506A/DG507A

Voltage Referenced to V-

V+ 44 V

GND 25 V

Digital Inputs¹ V_S, V_D -2 V to (V⁺ +2 V) or
20 mA, whichever occurs first.

Current (Any Terminal, Except S or D) 30 mA

Continuous Current, S or D 20 mA

Peak Current, S or D

(Pulsed at 1 msec, 10% Duty Cycle Max) 40 mA

Storage Temperature (A & B Suffix) -65 to 150°C

(C Suffix) -65 to 125°C

Operating Temperature (A Suffix) -55 to 125°C

(B Suffix) -25 to 85°C

(C Suffix) 0 to 70°C

Power Dissipation (Package)*

28 Pin Ceramic DIP** 1200 mW

28 Pin Plastic DIP*** 625 mW

*All leads soldered or welded to PC board.

**Derate 16 mW/°C above 75°C.

***Derate 8.3 mW/°C above 75°C.

ELECTRICAL CHARACTERISTICS²

T_A = 25°C

	PARAMETER	SYMBOL	TEST CONDITIONS, UNLESS OTHERWISE NOTED: ⁷ V _I = 15 V, V ₋ = -15 V, Ground = 0			LIMITS						UNIT
						DG506AA, 7AA			DG506A B/C, 7A B/C			
						MIN ³	TYP ⁴	MAX	MIN ³	TYP ⁴	MAX	
SWITCH	Analog Signal Range	V _{ANALOG}				-15		15	-15		15	V
	Drain-Source ON Resistance	r _{DS(on)}	V _D = 10 V, I _S = -200 μA	Sequence Each Switch On V _{AL} = 0.8 V, V _{AH} = 2.4 V V _{EN} = 2.4 V		270	400		270	450	Ω	
			V _D = -10 V, I _S = -200 μA			230	400		230	450		
	Greatest Change In Drain-Source ON Resistance Between Channels	Δr _{DS(on)}	$\Delta r_{DS(on)} = \left(\frac{r_{DS(on) \text{ MAX}} - r_{DS(on) \text{ MIN}}}{r_{DS(on) \text{ AVE}}} \right)$ -10 V ≤ V _S ≤ 10 V			6			6		%	
	Source OFF Leakage Current	I _{S(off)}	V _S = 10 V, V _D = -10 V	V _{EN} = 0.8 V, V _{AL} = 0.8 V	-1	0.002	1	-5	0.002	5	nA	
			V _S = -10 V, V _D = 10 V		-1	-0.005	1	-5	-0.005	5		
	Drain OFF Leakage Current	I _{D(off)}	V _D = 10 V, V _S = -10 V		-10	0.02	10	-20	0.02	20		
			V _D = -10 V, V _S = 10 V		-10	-0.03	10	-20	-0.03	20		
			V _D = 10 V, V _S = -10 V		-5	0.007	5	-10	0.007	10		
			V _D = -10 V, V _S = 10 V		-5	-0.015	5	-10	-0.015	10		
Channel ON Leakage Current	I _{D(on)} ⁵	V _{S(all)} = V _D = 10 V	-10	0.03	10	-20	0.03	20				
		V _{S(all)} = V _D = -10 V	-10	-0.06	10	-20	-0.06	20				
		V _{S(all)} = V _D = 10 V	-5	0.015	5	-10	0.015	10				
		V _{S(all)} = V _D = -10 V	-5	-0.03	5	-10	-0.03	10				
INPUT	Address Input Current, Input Voltage High	I _{AH}	V _A = 2.4 V	-10	-0.002		-10	-0.002		μA		
			V _A = 15 V		0.006	10		0.006	10			
	Address Input Current Input Voltage Low	I _{AL}	V _{EN} = 2.4 V	-10	-0.002		-10	-0.002				
			V _{EN} = 0	-10	-0.002		-10	-0.002				
DYNAMIC	Switching Time Of Multiplexer	t _{transition}	See Figure 1			0.6	1		0.6		μs	
	Break-Before-Make Interval	t _{open}	See Figure 3			0.2			0.2			
	Enable Turn-ON Time	t _{on(EN)}	See Figure 2			1			1			
	Enable Turn-OFF Time	t _{off(EN)}				0.4			0.4			
	OFF Isolation ⁶	OIRR	V _{EN} = 0, R _L = 1 kΩ, C _L = 15 pF V _S = 7 VRMS, f = 500 kHz			68			68		dB	
	Source OFF Capacitance	C _{S(off)}	V _S = 0	V _{EN} = 0, f = 140 kHz		6			6		pF	
	Drain OFF Capacitance	C _{D(off)}	V _D = 0			45			45			
DG507A				23			23					
SUPPLY	Positive Supply Current	I ⁺	V _{EN} = 0 V or 5 V, All V _A = 0			1.3	2.4		1.3	2.4	mA	
	Negative Supply Current	I ⁻				-1.5	-0.7		-1.5	-0.7		

NOTES

(See next page)

ELECTRICAL CHARACTERISTICS² (Cont.) T_A = Over Temperature Range

	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: ⁷ V+ = 15 V, V- = -15 V, Ground = 0		LIMITS						UNIT	
					DG506AA, 7AA			DG506A B/C, 7A B/C				
					MIN ³	TYP ⁴	MAX	MIN ³	TYP ⁴	MAX		
SWITCH	Analog Signal Range	V _{ANALOG}			-15		15	-15		15	V	
	Drain-Source ON Resistance	r _{DS(on)}	V _D = 10 V, I _S = -200 μA V _D = -10 V, I _S = -200 μA	Sequence Each Switch On V _{AL} = 0.8 V, V _{AH} = 2.4 V V _{EN} = 2.4 V			500			550	Ω	
	Source OFF Leakage Current	I _{S(off)}	V _S = 10 V, V _D = -10 V V _S = -10 V, V _D = 10 V	V _{EN} = 0.8 V, V _{AL} = 0.8 V	-50		50	-50		50	nA	
	Drain OFF Leakage Current	DG506A DG507A	I _{D(off)}		V _D = 10 V, V _S = -10 V V _D = -10 V, V _S = 10 V V _D = 10 V, V _S = -10 V V _D = -10 V, V _S = 10 V	-300		300	-300			300
					-300		300	-300		300		
					-200		200	-200		200		
				-200		200	-200		200			
	Channel ON Leakage Current	DG506A DG507A	I _{D(on)} ⁵	V _{S(all)} = V _D = 10 V V _{S(all)} = V _D = -10 V V _{S(all)} = V _D = 10 V V _{S(all)} = V _D = -10 V	Sequence Each Switch On V _{AL} = 0.8 V, V _{AH} = 2.4 V V _{EN} = 2.4 V	-300		300	-300			300
	-300			300	-300		300					
	-200			200	-200		200					
INPUT	Address Input Current, Input Voltage High	I _{AH}	V _A = 2.4 V V _A = 15 V		-30			-30			μA	
	Address Input Current Input Voltage Low	I _{AL}	V _{EN} = 2.4 V V _{EN} = 0	All V _A = 0	-30			-30		30		

NOTES:

1. Signals on S_X , D_X , or I_{N_X} exceeding V_+ or V_- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
2. Refer to PROCESS OPTION FLOWCHART for additional information.
3. The algebraic convention whereby the most negative value is a minimum, and the most positive value is a maximum, is used in this data sheet.
4. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
5. $I_{\text{D(on)}}$ is leakage from driver into "ON" switch.
6. OFF position = $20 \log \frac{V_D}{V_S}$. V_S = input to "OFF" switch, V_D = output due to V_S .
7. Functional operation is possible for supply voltage less than 15 V, but the input logic threshold will shift.

TRUTH TABLES
DG506A

A_3	A_2	A_1	A_0	EN	ON SWITCH
X	X	X	X	0	NONE
0	0	0	0	1	1
0	0	0	1	1	2
0	0	1	0	1	3
0	0	1	1	1	4
0	1	0	0	1	5
0	1	0	1	1	6
0	1	1	0	1	7
0	1	1	1	1	8
1	0	0	0	1	9
1	0	0	1	1	10
1	0	1	0	1	11
1	0	1	1	1	12
1	1	0	0	1	13
1	1	0	1	1	14
1	1	1	0	1	15
1	1	1	1	1	16

DG507A

A_2	A_1	A_0	EN	ON SWITCH
X	X	X	0	NONE
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

Logic "0" = $V_{\text{AL}} \leq 0.8\text{ V}$, Logic "1" = $V_{\text{AH}} \geq 2.4\text{ V}$

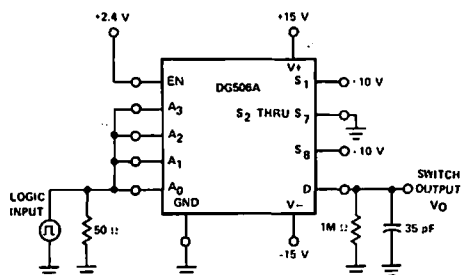


Figure 1(a)

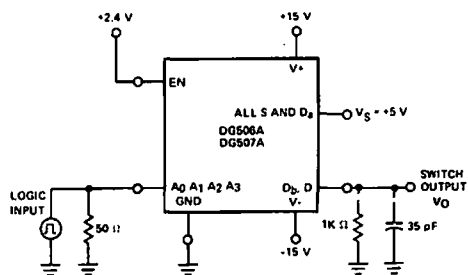


Figure 3

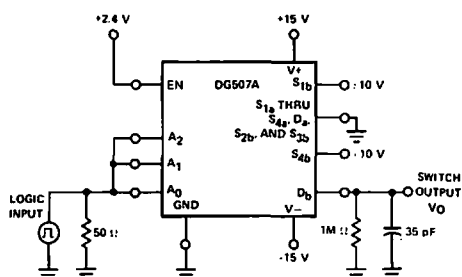


Figure 1(b)

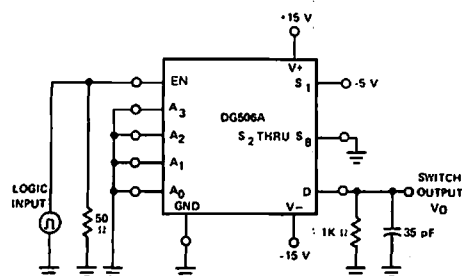


Figure 2(a)

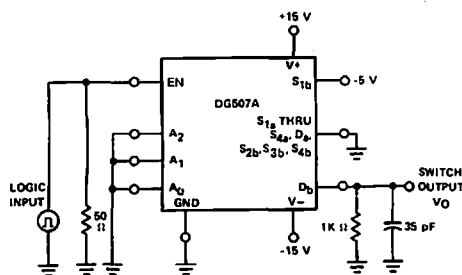
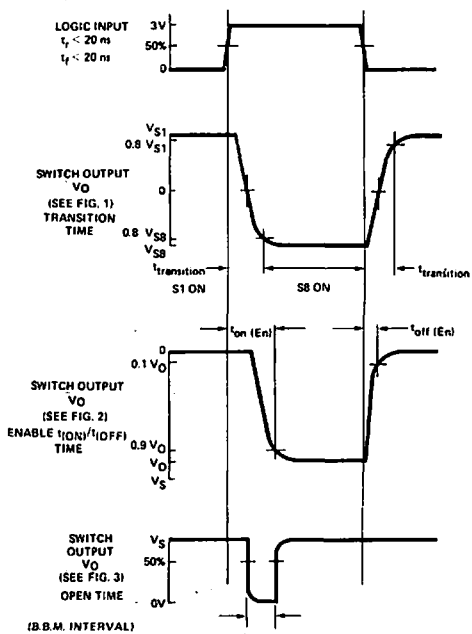
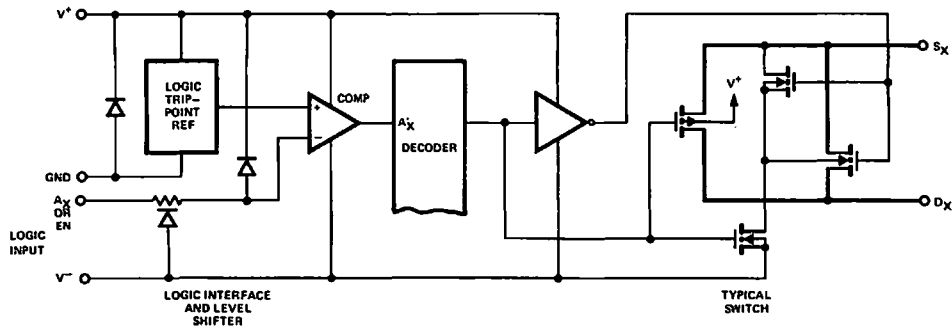


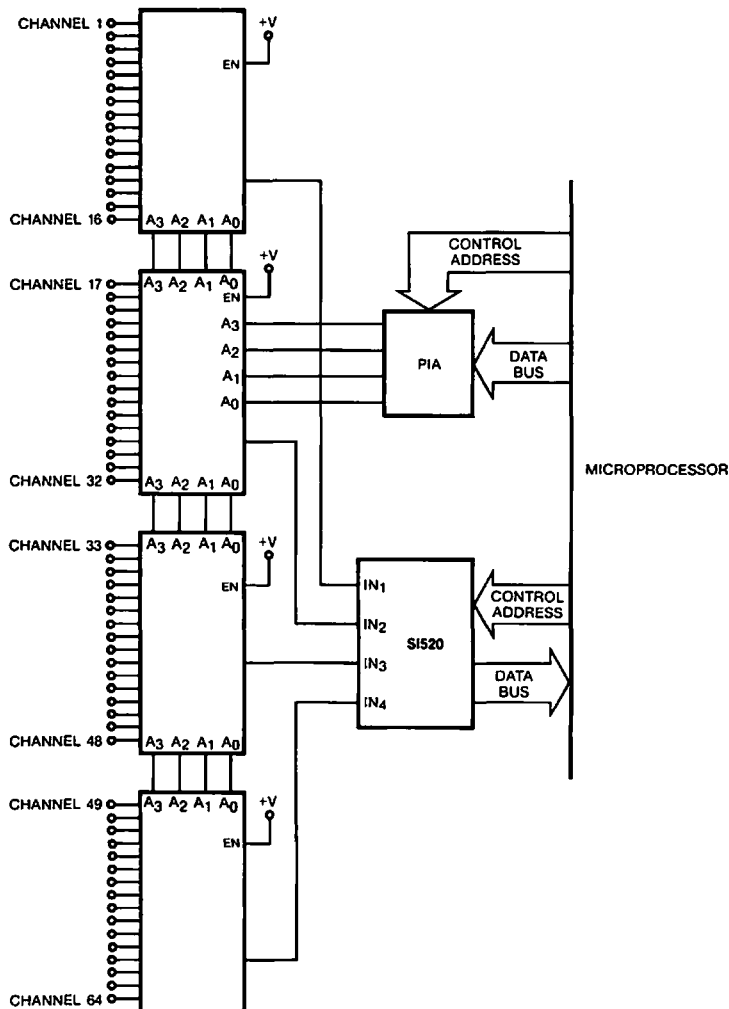
Figure 2(b)

Timing Diagrams For Figure 1, 2 & 3
Figure 4

SCHEMATIC DIAGRAM



APPLICATIONS



64-Channel 2-Level Multiplex System

DG508A/DG509A

8-Channel/Dual 4-Channel

CMOS Analog Multiplexer



FEATURES

- DTL, TTL & CMOS Direct Control Over Military Temperature Range
- 30 mW (typ) Quiescent Power
- Make-Before-Break Switching
- 44 V Power Supply Rating
- Latch Proof

BENEFITS

- Easily Interfaced
- Low Power
- Reduced System Cross-Talk
- Environmentally Rugged

APPLICATIONS

- Communication Systems
- Multiplexing Reference Signals
- Data Acquisition Systems

DESCRIPTION

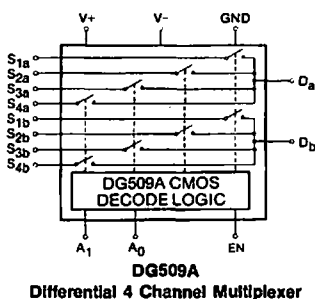
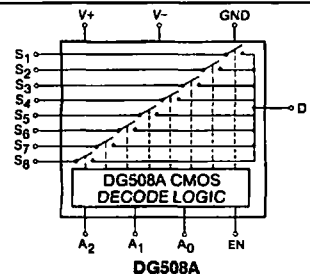
DG508A and DG509A are 8 and 4-channel analog multiplexers, respectively, designed for selecting 1 of 8 (or 4) analog input signals and connecting it to a common output or, conversely, routing an analog signal to 1 of 8 (or 4) output loads. This latter mode is commonly called demultiplexing. Break-Before-Make switching action protects against momentary shorting of the input signals.

DG508A, an 8-channel single-ended analog multiplexer, is designed to connect 1 of 8 inputs to a common output as determined by a 3-bit binary address (A_0, A_1, A_2). DG509A, a 4-channel differential analog multiplexer, is designed to connect 1 of 4 differential inputs to a common differential output as determined by its 3 bit binary address (A_0, A_1, A_2) logic.

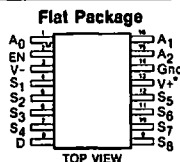
A channel in the ON state conducts current equally well in both directions (bidirectional switches). In the OFF state each channel blocks voltages up to the power supply rails, normally 30 V peak-to-peak. An enable (EN) function allows the user to reset the multiplexer/demultiplexer to all switches OFF. All control inputs, address (A_X) and enable (EN) are TTL or CMOS compatible over the full specified operating temperature range.

Both DG508A and DG509A are available in dual-in-line ceramic and plastic packages, and are specified for operation over the military (-55 to 125°C), industrial (-25 to 85°C), and commercial (0 to 70°C), temperature ranges.

FUNCTIONAL BLOCK DIAGRAM

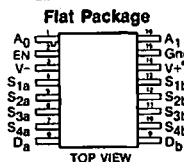


PIN CONFIGURATION

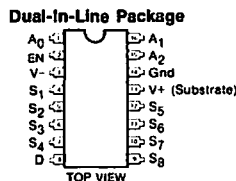


Order Number:
DG508AAL
See Package 17

*Common to Substrate and Base of Package

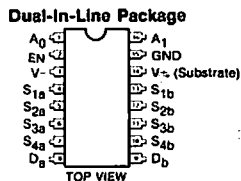


Order Number:
DG509AAL
See Package 17



Order Numbers:
DG508AAK, DG508ABK, or DG508ACK
See Package 10

DG508ACJ
See Package 8



Order Numbers:
DG509AAK, DG509ABK, or DG509ACK
See Package 10

DG509ACJ
See Package 8

ABSOLUTE MAXIMUM RATINGS

Voltage Referenced to V-

V+ 44 V

GND 25 V

 Digital Inputs¹, V_S, V_D -2 V to (V+ + 2 V) or
20 mA, whichever occurs first.

Current (Any Terminal, Except S or D) 30 mA

Continuous Current, S or D 20 mA

Peak Current, S or D

(Pulsed at 1 msec, 10% Duty Cycle Max) 40 mA

Operating Temperature (A Suffix) -55 to 125°C

(B Suffix) -20 to 85°C

(C Suffix) 0 to 70°C

Storage Temperature (A & B Suffix) -65 to 150°C

(C Suffix) -65 to 125°C

Power Dissipation (Package)*

16 Pin Ceramic DIP** 900 mW

16 Pin Plastic DIP*** 470 mW

Flat Package**** 750 mW

*All leads soldered or welded to PC board.

**Derate 12 mW/°C above 75°C.

***Derate 6.3 mW/°C above 75°C.

****Derate 10 mW/°C above 75°C.

ELECTRICAL CHARACTERISTICS²

 T_A = 25°C

	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: V+ = 15 V, V- = 15 V, Ground = 0	LIMITS						UNIT			
				DG508AA DG509AA			DG508A B/C DG509A B/C						
				MIN ³	TYP ⁴	MAX	MIN ³	TYP ⁴	MAX				
SWITCH	Analog Signal Range	V _{ANALOG}		-15		15	-15		15	V			
	Drain-Source ON Resistance	r _{DS(on)}	V _D = 10 V, I _S = -200 μA V _D = -10 V, I _S = -200 μA	Sequence Each Switch On V _{AL} = 0.8 V, V _{AH} = 2.4 V				270 230	400 400		270 230	450 450	Ω
	Greatest Change In Drain Source ON Resistance Between Channels	Δr _{DS(on)}	$\Delta r_{DS(on)} = \left(\frac{r_{DS(on)}^{MAX} - r_{DS(on)}^{MIN}}{r_{DS(on)}^{AVE}} \right)$ -10 V ≤ V _S ≤ 10 V				6		6		%		
	Source OFF Leakage Current	I _{S(off)}	V _S = 10 V, V _D = -10 V V _S = -10 V, V _D = 10 V	V _{EN} = 0				0.002 -1	1 -0.005		0.002 -5	5 -0.005	
	Drain OFF Leakage Current	DG508A	V _D = 10 V, V _S = -10 V V _D = -10 V, V _S = 10 V					0.01 -10	10 -0.015		0.01 -20	20 -0.015	
		DG509A	V _D = 10 V, V _S = -10 V V _D = -10 V, V _S = 10 V					0.005 -10	10 -0.008		0.005 -20	20 -0.008	
	Drain ON Leakage Current	DG508A	V _{S(all)} = V _D = 10 V V _{S(all)} = V _D = -10 V	Sequence Each Switch On V _{AL} = 0.8 V, V _{AH} = 2.4 V				0.015 -10	10 -0.03		0.015 -20	20 -0.03	
		DG509A	V _{S(all)} = V _D = 10 V V _{S(all)} = V _D = -10 V					0.007 -10	10 -0.015		0.007 -20	20 -0.015	
	INPUT	Address Input Current, Input Voltage High	I _{AH}	V _A = 2.4 V V _A = 15 V		-10	-0.002		-10	-0.002		μA	
		Address Input Current Input Voltage Low	I _{AL}	V _{EN} = 2.4 V V _{EN} = 0	All V _A = 0			-10	-0.002		-10	-0.002	
DYNAMIC	Switching Time Of Multiplexer	t _{transition}	See Figure 1		0.6	1		0.6					
	Break-Before-Make Interval	t _{open}	See Figure 3		0.2			0.2				μs	
	Enable Turn-ON Time	t _{on(EN)}	See Figure 2		1	1.5		1					
	Enable Turn-OFF Time	t _{off(EN)}			0.4	1		0.4					
	OFF Isolation ⁶	OIRR	V _{EN} = 0, R _L = 1 kΩ, C _L = 15 pF V _S = 7 VRMS, f = 500 kHz		68			68				dB	
	Source OFF Capacitance	C _{S(off)}	V _S = 0	V _{EN} = 0, f = 140 kHz				5			5		
	Drain OFF Capacitance	DG508A	V _D = 0					25			25		
DG509A							12			12			
SUPPLY	Positive Supply Current	I+	V _{EN} = 2.4 V	All V _A = 0, or 2.4 V				1.3	2.4		1.3	2.4	
	Negative Supply Current	I-						-1.5	-0.7		-1.5	-0.7	
	Positive Supply Current	I+ Standby	V _{EN} = 0 V					1.3	2.4		1.3	2.4	
	Negative Supply Current	I- Standby						-1.5	-0.7		-1.5	-0.7	

NOTES:

1. Signals on S_X, D_X, or I_{NX}, exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
2. Refer to PROCESS OPTION FLOWCHART for additional information.
3. The algebraic convention whereby the most negative value is a minimum, and the most positive is a maximum, is used in this data sheet.
4. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
5. OFF isolation = 20 log $\frac{|V_S|}{|V_D|}$, V_S = input to "OFF" switch, V_D = output due to V_S.
6. I_{D(on)} is leakage from driver into "ON" switch.

ELECTRICAL CHARACTERISTICS² (Cont.) T_A = Over Temperature Range

	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: V ⁺ = 15 V, V ⁻ = 15 V, Ground = 0		LIMITS						UNIT
					DG508AA DG509AA			DG508A B/C DG509A B/C			
					MIN ³	TYP ⁴	MAX	MIN ³	TYP ⁴	MAX	
SWITCH	Analog Signal Range	V _{ANALOG}			-15		15	-15		15	V
	Drain-Source ON Resistance	r _{DS(on)}	V _D = 10 V, I _S = -200 μA V _D = -10 V, I _S = -200 μA	Sequence Each Switch On V _{AL} = 0.8 V, V _{AH} = 2.4 V			500			550	Ω
	Source OFF Leakage Current	I _{S(off)}	V _S = 10 V, V _D = -10 V V _S = -10 V, V _D = 10 V	V _{EN} = 0			50			50	
	Drain OFF Leakage Current	I _{D(off)}	V _D = 10 V, V _S = -10 V				200		200		
			V _D = -10 V, V _S = 10 V				-200		-200		
			V _D = 10 V, V _S = -10 V				100		100		
			V _D = -10 V, V _S = 10 V				-100		-100		
	Drain ON Leakage Current	DG508A DG509A	I _{D(on)} ⁵	V _{S(all)} = V _D = 10 V V _{S(all)} = V _D = -10 V V _{S(all)} = V _D = 10 V V _{S(all)} = V _D = -10 V	Sequence Each Switch On V _{AL} = 0.8 V, V _{AH} = 2.4 V			200		200	
	DG508A				-200		-200				
	DG509A				100		100				
DG509A				-100		-100					
INPUT	Address Input Current, Input Voltage High	I _{AH}	V _A = 2.4 V		-30			-30			μA
			V _A = 15 V				30		30		
	Address Input Current Input Voltage Low	I _{AL}	V _{EN} = 2.4 V		-30			-30			
			V _{EN} = 0		All V _A = 0	-30			-30		

NOTES:

1. Signals on S_X , D_X , or IN_X , exceeding V^+ or V^- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
2. Refer to PROCESS OPTION FLOWCHART for additional information.
3. The algebraic convention whereby the most negative value is a minimum, and the most positive is a maximum, is used in this data sheet.
4. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
5. OFF isolation = $20 \log \frac{|V_S|}{|V_D|}$, V_S = input to "OFF" switch, V_D = output due to V_S .
6. $I_{\text{D(on)}}$ is leakage from driver into "ON" switch.

TRUTH TABLES
DG508A

A_2	A_1	A_0	EN	ON SWITCH
X	X	X	0	NONE
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

DG509A

A_1	A_0	EN	ON SWITCH
X	X	0	NONE
0	0	1	1
0	1	1	2
1	0	1	3
1	1	1	4

Logic "0" = $V_{\text{AL}} \leq 0.8\text{ V}$, Logic "1" = $V_{\text{AH}} \geq 2.4\text{ V}$

SWITCHING TIME TEST CIRCUIT

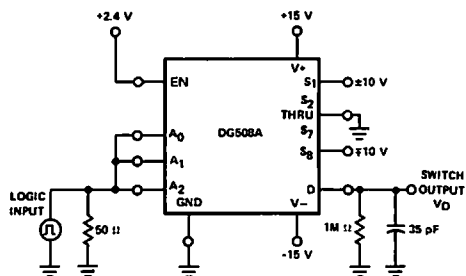


Figure 1(a)

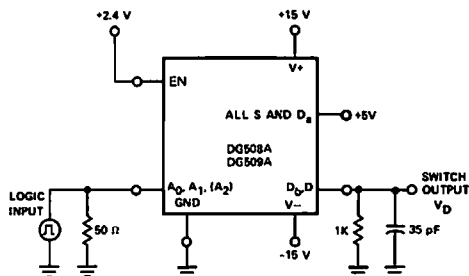


Figure 3

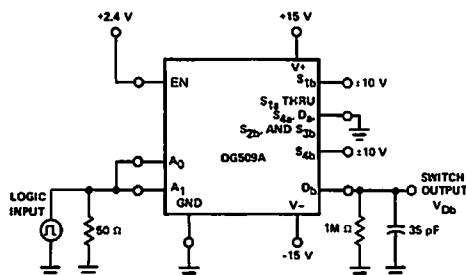


Figure 1(b)

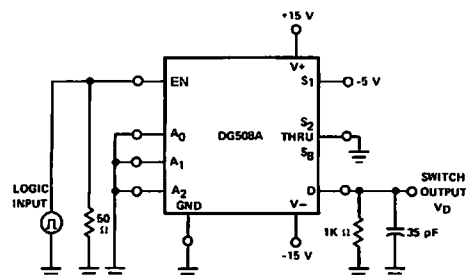


Figure 2(a)

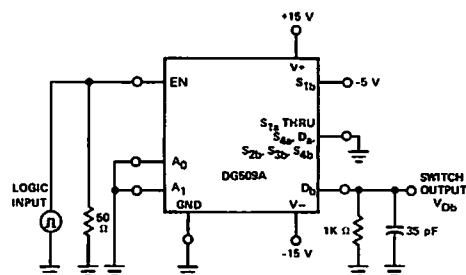
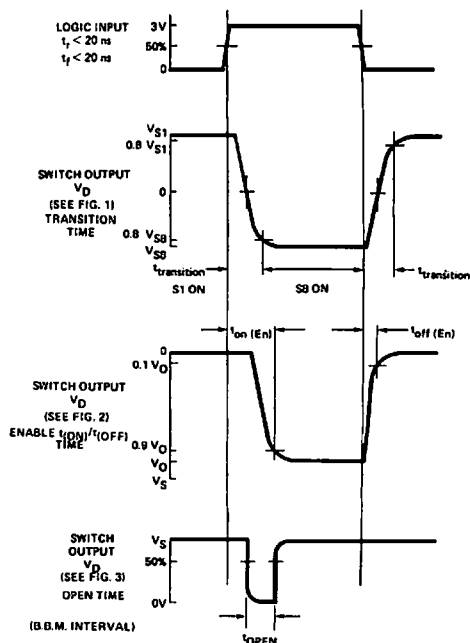


Figure 2(b)



Timing Diagram For Figure 1, 2 & 3
Figure 4

APPLICATION HINTS

Logic Inputs

Logic input circuitry protects the input MOS gate from static transients. A series MOS device shuts off when V_{IN} exceeds the positive power supply. Negative transients are clamped to ground by a diode clamp.

The input voltage characteristics have a current spike

V+	V-	V _{IN} Logic Input Voltage	V _S or V _D Analog Voltage Range
Positive Supply Voltage (V)	Negative Supply Voltage (V)	V _{INH} Min/ V _{INL} Max (V)	
+15**	-15	2.4/0.8	-15 to +15
+12	-12	2.4/0.8	-12 to +12
+10	-10	2.4/0.6	-10 to +10
+8***	-8	2.4/0.4	-8 to +8

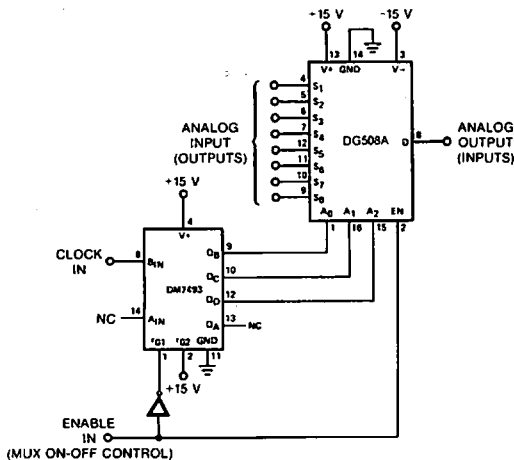
*Application Hints are for DESIGN AID ONLY, not guaranteed and not subject to production testing.

**Electrical Characteristics chart based on V+ = +15 V, V- = -15 V.

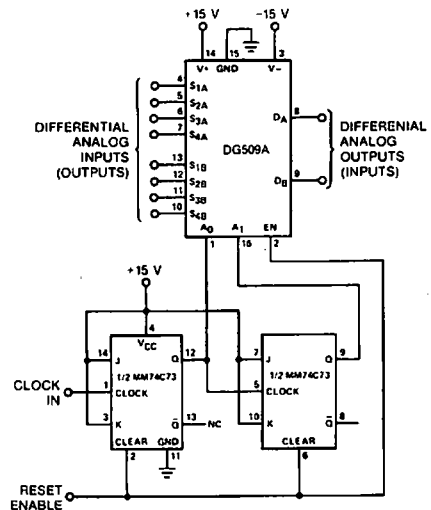
***Operation below ±8 V is not recommended due to the shift in V_{INL}(MAX).

TYPICAL APPLICATIONS

8 Channel Sequential Mux/Demux



Differential 4 Channel Sequential Mux/Demux



Truth Table

	ENABLE	MUX SEQUENCE RATE	MUX INPUTS			DG508A SWITCH PAIR STATES (-DENOTES OFF)							
			A ₀	A ₁	A ₂	S1	S2	S3	S4	S5	S6	S7	S8
DG508A	0	0	X	X	X	-	-	-	-	-	-	-	-
	1	0	0	0	0	ON	-	-	-	-	-	-	-
	1	1 pulse	1	0	0	-	ON	-	-	-	-	-	-
	1	2 pulses	0	1	0	-	-	ON	-	-	-	-	-
	1	3 pulses	1	1	0	-	-	-	ON	-	-	-	-
	1	4 pulses	0	0	1	-	-	-	-	ON	-	-	-
	1	5 pulses	1	0	1	-	-	-	-	-	ON	-	-
	1	6 pulses	0	1	1	-	-	-	-	-	-	ON	-
	1	7 pulses	1	1	1	-	-	-	-	-	-	-	ON
	1	8 pulses	0	0	0	ON	-	-	-	-	-	-	-

DG526/DG527

16-Channel and Dual 8-Channel Latchable Multiplexers



FEATURES

- Microprocessor Bus Compatible
- Accepts 300 nS Write Pulse Width
- Direct RESET
- TTL Compatible
- ΔR_{DS} (on) Channel to Channel Less Than 6%

BENEFITS

- Reduced Parts Count
- Directly Interface with Bus
- Sets up to Known Condition
- No Pull-Up Resistors Required

APPLICATIONS

- Data Acquisition System
- Automatic Test Equipment
- Communication Systems
- Microprocessor Controlled System

DESCRIPTION

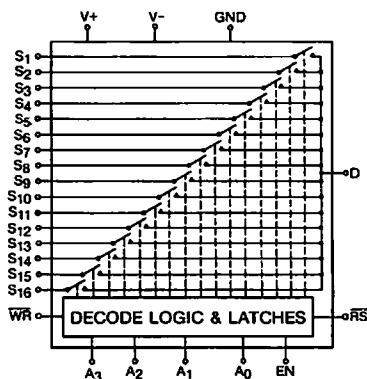
DG526 and DG527 are 16 and 8-channel analog multiplexers, respectively, with on-chip address and control latches to simplify design in microprocessor based applications. Break-Before-Make switching action protects against momentary shorting of the input signals. Designed on the Siliconix PLUS-40 CMOS process, each bi-directional switch features low 400 Ω ON resistance over the full analog range, and will block signals to 30 V peak-to-peak in the unselected channels. All logic levels are TTL compatible.

DG526 is a 16-channel single-ended analog multiplexer designed to connect 1 of 16 inputs to a common output as determined by a 3 bit binary address (A_0, A_1, A_2). DG527, an 8-channel differential analog multiplexer, is designed to connect 1 of 8 differential inputs to a common differential output as determined by its 3 bit binary address (A_0, A_1, A_2) logic.

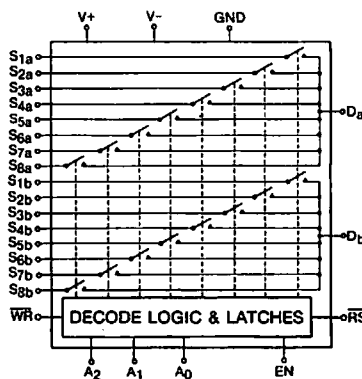
The enable (EN) pin is used to enable the address latches during the $\overline{WR}$ pulse. It can be hard wired to the logic supply if one of the channels will always be used (except during a reset) or it can be tied to address decoding circuitry for memory mapped operation. The $\overline{RS}$ pin is used as a master reset. All latches are cleared regardless of the state of any other latch or control line. The $\overline{WR}$ pin is used to transfer the state of the address control lines to their latches, except during a reset or when EN is low (see Tables 1 and 2).

Both DG526 and DG527 are available in dual-in-line Cerdip and plastic packages, and are specified for operation over the popular military (-55 to 125°C), industrial (-25 to 85°C), and commercial (0 to 70°C), temperature ranges.

FUNCTIONAL BLOCK DIAGRAM



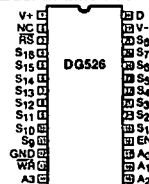
DG526
16 CHANNEL SINGLE ENDED MULTIPLEXER



DG527
DIFFERENTIAL 8 CHANNEL MULTIPLEXER

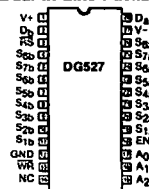
PIN CONFIGURATION

Dual-In-Line Package



TOP VIEW

Dual-In-Line Package



TOP VIEW

Order Numbers:
DG526AK, DG526BK, DG526CK
DG527AK, DG527BK, DG527CK
See Package 24
DG526CJ or DG527CJ
See Package 14

ABSOLUTE MAXIMUM RATINGS

Voltages referenced to V-

V+ 44 V

GND 25 V

Digital Inputs¹, V_S, V_D -2 V to (V+ + 2 V) or
20 mA, whichever occurs first.

Current (Any Terminal Except S or D) 30 mA

Continuous Current, S or D 20 mA

Peak Current, S or D

(Pulsed at 1 msec, 10% Duty Cycle Max.) .. 40 mA

Operating Temperature (A Suffix) -55 to 125°C

(B Suffix) -25 to 85°C

(C Suffix) 0 to 70°C

Storage Temperature (A & B Suffix) -65 to 150°C

(C Suffix) -65 to 125°C

ELECTRICAL CHARACTERISTICS²(T_A = 25°C)

	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: ⁷ V _I = 15 V, V _O = 15, Ground 0 WR = 0, RS = 2.4 V	LIMITS			UNIT
				MIN ³	TYP ⁴	MAX	
SWITCH	Analog Signal Range	V _{ANA-LOG}		-15		+15	V
	Drain - Source ON Resistance	r _{DS(on)}	V _D = + or -10 V, V _{AL} = 0.8 V I _S = -200 μA, V _{AH} = 2.4 V Sequence Each Switch ON		250	400	Ω
	Greatest Change in r _{DS(on)} Between Channels	Δr _{DS(on)}	$\Delta r_{DS(on)} = \frac{(r_{DS(on)MAX} - r_{DS(on)MIN})}{r_{DS(on)AVE}}$ -10V ≤ V _S ≤ 10V		6		%
	Source OFF Leakage Current	I _{S(OFF)}	V _S = 10 V, V _D = -10 V or V _{ON} = 0 V _S = -10 V, V _D = 10 V	-1	0.02	1	nA
	Drain OFF Leakage	I _{D(OFF)}	V _D = 10 V, V _S = -10 V V _D = -10 V, V _S = 10 V V _{EN} = 0	-10	0.2	10	
				-5	0.2	5	
	Drain ON Leakage	I _{D(on)} ⁵	V _{S(alt)} = V _D = 10 V V _{S(alt)} = V _D = -10 V Sequence Each Switch ON V _{AL} = 0.8 V, V _{AH} = 2.4 V V _{EN} = 2.4 V	-10	0.2	10	nA
				-5	0.2	5	
INPUT	Logic Input Current Input Voltage High	I _{AH}	V _A = 2.4 V	-10	0.02	10	μA
			V _A = 15 V	-10	0.02	10	
	Logic Input Current Input Voltage Low	I _{AL}	V _{EN} = 0, 2.4 V All V _A = 0 WR = 0, RS = 0	-10	0.01	10	μA
DYNAMIC	Switching Time Of Multiplexer	t _{transition}	See Figure 3		0.65	1	μs
	Break-Before-Make Interval	t _{open}	See Figure 5		0.2		
	Enable Turn ON Time	t _{on} (EN, WR)	See Figure 4 & 6		0.7	1.5	
	Enable And Reset Turn OFF Time	t _{off} (EN, RS)	See Figure 4 & 7		0.4	1	
	Charge Coupling (Injection)	O	See Figure 8		10		pC
	OFF Isolation ⁶		V _{EN} = 0, R _L = 1 kΩ, C _L = 15 pF V _S = 7 VRMS, f = 500 kHz		55		dB
	Logic Input Capacitance	C _{in}	f = 1 MHz		6		pF
	Source OFF Capacitance	C _{S(OFF)}	V _S = 0, V _{EN} = 0 f = 140 kHz		10		
	Drain OFF Capacitance	C _{D(OFF)}	V _D = 0, V _{EN} = 0		35		
			f = 140 kHz		35		
SUPPLY	Positive Supply Current	I ₊	V _{EN} = 0V All V _A = 0		2.0	3.0	mA
	Negative Supply Current	I ₋		-2.0	-1.2		

NOTES:

1. Signals on S_X, D_X, or I_{N_X} exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
2. Refer to PROCESS OPTION FLOWCHART for additional information.
3. The algebraic convention whereby the most negative value is a minimum, and the most positive is a maximum, is used in this data sheet.
4. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
5. I_{D(on)} is leakage from driver into "ON" switch.
6. OFF isolation = 20 log $\frac{|V_S|}{|V_D|}$, V_S = input to "OFF" switch, V_D = output due to V_S.
7. Period of Reset (RS) pulse must be at least 50 μs during or after power ON.

ELECTRICAL CHARACTERISTICS² (Cont.)
T_A = Over Temperature Range

	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: ⁷ V ₊ = 15 V, V ₋ = -15, Ground = 0 WR = 0, RS = 2.4 V	LIMITS			UNIT
				MIN ³	TYP ⁴	MAX	
SWITCH	Minimum Analog Signal Handling Capability	V _{ANA-LOG}		-15		+15	V
	Drain - Source ON Resistance	r _{DS(on)}	V _D = + or -10 V, V _{AL} = 0.8 V I _S = -200 μA, V _{AH} = 2.4 V Sequence Each Switch ON		380	500	Ω
	Greatest Change In r _{DS(on)} Between Channels	Δr _{DS(on)}	$\Delta r_{DS(on)} = \frac{(r_{DS(on)MAX} - r_{DS(on)MIN})}{r_{DS(on)AVE}}$ -10V ≤ V _S ≤ 10V		6		%
	Source OFF Leakage Current	I _{S(OFF)}	V _S = 10 V, V _D = -10 V or V _{ON} = 0 V _S = -10 V, V _D = 18 V	-50	0.1	50	nA
	Drain OFF Leakage	DG526 DG527	V _D = 10 V, V _S = -10 V V _D = -10 V, V _S = 10 V V _{EN} = 0	-300	0.2	300	
	Drain ON Leakage	DG526 DG527		-200	0.2	200	
INPUT	Logic Input Current Input Voltage High	I _{AH}	V _A = 2.4 V	-30	-0.25	30	μA
	Logic Input Current Input Voltage Low	I _{AL}	V _{EN} = 0, 2.4 V All V _A = 0 WR = 0, RS = 0	-30	0.25	30	
				-10	0.25	10	
DYNAMIC	Switching Time Of Multiplexer	t _{transition}	See Figure 3		0.88	1.3	μs
	Break-Before-Make Interval	t _{open}	See Figure 5	5			ns
	Enable Turn ON Time	t _{on} (EN, WR)	See Figure 4 & 6		0.95	1.8	μs
	Enable And Reset Turn OFF Time	t _{off} (EN, RS)	See Figure 4 & 7		0.5	1.2	
SUPPLY	Positive Supply Current	I ₊	V _{EN} = 0V All V _A = 0		3.0	4.5	mA
	Negative Supply Current	I ₋		-3.2	-2.0		

MINIMUM INPUT TIMING REQUIREMENTS
(T_A = Over Temperature Range)

PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: ⁷ V ₊ = 15 V, V ₋ = -15, Ground = 0 WR = 0, RS = 2.4 V	LIMITS			UNIT
			MIN ³	TYP ⁴	MAX	
WRITE Pulse Width	t _{WW}	See Figure 1	300	260		ns
A, EN Data Valid to WRITE (Stabilization Time)	t _{DW}		180	150		
A, EN Data Valid after WRITE (Hold Time)	t _{WD}		30	20		
RESET Pulse Width	t _{RS}	See Figure 2 V _S = 5V	500	350		

NOTES:

1. Signals on S_X, D_X, or I_{NX}, exceeding V₊ or V₋ will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
2. Refer to PROCESS OPTION FLOWCHART for additional information.
3. The algebraic convention whereby the most negative value is a minimum, and the most positive is a maximum, is used in this data sheet.
4. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
5. I_{D(on)} is leakage from driver into "ON" switch.
6. OFF isolation = 20 log $\frac{|V_S|}{|V_D|}$, V_S = Input to "OFF" switch, V_D = output due to V_S.
7. Period of Reset (RS) pulse must be at least 50 μs during or after power ON.

Table 1

	A ₃	A ₂	A ₁	A ₀	EN	$\overline{WR}$	$\overline{RS}$	ON Switch
Latching	X	X	X	X	X	$\overline{1}$	1	Maintains previous switch state
Reset	X	X	X	X	X	X	0	None (latches cleared)
	X	X	X	X	0	0	1	None
	0	0	0	0	1	0	1	1
	0	0	0	1	1	0	1	2
	0	0	1	0	1	0	1	3
	0	0	1	1	1	0	1	4
	0	1	0	0	1	0	1	5
	0	1	0	1	1	0	1	6
	0	1	1	0	1	0	1	7
Transparent Operation	0	1	1	1	1	0	1	8
	1	0	0	0	1	0	1	9
	1	0	0	1	1	0	1	10
	1	0	1	0	1	0	1	11
	1	0	1	1	1	0	1	12
	1	1	0	0	1	0	1	13
	1	1	0	1	1	0	1	14
	1	1	1	0	1	0	1	15
	1	1	1	1	1	0	1	16

Decode Truth Table-DG526

Table 2

	A ₂	A ₁	A ₀	EN	$\overline{WR}$	$\overline{RS}$	ON Switch
Latching	X	X	X	X	$\overline{1}$	1	Maintains previous switch state
Reset	X	X	X	X	X	0	None (latches cleared)
	X	X	X	0	0	1	None
	0	0	0	1	0	1	1
Transparent Operation	0	0	1	1	0	1	2
	0	1	0	1	0	1	3
	0	1	1	1	0	1	4
	1	0	0	1	0	1	5
	1	0	1	1	0	1	6
	1	1	0	1	0	1	7
	1	1	1	1	0	1	8

Decode Truth Table-DG527

TIMING DIAGRAMS

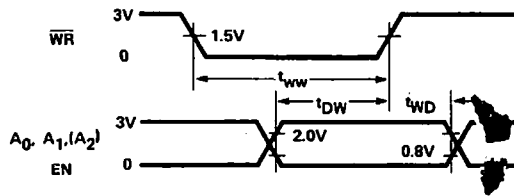


Figure 1

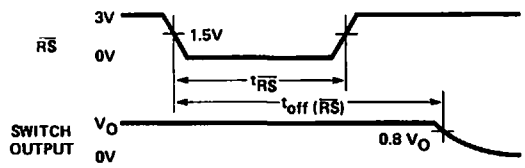
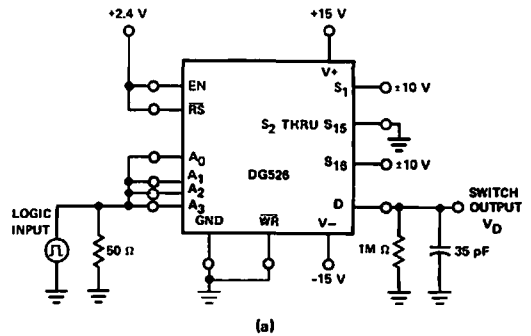
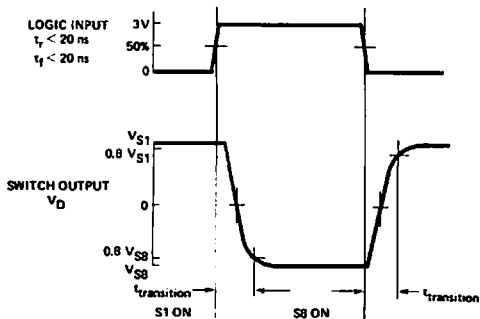
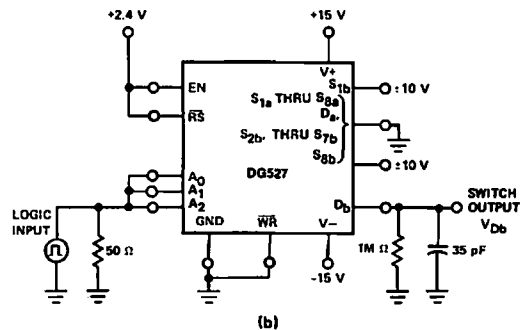


Figure 2

SWITCHING TIME TEST CIRCUITS



(a)



(b)

Transition Time Test Circuit
Figure 3

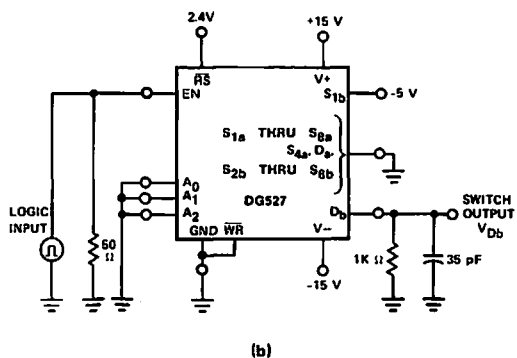
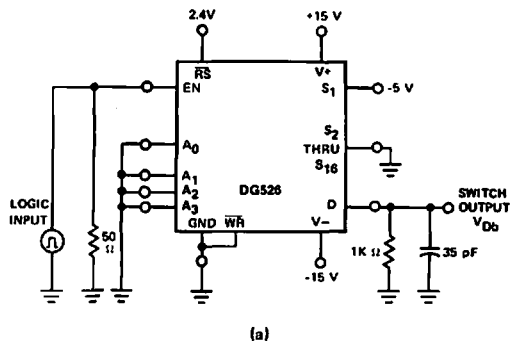
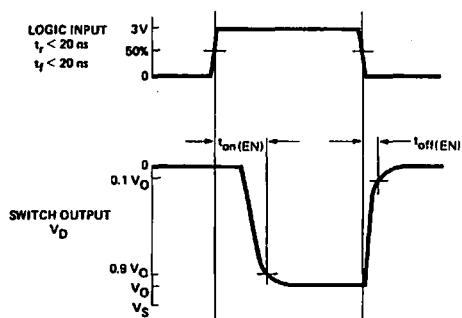
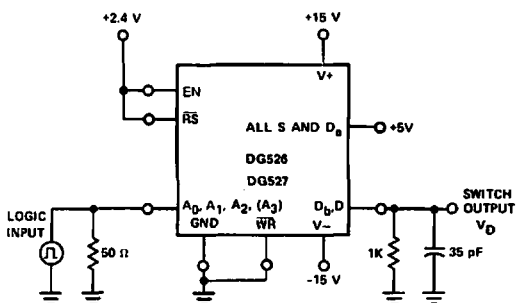
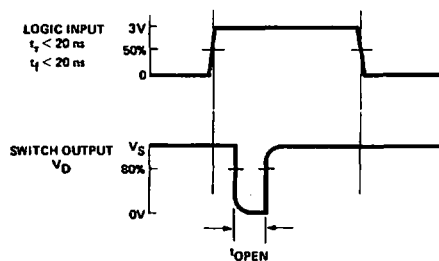
Enable t_{on}/t_{off} Time

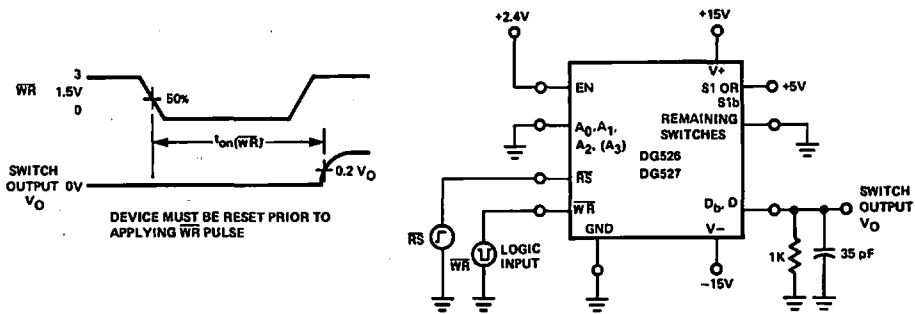
Figure 4



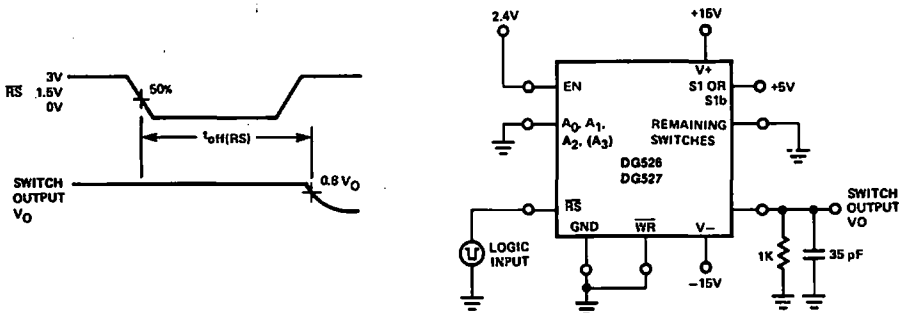
Open Time (B.B.M. Interval)

Figure 5

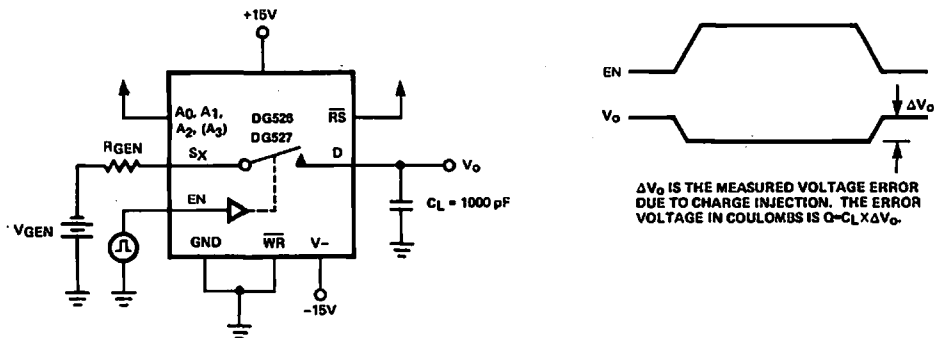
SWITCHING TIME TEST CIRCUITS(Cont.)



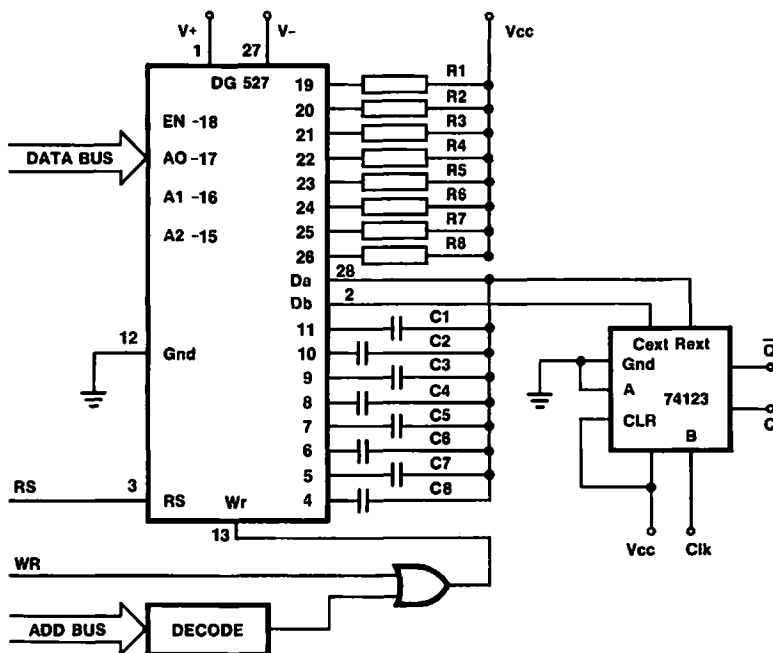
Write Turn-On Time $t_{on}(\overline{WR})$
Figure 6



Reset Turn-Off Time $t_{off}(\overline{RS})$
Figure 7



Charge Injection Test Circuit
Figure 8



μP Selected Pulse Width Control
Figure 9

Figure illustrates one use of the DG527. Differential multiplexers are generally used in process control applications to eliminate errors due to common mode signals. In this circuit however, advantage is taken of the dual multiplexing capability of the switch. This is achieved by using the

multiplexer to select pairs of R.C. networks to control the pulse width of the multivibrator. This can be a particularly useful feature in process control applications where there is a requirement for a variable width sample "window" for different control signals.

DG528/DG529

8-Channel and Dual 4-Channel Latchable Multiplexers



FEATURES

- TTL Compatible
- 44 V Power Supply Rating
- Latch-Proof
- 300 nSec WRITE Pulse Width
- $r_{DS(ON)} < 400 \Omega$

BENEFITS

- Easily Interfaced
- Environmentally Rugged
- Microprocessor Bus Compatible
- Improved System Accuracy

APPLICATIONS

- Data Acquisition Systems
- Automatic Test Equipment
- Communication Systems
- Microprocessor Controlled Systems

DESCRIPTION

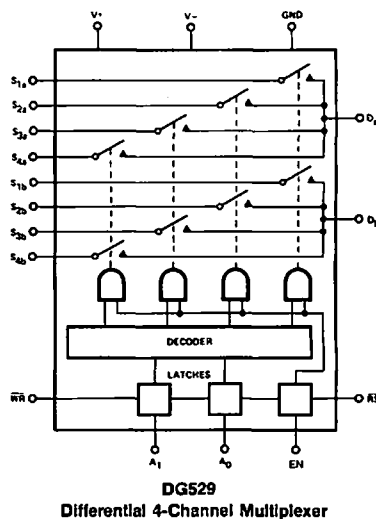
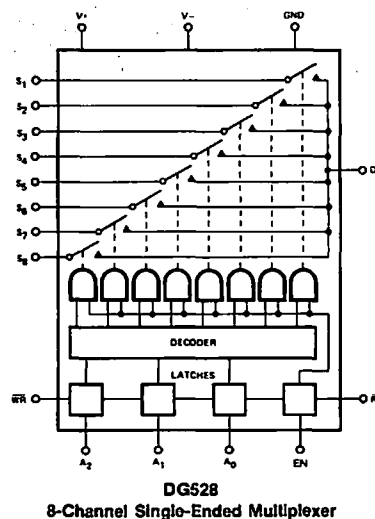
DG528 and DG529 are 8 and 4-channel analog multiplexers, respectively, with on-chip address and control latches to simplify design in microprocessor based applications. Break-Before-Make switching action protects against momentary shorting of the input signals. Designed on the Siliconix PLUS-40 CMOS process, each bidirectional switch features low 400Ω ON resistance over the full analog range, and will block signals to 30 V peak-to-peak in the unselected channels. All logic levels are TTL compatible.

DG528 is an 8-channel single-ended analog multiplexer designed to connect 1 of 8 inputs to a common output as determined by a 3-bit binary address (A_0, A_1, A_2). DG529, a 4-channel differential analog multiplexer, is designed to connect 1 of 4 differential inputs to a common differential output as determined by its 3-bit binary address (A_0, A_1, A_2) logic.

The enable (EN) pin is used to enable the address latches during the $\overline{WR}$ pulse. It can be hard wired to the logic supply if one of the channels will always be used (except during a reset) or it can be tied to address decoding circuitry for memory mapped operation. The $\overline{RS}$ pin is used as a master reset. All latches are cleared regardless of the state of any other latch or control line. The $\overline{WR}$ pin is used to transfer the state of the address control lines to their latches, except during a reset or when EN is low (see Tables 1 and 2).

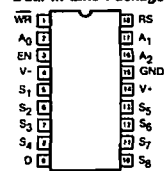
Both DG528 and DG529 are available in ceramic and plastic DIP packages, and are specified for operation over the popular military (-55 to 125°C), industrial (-25 to 85°C), and commercial (0 to 70°C), temperature ranges.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION

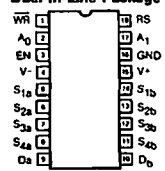
Dual-In-Line Package



Order Numbers:

DG528AK, DG528BK, or DG528CK
See Package 23
DG528CJ See Package 19

Dual-In-Line Package



Order Numbers:

DG529AK, DG529BK, or DG529CK
See Package 23
DG529CJ See Package 19

ABSOLUTE MAXIMUM RATINGS

Voltage Referenced to V-

V+ 44 V

GND 25 V

 Digital inputs¹ V_S, V_D -2 V to (V⁺ +2 V) or
 20 mA, whichever occurs first.

Current (Any Terminal Except S or D) 30 mA

Continuous Current, S or D 20 mA

Peak Current, S or D

(Pulsed at 1 msec, 10% Duty Cycle Max) 40 mA

Operating Temperature (A Suffix) -55 to 125°C

(B Suffix) -25 to 85°C

(C Suffix) 0 to 70°C

Storage Temperature (A & B Suffix) -65 to 150°C

(C Suffix) -65 to 125°C

Power Dissipation (Package)*

18 Pin Ceramic DIP** 900 mW

18 Pin Plastic DIP*** 470 mW

*All leads soldered or welded to PC board.

**Derate 12 mW/°C above 75°C.

***Derate 6.3 mW/°C above 75°C.

ELECTRICAL CHARACTERISTICS²

 T_A = 25°C

	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: ⁷ V ⁺ = 15 V, V ⁻ = 15 V, GND = 0, $\overline{WR}$ = 0, $\overline{RS}$ = 2.4 V	LIMITS						UNIT	
				DG528AA,9AA			DG528A B/C,9A B/C				
				MIN ³	TYP ⁴	MAX	MIN ³	TYP ⁴	MAX		
SWITCHING	Analog Signal Range	V _{ANALOG}		-15		15	-15		15	V	
	Drain-Source ON Resistance	r _{DS(on)}	V _D = ±10 V, V _{AL} = 0.8 V, I _S = -200 μA, V _{AH} = 2.4 V, Sequence Each Switch ON		270	400		270	450	Ω	
	Greatest Change In Drain Source ON Resistance Between Channels	Δr _{DS(on)}	Δr _{DS(on)} = $\frac{(r_{DS(on)} \text{ MAX} - r_{DS(on)} \text{ MIN})}{r_{DS(on)} \text{ AVE}}$ -10 V < V _S < 10 V		6			6		%	
	Source OFF Leakage Current	I _{S(off)}	V _S = ±10 V V _D = ±10 V	-1	-0.005	1	-5.0	-0.005	5	nA	
	Drain OFF Leakage Current	DG528 DG529	I _{D(off)}	V _D = ±10 V V _S = ±10 V	-10	-0.015	10	-20	-0.015		20
				V _D = ±10 V V _S = ±10 V	-10	-0.008	10	-20	-0.008		20
	Drain ON Leakage Current	DG528 DG529	I _{D(on)} ⁵	V _{S(all)} = V _D = ±10 V Sequence Each Switch On V _{AL} = 0.8 V, V _{AH} = 2.4 V	-10	-0.03	10	-20	-0.03		20
V _{S(all)} = V _D = ±10 V				-10	-0.015	10	-20	-0.015	20		
INPUT	Logic Input Current, Input Voltage High	I _{AH}	V _A = 2.4 V	-10	-0.002		-10	-0.002		μA	
	V _A = 15 V			0.006	10		0.006	10			
	Logic Input Current, Input Voltage Low	I _{AL}	V _{EN} = 0, 2.4 V, V _{A(all)} = 0 $\overline{RS}$ = 0	-10	-0.002		-10	-0.002			
DYNAMIC	Switching Time Of Multiplexer	t _{transition}	See Figure 3		0.6	1		0.6		μs	
	Break-Before-Make Interval	t _{open}	See Figure 5		0.2			0.2		ns	
	Enable And Write Turn ON Time	t _{on(EN, $\overline{WR}$)}	See Figure 4 & 6		1	1.5		1		μs	
	Enable And Reset Turn OFF Time	t _{off(EN, $\overline{RS}$)}	See Figure 4 & 7		0.4	1		0.4			
	Charge Coupling (Injection)	Q	See Figure 8		4			4		pC	
	OFF Isolation ⁶		V _{EN} = 0, R _L = 1 kΩ, C _L = 15 pF V _S = 7 V _{RMS} , f = 500 kHz		68			68		dB	
	Logic Input Capacitance	C _{in}	f = 1MHz		2.5			2.5		pF	
	Source OFF Capacitance	C _{S(off)}	V _S = 0		5			5			
	Drain OFF Capacitance	DG528 DG529	C _{D(off)}	V _D = 0	V _{EN} = 0, f = 140 kHz		25		25		
							12				12
SUPPLY	Positive Supply Current	I ⁺	V _{EN} = 0, V _{A(all)} = 0			2.5			2.5	mA	
	Negative Supply Current	I ⁻		-1.5			-1.5				

NOTES

(See Next Page)

ELECTRICAL CHARACTERISTICS² (Cont.) $T_A = \text{Over Temperature Range}$

	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: ⁷ V+ = 15 V, V- = 15 V, GND = 0, WR = 0, RS = 2.4 V	LIMITS						UNIT	
				DG528AA,9AA			DG528A B/C,9A B/C				
				MIN ³	TYP ⁴	MAX	MIN ³	TYP ⁴	MAX		
SWITCHING	Analog Signal Range	VANALOG			-15		15	-15		15	V
	Drain-Source ON Resistance	rDS(on)	VD = ±10 V, VAL = 0.8 V, IS = -200 μA, VAH = 2.4 V, Sequence Each Switch ON				500			500	Ω
	Source OFF Leakage Current	IS(off)	VS = ±10 V VD = ∓10 V	VEN = 0	-50		50	-50		50	nA
	Drain OFF Leakage Current	ID(off)	VD = ±10 V VS = ∓10 V		-200		200	-200		200	
			VD = ±10 V VS = ∓10 V		-100		100	-100		100	
	Drain ON Leakage Current	ID(on) ⁵	VS(all) = VD = +10 V Sequence Each Switch On VAL = 0.8 V, VAH = 2.4 V VEN = 2.4 V		-200		200	-200		200	
			VS(all) = VD = -10 V	-100		100	-100		100		
INPUT	Logic Input Current, Input Voltage High	IAH	VA = 2.4 V		-30			-30			μA
			VA = 15 V				30		30		
	Logic Input Current, Input Voltage Low	IAL	VEN = 0, 2.4 V, VA(all) = 0 RS = 0		-30			-30			

NOTES:

1. Signals on S_X , D_X or IN_X , exceeding V_+ or V_- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
2. Refer to PROCESS OPTION FLOWCHART for additional information.
3. The algebraic convention whereby the most negative value is a minimum, and the most positive value is a maximum, is used in this data sheet.
4. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
5. $I_{D(on)}$ is leakage from driver into "ON" switch.
6. OFF Isolation = $20 \log \frac{|V_S|}{|V_D|}$, V_S = input to "OFF" switch, V_D = output due to V_S .
7. Period of Reset (RS) pulse must be at least $50 \mu\text{s}$ during or after power ON.

TRUTH TABLES
DG528

A_2	A_1	A_0	EN	WR	RS	On Switch
X	X	X	X	$\overline{1}$	1	Maintains previous switch condition
X	X	X	X	X	0	NONE (latches cleared)
X	X	X	0	0	1	NONE
0	0	0	1	0	1	1
0	0	1	1	0	1	2
0	1	0	1	0	1	3
0	1	1	1	0	1	4
1	0	0	1	0	1	5
1	0	1	1	0	1	6
1	1	0	1	0	1	7
1	1	1	1	0	1	8

DG529

A_1	A_0	EN	WR	RS	On Switch
X	X	X	$\overline{1}$	1	Maintains previous switch condition
X	X	X	X	0	NONE (latches cleared)
X	X	0	0	1	NONE
0	0	1	0	1	1
0	1	1	0	1	2
1	0	1	0	1	3
1	1	1	0	1	4

 Logic "1": $V_{AH} > 2.4 \text{ V}$

 Logic "0": $V_{AL} < 0.8 \text{ V}$

TIMING DIAGRAMS

Minimum Input Timing Requirements

	Parameter	Measured Terminal	Min Limits over full temp range	Unit	Test Circuit
30	t_{WW} WRITE Pulse Width	$\overline{WR}$	300	ns	See Figure 1
31	t_{DW} A, EN Data Valid to WRITE (Stabilization Time)	$A_0, A_1, (A_2), E_n$ $\overline{WR}$	180		
32	t_{WD} A, EN Data Valid after WRITE (Hold Time)	$\overline{WR}$ $A_0, A_1, (A_2), E_n$	30		
33	t_{RS} RESET Pulse Width Note 4	$\overline{RS}$	500		See Figure 2 $V_S = 5V$

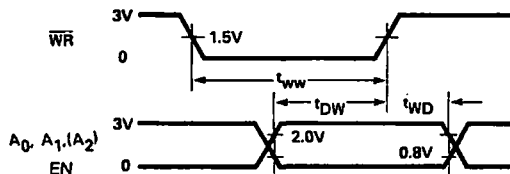


Figure 1

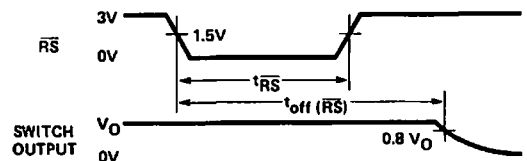
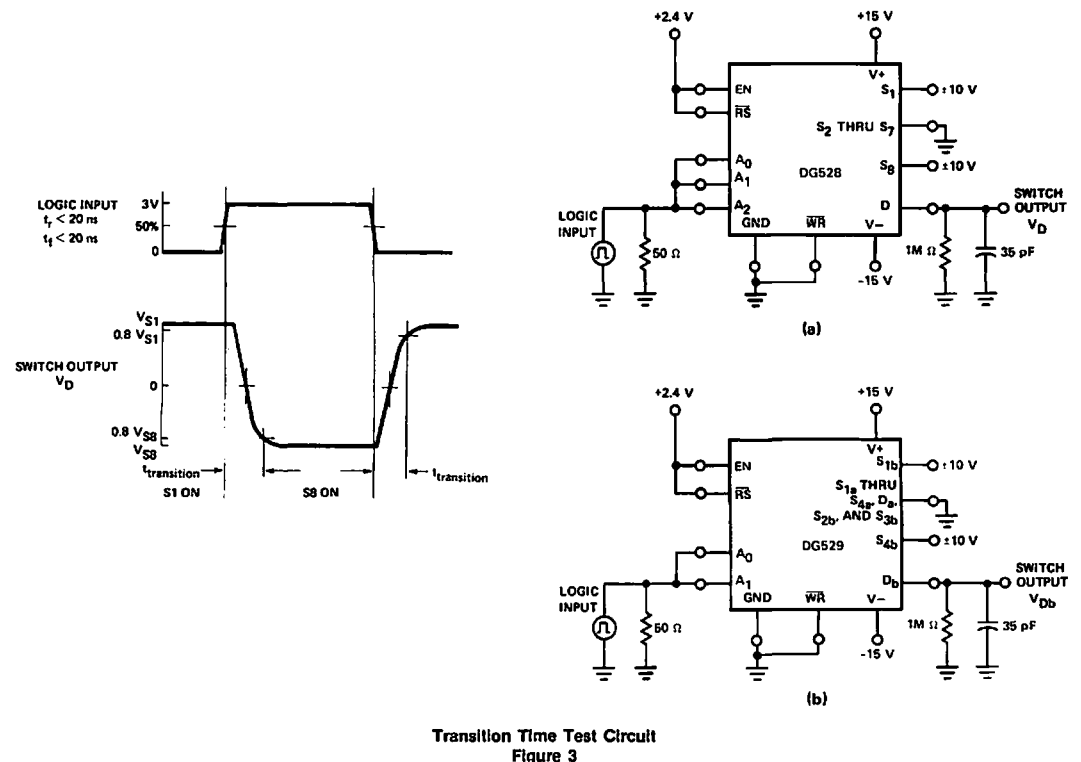


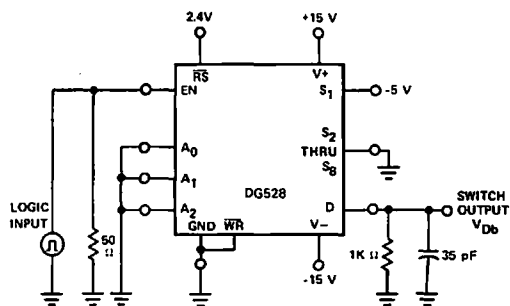
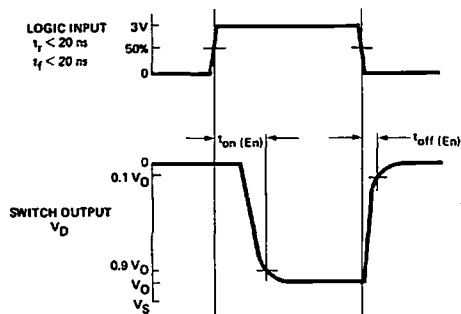
Figure 2

SWITCHING TIME TEST CIRCUIT

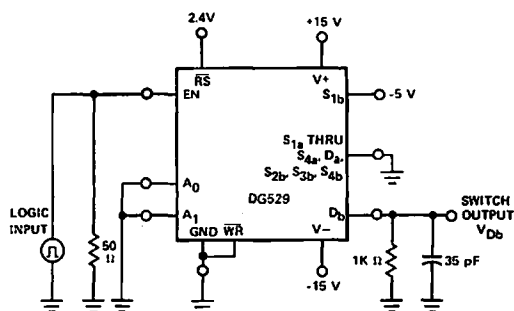


Transition Time Test Circuit
Figure 3

SWITCHING TIME TEST CIRCUIT (Cont.)

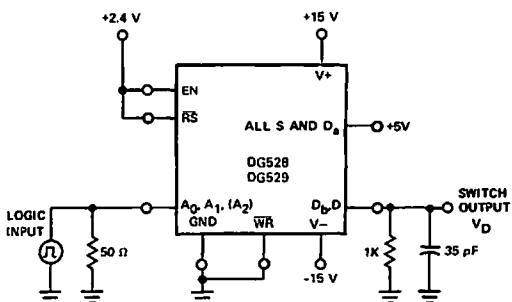
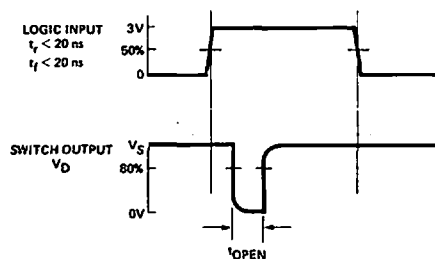


(a)

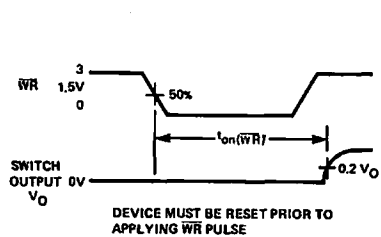


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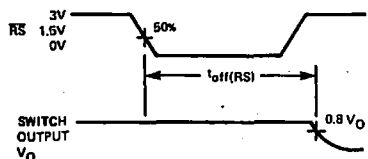
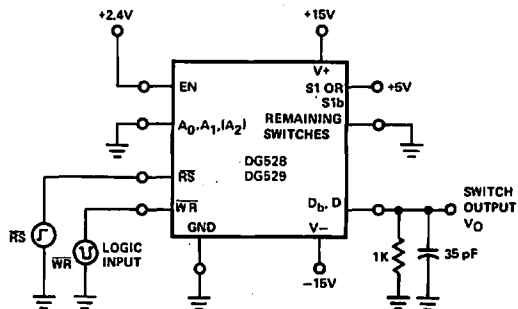
Enable t_{on}/t_{off} Time
Figure 4



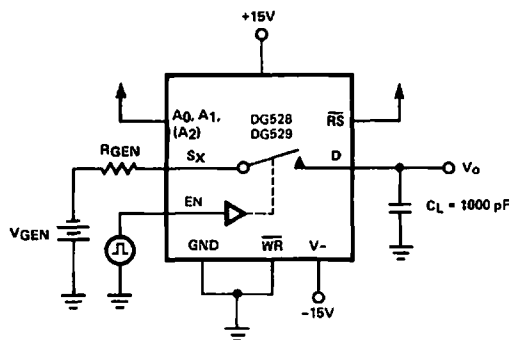
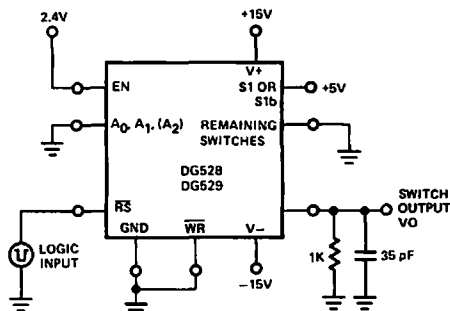
Open Time (B.B.M. Interval)
Figure 5



Write Turn-On Time $t_{on}(WR)$
Figure 6



Reset Turn-Off Time $t_{off}(RS)$
Figure 7



ΔV_O IS THE MEASURED VOLTAGE ERROR DUE TO CHARGE INJECTION. THE ERROR VOLTAGE IN COULOMBS IS $Q = C_L \times \Delta V_O$.

Charge Injection Test Circuit
Figure 8

DETAILED DESCRIPTION

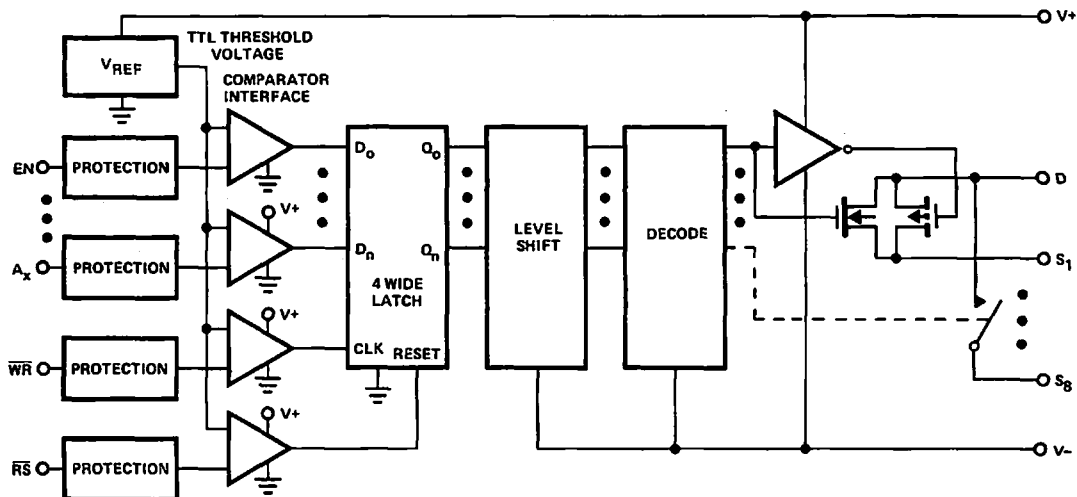
The internal structure of the DG528 and DG529 includes a 5 volt logic interface with input protection circuitry followed by a latch, level shifter, decoder and finally the switch constructed with parallel N and P channel MOSFETs (see figure 9).

The input protection on the logic lines A_0 , A_1 , A_2 , E_n and control lines $\overline{WR}$, $\overline{RS}$ shown in figure 9 minimize susceptibility to static encountered during handling and operational transients.

The logic interface circuit compares the TTL input signal against a TTL threshold reference voltage. The output of the comparator feeds the data input of a D-type latch. The

level sensitive D latch continuously places the D_x input signal on the Q_x output when the CLK ($\overline{WR}$) input is low, resulting in transparent operation. As soon as CLK ($\overline{WR}$) returns high the latch holds the data last present on the D_x input at the Q_x output, subject to the "Minimum Input Timing Requirements" table.

Following the latches the Q_x signals are level shifted and decoded to provide proper drive levels for the CMOS switches. This level shifting insures full ON/OFF switch operation for any analog signal present between the V^+ and V^- supply pins.



DG528 Simplified Internal Structure
Figure 9

INTRODUCTION:

The DG528 and DG529 minimize the amount of interface hardware between a microprocessor system bus and the analog system being controlled or measured. The internal TTL compatible latches give these multiplexers memory, that is, they can be programmed to stay in a particular switch state (e.g., switch 1 ON) until the microprocessor determines it is necessary to turn different switches ON or turn all switches OFF.

The input latches become transparent when $\overline{WR}$ is held low; therefore, these multiplexers operate by direct command of the coded switch state on A₂, A₁, A₀. In this mode the DG528 is identical to the very popular DG508 even sharing the same pin locations. The same is true of the DG529 versus the popular DG509.

CIRCUIT OPERATION: (See Figure 10)

Initially during system power-up $\overline{RS}$ would be active LOW

maintaining all 8 switches in the OFF state. After $\overline{RS}$ returned HIGH the DG528 maintains all switches in the OFF state. As soon as the system program was ready to perform a write operation to the address assigned to the DG528, the address decoder would provide a $\overline{CS}$ active LOW signal which is gated with the WRITE ($\overline{WR}$) control signal. At this time the data on the DATA BUS (that will determine which switch to close) is stabilizing. When the $\overline{WR}$ signal returns to the HIGH state, (positive edge) the input latches of the DG528 save the data from the DATA bus. The coded information in the A₀, A₁, A₂, and E_n latches is decoded and the appropriate switch is turned ON.

The EN latch allows all switches to be turned OFF under program control. This becomes useful when two or more DG528s are cascaded to build 16-line and larger analog input multiplexers.

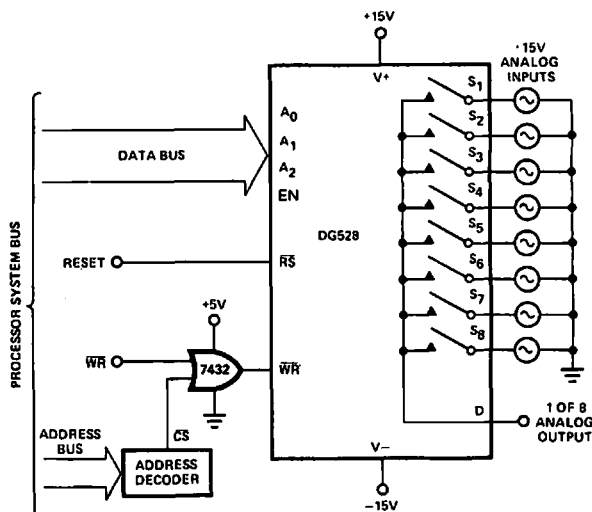


Figure 10

APPLICATION HINTS

V+ Positive Supply Voltage (V)	V- Negative Supply Voltage (V)	GND Analog & Power Supply GND (V)	V _{in} Logic Input Voltage V _{inH} Min/ V _{inL} Max (V)	V _s or V _d Analog Voltage Range (V)
20	-20	GND	2.4/0.8	±20
15	-15	GND	2.4/0.8	±15
8	-8	GND	2.4/0.8	±8

Figure 11



DG568/DG569

8-Channel and Dual 4-Channel

Latchable High-Voltage Multiplexers

FEATURES

- Latchable Logic Inputs
- Low $r_{DS(on)}$
- Direct Reset ($\overline{RS}$)
- ± 50 V Signal Range
- Low $\Delta r_{DS(on)}$
- Low Error Voltage

BENEFITS

- Microprocessor Compatible
- CMOS Compatible
- Rugged

APPLICATIONS

- Data Acquisition
- Automatic Test Equipment
- Communications Systems
- Microprocessor Controlled Systems

DESCRIPTION

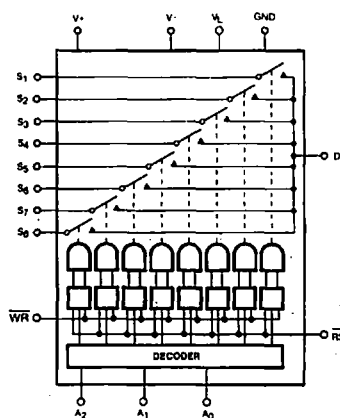
DG568 and DG569 are 8 and 4-channel multiplexers designed for high voltage (± 50 V) applications in microprocessor based instrumentation and process control. Both multiplexers feature low on resistance (30 Ω , typ.) and true bi-directional switch action over the full analog signal range. In addition, on-board data latches and control pins are provided to simplify interfacing with most microprocessors.

The DG568 provides 8-channel single ended multiplexing and demultiplexing, while the DG569 is designed for 4-

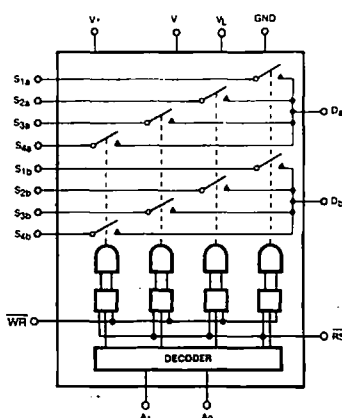
channel differential applications. Binary coded input channel select data latches (A_0 , A_1 , and A_2), chip select $\overline{WR}$ and device reset $\overline{RS}$ (all channels off), complete the logic controls which store, or clear, the switch state inputs. $\overline{RS}$ also simplifies switch turn-off during system powerup or reset.

Both devices are provided in the 18-pin sidebrazed package, and are specified over the industrial (-25 to 85°C) and commercial (0 to 70°C) temperature ranges.

FUNCTIONAL BLOCK DIAGRAM



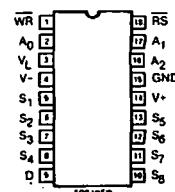
DG568
8 Channel Single Ended Multiplexer



DG569
Differential 4 Channel Multiplexer

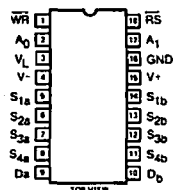
PIN CONFIGURATION

Dual In-Line Package



Order Numbers:
DG568BP or DG568CP
See Package 20

Dual In-Line Package



Order Numbers:
DG569BP or DG569CP
See Package 20

ABSOLUTE MAXIMUM RATINGS

DG568/DG569

V+	62 V
V-	-62 V
V _L	18 V
Digital Inputs	-0.3 V to V _L + 0.3 V
Continuous Current, S or D	70 mA
Peak Current, S or D ¹	100 mA

Operating Temperature (B Suffix)	-25 to 85°C
(C Suffix)	0 to 70°C
Storage Temperature	-55 to 125°C
Power Dissipation (Package*)	250 mW

*All leads soldered or welded to PC board.

ELECTRICAL CHARACTERISTICS²

T_A = 25°C

	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: V+ = 60 V, V- = -60 V, GND = V_{WR} = 0, $V_{RS} = V_L = 15\text{ V}$		LIMITS			UNIT	
					MIN ³	TYP ⁴	MAX		
MULTIPLEXER	Analog Signal Range	V_{ANALOG}			-50		50	V	
	Drain-Source ON Resistance	$r_{DS(on)}$	$-50\text{ V} < V_D < 30\text{ V}, I_S = 70\text{ mA}$			30	50	Ω	
			$30\text{ V} < V_D < 40\text{ V}, I_S = 1\text{ mA}$			50	100		
			$40\text{ V} < V_D < 50\text{ V}, I_S = 1\text{ mA}$			300	500		
	Source OFF Leakage Current	$I_{S(off)}$	See Figure 1 $V_D = -50\text{ V}$	$V_S = 0\text{ V}$ $V_S = 60\text{ V}$		0.75 1.5	7.5 15	nA	
	Drain OFF Leakage Current	$I_{D(off)}$	See Figure 2 $V_S = -50\text{ V}$	$V_D = 0\text{ V}$ $V_D = 50\text{ V}$		5 12	50 120		
Drain ON Leakage Current				$I_{D(on)}$	See Figure 3 $V_S = -50\text{ V}$	$V_D = 0\text{ V}$ $V_D = 50\text{ V}$			6 15
	INPUT	Input Current Input Voltage Low	I_{INH}			$V_{in} = V_L^5$			0.1
	Input Current Input Voltage High	I_{INL}	$V_{in} = 0\text{ V}^5$			0.1	10		
DYNAMIC	Transition Time	$t_{TRANSITION}$	$R_L = 5\text{ k}\Omega, C_L = 50\text{ pF}$, See Figure 4			1	2	μs	
	Turn-OFF Time	t_{off}	$R_L = 5\text{ k}\Omega, C_L = 50\text{ pF}$, See Figure 5			0.5	1		
	Break-Before-Make Interval	t_{open}			50	100			
	Access Time	t_A	See Figure 4				100	ns	
	Reset Pulse Width	t_{RS}	See Figure 5				300		
	Write Pulse Width	t_{WR}	See Figure 4				300		
	Source OFF Capacitance	$C_{S(off)}$	$V_S = 0\text{ V}$			14		pF	
	Drain OFF Capacitance	$C_{D(off)}$	$V_D = 0\text{ V}$			85			
	Channel ON Capacitance	$C_{D+S(on)}$	$V_S = 0, V_{WR} = V_L, f = 140\text{ kHz to }1\text{ MHz}$			110			
		OFF Isolation		$V_{RS} = 0, R_L = 2\text{ k}\Omega, C_L = 3\text{ pF}$ $V_{ANALOG} = 10\text{ V}_{p-p}, f = 10\text{ kHz}$			65		dB
	SUPPLY	Positive Supply Current	I^+	$V_{in(all)} = 0\text{ or }15\text{ V}^5$			0.2	10	μA
Negative Supply Current		I^-				0.2	10		
Logic Supply Current		I_L				0.1	10		

NOTES:

- Pulsed @ 1 ms, 10% duty cycle.
- Refer to PROCESS OPTION FLOWCHART for additional information.
- The algebraic convention whereby the most negative value is a minimum, and the most positive value is a maximum, is used in this data sheet.
- Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- Inputs are digital inputs (A₀, A₁, A₂, RS, and WR).

TRUTH TABLES

DG568

A ₂	A ₁	A ₀	WR	RS	On Switch
X	X	X	$\overline{1}$	1	Maintains previous switch condition
X	X	X	X	0	NONE
0	0	0	0	1	1
0	0	1	0	1	2
0	1	0	0	1	3
0	1	1	0	1	4
1	0	0	0	1	5
1	0	1	0	1	6
1	1	0	0	1	7
1	1	1	0	1	8

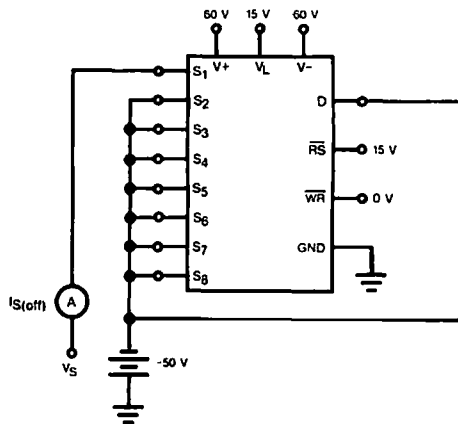
DG569

A ₁	A ₀	WR	RS	On Switch
X	X	$\overline{1}$	1	Maintains previous switch condition
X	X	X	0	NONE
0	0	0	1	1
0	1	0	1	2
1	0	0	1	3
1	1	0	1	4

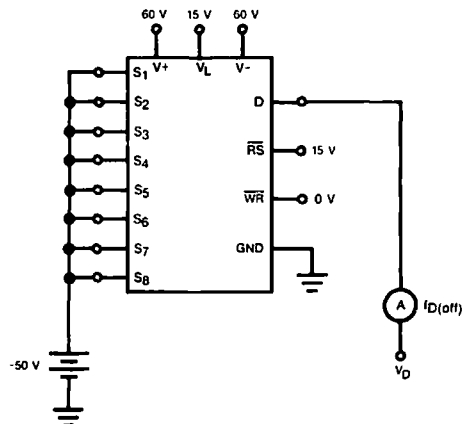
Logic "1": $V_{in} = V_{WRH} \geq 0.7 (V_L)$

Logic "0": $V_{in} = V_{WRL} \leq 1 \text{ V}$

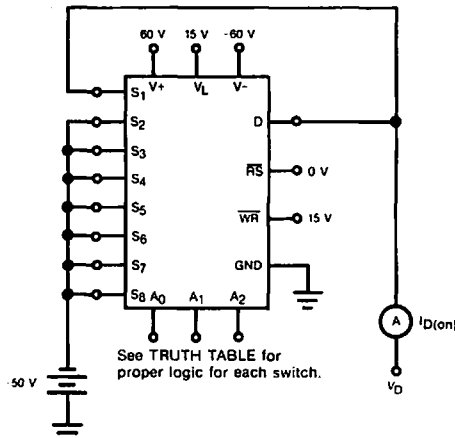
TEST CIRCUITS



$I_{S(off)}$ Test Circuit
Figure 1



$I_{D(off)}$ Test Circuit
Figure 2



$I_{D(on)}$ Test Circuit
Figure 3

ABSOLUTE MAXIMUM RATINGS

V+ to V-	-0.3, 35 V	Storage Temperature	-65 to 150°C
V+ to V _A , V _{EN}	-0.3, 35 V	Operating Temperature (142 Suffix)	-55 to 125°C
V+ to V _D or V _S	-0.3, 35 V	(192 Suffix)	0 to 70°C
V _D to V _S	±25 V	Power Dissipation*	900 mW
V _A , V _{EN} to V-	35 V	*All leads soldered or welded to PC board. Derate 12 mW/°C above 75°C.	
V _D or V _S to V-	35 V		
Current (Any Terminal)	-20 mA		

ELECTRICAL CHARACTERISTICS¹T_A = 25°C

	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: V ₋ = -20 V, V ₊ = 5 V, V _{EN} = 3.5 V, V _{AL} = 0.6 V, V _{AH} = 3.5 V	LIMITS						UNIT	
				Si3705142			Si3705192				
				MIN ²	TYP ³	MAX	MIN ²	TYP ³	MAX		
SWITCH	Drain-Source ON Resistance	r _{DS(on)}	I _S = -1 mA			150			150	Ω	
			V _D = 5 V								
			V _D = 0			200			200		
			V _D = -5 V			400			400		
	Source OFF Leakage Current	I _{S(off)}	V _{EN} = 0.6 V	V _S = -5 V, V _D = 5 V	-1		-3			nA	
	Drain OFF Leakage Current	I _{D(off)}		V _D = -5 V, V _S = 5 V	-8		-10				
IN	Input Current, Input Voltage Low	I _{INL}	V _{AL} = 0			-1		-1		μA	
DYNAMIC	Switching Time Of Multiplexer	t _{transition}	See Switching Time Test Circuit V _{S1} = ±1 V, V _{S8} = ±1 V, V _{S2-7} = gnd					2		2	μs
	Turn-ON Time	t _{on}					1.2		1.2		
	Turn-OFF Time	t _{off}	See Switching Time Test Circuit V _{S(all)} = 1 V				0.8		0.8		
	Break Before-Make Interval	t _{open}					0.05		0.05		
	Source OFF Capacitance	C _{S(off)}	V _{EN} = 0.6 V f = 1 MHz	V _S = V _D = 5 V		10		10		pF	
	Drain OFF Capacitance	C _{D(off)}		V _D = 5 V		20		20			
	Power Dissipation	P _D	V ₋ = -31 V, V ₊ = 0					175		175	mW

T_A = Over Temperature Range

	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: V ₋ = -20 V, V ₊ = 5 V, V _{EN} = 3.5 V, V _{AL} = 0.6 V, V _{AH} = 3.5 V	LIMITS						UNIT	
				Si3705142			Si3705192				
				MIN ²	TYP ³	MAX	MIN ²	TYP ³	MAX		
SWITCH	Drain-Source ON Resistance	r _{DS(on)}	I _S = -1 mA	V _D = 5 V			225			200	Ω
				V _D = 0			300			300	
				V _D = -5 V			400			400	
	Source OFF Leakage Current	I _{S(off)}	V _{EN} = 0.6 V	V _S = -5 V, V _D = 5 V	-100			-150			nA
	Drain OFF Leakage Current	I _{O(off)}		V _D = -5 V, V _S = 5 V	-500			-500			

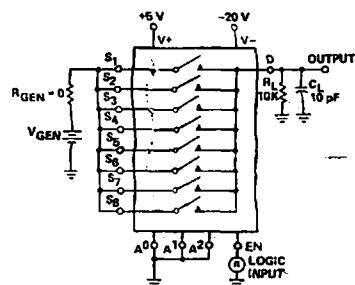
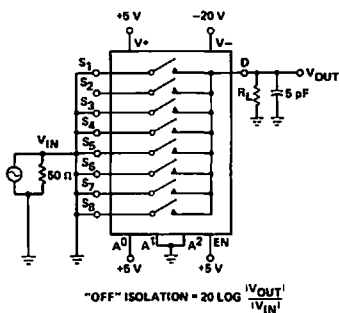
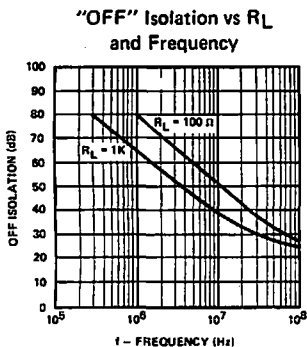
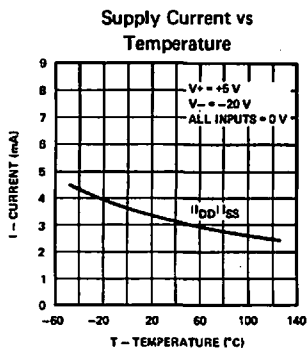
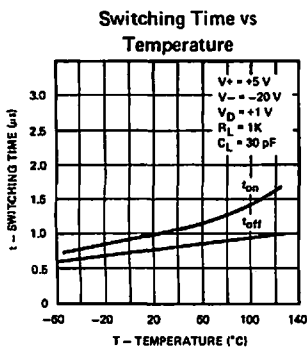
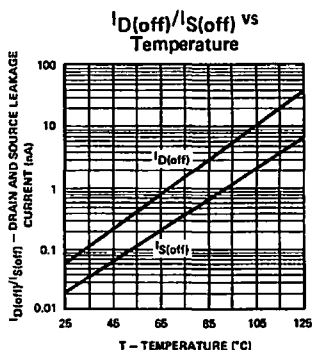
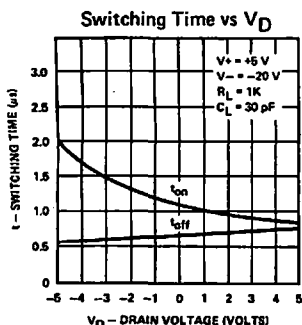
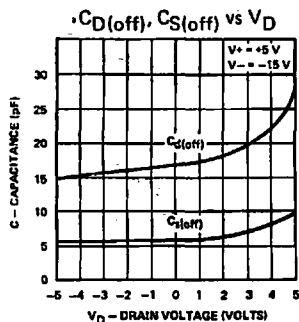
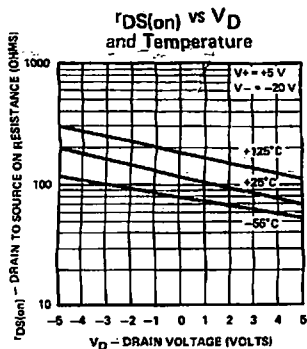
NOTES:

- All DC parameters are 100% tested at 25°C. Lots are sample-tested for AC parameters and high and low temperature limits to assure conformance with specifications.
- The algebraic convention whereby the most negative value is a minimum, and the most positive value is a maximum, is used in this data sheet.
- Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

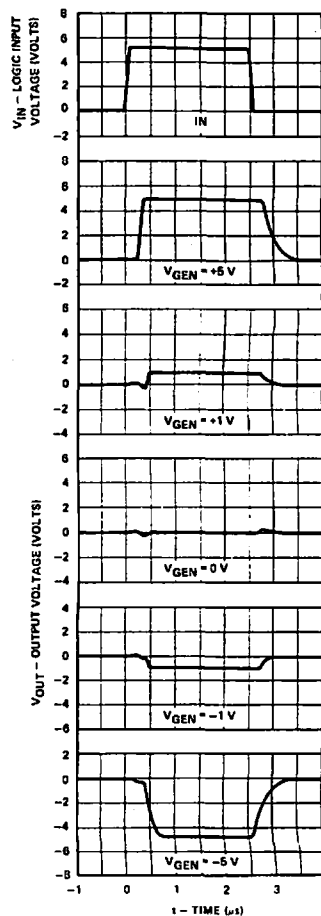
TRUTH TABLE

LOGIC INPUTS				CHANNEL
A ⁰	A ¹	A ²	EN	'ON'
L	L	L	H	S ₁
H	L	L	H	S ₂
L	H	L	H	S ₃
H	H	L	H	S ₄
L	L	H	H	S ₅
H	L	H	H	S ₆
L	H	H	H	S ₇
H	H	H	H	S ₈
X	X	X	L	OFF

TYPICAL CHARACTERISTICS



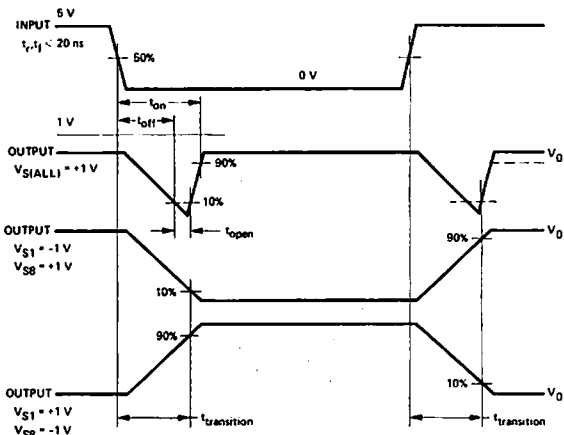
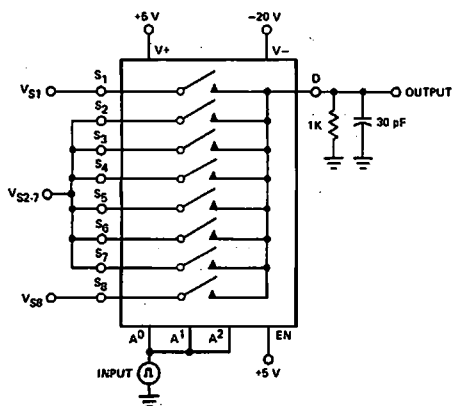
If R_{GEN} , R_L or C_L is increased, there will be proportional increases in rise and/or fall RC times.



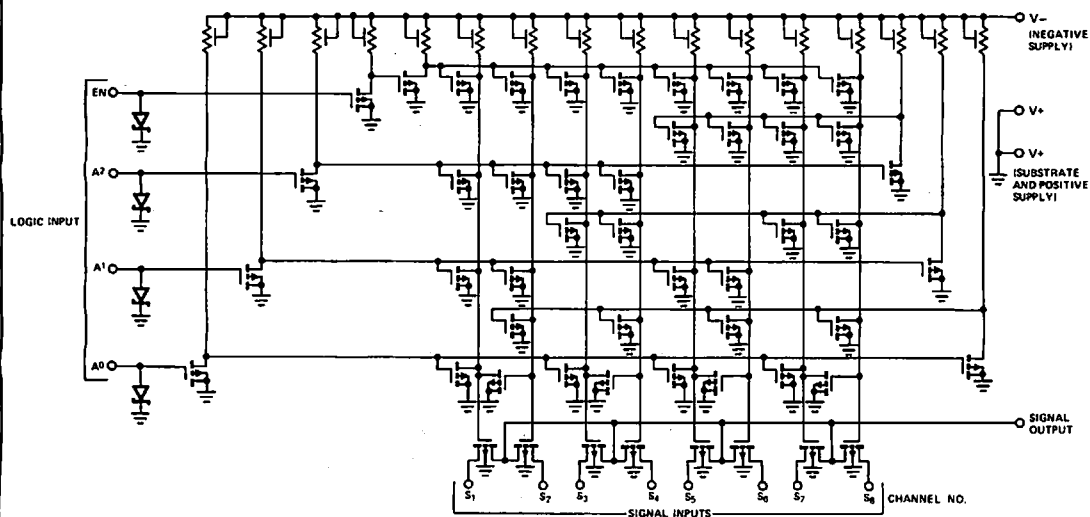
SWITCHING TIME TEST CIRCUIT

Switch output waveform shown for $V_S = \text{constant}$ with logic input waveform as shown. Note that V_S may be + or - as per switching time test circuit. V_O is the steady state

output with switch on. Feedthrough via gate capacitance may result in spikes at leading and trailing edge of output waveform.



SCHEMATIC DIAGRAM





APPLICATION HINTS*

**Electrical parameters chart based on $V_+ = 5\text{ V}$, $V_- = -20\text{ V}$.

0	Introduction
1	Interface
2	Analog Switches/Multiplexers
3	A/D Converters
4	D/A Converters
5	Linear
6	Power Conversion
7	Telecommunications
8	Die Process & Topography
9	Package Data
10	Applications Information
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ANALOG-TO-DIGITAL CONVERTERS

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LD120/LD121A	3-13
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Si520	3-36
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Si8602	3-55
Si25HC04	3-64

Analog-To-Digital Converter Product Selector Guide¹

Function	Part No. Package Information	Specifications	Features
8 Channel, 8-bit Data Acquisition System	SI520 28 pin plastic, 28 pin ceramic DIP	Conversion Time: 70 μ s TTL compatible 5 mW power consumption No missing codes	Microprocessor compatible logic inputs and outputs Onboard 8 channel analog multiplexer and sample/hold
	SI6601 28 pin plastic, 28 pin ceramic DIP	Conversion Time: 25 μ s TTL and CMOS compatible 5 mW power consumption No missing codes	Microprocessor compatible logic inputs and outputs Onboard 8 channel analog multiplexer and sample/hold
	SI6602² 28 pin plastic, 28 pin ceramic DIP	Conversion Time: 25 μ s CMOS compatible No missing codes	Microprocessor compatible logic inputs and outputs Onboard 8 channel analog multiplexer and sample/hold
4½-Digit Integrating A/D Converter	SI7135² 28 pin plastic DIP	±4½-Digit Resolution Accuracy 0.005% ±1 count Auto zero Auto polarity TTL compatible Rollover error ±1 count max.	2.0V full scale input Over-range and under-range signals MUX BCD outputs Monolithic design
	LD120/121A 16-pin & 18-pin plastic DIP respectively	±4½-Digit Resolution Accuracy 0.005% ±1 count Auto Zero Auto polarity TTL compatible Internal clock Linear to 28,500 counts	Two voltage ranges: 2.0V & 200.00mV 1 to 5 samples/s 25% inter-digit blanking MUX BCD outputs 0.5 count stability on 2.0V range Monolithic design
	LD122/121A 16-pin and 18-pin plastic DIP respectively	±4½-Digit Resolution Accuracy 0.005% ±1 count Auto Zero Auto polarity TTL compatible Internal clock Linear to 28,500 counts	Same as LD120/121A but without internal input buffer amplifier
3½-Digit High Performance Integrating A/D Converter	LD110/LD111A 16-pin plastic DIPs	±3½-Digit Resolution Accuracy 0.02% ±1 count Auto zero Auto polarity 10 V resolution Typical TC of 5 ppm/°C	Three voltage ranges: 1.999V, 199.9mV, & 19.99mV Sampling rate up to 40 samples/s Differential input capability Over-range & under-range signals TTL compatible
12-bit Successive Approximation Register	SI25HC04² 24-pin plastic, 24-pin ceramic DIP	TTL compatible 110 mW power consumption	Control logic on board three-state outputs CMOS

NOTE:

1. Devices shown in **boldface** are recommended for new designs.
2. Preliminary product. Specifications subject to change. Contact factory on availability.

INTRODUCTION

The converters discussed in this section employ either the successive approximation or the integrating concepts to achieve their conversion. Si8601 is an example of the former, while Si7135 is representative of the latter.

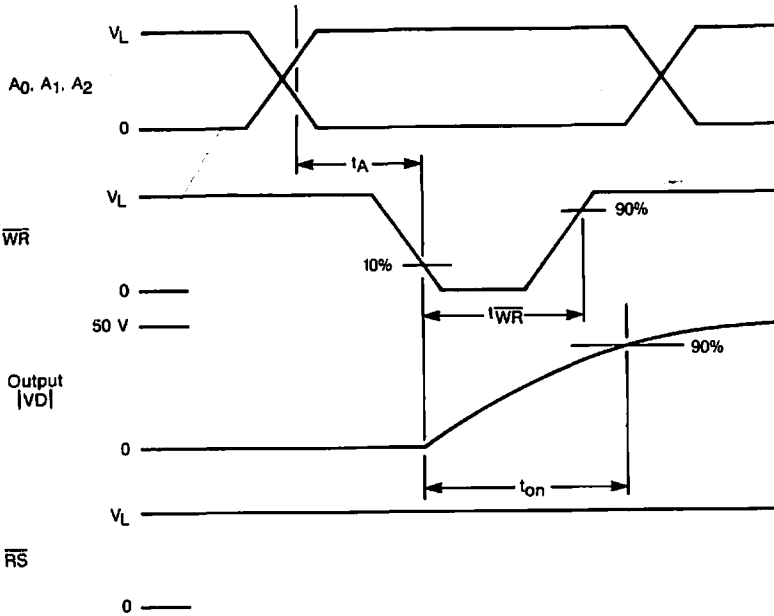
In successive approximation the unknown input is compared with a known (reference) input (generally the output of a D/A converter) presented as a series of binary weighted fractions of full scale ($1/2, 1/4, 1/8$, etc.,) starting with $1/2 (= 2^{-1})$. Any incremental reference input that would result in the comparison $V_{ref}(k \cdot 2^{-1} + k \cdot 2^{-2} + \dots + k \cdot 2^{-n}) > V_{in}$ is rejected (k is made = 0.) The resultant

facing to UARTS and microprocessors. The LD110/111, LD120/121, and LD122/121, are $3\frac{1}{2}$, $4\frac{1}{2}$, and $4\frac{1}{2}$ charge injection A/D converters that have been available for some time from Siliconix. While not recommended for new designs (use Si7135), they nevertheless offer guaranteed ± 1 count accuracies over their design input range.

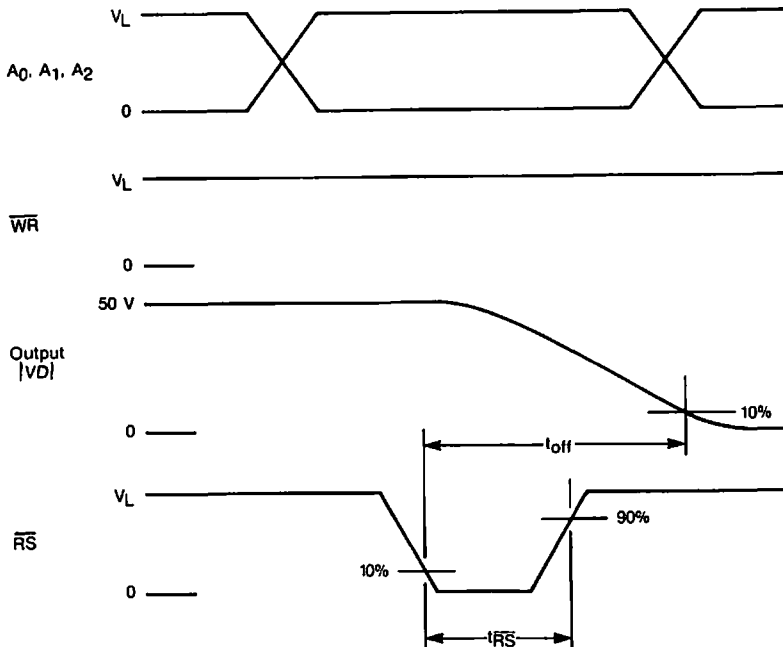
For full data acquisition performance, the Si8601 features an 8-channel multiplexer, a quasi sample hold and an 8-bit A/D converter, all on a single chip. Differential non-linearity is typically $1/4$ LSB.

DG568/DG569

TIMING DIAGRAMS



"On" Time
Figure 4



"OFF" Time
Figure 5

DEFINITION OF SPECIFICATIONS

Absolute Accuracy

The absolute error of an A/D converter is expressed as the difference between the theoretical and the actual analog input voltages required to produce that code. As a given code can be produced by a range of analog voltages in a finite band (see Quantization Uncertainty,) the input required to produce a given code is defined as the midpoint of the band of inputs that will produce that code. Thus, if 5 volts (± 19.5 mV) will produce an 8-bit half scale code of 10000000, then a converter for which any voltage between 4.98 and 5.00 V will produce that code is said to have an absolute error of $1/2 (4.98 + 5.00) \text{ V} - 5 \text{ V} = -10 \text{ mV}$.

Absolute error comprises gain error, zero error and non-linearity, and is generally expressed in fractions of an LSB, % or ppm.

Relative Accuracy

Relative accuracy is the deviation between the actual analog input voltage required to produce a give code and the theoretical value relative to actual full scale for the converter. It is generally expressed in fractions of an LSB, % or ppm. This parameter is also a measure of the linearity of the A/D converter as it is based on the deviation of the discrete points of the converter from an idealized straight line. These discrete points are defined as the midpoints of the quantization bands at each code.

Linearity

The linearity error of a converter is its deviation from an idealized straight line. This straight line can be either "best straight line", determined by manipulating the offset and/or gain to equalize positive and negative deviations, or "endpoint", defined by a line passing through the end points of the transfer function. Siliconix uses this latter definition as it is generally the way our customers will use the product, and it is much easier to verify.

Differential Linearity

The measure of linearity from one digital state to the next adjacent state. If the differential linearity is specified as $+1/2$ LSB, the step size from one state to the next adjacent state may be from $1/2$ to $3/2$ of an ideal 1 LSB step.

Common Mode Rejection

Ideally a differential device rejects, as noise, any signals in common with both inputs. Thus, common mode rejection is a measure of the equivalent differential input signal generated by a common mode signal. It is expressed as a ratio, and generally in dB. Thus, if a device has a CMR of 80 dB and a common mode signal of 10 volts, the equivalent differential input error signal would be 1 mV.

Conversion Speed

This is the time it takes for the converter to complete the measurement. For successive approximation converters this parameter is the same for each conversion. Integrating converters are specified for a full scale conversion as the conversion time may be less for measurements less than full scale.

Gain

The gain of a converter is the scale factor setting required to achieve the nominal relationship, e.g. 10 V full scale for fixed reference converters, and 100% of full scale for rationmetric designs.

Least Significant Bit (LSB)

In a binary system the LSB is that bit which represents the smallest incremental change possible, or the resolution of the converter. In the natural binary number 1101 the LSB is the rightmost bit '1', which also represents the decimal value 2^0 .

Most Significant Bit (MSB)

In a binary system the MSB is that bit which represents the largest incremental change possible, or carries the greatest weight of the converter. In the natural binary number 1101 the MSB is the leftmost bit '1', which also represents the decimal value 2^3 .

Quantizing Uncertainty

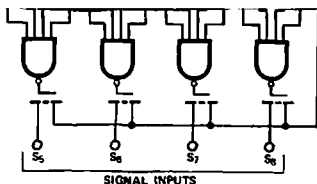
In an n-bit converter, each digital code is represented by a discrete range of analog values defined to occur within the resolution of the converter ($\approx 2^{-n}$). Thus, as the discrete digital value is said to be defined by the mid point of the analog input signal range required to select that value, there is an inherent quantization uncertainty of $\pm 1/2$ LSB.

Missing Codes

This is a property of an A/D converter that relates to monotonicity (as for D/A converters) but is more stringent. When an A/D converter is specified to have "no missing codes", this guarantees that the device will not skip codes on the digital output when the analog input is varied over the entire signal range.

Resolution

The number of bits on the output of an A/D converter which defines the number of states or discrete steps equal to 2^n , where n is the resolution or number of bits in an A/D converter. n number of bits does not guarantee n bits of accuracy.



SI3705192P
See Package 12

†Both V+ lines are internally connected, either one or both may be used. V+ common to substrate.

Si3705

Monolithic 8-Channel Multiplex Switch with Decoder



FEATURES

- On Board Decoding
- Internal Zener Diodes Protect MOS Gates
- Break-Before-Make Switching

BENEFITS

- Reduces External Component Requirements
- Minimizes Channel Cross-Talk Problems

APPLICATIONS

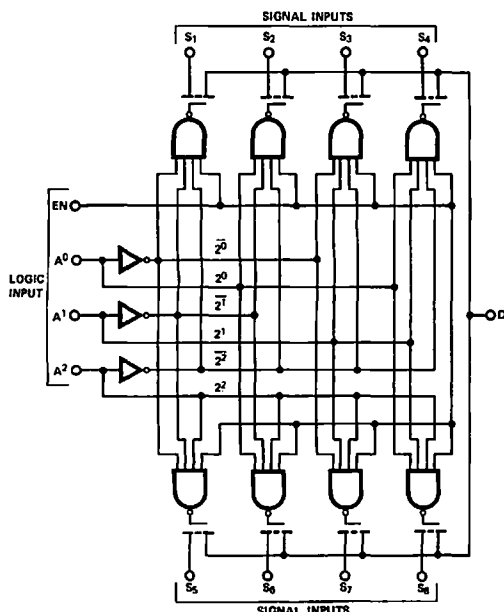
- Multiplexing Analog Signals
- Data Acquisition Systems

DESCRIPTION

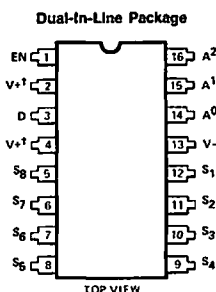
The Si3705 is designed to function as a single-pole, 8-position (plus OFF) electronic switch. The function is implemented by using eight P-channel MOS field-effect transistors as analog switches. In the ON state, each switch will conduct current equally well in either direction, and in the OFF state each switch will block voltages up to 10 V peak-to-peak. The ON-OFF state of each switch is controlled by drivers, which are in turn controlled by a

3-bit binary word plus an Enable-Inhibit input. The truth table shown indicates the binary word required to select any one of the eight switch positions. Logic input levels "L" and "H" correspond to positive logic "0" and "1". Assuming supply voltages of 5 V and -20 V, logic "L" ≤ 0.6 V and logic "H" ≥ 3.5 V. The rise and fall times of the drivers are designed to provide Break-Before-Make switch action.

FUNCTIONAL BLOCK DIAGRAM



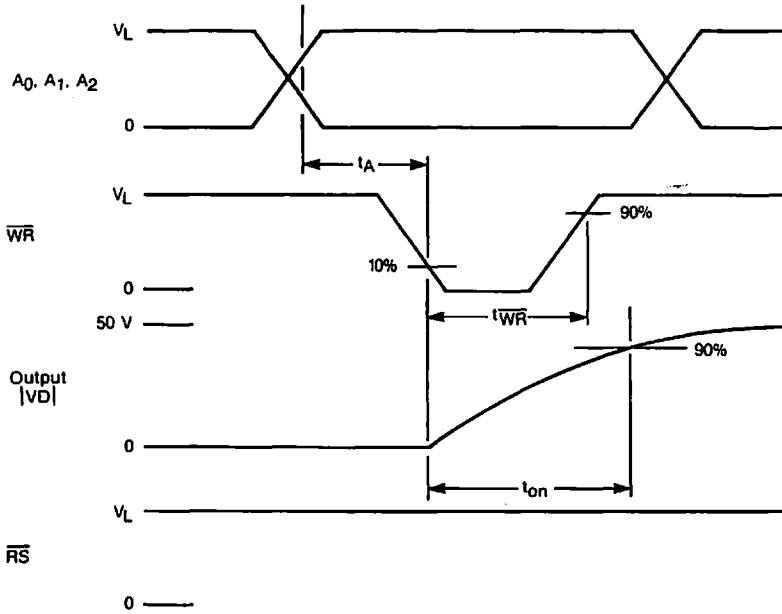
PIN CONFIGURATION



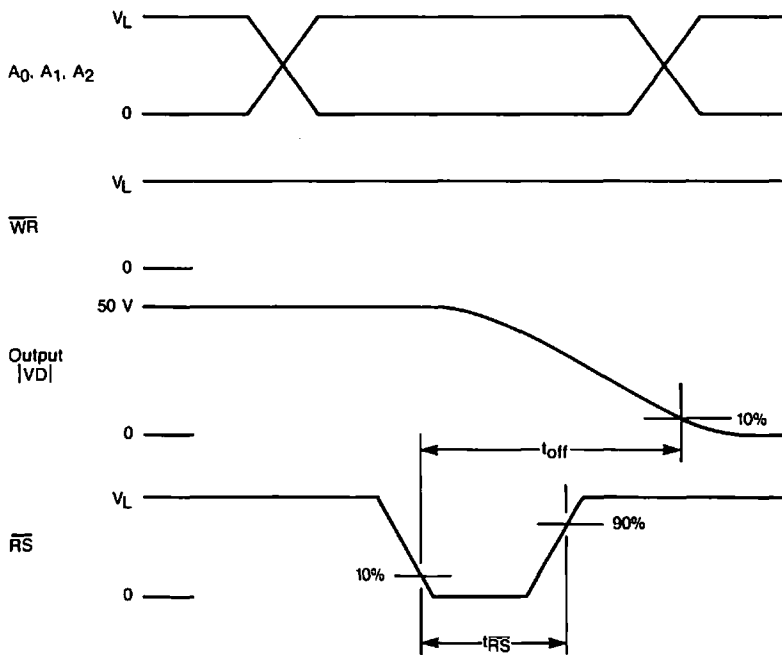
Order Numbers:
 SI3705142K or SI3705192K
 See Package 10
 SI3705192P
 See Package 12

†Both V+ lines are internally connected, either one or both may be used. V+ common to substrate.

TIMING DIAGRAMS



"On" Time
Figure 4



"OFF" Time
Figure 5

ABSOLUTE MAXIMUM RATINGS

V+ to V-	-0.3, 35 V	Storage Temperature	-65 to 150°C
V+ to V _A , V _{EN}	-0.3, 35 V	Operating Temperature (142 Suffix)	-55 to 125°C
V+ to V _D or V _S	-0.3, 35 V	(192 Suffix)	0 to 70°C
V _D to V _S	±25 V	Power Dissipation*	900 mW
V _A , V _{EN} to V-	35 V	*All leads soldered or welded to PC board. Derate	
V _D or V _S to V-	35 V	12 mW/°C above 75°C.	
Current (Any Terminal)	-20 mA		

ELECTRICAL CHARACTERISTICS¹T_A = 25°C

	PARAMETER	SYMBOL	TEST CONDITIONS. UNLESS OTHERWISE NOTED: V ₋ = -20 V, V ₊ = 5 V, V _{EN} = 3.5 V, V _{AL} = 0.6 V, V _{AH} = 3.5 V		LIMITS						UNIT
					SI3705142			SI3705192			
					MIN ²	TYP ³	MAX	MIN ²	TYP ³	MAX	
SWITCH	Drain-Source ON Resistance	r _{DS(on)}	I _S = -1 mA	V _D = 5 V			150			150	Ω
				V _D = 0			200			200	
				V _D = -5 V			400			400	
	Source OFF Leakage Current	I _{S(off)}	V _{EN} = 0.6 V	V _S = -5 V, V _D = 5 V	-1			-3			nA
Drain OFF Leakage Current	I _{D(off)}	V _D = -5 V, V _S = 5 V		-8			-10				
IN	Input Current, Input Voltage Low	I _{INL}	V _{AL} = 0		-1			-1			μA
DYNAMIC	Switching Time Of Multiplexer	t _{transition}	See Switching Time Test Circuit V _{S1} = ±1 V, V _{S8} = ±1 V, V _{S2-7} = gnd				2			2	μs
	Turn-ON Time	t _{on}				1.2		1.2			
	Turn-OFF Time	t _{off}	See Switching Time Test Circuit			0.8		0.8			
	Break Before-Make Interval	t _{open}	V _{S(all)} = 1 V			0.05		0.05			
	Source OFF Capacitance	C _{S(off)}	V _{EN} = 0.6 V f = 1 MHz	V _S = V _D = 5 V		10		10		pF	
	Drain OFF Capacitance	C _{D(off)}		V _D = 5 V		20		20			
	Power Dissipation	P _D	V ₋ = -31 V, V ₊ = 0				175			175	mW

T_A = Over Temperature Range

PARAMETER		SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: V ₋ = -20 V, V _A = 5 V, V _{EN} = 3.5 V, V _{AL} = 0.6 V, V _{AH} = 3.5 V	LIMITS						UNIT	
				Si3705142			Si3705192				
				MIN ²	TYP ³	MAX	MIN ²	TYP ³	MAX		
SWITCH	Drain-Source ON Resistance	r _{DS(on)}	I _S = -1 mA	V _D = 5 V			225			200	Ω
				V _D = 0			300			300	
				V _D = -5 V			400			400	
	Source OFF Leakage Current	I _{S(off)}	V _{EN} = 0.6 V	V _S = -5 V, V _D = 5 V	-100			-150			nA
	Drain OFF Leakage Current	I _{D(off)}		V _D = -5 V, V _S = 5 V	-500			-500			

NOTES:

- All DC parameters are 100% tested at 25°C. Lots are sample-tested for AC parameters and high and low temperature limits to assure conformance with specifications.
- The algebraic convention whereby the most negative value is a minimum, and the most positive value is a maximum, is used in this data sheet.
- Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

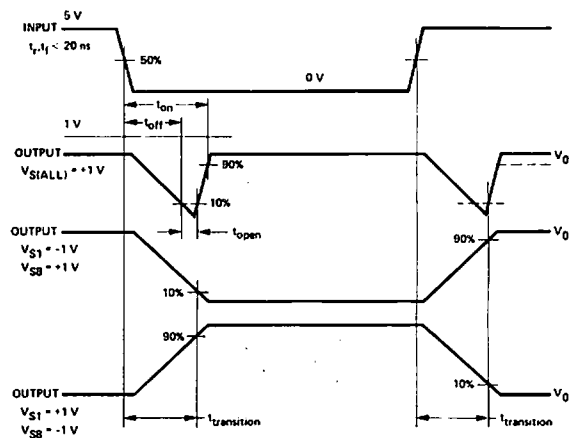
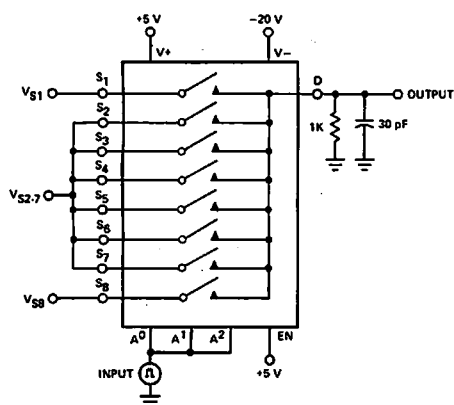
TRUTH TABLE

LOGIC INPUTS				CHANNEL
A ⁰	A ¹	A ²	EN	'ON'
L	L	L	H	S ₁
H	L	L	H	S ₂
L	H	L	H	S ₃
H	H	L	H	S ₄
L	L	H	H	S ₅
H	L	H	H	S ₆
L	H	H	H	S ₇
H	H	H	H	S ₈
X	X	X	L	OFF

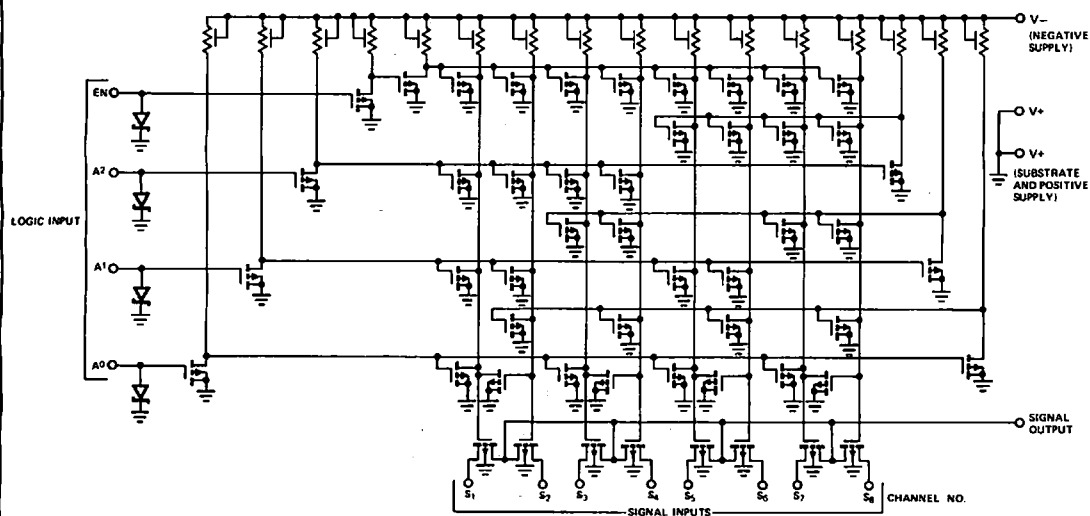
SWITCHING TIME TEST CIRCUIT

Switch output waveform shown for $V_S = \text{constant}$ with logic input waveform as shown. Note that V_S may be + or - as per switching time test circuit. V_O is the steady state

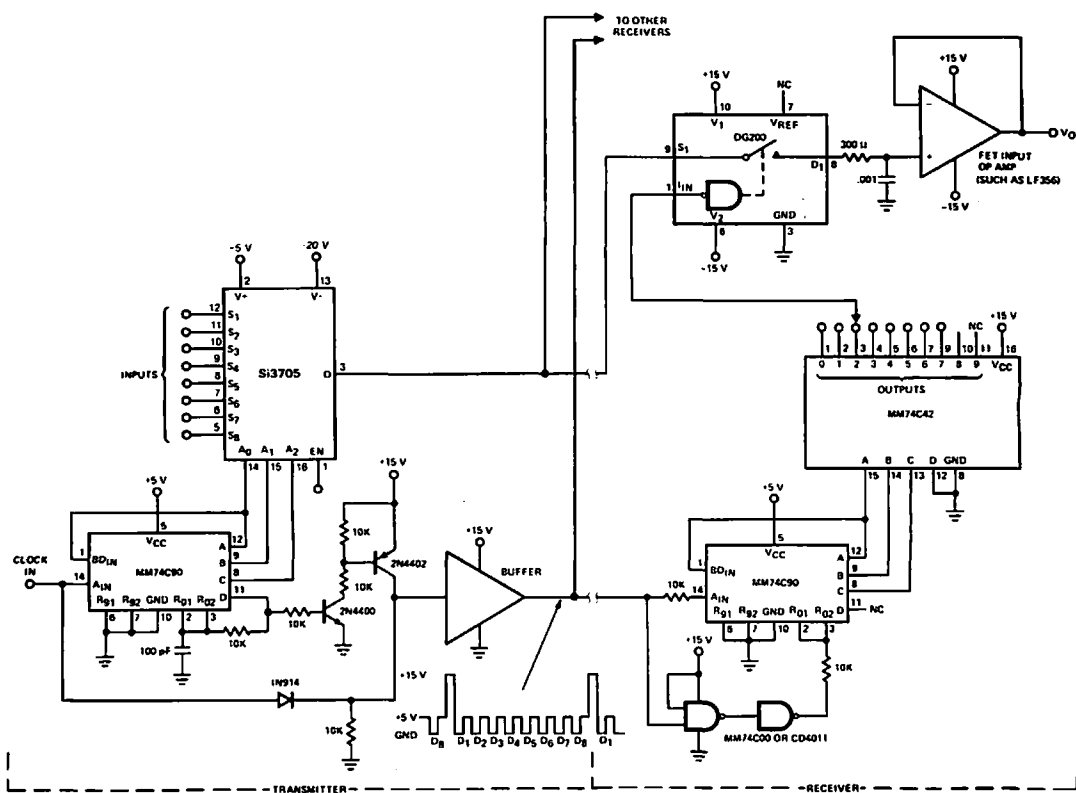
output with switch on. Feedthrough via gate capacitance may result in spikes at leading and trailing edge of output waveform.



SCHEMATIC DIAGRAM



TYPICAL APPLICATION



A One of 8-channel Transmission System

APPLICATION HINTS*

V+	V-	V _{EN}	V _{IN}	V _S or V _D
Positive Supply Voltage (V)	Negative Supply Voltage (V)	Enable Input Voltage Min High/Max Low (V)	Logic Input Voltage V _{INH} Min/V _{INL} Max (V)	Analog Signal Range (V)
+5**	-20	3.5/0.6	3.5/0.6	-5 to +5
+5	-15	3.5/0.6	3.5/0.6	-5 to +5

*Application Hints are for DESIGN AID ONLY, not guaranteed and not subject to production testing.

**Electrical parameters chart based on V+ = 5 V, V- = -20 V.

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ANALOG-TO-DIGITAL CONVERTERS

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Analog-To-Digital Converter Product Selector Guide¹

Function	Part No. Package Information	Specifications	Features
8 Channel, 8-bit Data Acquisition System	SI520 28 pin plastic, 28 pin ceramic DIP	Conversion Time: 70 μ s TTL compatible 5 mW power consumption No missing codes	Microprocessor compatible logic inputs and outputs Onboard 8 channel analog multiplexer and sample/hold
	SI8601 28 pin plastic, 28 pin ceramic DIP	Conversion Time: 25 μ s TTL and CMOS compatible 5 mW power consumption No missing codes	Microprocessor compatible logic inputs and outputs Onboard 8 channel analog multiplexer and sample/hold
	SI8602² 28 pin plastic, 28 pin ceramic DIP	Conversion Time: 25 μ s CMOS compatible No missing codes	Microprocessor compatible logic inputs and outputs Onboard 8 channel analog multiplexer and sample/hold
4½-Digit Integrating A/D Converter	SI7135² 28 pin plastic DIP	±4½-Digit Resolution Accuracy 0.005% ±1 count Auto zero Auto polarity TTL compatible Rollover error ±1 count max.	2.0V full scale input Over-range and under-range signals MUX BCD outputs Monolithic design
	LD120/121A 16-pin & 18-pin plastic DIP respectively	±4½-Digit Resolution Accuracy 0.005% ±1 count Auto Zero Auto polarity TTL compatible Internal clock Linear to 28,500 counts	Two voltage ranges: 2.0V & 200.00mV 1 to 5 samples/s 25% inter-digit blanking MUX BCD outputs 0.5 count stability on 2.0V range Monolithic design
	LD122/121A 16-pin and 18-pin plastic DIP respectively	±4½-Digit Resolution Accuracy 0.005% ±1 count Auto Zero Auto polarity TTL compatible Internal clock Linear to 28,500 counts	Same as LD120/121A but without internal input buffer amplifier
3½-Digit High Performance Integrating A/D Converter	LD110/LD111A 16-pin plastic DIPs	±3½-Digit Resolution Accuracy 0.02% ±1 count Auto zero Auto polarity 10 V resolution Typical TC of 5 ppm/°C	Three voltage ranges: 1.999V, 199.9mV, & 19.99mV Sampling rate up to 40 samples/s Differential input capability Over-range & under-range signals TTL compatible
12-bit Successive Approximation Register	SI25HC04² 24-pin plastic, 24-pin ceramic DIP	TTL compatible 110 mW power consumption	Control logic on board three-state outputs CMOS

NOTE:

1. Devices shown in **boldface** are recommended for new designs.
2. Preliminary product. Specifications subject to change. Contact factory on availability.

DEFINITION OF SPECIFICATIONS

Absolute Accuracy

The absolute error of an A/D converter is expressed as the difference between the theoretical and the actual analog input voltages required to produce that code. As a given code can be produced by a range of analog voltages in a finite band, (see Quantization Uncertainty,) the input required to produce a given code is defined as the midpoint of the band of inputs that will produce that code. Thus, if 5 volts (± 19.5 mV) will produce an 8-bit half scale code of 10000000, then a converter for which any voltage between 4.98 and 5.00 V will produce that code is said to have an absolute error of $1/2 (4.98 + 5.00) \text{ V} - 5 \text{ V} = -10 \text{ mV}$.

Absolute error comprises gain error, zero error and non-linearity, and is generally expressed in fractions of an LSB, % or ppm.

Relative Accuracy

Relative accuracy is the deviation between the actual analog input voltage required to produce a give code and the theoretical value relative to actual full scale for the converter. It is generally expressed in fractions of an LSB, % or ppm. This parameter is also a measure of the linearity of the A/D converter as it is based on the deviation of the discrete points of the converter from an idealized straight line. These discrete points are defined as the midpoints of the quantization bands at each code.

Linearity

The linearity error of a converter is its deviation from an idealized straight line. This straight line can be either "best straight line", determined by manipulating the offset and/or gain to equalize positive and negative deviations, or "endpoint", defined by a line passing through the end points of the transfer function. Siliconix uses this latter definition as it is generally the way our customers will use the product, and it is much easier to verify.

Differential Linearity

The measure of linearity from one digital state to the next adjacent state. If the differential linearity is specified as $+1/2$ LSB, the step size from one state to the next adjacent state may be from $1/2$ to $3/2$ of an ideal 1 LSB step.

Common Mode Rejection

Ideally a differential device rejects, as noise, any signals in common with both inputs. Thus, common mode rejection is a measure of the equivalent differential input signal generated by a common mode signal. It is expressed as a ratio, and generally in dB. Thus, if a device has a CMR of 80 dB and a common mode signal of 10 volts, the equivalent differential input error signal would be 1 mV.

Conversion Speed

This is the time it takes for the converter to complete the measurement. For successive approximation converters this parameter is the same for each conversion. Integrating converters are specified for a full scale conversion as the conversion time may be less for measurements less than full scale.

Gain

The gain of a converter is the scale factor setting required to achieve the nominal relationship, e.g. 10 V full scale for fixed reference converters, and 100% of full scale for rationmetric designs.

Least Significant Bit (LSB)

In a binary system the LSB is that bit which represents the smallest incremental change possible, or the resolution of the converter. In the natural binary number 1101 the LSB is the rightmost bit '1', which also represents the decimal value 2^0 .

Most Significant Bit (MSB)

In a binary system the MSB is that bit which represents the largest incremental change possible, or carries the greatest weight of the converter. In the natural binary number 1101 the MSB is the leftmost bit '1', which also represents the decimal value 2^3 .

Quantizing Uncertainty

In an n-bit converter, each digital code is represented by a discrete range of analog values defined to occur within the resolution of the converter ($= 2^{-n}$.) Thus, as the discrete digital value is said to be defined by the mid point of the analog input signal range required to select that value, there is an inherent quantization uncertainty of $\pm 1/2$ LSB.

Missing Codes

This is a property of an A/D converter that relates to monotonicity (as for D/A converters) but is more stringent. When an A/D converter is specified to have "no missing codes", this guarantees that the device will not skip codes on the digital output when the analog input is varied over the entire signal range.

Resolution

The number of bits on the output of an A/D converter which defines the number of states or discrete steps equal to 2^n , where n is the resolution or number of bits in an A/D converter. n number of bits does not guarantee n bits of accuracy.

INTRODUCTION

The converters discussed in this section employ either the successive approximation or the integrating concepts to achieve their conversion. Si8601 is an example of the former, while Si7135 is representative of the latter.

In successive approximation the unknown input is compared with a known (reference) input (generally the output of a D/A converter) presented as a series of binary weighted fractions of full scale ($1/2$, $1/4$, $1/8$, etc.) starting with $1/2$ ($= 2^{-1}$). Any incremental reference input that would result in the comparison $V_{ref}(k \cdot 2^{-1} + k \cdot 2^{-2} + \dots + k \cdot 2^{-n}) > V_{in}$ is rejected (k is made $= 0$). The resulting (binary) fraction of the reference used to balance the input is then interpreted as the actual value of the input. Since the result can have an uncertainty of 1 Least Significant Bit (LSB, $= 2^{-n}$) all such A/D converters have a "quantization error" of 1 LSB.

The integrating converter works by comparing the average value of the unknown input (over a fixed period) with the output of a precision integrator and counting the number of clock periods required for the integrator to achieve equivalence. The number of clock periods so counted is then used to represent the digital value of the input.

The Si7135 is a monolithic CMOS 4-12/ digit A/D converter. Features include accuracy guaranteed to ± 1 count, over-range and under-range signals for autoranging and auxiliary I/O's for inter-

facing to UARTS and microprocessors. The LD110/111, LD120/121, and LD122/121, are 3-1/2, 4-1/2, and 4-1/2 charge injection A/D converters that have been available for some time from Siliconix. While not recommended for new designs (use Si7135), they nevertheless offer guaranteed ± 1 count accuracies over their design input range.

For full data acquisition performance, the Si8601 features an 8-channel multiplexer, a quasi sample hold and an 8-bit A/D converter, all on a single chip. Differential non-linearity is typically 1/4 LSB, and a single conversion can be completed in 25 μ s. Si8601 is characterized for a full scale range of 0 to 5 V and is available in the three normal temperature ranges (commercial, industrial, and military.) For less demanding applications, there is the Si520, and 8-channel, 8-bit data acquisition system, specified for the industrial temperature range only.

Also included in this section is the Si25HC04 Successive Approximation Register (SAR). The Si25HC04 incorporates all the necessary logic and control functions to be directly connected to a 12-bit DAC to perform successive approximation A/D conversion. CMOS processing provides low power consumption (50 mW) and conversion speeds exceeding 750 kHz. The digital outputs are 3-state for microprocessor bus compatibility, and the E pin allows cascading of SARs to perform even higher resolution conversions.

CIRCUIT DESIGN CONSIDERATIONS

THE ANALOG SECTION

The analog section of an A/D converter requires a precision reference, a comparator and either a D/A converter and a successive approximation register or a precision controllable integrator. The reference can be external, internal, fixed (generally) or variable. Polarity is determined by the application and the specifications of the particular A/D converter being used.

Successive Approximation A/D Converters

In most successive approximation A/D converters, the comparator is used in the "current summing" mode. In such a case, the current output of the D/A converter is compared with a current developed in an input resistor by the input voltage signal. The D/A converter is then stepped through each bit, starting with the Most Significant Bit (MSB), and its output is compared with the input signal to achieve the best balance, without going over it (if any bit presented causes the output of the D/A converter to be larger than the input signal, then that bit is rejected or turned off.) One significant problem with these converters is that the current switching action of the D/A converter can result in undesirable interaction with the analog input.

Another has to do with the linearity of the successive approximation attenuator (or the D/A converter) itself. If the D/A converter is not monotonic, then the A/D converter is likely to have missing codes. (See Linearity, Differential and Integral for an explanation.)

The Si8601 and Si520 both use the charge redistribution principle in their successive approximation designs. The analog input charges an input capacitor (quasi sample-hold,) and that charge is then compared with the output of a successive approximation D/A converter. Thus the input does see the "noise" on the comparator input, but must charge the small input capacitance through the resistance of the built in multiplexer switch.

Integrating A/D Converters

The analog section of the integrating A/D converters requires a precision reference, high gain amplifier(s) and comparator(s). These converters are frequently used where speed is NOT a consideration, but noise and linearity are. As integrators are inherently monotonic, these converters generally have no problem with missing codes. However, they are slow, and linearity can be a problem.

THE DIGITAL SECTION

The digital section of the successive approximation A/D converter comprises a SAR (Successive Approximation Register), clock and the appropriate control circuitry. The digital output word is read directly from the input to the D/A converter, or through a (three state) latch. Coding is generally straight binary (or offset binary for bipolar options,) and positive true logic for this type converter. Other coding options such as BCD and sign magnitude, and negative true logic may also be available.

For integrating A/D converters the digital section comprises the clock-pulse generator, the counter(s), the input from the comparator, and ancillary controls. BCD coding is most often used to simplify interfacing with displays. But options frequently include sign-magnitude and binary.

And finally, the desired output data levels must be considered. Options here include CMOS and TTL compatibility. If the converter is built to communicate directly with a microprocessor bus it will have three-state outputs. With BCD coding, the digital output may be multiplexed to reduce pin count. The status (BUSY or EOC) output is used to indicate when the converter is busy and when the data is valid. The timing diagrams on the specification sheets fully describe this important timing function. Other signal outputs may include UART controls, serial output, low, mid and/or high byte enables, etc. These are fully described in the individual data sheets.

POWER SUPPLIES

In A/D converters the power supply considerations and connections can make or break the application. Analog power supplies should have the appropriate accuracy and stability. They should be kept well filtered and clean. In most cases, separate analog and digital grounds are appropriate, and ground wire routing should follow best practice to insure no interaction with high quality analog signal or supply paths

LD110/111A

3½ Digit A/D Converter Set



FEATURES

- Buffered Reference Input
- MOSFET Input
- Auto-Zero System
- Auto-Polarity
- Over and Under Range Signals

BENEFITS

- High Gain Stability
- Reduced Signal Loading
- Reduced Offset and Drift Over Temperature
- Reduced External Parts Count
- Easily Interfaced

APPLICATIONS

- High Performance Digital Voltmeters
- Digital Panel Meters
- Digital Instrumentation Readouts
- μ P A/D Interface Subsystem
- Auto-Zeroed Microvolt or Strain Gauge Systems

DESCRIPTION

The LD110 and LD111A form a precision 3 1/2 digit A/D converter system for use in display and microprocessor based data acquisition applications. Based on Siliconix's "Quantized Feedback" technique, intrinsic features include auto-polarity, auto-zero, and ratiometric operation. Except for a stable reference, no critical components are required to achieve rated performance. The technique used offers superior linearity, normal mode rejection, and stability due to the simultaneous integration of the unknown input and the reference voltages. Unlike other conversion techniques, the integrator output voltage never represents more than 100 counts. Thus, critical, high resolution performance is not required of either the integrator or the comparator.

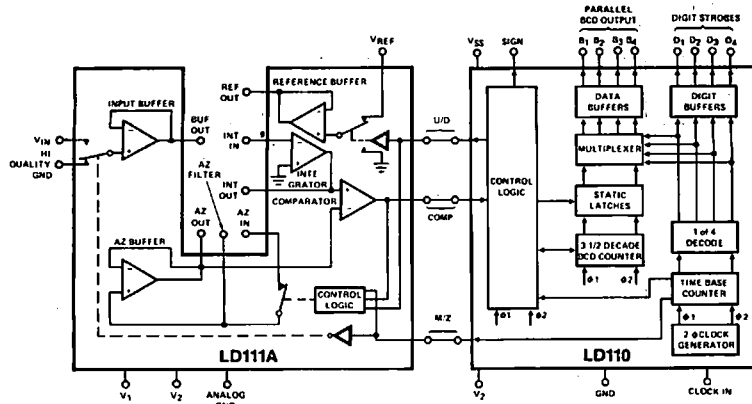
The monolithic LD111A high performance analog processor contains a bipolar comparator, a bipolar integrating amplifier, a bipolar reference amplifier, two MOSFET input unity gain amplifiers, several P-channel enhancement mode analog switches and the necessary level shifting drivers to allow the analog and digital processors to be

directly interfaced. The high impedance input and reference buffer amplifiers eliminate source loading errors and provide the outstanding temperature coefficient inherent in this system. Break-before-make switch action insures that neither the analog input nor the reference voltage will be shorted to ground at any time.

The PMOS LD110 synchronous digital processor combines the counting, storage and data multiplexing functions with the random logic necessary to control the quantized charge-balancing function of the analog processor. Seventeen static latches store the 3½ digits of BCD data as well as overrange, underrange and polarity information. Nine push-pull output buffers (capable of driving one standard TTL load each) provide the sign, digit strobe and multiplexed BCD data outputs, all of which are active high. The digit scan is an interlaced format of digits 1, 3, 2 and 4.

Both devices are supplied in the 16-pin plastic DIP, and are specified for operation over the 0 to 70°C temperature range.

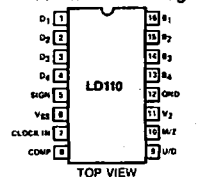
FUNCTIONAL BLOCK DIAGRAM



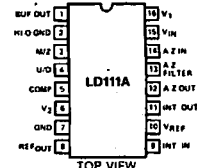
SWITCHES SHOWN FOR A LOGIC "0" AT U/D AND M/Z INPUTS.

PIN CONFIGURATION

Dual-In-Line Package



Dual-In-Line Package



Order Numbers:
LD110CJ and LD111ACJ
See Package 8

ABSOLUTE MAXIMUM RATINGS

I_{IN} (Pin 15, 2)	± 1 mA
$V_1 - V_2$ (LD111A)	30 V
V_{SS}	6 V
$V_{SS} - V_2$ (LD110)	20 V
V On Any Pin Relative to V_{SS} (LD110)	0.3 V to -20 V
V_{REF}	V_1

Operating Temperature	0 to 70°C
Storage Temperature	-65 to 125°C
Power Dissipation (Package)*	750 mW

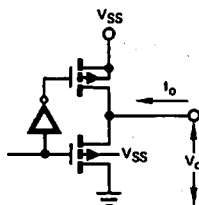
*Device mounted with all leads welded or soldered to PC Board. Derate 6.3 mW/°C above 25°C.

ELECTRICAL CHARACTERISTICS¹ $T_A = 25^\circ\text{C}$

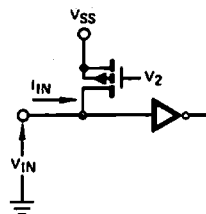
	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: $V_1 = +12\text{ V}$, $V_2 = -12\text{ V}$, $V_{SS} = 5\text{ V}$ $V_{REF} = 8.2\text{ V}$, $R_1 = 100\text{ K } \Omega$	LIMITS			UNIT
				MIN ²	TYP ³	MAX	
SYSTEM	Analog Input Range	V_{ANALOG}		-2 V		2 V	% rdg
	Linearity				0.02		
	Noise		Peak-to-Peak Noise Apparent When Going From One Steady Reading to Another		0.1		LSB
	Gain T.C.				5		ppm/°C
	Normal Mode Rejection	NMR	$f_{noise} = 60\text{ Hz}$		40		dB
	Clock Frequency	f_{IN}	50% Duty Cycle		30.7	250	kHz
INPUT	ON Resistance, Auto Zero Switch	$r_{DS(on)}$	$V_{AZ(in)} = -4.0\text{ V}$, $I_S = -30\text{ } \mu\text{A}$		6	20	K Ω
	Clock Input Current, Low	I_{CL}	$V_{CLOCK\text{ in}} = 0.4\text{ V}$	-500			μA
	Input Bias Current	I_{IN}			4		pA
AMP	Comp. LD110	I_{INL}	$V_{IN} = -12\text{ V}$	-1500	-700	-50	μA
	Reference Buffer	I_{source}	$V_{INL} (U/D) = 0.8\text{ V}$, $V_{OUT} = 0$		-800	-400	μA
	AZ Buffer	I_{sink}	$V_{AZ} = -4\text{ V}$, $V_{OUT} = 0\text{ V}$		800		
	Input Buffer	I_{sink}	$V_{IN} = -2\text{ V}$, $V_{OUT} = 0\text{ V}$	400	800		
	Input Buffer	I_{source}	$V_{IN} = 2\text{ V}$, $V_{OUT} = 0\text{ V}$		-100	-50	mV
	AZ Buffer	V_{offset}	$V_{OUT} = 0\text{ V}$	-100		100	
OUTPUT	Measure/Zero Voltage, Low	V_{OL1}	$I_{OL} = 150\text{ } \mu\text{A}$			0.6	V
	Measure/Zero Voltage, High	V_{OH1}	$I_{OH} = -200\text{ } \mu\text{A}$	2.4			
	Up/Down Logic Voltage, Low	V_{OL2}	$I_{OL} = 250\text{ } \mu\text{A}$			0.6	
	Up/Down Logic Voltage, High	V_{OH2}	$I_{OH} = -200\text{ } \mu\text{A}$	2.4			
	Analog Comparator Voltage	V_{OH3}	$I_{OH} = -100\text{ } \mu\text{A}$	2.4			
	Digits, Bits, Voltage, Low	V_{OL3}	$I_{OL} = 1.6\text{ mA}$			0.6	
	Sign Voltage, Low	V_{OL4}	$I_{OL} = 1.6\text{ mA}$			0.65	
	Data Bits Voltage, High	V_{OH4}	$I_{OH} = -200\text{ } \mu\text{A}$	2.4			
	Digits, Sign Voltage, High	V_{OH5}	$I_{OH} = -800\text{ } \mu\text{A}$	2.4			
SUPPLY	V_1 Supply Current, LD111A	I_1			2.2	4	mA
	V_2 Supply Current, LD111A	I_{2A}		-4	-1.8		
	V_2 Supply Current, LD110	I_{2D}		-23	-17		
	V_{SS} Supply Current, LD110	I_{SS}			17.4	24	
	Power Supply Rejection Ratio, V_1	PSRR ₁		80	85		dB
	Power Supply Rejection Ratio, V_2	PSRR ₂		60	65		
	Reference Voltage Rejection		$R_{REF} = R_2 = 100\text{ K } \Omega$, $V_{IN} = 2\text{ V}$		1		% Δ rdg/ ΔV_{REF}

NOTES:

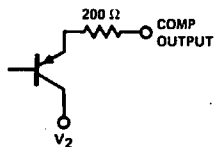
1. Refer to PROCESS OPTION FLOWCHART for additional information.
2. The algebraic convention whereby the most negative value is a minimum, and the most positive value is a maximum, is used in this data sheet.
3. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.



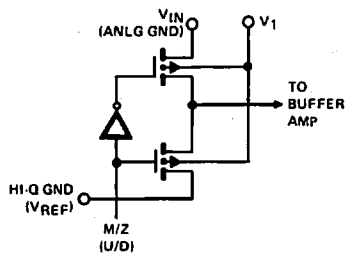
LD110 OUTPUT BUFFERS
(Digits, Bits, Sign, M/Z, U/D)



LD110 COMPARATOR, CLOCK INPUTS

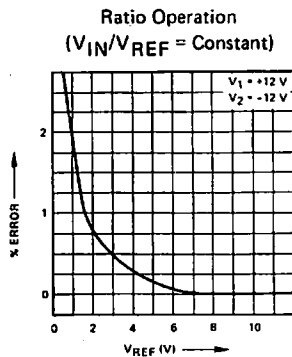
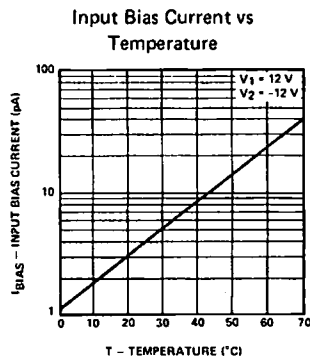
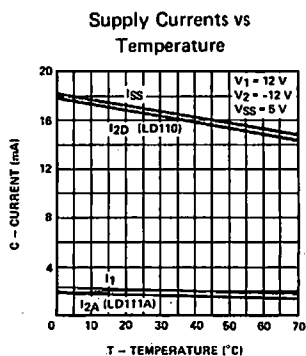


LD111A Comparator Output



LD111A Inputs (V_{IN} , V_{REF})

TYPICAL CHARACTERISTICS



DESCRIPTION OF PIN FUNCTIONS—LD111A

BUF OUT — The output of this unity gain input buffer amplifier is applied to the integrator summing node through a scaling resistor R_2 . The value of this resistor is typically 10K Ω for a 200.0 mV full scale and 100K Ω for a 2.000 V full scale. The digital output is inversely proportional to the value of this resistor.

$$\text{Count} = \frac{V_{IN}}{V_{REF}} \times \frac{R_1}{R_2} \times 8192$$

HI-QUALITY GND — This pin, typically connected to a High Quality Ground point for single ended inputs *can be used as the inverting input for differential signals*. The digital output will be $V_{IN} - V_{HI-Q}$. When using this differential mode, it is important that resistor R_3 be less than resistor R_2 for proper operation.

M/Z — Measure/Zero Logic Input. Internal level shifting drivers operate the PMOS switches in response to this digital signal.

U/D — Up/Down Logic Input. The logic signal applied to this pin operates a SPDT switch to provide Quantized pulses of charge to the integrator.

COMP — This analog comparator output is an open collector configuration which goes to V_2 when "low."

V_2 — Negative Supply Voltage. Recommended level is -12 V $\pm 10\%$.

GND — Analog Processor Ground. Should be kept separate from Digital Grounds.

REF_{out} — This buffered voltage output of the SPDT U/D switch, converted to a current by resistor R_1 , supplies the reference current to the integrator.

INT. IN — Integrator Summing Node.

V_{REF} — A stable positive reference voltage (2 to 10 V) applied to this pin is the standard to which the input voltage V_{IN} is measured. Ratio measurements can be made by applying a variable to this input (1.0 to 10 V).

INT. OUT — The output of the integrating amplifier is made available for application to the Auto-Zero amplifier by means of resistor R_4 .

AZ OUT — The output of the unity gain Auto-Zero amplifier provides a second negative reference current to the integrator through resistor R_3 .

AZ FILTER — The Auto-Zero Capacitor (C_{AZ}) connected to this pin stores D.C. voltage components to balance amplifier offset and drift components.

AZ IN — This input is switched into the AZ filter during the zeroing interval.

V_{IN} — Analog Voltage Input. The A/D System digitizes the voltage appearing at this input.

V_1 — Positive Supply Voltage. The recommended level is +12 volts $\pm 10\%$.

DESCRIPTION OF PIN FUNCTIONS — LD110

V_{SS} — Positive Supply Voltage. Recommended level is +5 V $\pm 10\%$.

V_2 — Negative Supply Voltage. Recommended level is -12 V $\pm 10\%$.

CLOCK IN — This input accepts a TTL or MOS level clock to drive the synchronous digital circuitry. Acceptable duty cycles on the external clock range from 30% high, 70% low to 70% high, 30% low for clock frequencies from 2 kHz to 250 kHz. Although any clock frequency between 2 kHz and 250 kHz may be used, clock frequencies that are integer divisions of 2048F_L (F_{IN} = 2048F_L/n, n = 1, 2, 3, ..., 51), (F_L = Line Frequency) provide measure and zero periods that are integer multiples of the line frequency period (T_{zero} = n/F_L, T_{measure} = 2n/F_L). Line frequency interference is minimized by the selection of one of these 51 frequencies.

This input has an active pull-up to V_{SS} .

M/Z — Measure/Zero Logic Output. This 0 to 5 volt logic output successively provides Autozero and Measurement intervals of 2048 and 4096 clock periods respectively. This output is compatible with CMOS logic and directly interfaces with the LD111A analog processor.

U/D — Up/Down Logic Output. This output has logic levels of 0 and +5 volts to provide pulse-width modulation of the reference current when used with the LD111A analog processor. This output is CMOS compatible.

COMP — Analog Comparator Input. This input has an active pull-up to V_{SS} for a comparator "high" state. This pin must be pulled down to V_2 for a "low" comparator state.

An End-of-Conversion Signal can be decoded from the three interconnecting logic lines (M/Z, U/D, Comp) using the following CMOS logic.

$$M/Z + U/D + \text{Comp} = \text{E.O.C.}$$

B₁, B₂, B₃, B₄ — BCD Data Bit Output. B₄ represents the most significant bit and B₁ the least significant bit of the BCD output. Bit 4 of digit 4 goes high for an underrange condition (less than 100 counts). These outputs are compatible with 1 standard TTL load.

$$\text{MUX Underrange} = B_4 \times D_4 \text{ (5\% of full scale)}$$

D₁, D₂, D₃, D₄ — Digit Strobe Outputs. D₄ is the most significant and D₁ the least significant digit of the 3 1/2 digit output. The digit strobes are each selected in turn when the BCD data bits for that digit appear at the bit outputs (see Figure 4).

$$\text{MUX Overrange} = D_1 + D_2 + D_3 + D_4 \\ \text{(100\% of full scale, count} \geq 2000\text{)}$$

SIGN — Sign of Analog Input Polarity. This TTL level output is a static signal which is either 0 or V_{SS} for a negative or positive input polarity respectively.

GND — Digital Processor Ground. Should be kept separate from Analog Grounds. Common connection should be made at the power supply.

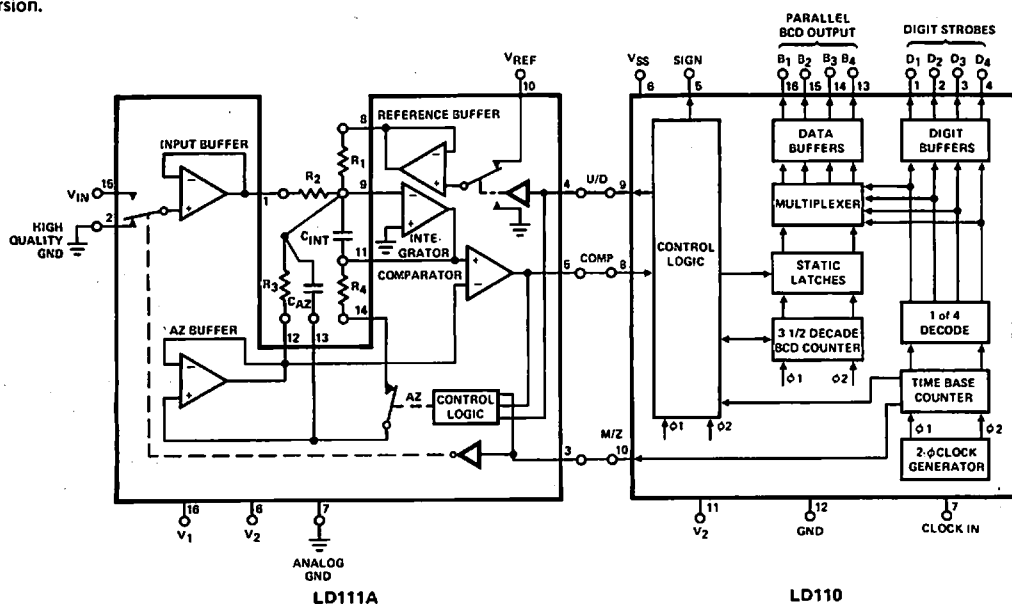
The Connection Diagram of Figure 1 should be referred to along with the timing diagrams of Figures 2, 3, and 4 in this discussion of functional operation.

Time Base Counter: An external clock signal using either TTL or MOS logic levels drives a 2- ϕ clock generator on the synchronous digital chip. The clock frequency is divided by the time base counter into sampling intervals of 6144 pulses of which 4096 constitute the measurement interval and 2048 the auto-zero interval. Intermediate frequency divisions are utilized by both the control logic and the 1 of 4 decoder for the digit enables and bit scan.

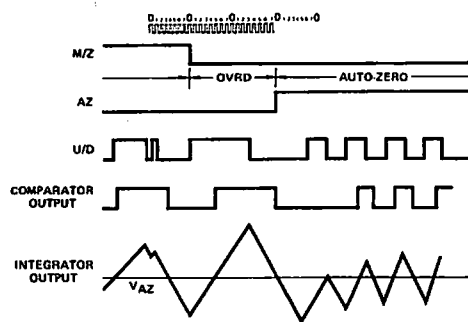
AUTO-ZERO INTERVAL

The Auto-Zero interval provides a means to null out the offset voltages of the amplifiers used in the LD110/LD111A system. In addition, it automatically establishes a second tracking reference voltage necessary for bipolar A/D conversion.

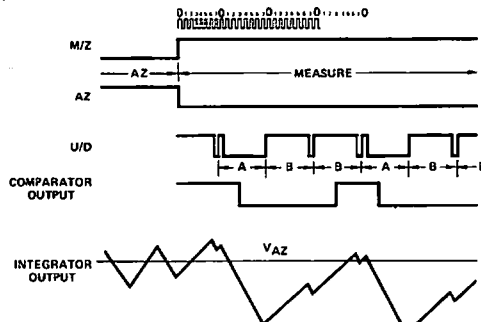
The Auto-Zero sequence is initiated when the M/Z (Measure/Zero) signal switches the input buffer amp to analog ground. After a brief count-correcting override period, the AZ switch is closed connecting the AZ amplifier and Integrator together in a closed-loop second-order system. During this time the control logic ignores the comparator output and pulses the U/D switch at a 50% duty cycle of 4 clock periods "Up" and 4 "Down" (see Figure 2). Equilibrium of this closed-loop system is attained when the average currents through R_1 and R_3 are equal and opposite. This is achieved when V_{AZ} , the Auto-Zero voltage, is equal to $-\frac{1}{2} V_{REF}$ ($R_1 = R_3$). Establishing V_{AZ} and storing it on C_{AZ} gives the U/D logic the capability of switching either a + or - reference current to the integrator during conversion. Thus when U/D is "Up," $I_1 + I_3 = -V_{REF}/2R_1$ and when U/D is "Down," $I_1 + I_3 = V_{REF}/2R_1$. The Auto-Zero interval is of sufficient duration to insure that V_{AZ} will be well established.



Connection Diagram
Figure 1



Auto-Zero Timing
Figure 2



Measure Interval Timing
Figure 3

FUNCTIONAL OPERATION (Cont.)

MEASUREMENT INTERVAL

The "Quantized Feedback" conversion system is characterized by a single phase Digitization interval in which a digital control system feeds back quantized units of charge in response to the sampled state of an analog comparator. These quanta of charge balance the charge being supplied to the integrator by the analog voltage. The magnitude ($V_{REF}/2R_1 \times 6/f_{clock}$) of the Quantized charge being fed back and its sign (+ or -) arise from the fact that the control logic has two U/D duty cycles available during the Measure interval as shown in Figure 3.

The U/D logic is "up" one clock cycle and "down" 7 cycles for a high comparator output in the clock cycle preceding a set of 8 cycles. This will be designated duty cycle "A." With a low comparator output in clock cycle number 7 the U/D logic will be "up" for 7 cycles and "down" for 1 cycle in the following 8 clock cycles. This is duty cycle "B." The effect of these two reference current duty cycles on the integrator output is shown in Figure 3. It can be seen that the "up" state of the U/D logic drives the integrator output voltage up. The up/down BCD counter increments by each clock pulse when the U/D logic is "up" and decrements by each clock pulse when the U/D logic is "down." Consequently the net count goes up 6 counts for a "B" duty cycle and down 6 for an "A" duty cycle.

Input polarity is determined by the first appearance of two consecutive duty cycles of the same type. The control logic would determine the analog input to be negative if two "A" duty cycles occur in succession and positive if two "B" duty cycles occur in succession.

Since the counting process is done by increments (or decrements) of 6 during the measure interval, a short override interval is required at the end of the Measurement to "fine tune" the count to the nearest LSB. This occurs within the first 32 clock periods of the AZ interval.

Following the count correcting override sequence; the contents of the BCD counters and sign flip-flop are loaded into the internal latches. Counter states of less than 100 or greater than 1999 are decoded as underrange or overrange conditions respectively. The underrange signal is forced on Bit 4 during D₄ time. The overrange signal will be used to blank the display during the zero interval giving a visual overrange cue by means of a blinking display.

The BCD data stored in the latches is continuously scanned every 32 clock periods (8 clock times per digit). This data format is shown in Figure 4. Sign information is available as a static signal on a separate pin (high for +, low for -).

The BCD data output is an interlaced scan of digits 1, 3, 2, and 4 where digit 4 is the most significant digit. All outputs are active high and TTL compatible.

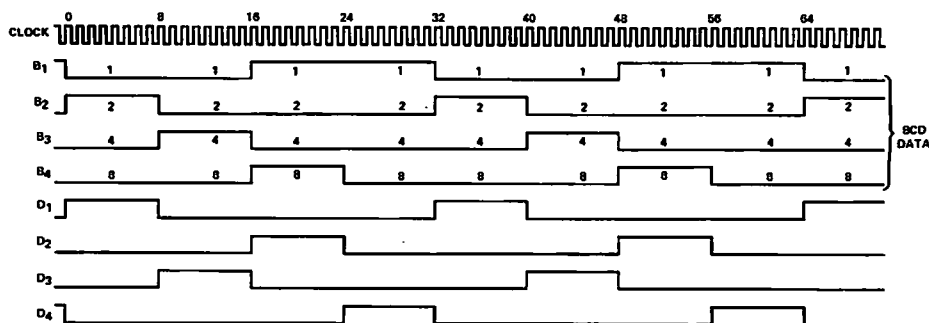
APPLICATIONS INFORMATION
(Refer to Figure 5)

1. Power Supplies

- a) The recommended supply voltages are:

V_1	= 12 V $\pm 10\%$
V_2	= -12 V $\pm 10\%$
V_{SS}	= 5 V $\pm 10\%$
V_{REF}	= 2.00 V to 10 V

Operation is possible with V_1 and V_2 supplies from ± 9 V to ± 15 V. These minimum voltages (± 9 V) require that the LD110/LD111A system be operated on the 200.0 mV scale to maintain input buffer linearity. It should be realized that operation below ± 10.8 volts is not guaranteed. V_2 voltages greater than -13.2 V allows the LD110 to dissipate a considerable amount of power (400 mW, warm to the touch). A 150 Ω resistor in series with pin 11 of the LD110 will limit the current resulting in cooler operation and longer life with large values of V_2 .



Data Output Format (Output = 1492)

Figure 4

APPLICATIONS INFORMATION (Cont.)

2. Input Protection. Under normal operating conditions the inputs of the LD111A should not be exposed to a voltage exceeding either V_1 or V_2 (see absolute maximum ratings). In many applications however, such as a DMM/DVM, the V_{IN} or V_{REF} input may have a high voltage source connected which is capable of supplying destructive currents into the LD111A. To prevent such an occurrence, a current limiting resistor should be placed in series with the appropriate input pin. The 1 mA maximum current rating should be observed. A 1M Ω resistor in series with pin 15 of the LD111A would offer input protection up to a 1000 V overvoltage.

3. Operation Over the Full Sampling Range. Any sampling rate from 1/3 to 40 samples/second can be accommodated by simply changing the values for C_{INT} and C_{AZ} (R_3 and R_4 will remain as shown in Figure 5).

To find the proper value for C_{INT} and C_{AZ} (shown as C_1 and C_2 respectively on Figure 5) find the needed clock frequency for a specific sampling rate from the following relationship.

$$f_{\text{clock}} = \text{Sampling Rate} \times 6144$$

Once the clock frequency has been determined, the values for C_{INT} and C_{AZ} can be found.

$$C_{INT} \cong \frac{200 \mu\text{F}/\text{sec}}{f_{\text{clock}}}$$

$$C_{AZ} \cong 10 C_{INT}$$

4. Resistor Selection. Resistor R_2 is the scaling resistor and is selected to provide 10 nA per LSB into the integrator summing junction. Thus,

$$\begin{aligned} R_2 &= \frac{V_{IN}(\text{Full Scale})}{(2000 \text{ Counts}) (10 \text{ nA/Count})} \\ &= 100\text{K } \Omega \text{ (2.000 V Scale)} \\ &= 10\text{K } \Omega \text{ (200.0 mV Scale)} \\ &= 1\text{K } \Omega \text{ (20.00 mV Scale)} \end{aligned}$$

The reference resistor R_1 is chosen to satisfy the relationship

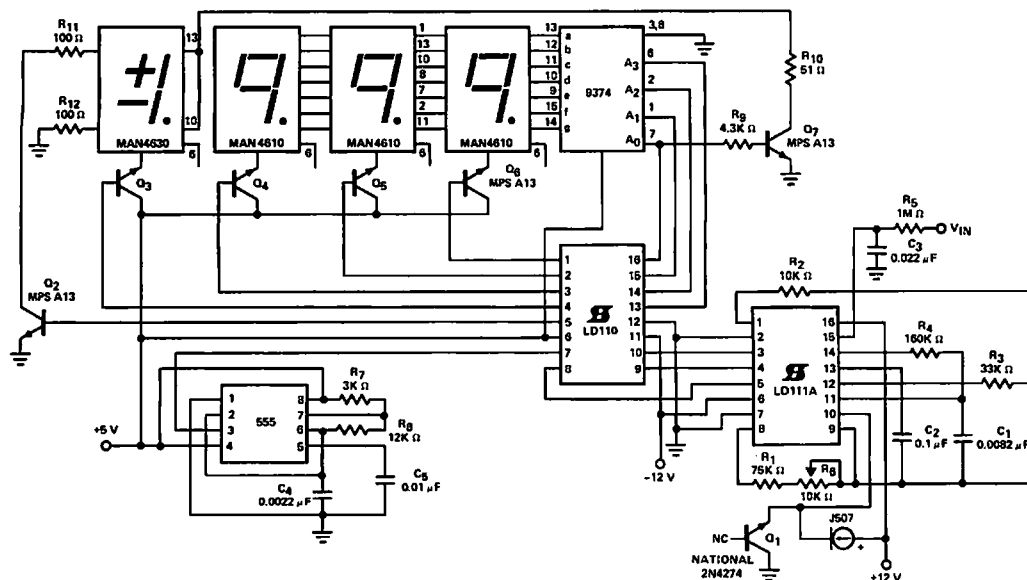
$$R_1 = \frac{V_{REF}}{81.92 \text{ V}} \text{ M } \Omega$$

(Trimmed)

5. 20.00 mV Scale (10 μV Resolution). The improved noise performance of the LD111A allows it to be used in a 20.00 mV DPM when R_2 is selected to be 1K Ω . This high resolution range, while useful, does not have the same degree of zero and LSD stability as the 200.0 mV and 2.000 V ranges. Extreme care in layout is required to minimize noise and offsets at V_{IN} and Hi-Q GND.

6. Ratio Operation. The LD110/LD111A is a ratio measuring system — the output being

$$\text{Count} = \frac{V_{IN}}{V_{REF}} \frac{R_1}{R_2} \quad 8192$$

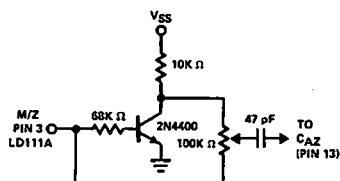


3 1/2 Digit DVM (± 200.0 mV) Common Anode Display

Figure 5

The high impedance input and reference buffer amplifiers offer a system with ratio operation and minimal source loading. The ratio curve shown with the typical characteristics illustrates the ratio performance.

7. Zero Adjustment. The LD110/LD111A converter set is an Auto-zeroing system. Many applications exist, however, in which a means of nulling out external offsets is needed. The circuit of Figure 6 provides this offset nulling feature.

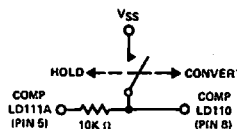


Offset Nulling Circuit
Figure 6

8. Replacing the LD111 with the LD111A. The LD111A offers a significant improvement in linearity, noise and temperature stability over the LD111. It also eliminates the need for the integrator clamp zener required on the LD111. The LD111A is a plug-in replacement for the LD111.

9. Data Valid (End-of Conversion). The BCD data from the LD110 is changed only once per conversion, at the end of the override interval. The 3½ digits of data are then repeatedly multiplexed out during the rest of the zero and for the full Measure Interval. Since the data cannot change during the Measure Interval and since the Measure Interval occurs once each sampling interval, this high state of the M/Z line can be used as a Data Valid or End-of-Conversion signal.

10. "Hold". The last conversion of the LD110/LD111A may be held indefinitely by means of the added circuitry shown in Figure 7. Forcing the comparator input of the LD110 to the high state eliminates any future data transfers. The resistor protects the LD111A comparator output. Opening the connection to VSS allows normal comparator action and data transfer. The first conversion after a "hold" will always be in error since the AZ voltage has not been maintained during "hold".



"Hold" Circuit
Figure 7

LD120/121A

4½ Digit A/D Converter Set



FEATURES

- 0.005% ± 1 Count Accuracy
- ± 200.0 mV and ± 2.000 V Ranges
- Auto Zero
- Auto-Polarity
- Over and Under Range Outputs

BENEFITS

- High System Performance
- Single Resistor Programming
- Nulls Out Offsets
- Single Reference
- Easily Interfaced

APPLICATIONS

- High Accuracy Digital Voltmeters and Panel Meters
- Digital Scales and Thermometer
- μ P Data Acquisition Systems
- Scientific Instrumentation

DESCRIPTION

The LD120 and LD121A form a precision 4 1/2 digit A/D converter system for use in display and microprocessor based data acquisition applications. Based on Siliconix's "Quantized Feedback" technique, intrinsic features include auto-polarity, auto-zero, and ratiometric operation. Except for a stable reference, no critical components are required to achieve rated performance. The technique used offers superior linearity, normal mode rejection, and stability due to the simultaneous integration of the unknown input and the reference voltages. Unlike other conversion techniques, the integrator output voltage never represents more than 100 counts. Thus, critical, high resolution performance is not required of either the integrator or the comparator.

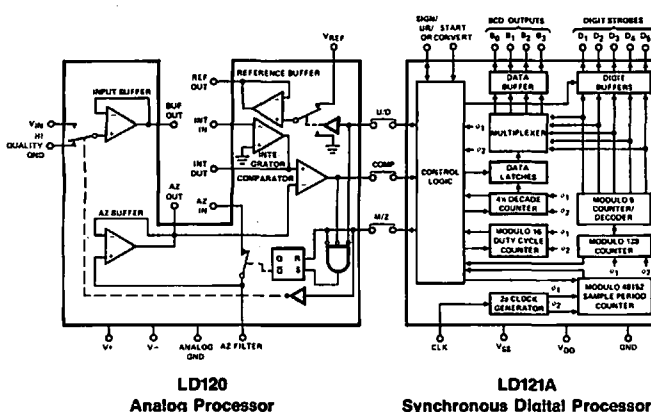
The LD120 analog processor is fabricated with a unique PMOS/Bipolar process. It contains all the necessary amplifiers, MOSFET switches, and switch driver circuits for the system. The reference voltage input is fully buffered in

LD120 to eliminate the reference switch resistance as a source of error. All the amplifiers are internally compensated. The LD120 directly interfaces the LD121A digital processor with no additional active components required.

The LD121A synchronous processor contains all the digital circuitry for the quantized feedback system. Device outputs supply two overrange signals, underrange, sign and 4½ digits of multiplexed BCD data. (All outputs are TTL compatible). Overage is also indicated by blinking digit strobes above 20,000 counts. An input is provided to inhibit this feature at user option. Microprocessor controlled operation is simplified by a start conversion input that allows conversion-on-command.

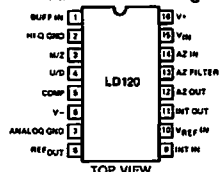
Both devices are supplied in space saving 300 mil dual-in-line plastic packages. The LD120 has 16 pins and the LD121A has 18 pins.

FUNCTIONAL BLOCK DIAGRAM

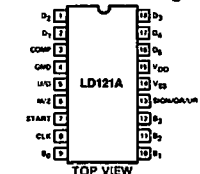


PIN CONFIGURATION

Dual-In-Line Package



Dual-In-Line Package



Order Numbers:
LD120CJ
See Package 8
LD121ACJ
See Package 19

Switch States are for a Logic "0" at U/D and M/Z Inputs.

ABSOLUTE MAXIMUM RATINGS

V_{IN} (Pin 15, 2 LD120)	$V^- < V_{IN} < V^+$
I_{INPUT} (LD120)	± 1 mA
$V^+ - V^-$ (LD120)	32 V
$V_{SS} - V_{DD}$ (LD121A)	20 V
Any Pin (LD121A)	V_{DD} to $V_{SS} \pm 0.3$
V_{REF}	V^+

Operating Temperature	0 to 70°C
Storage Temperature	-65 to 125°C
Power Dissipation (Package)*	750 mW
*Device mounted with all leads welded or soldered to PC Board. Derated 6.3 mW/°C above 25°C	

ELECTRICAL CHARACTERISTICS¹ $T_A = 25^\circ\text{C}$

	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: V+ = 12 V, V- = VDD = -12 V, VSS = 5 V		LIMITS			UNIT
					MIN ²	TYP ³	MAX	
SYSTEM ⁴	Linearity		fCLK = 163.84 kHz VREF = 6.8 V	2 V Scale	-1	±1/4	1	Count
		200 mV Scale		-2	±1/2	2		
	Noise ⁵			2 V Scale		1/3	1	
		200 mV Scale			1/2	2		
	Normal Mode Rejection Ratio	NMRR		fL = 50 or 60 Hz		40		dB
	Power Supply Rejection Ratio	PSRR			80			
	Gain T.C.				5	15	ppm/°C	
	Zero Drift		CSTRG = 1 μF, RIN ≤ 100 kΩ			1	5	Count
LD120 LINEAR	Analog Input Voltage	VANALOG			-5		5	V
	Output Source Current	ISOURCE	VIN = 2 V, Buff Out = 0 V			-100	-50	μA
	Output Sink Current	ISINK	VIN = -2 V, Buff Out = 0 V		400	800		
	Input Current	IIN	VIN = ±2.8 V			2	pA	
	Common Mode Rejection Ratio	CMRR				-72		dB
	Input Current/Input Voltage High	IIH	M/Z, U/D Inputs	VIN = 2.0 V			20	μA
	Input Current/Input Voltage Low	IIL		VIN = 0.8 V	-100			
	Output Source Current	ISOURCE				-100		μA
	Output Sink Current	ISINK				800		
	Offset Voltage	VOFFSET	VOUT = 0 V		-50		50	mV
	Switch Resistance (on) ⁹		VSTRG = -4 V, IDS = 30 μA			6	20	kΩ
	LD121A DIGITAL	Reference Buffer Source Current	ISOURCE	VIN (U/D IN) = 0.8 V, VO = 0 V			-800	-400
Reference Buffer Sink Current		ISINK	VIN (U/D IN) = 2.0 V, VO = 2 V			100		
Integrator Source Current ¹⁰		ISOURCE	VIN (Int. IN) = -100 mV, VO = 0 V			-100	-50	
Integrator Sink Current ¹⁰		ISINK	VIN (Int. IN) = 100 mV, VO = 0 V		400	800		
Output Swing					-10		10	V
SUPPLY		Comparator Output Voltage	VOUT	RL = 10 k to 5 V AZ FILTER IN = 100 mV INTEGRATOR OUT = 0 V		-5		
	Comparator Offset Voltage	VOFFSET	-5				5	
	Positive Supply Voltage	V+			9	12	15	V
	Negative Supply Voltage	V-			-15	-12	-9	V
DYNAMIC	Positive Supply Current	I+					3.5	mA
	Negative Supply Current	I-			-3.5			
	Input Voltage High	VINH	Comparator Input, Sign/UR/OR/ Blink ⁶ , Start, CLK IN		4			V
	Input Voltage Low	VINL					0.5	
	Input Current/Input Voltage High	IINH	VIN = 5 V (Sign/OR/UR ⁶)			170	300	μA
	Input Current/Input Voltage Low	IINL	VIN = 0 V (Start Convert, Clock)		-400	-150		
	Output Voltage High	VOH	Bit Lines, Sign/OR/UR, Digit Strobes	I _{OH} = -40 μA	2.4			V
	Output Voltage Low	VOL		I _{OL} = 1.6 mA			0.6	
	Output Voltage High	VOH	M/Z	I _{OH} = -150 μA	4			V
	Output Voltage Low	VOL		I _{OL} = 0.8 mA			0.6	
Output Voltage High	VOH	U/D	I _{OH} = -0.5 mA	4			V	
Output Voltage Low	VOL		I _{OL} = 0.8 mA			0.6		
SUPPLY	Start Convert ⁷	t _p			20			μs
	Clock Frequency	fCLK	50% Duty Cycle		50		250	kHz
	Rep Rate (Strobes)		fCLK ~640		78		470	Hz
	Positive Supply Voltage	VSS	Range Over which Functionality is Guaranteed		4.5	5	5.5	V
	Negative Supply Voltage	VDD			-13.2	-12	-10.8	
	Positive Supply Current ⁸	ISS				14	25	mA
Negative Supply Current	IDD			-25	-14			

NOTES

(See next page)

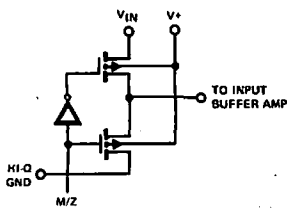
ELECTRICAL CHARACTERISTICS¹ (Cont.)

PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: $V^+ = 12\text{ V}$, $V^- = V_{DD} = -12\text{ V}$, $V_{SS} = 5\text{ V}$	LIMITS			UNIT
			MIN ²	TYP ³	MAX	
Zero Drift ⁴		$I_{CLK} = 163.84\text{ kHz}$, $V_{REF} = 6.8\text{ V}$ $C_{STRG} = 1\text{ }\mu\text{F}$, $R_{in} \leq 100\text{ k}\Omega$			5	Count

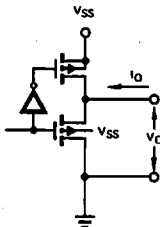
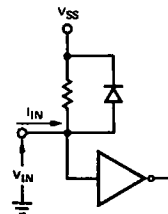
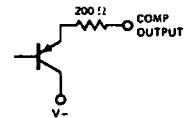
NOTES:

1. Refer to PROCESS OPTION FLOWCHART for additional information.
2. The algebraic convention whereby the most negative value is a minimum, and the most positive value is a maximum, is used in this data sheet.
3. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
4. System parameters not directly tested.
5. Bit width over which reading is stable 95% of the time.
6. Pin characteristic only during D_4 strobe time.
7. Minimum positive going pulse width to initiate a conversion.
8. All outputs disconnected.
9. V_{STRG} must be more positive than -4 V .
10. Reference source impedance must be less than $10\text{ k}\Omega$.

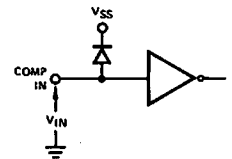
INPUT/OUTPUT SCHEMATICS



LD120 Input

LD121A Output Buffers
(Digits, Bits, Sign, M/Z U/D)LD121A Clock Input
Start Convert

LD120 Comparator Output



LD121A Comparator Input

Timing: The external oscillator is divided to generate a 2- ϕ clock on the synchronous digital chip. A time base generator divides the clock frequency into sampling intervals of 49,152 pulses of which 16,384 pulses are the Auto-Zero interval and 32,768 pulses are the measure interval.

Auto-Zero Interval: The connection diagram in Figure 1 illustrates the system during the Auto-Zero interval. The input buffer is switched to reference ground and supplies a current equal to its offset voltage divided by R_2 to the integrator summing node. The U/D buffer is toggled by the digital processor between V_{REF} and ground with a 50% duty cycle. This results in a current flow equal to V_{REF}/R_1 to the summing node half of the time. The AZ capacitor, C_{STRG} , assumes a voltage, V_{STRG} , that is equal to the average value of integrator output. The AZ buffer supplies a current to the summing node equal to the V_{STRG} voltage divided by R_3 .

The system will reach an equilibrium when the sum of the DC currents into the summing node equal zero. At this time, the current through R_3 equals $-\frac{1}{2} V_{REF}/R_1$ plus the small currents necessary to cancel the offset of the input buffer and integrator input bias current. Capacitor

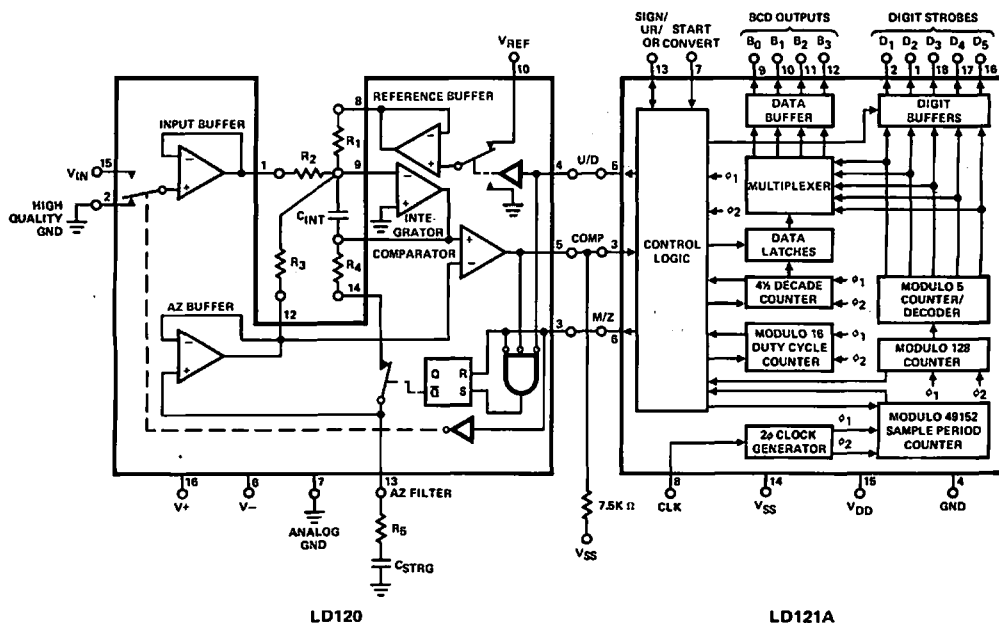
C_{STRG} "stores" V_{STRG} when the AZ switch opens at the end of the Auto-Zero interval. The digital BCD counter is inactive during Auto-Zero. It is reset to zero during the last clock pulse of the Auto-Zero interval.

THE U/D CONTROL DURING THE MEASURE INTERVAL

The U/D buffer is switched to V_{REF} when the U/D control is low. In this state the currents through R_1 and R_3 sum to $\frac{1}{2} V_{REF}/R_1$. A high level on the U/D control connects the U/D buffer to ground. During this state the sum of the currents through R_1 and R_3 sum to $-\frac{1}{2} V_{REF}/R_1$. In one clock cycle, a charge equal to $V_{REF}/2R_1 f_{IN}$ coulombs is either added or subtracted to the integrator capacitor. The BCD counter is decremented for each addition of this quantized charge and incremented for each subtraction of quantized charge.

THE MEASURE ALGORITHM

The input is connected to V_{IN} during the measure interval and supplies a current to the integrator equal to V_{IN}/R_2 .



Connection Diagram
Figure 1

FUNCTIONAL SYSTEM OPERATION (Cont.)

This causes the integrator output to move away from V_{STRG} . The digital processor attempts to keep the integrator output near V_{STRG} by adding or subtracting quantized charge to C_{INT} . The net amount of charge required to accomplish this is totaled by the BCD counter. The BCD count at the end of conversion equals the number of charge parcels necessary to cancel the input current supplied through R_2 . The resulting count is proportional to the voltage at V_{IN} .

U/D DUTY CYCLE CONTROL DURING THE MEASURE INTERVAL

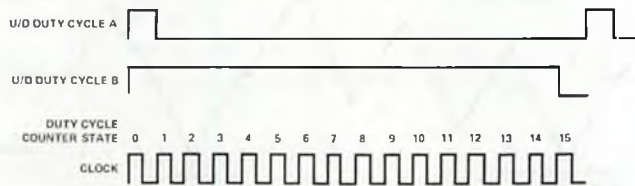
The digital processor contains a modulo 16 duty cycle counter that provides the U/D control output. This counter examines the state of the comparator once each 16 clock cycles during state 15. If the comparator is high, the U/D control will be high for one cycle and low for 15 cycles in the next 16 clock cycle period of the duty cycle counter. If the comparator output is low, the U/D control will be high for 15 cycles and low for one cycle in the next period of the duty cycle counter. Figure 2 illustrates these waveforms. The effect of these two duty cycles is to source or sink a net 14 charge parcels to C_{INT} , thus driving the

integrator output toward V_{STRG} and accumulating counts in the BCD counter in groups of 14 counts. This dual duty cycle control technique results in a fixed number of U/D control transitions, regardless of the value of V_{IN} ; therefore, these transitions cannot cause linearity error. The first few periods of the measure interval are illustrated in Figure 3 for a negative V_{IN} .

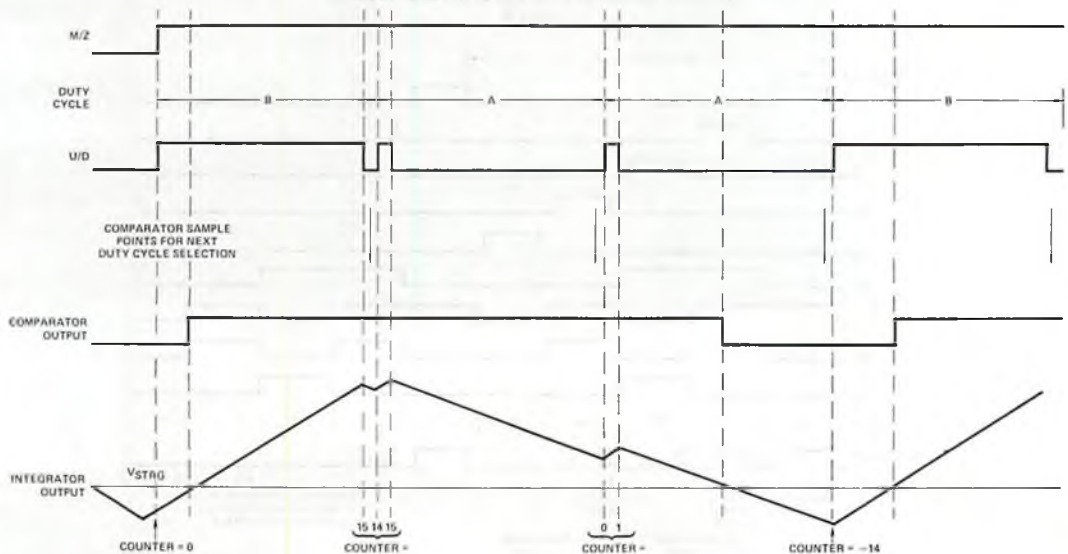
AUTO-ZERO OVERRIDE AT THE END OF MEASURE

The BCD counter contents equal a multiple of 14 counts at the end of the measure interval. A residual voltage on C_{INT} represents the remaining unresolved portion of the input voltage. This voltage is cancelled and the corresponding counts accumulated during a brief override period at the start of the AZ interval. Normal AZ interval action is inhibited until this residual count is resolved.

The override period starts at the end of the Measure Interval. The input buffer is switched to reference ground as no additional charge is desired from V_{IN} . The U/D control is set high. After the comparator goes high, the U/D control is switched low at the next state 8 of the duty cycle counter. The next transition of the comparator ends the



Modulo 16 Dual Duty Cycle Counter Waveforms
Figure 2



Measure Interval Timing ($V_{IN} \approx -1 V$)
Figure 3

conversion and the BCD counter is synchronously inhibited. The output latches are updated on the next clock pulse with the sign and contents of the BCD counter. The override period ends (end of conversion) and normal AZ action is initiated by the closing of the AZ switch. The duty cycle counter now drives the U/D control high during states 0 through 7 and low during states 8 through 15 for the required AZ interval 50% duty cycle.

Figure 4 illustrates the events at the end of the measure interval. The slope of the dotted lines is proportional to the unknown current through R_2 .

The self oscillation following the override period keeps V_{INT} near V_{STRG} until sync is achieved with the duty cycle counter. This feature eliminates large transients on C_{STRG} and results in highly stable Auto-Zero loop characteristics.

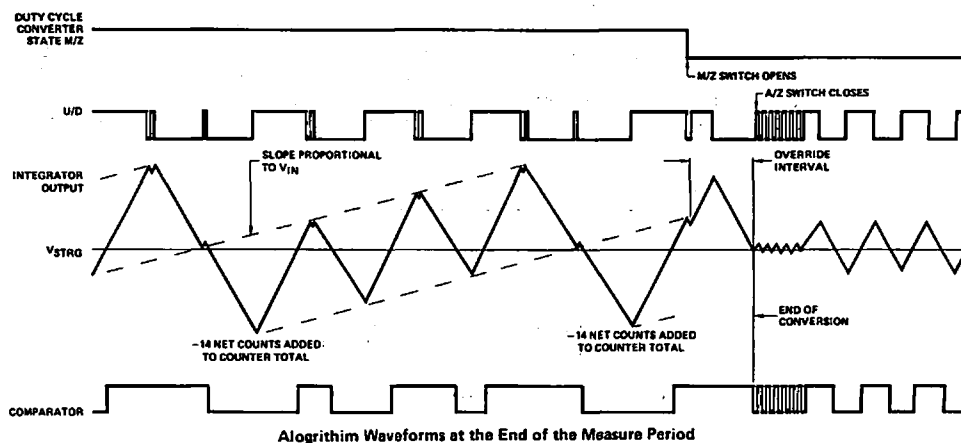
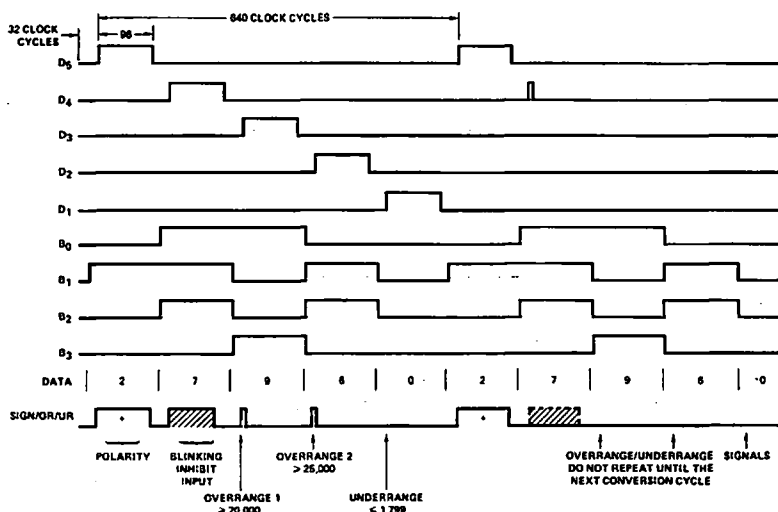


Figure 4



LD121 Digital Output Timing Diagram

Figure 5

DIGITAL INTERFACE FUNCTIONAL DESCRIPTION

BCD Outputs—(Pins 9, 10, 11 and 12): The output latch contents are time multiplexed in a digit serial, bit parallel fashion through 4 push-pull TTL compatible output buffers. A high level (sourcing current from V_{SS}) indicates a one and a low level (sinking current to ground) indicates a zero. B_0 is the least significant Bit. Figure 5 illustrates the timing relationship. All BCD outputs are valid during digit strobe time.

Digit Strokes—(Pins 1, 2, 16, 17 and 18): Figure 5 indicates the operation of these outputs. The strobes are TTL compatible. Only one strobe is high at one time. The strobe period is equal to 640 clock cycles with a 15% duty cycle. An inter-digit blanking period of 32 clock cycles permits easy interface with gas discharge displays. The strobe sequence is D_5 (MSD), D_4 , D_3 , D_2 , D_1 (LSD).

FUNCTIONAL SYSTEM OPERATION (Cont.)

Clock Input (Pin 8): Pin 8 requires an external clock input. The system operates from the positive clock transition allowing a 30 to 70% duty cycle in the external oscillator waveform. To maintain the linearity specifications of the A/D converter set the short term stability of this oscillator should be better than 1 part in 2×10^4 .

Sign/Overrange/Underrange (Pin 13): This pin operates as a TTL compatible output during D_1 , D_2 , D_3 and D_5 strobe times and as an input during D_4 strobe time. Figure 5 indicates the timing relationship. Information is presented to this output as follows:

At D_5 Time — Polarity is indicated by a high level for positive and a low level for negative. It is valid approximately 0.25 μsec after D_5 goes high until the end of each D_5 strobe.

At D_4 Time — The output buffer assumes a high impedance state. An input latch samples the voltage level imposed on this pin during D_4 time. A high level will inhibit the overrange blinking (digit strobes are suppressed during zero interval). An internal pull down resistor will hold the pin voltage low if the pin is unconnected or the load is high impedance. An alternative method for selecting overrange blinking is the choice of output buffer. A TTL buffer connected to pin 13 provides a pullup inhibiting overrange blinking. A NPN buffer driver provides a pulldown yielding normal

overrange blinking.

At D_3 Time — If the count is equal to or greater than 20,000, a single positive going pulse will occur at the beginning of the first D_3 time after the end of conversion cycle. The pulse width equals one clock cycle. The overrange blinking is momentarily inhibited when overrange pulses are present to prevent the display blinking feature from interfering with the decoding of the overrange output.

At D_2 Strobe—Time A second overrange pulse occurs at the beginning of the first D_2 time, after the end of conversion, if the count is equal or exceeds 25,000 counts.

At D_1 Strobe—Time A single pulse occurs at the beginning of the first D_1 time after the end of conversion, if the count is less than 1800 counts.

All overrange and underrange signals are one clock pulse wide. They occur only once per measure/zero cycle.

Start Conversion (Pin 7): A low level on this TTL compatible input holds the system in the zero mode continuously. A positive going pulse at least one clock time wide initiates one conversion cycle within 16 clock cycles after system has completed minimum auto zero cycle. The digital data is valid after 32,850 clock cycles. A static high level on this input provides normal cyclical operation. An internal pull up resistor allows this input to remain unconnected when conversion control is not desired.

APPLICATIONS

1. The recommended supply voltages are:

$$\begin{aligned} V_+ &= 12 \text{ V} \pm 10\% & V_{SS} &= 5 \text{ V} \pm 10\% \\ V_{DD}, V_- &= -12 \text{ V} \pm 10\% & V_{REF} &= 2 \text{ V to } 10 \text{ V} \end{aligned}$$

2. The reading is essentially the proportionality of V_{IN} compared to V_{REF} as shown in the gain equation:

$$\text{READOUT} = (V_{IN} - V_{HI-Q GND}) \cdot \frac{R_1}{R_2} \cdot \frac{65,536}{V_{REF}}$$

R_1 is independent of the U/D switch resistance due to the incorporation of the U/D buffer amplifier in the LD120. Gain can be calibrated either by varying V_{REF} or trimming the resistance of R_1 to obtain the correct full scale reading.

3. The output of the integrator should always be more positive than -9 V (for $V_{DD} = -12 \text{ V}$) to obtain specified accuracy:

$$V_O (\text{min}) > -9 \text{ V}$$

$$V_O (\text{min}) = -\frac{V_{REF} R_3}{2R_1} - \frac{15}{f_{CLK} C_{INT}} \left[\frac{V_{REF}}{2R_1} + \frac{V_{IN} (\text{max})}{R_2} \right]$$

Change value of C_{INT} to set $V_{INT}(P-P)$.

Large integrator swing provides the best performance. $V_{INT}(P-P) = 6$ to 8 volts is recommended.

$$V_{INT}(P-P) = \frac{30}{f_{CLK} C_{INT}} \left[\frac{V_{REF}}{2R_1} + \frac{V_{IN} (\text{max})}{R_2} \right]$$

APPLICATIONS (Cont.)

4. Although any oscillator frequency from 50 kHz to 250 kHz can be used, frequencies that provide integer number of line frequency cycles per measure period provide maximum line noise rejection. These frequencies are:

$$f_{CLK} = \frac{32,768 F_{LINE}}{n}, n = 8, 9, 10, \dots 40$$

$f_{CLK} = 163,840$ is popular since it provides both 50 and 60 Hz rejection.

5. The sampling rate = $f_{CLK}/49,152$ cycles/sample.

6. After a start conversion pulse, data is valid 32,850 clock pulses later and remains valid until at least 32,768 clock pulses after the next start pulse. During continuous cycle operation, data is assured valid when M/Z is high or 100 clock cycles after the one/zero transition of M/Z.

7. Any capacitive coupling between U/D and Comp. is detrimental to proper algorithm operation. PC board layouts should not allow these traces to be adjacent.

8. All power supplies should be capacitively bypassed to ground for maximum count stability.

9. C_{INT} and C_{STRG} should be selected for low leakage. Silvered mica is recommended for C_{INT} and mylar for C_{STRG}. Polypropylene capacitors also work well for both C_{STRG} and C_{INT}.

10. For a given leakage into C_{STRG} of I_{STRG}:

$$\Delta V_{STRG} = \frac{\Delta t I_{AZ}}{C_{STRG}}$$

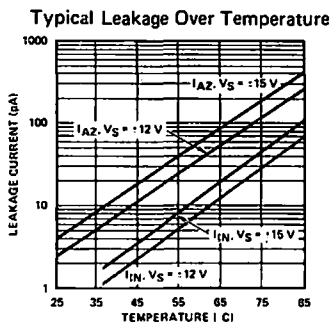
$$\text{where } \Delta t = \text{a measure interval} = \frac{2}{3} \times \frac{1}{F_{SAMPLE}}$$

ΔV_{STRG} will inject a ΔI integrator of $\Delta V_{STRG}/R_3$

Now a ΔI integrator would have been equivalent to a $\Delta V_{IN}/R_2$

So the equivalent input drift is

$$\Delta V_{IN} = \frac{1}{2} \times \frac{R_2}{R_3} \times \frac{2}{3} \times \frac{I_{STRG}}{F_{SAMPLE} \cdot C_{STRG}}$$



the $\frac{1}{2}$ factor is provided by integrator action.

Example: We wish to see 1 count (0.1 mV of ΔV_{IN} on the 2 V range) of drift for the circuit of Figure 7 with $I_{STRG} = 100 \text{ pA}$ @ 70°C . What C_{STRG} is needed?

Answer:

$$C_{STRG} = \frac{R_2}{R_3} \times \frac{1}{3} \times \frac{I_{STRG}}{F_{SAMPLE} \cdot \Delta V_{IN}} =$$

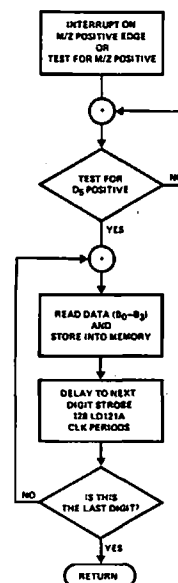
$$\frac{100K \Omega}{62K \Omega} \times \frac{1}{3} \times \frac{10^{-10} \text{ F}}{3 \text{ Hz} \times 10^{-4} \text{ V}}$$

$$= 0.18 \mu\text{F Minimum}$$

11. Interfacing the LD120/LD121A to Microprocessors: A description of interfacing the LD120/LD121A to the 8080 μP is given in AN77-3. Some of the timing details warrant description here.

The end-of-conversion is determined by gating $\overline{M/Z} \cdot \overline{U/D} \cdot \overline{COMP}$. At this time, all BCD latches are updated with the contents of the latest conversion.

We recommend using the negative edge of M/Z to interrupt the processor. Next, test for a high D₅ digit strobe (MSD). Once D₅ is high load the BCD data from B₀–B₃ lines and the polarity information from the SIGN/OR/UR line. Next delay 128 LD121A clock times (this assures that the D₄ data is valid) then load B₀–B₃ lines containing the D₄ data. Next delay another 128 LD121A clock times (this assures that the D₃ data is valid) then load B₀–B₃ lines containing the D₃ data. Repeat this process for D₂ and finally the D₁ (LSD) data load. In flowchart form (see Figure 6).

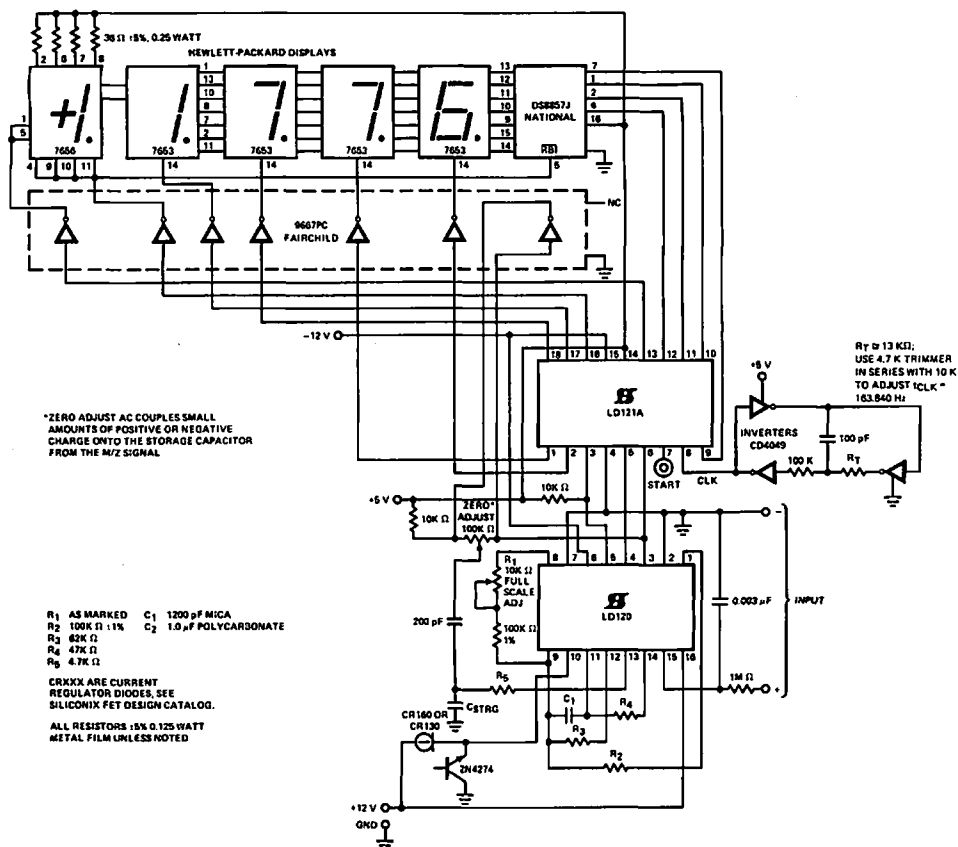


Flow Chart for 8080 Interface
Figure 6

APPLICATIONS (Cont.)

CIRCUIT BENEFITS

- Overrange Blinking
- $0 \rightarrow \pm 1.9999$ Input Voltages
- Zero Adjust to Null Offset Introduced by PC Board Leakages and Comparator



4 1/2 Digit DVM
Figure 7

LD122/LD121A

4½ Digit A/D Converter Set



FEATURES

- 0.005% ±1 Count Accuracy
- Two Ranges
- Auto Zero
- Auto-Polarity
- Over and Under Range Outputs

BENEFITS

- High System Performance
- Single Resistor Programming
- Nulls Out Offsets
- Single Reference
- Easily Interfaced

APPLICATIONS

- High Accuracy Digital Voltmeters and Panel Meters
- Digital Scales and Thermometer
- μ P Data Acquisition Systems
- Scientific Instrumentation

DESCRIPTION

The LD122 and LD121A form a precision 4 1/2 digit A/D converter system for use in display and microprocessor based data acquisition applications. Based on Siliconix's "Quantized Feedback" technique, intrinsic features include auto-polarity, auto-zero, and ratiometric operation.

The LD122/LD121A combination is used to extend system resolution beyond the 10 μ V maximum available from the LD120/LD121A system. By adding a user selected low noise input amplifier, and appropriate filter, any input resolution can be achieved. Except for this added buffer and a stable reference, no critical components are required to achieve rate performance. The technique used offers superior linearity, normal mode rejection, and stability due to the simultaneous integration of the unknown input and the reference voltages. Unlike other conversion techniques, the integrator output voltage never represents more than 100 counts. Thus, critical, high resolution performance is not required of either the integrator or the comparator.

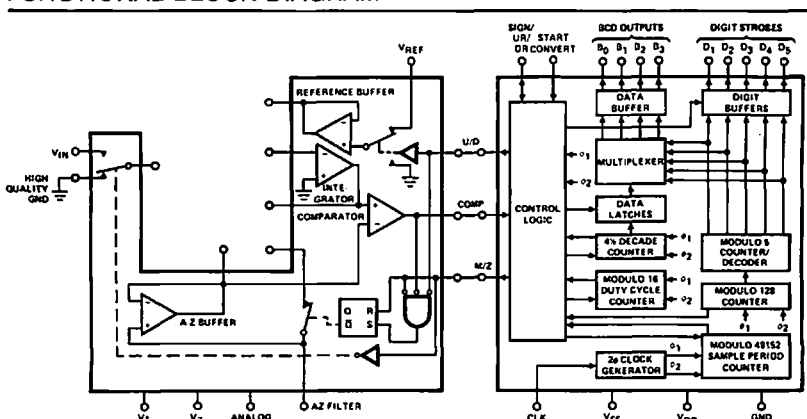
The LD122 analog processor is fabricated with a unique combined PMOS/Bipolar process. It contains all the

necessary amplifiers, MOSFET switches, and switch driver circuits for the system. The reference voltage input is fully buffered on the LD122 to eliminate the reference switch resistance as a source of error. All the amplifiers are internally compensated. The LD122 directly interfaces the LD121A digital processor with no additional active components required.

The LD121A synchronous processor contains all the digital circuitry for the quantized feedback system. Device outputs supply two overrange signals, underrange, sign and 4½ digits of multiplexed BCD data. (All outputs are TTL compatible). Overage is also indicated by blinking digit strobes above 20,000 counts. An input is provided to inhibit this feature at user option. Microprocessor controlled operation is simplified by a start conversion input that allows conversion-on-command.

Both devices are supplied in space saving 300 mil dual-in-line plastic packages. The LD122 has 16 pins and the LD121A has 18 pins.

FUNCTIONAL BLOCK DIAGRAM



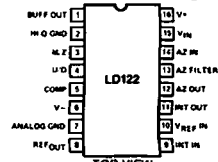
LD122-Analog Processor

LD121A-Synchronous Digital Processor

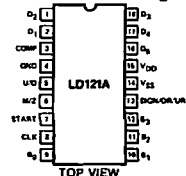
Switch States are for a Logic "0" at U/D and M/Z Inputs.

PIN CONFIGURATION

Dual-In-Line Package



Dual-In-Line Package



Order Numbers:
LD122CJ, See Package 8
LD121ACJ, See Package 19

ABSOLUTE MAXIMUM RATINGS

V_{in} (Pin 15, 2 of LD122) $V^- < V_{in} < V^+$
 $V^+ - V^-$ (LD122) 32 V
 $V_{SS} - V_{DD}$ (LD121A) 20 V
 Any Pin (LD121A) V_{DD} to $V_{SS} \pm 0.3$
 V_{REF} +V

Operating Temperature 0 to 70°C
 Storage Temperature -65 to 125°C
 Power Dissipation (Package)* 750 mW
 *Device mounted with all leads welded or soldered to PC Board. Derated 6.3 mW/°C above 25°C.

ELECTRICAL CHARACTERISTICS¹ $T_A = 25^\circ\text{C}$

	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: V+ = 12 V, V- = VDD = -12 V, VSS = 5 V	LIMITS			UNIT		
				MIN ²	TYP ³	MAX			
SYSTEM ⁴	Linearity		fCLK = 163.84 kHz VREF = 6.8 V	2 V Scale	-1	±1/4	1	Count	
	Noise ⁵			200 mV Scale	-2	±1/2	2		
				2 V Scale		1/3	1		
	Normal Mode Rejection Ratio	NMRR		200 mV Scale		1/2	2	dB	
	Power Supply Rejection Ratio	PSRR		fL = 50 or 60 Hz		80			
	Gain T.C.					5	15	ppm/°C	
	Zero Drift		CSTRG = 1 μF, Rin ≤ 100 kΩ		1	5	Count		
LD122 LINEAR	Analog Input Voltage	VANALOG		-3		3	V		
	ON Resistance, Vin or Hi-Q Switches	rDS(on)	VA = 1 V			5.5	kΩ		
			VA = -1 V			8			
	Leakage Current, Switch ON or OFF	ILEAKAGE	vin = ±2.8 V		2		pA		
	Input Current/Input Voltage High	IIH	M/Z, U/D Inputs	vin = 2.0 V		20	μA		
	Input Current/Input Voltage Low	IL	vin = 0.8 V	-100					
	Output Source Current	ISOURCE			-100		μA		
	Output Sink Current	ISINK			800				
	Offset Voltage	VOFFSET	VOUT = 0 V	-50		50	mV		
	Switch Resistance (on) ⁹		VSTRG = -4 V, IDS = 30 μA		6	20	kΩ		
	Reference Buffer Source Current	ISOURCE	vin (U/D IN) = 0.8 V, VO = 0 V		-800	-400	μA		
Reference Buffer Sink Current	ISINK	vin (U/D IN) = 2.0 V, VO = 2 V		100					
Integrator Source Current ¹⁰	ISOURCE	vin (Int. IN) = -100 mV, VO = 0 V		-100	-50				
Integrator Sink Current ¹⁰	ISINK	vin (Int. IN) = 100 mV, VO = 0 V	400	800					
Output Swing			-10		10	V			
COMP	Comparator Output Voltage	VOUT	RL = 10 k to 5 V AZ FILTER IN = 100 mV INTEGRATOR OUT = 0 V	-5			mV		
	Comparator Offset Voltage	VOFFSET		-5		5			
SUPPLY	Positive Supply Voltage	V+		9	12	15	V		
	Negative Supply Voltage	V-		-15	-12	-9			
	Positive Supply Current	I+				3.5	mA		
	Negative Supply Current	I-		-3					
	Ground Current	IGND	M/Z, U/D = 2.4 V	-2					
INPUTS	Input Voltage High	VINH	Comparator Input, Sign/UR/OR/ Blink ⁶ , Start, CLK IN	4			V		
	Input Voltage Low	VINL				0.5			
	Input Current/Input Voltage High	IINH	vin = 5 V (Sign/OR/UR ⁶)		170	300	μA		
	Input Current/Input Voltage Low	IINL	vin = 0 V (Start Convert, Clock)	-400	-150				
OUTPUTS	Output Voltage High	VOH	Bit Lines, Sign/OR/UR, Digit Strokes	I _{OH} = -40 μA	2.4				
	Output Voltage Low	VOL		I _{OL} = 1.6 mA		0.6			
	Output Voltage High	VOH	U/D	I _{OH} = -0.5 mA	4				
	Output Voltage Low	VOL		I _{OL} = 0.8 mA		0.6			
DYNAMIC	Start Convert ⁷	tp		20			μs		
	Clock Frequency	fCLK	50% Duty Cycle	50		250	kHz		
	Rep Rate (Strokes)		fCLK = 640	78		470	Hz		
SUPPLY	Positive Supply Voltage	VSS	Range Over which Functionality is Guaranteed	4.5	5	5.5	V		
	Negative Supply Voltage	VDD		-13.2	-12	-10.8			
	Positive Supply Current ⁸	ISS				14		mA	
	Negative Supply Current	IDD			-25	-14			

NOTES

(See Next Page)

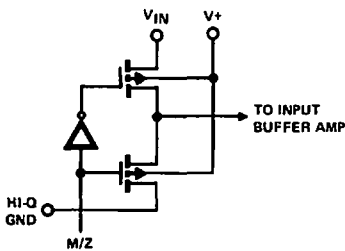
ELECTRICAL CHARACTERISTICS (Cont.)

	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: $V_+ = 12\text{ V}$, $V_- = V_{DD} = -12\text{ V}$, $V_{SS} = 5\text{ V}$	LIMITS			UNIT
				MIN ²	Typ ³	MAX	
SYS	Zero Drift ⁴		$I_{CLK} = 183.84\text{ kHz}$, $V_{REF} = 6.8\text{ V}$ $C_{STRG} = 1\text{ }\mu\text{F}$, $R_{in} \leq 100\text{ k}\Omega$			5	Count

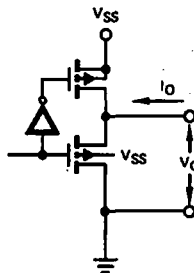
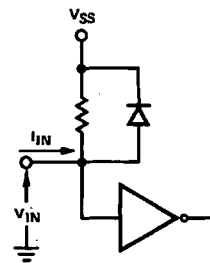
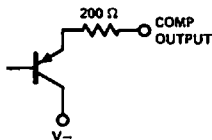
NOTES:

1. Refer to PROCESS OPTION FLOWCHART for additional information.
2. The algebraic convention whereby the most negative value is a minimum, and the most positive value is a maximum, is used in this data sheet.
3. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
4. System parameters not directly tested.
5. Bit width over which reading is stable 95% of the time.
6. Pin characteristic only during D_4 strobe time.
7. Minimum positive going pulse width to initiate a conversion.
8. All outputs disconnected.
9. V_{STRG} must be more positive than -4 V .
10. Reference source impedance must be less than 10 k .

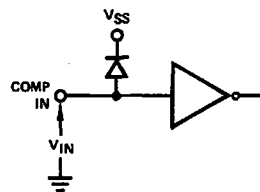
INPUT/OUTPUT SCHEMATICS



LD122 Input

LD121 Output Buffers
(Digits, Bits, Sign, M/Z U/D)LD121A Clock Input
Start Convert

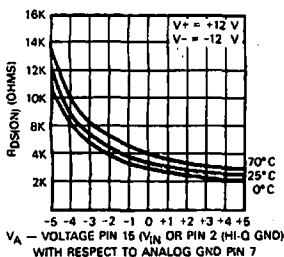
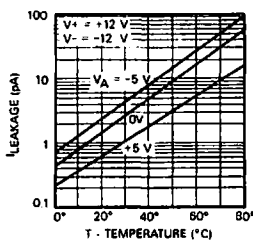
LD122 Comparator Output



LD121A Comparator Input

TYPICAL CHARACTERISTICS

V_{IN} AND V_{HI-Q} GND Switches
Typical $r_{DS(on)}$ vs V_A And Temp

Typical Input Leakage vs Temp And V_A 

Input Leakage Test Set-Up

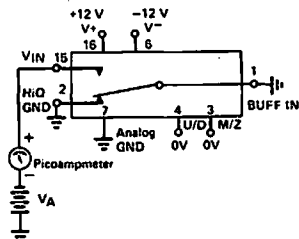
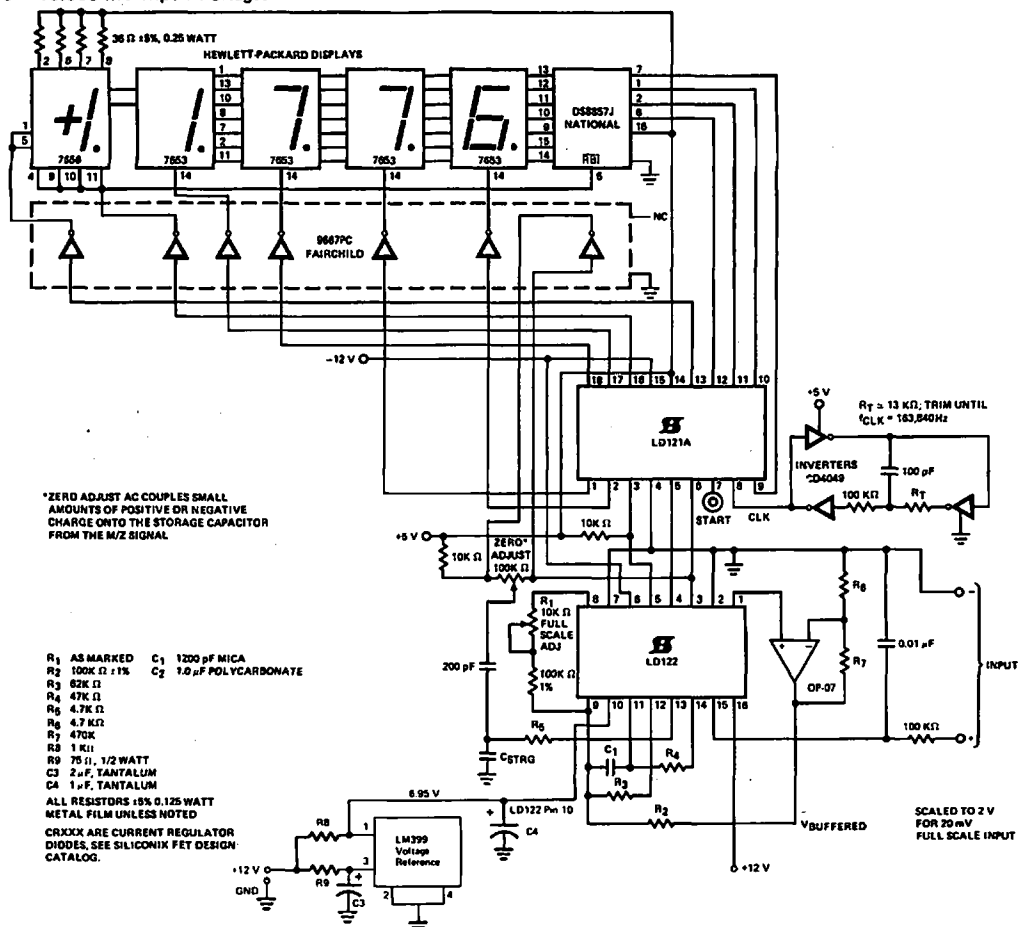


Figure 1 shows the arrangement for a 20 mV full scale, 1 μ V resolution DVM. The OP-07 provides the necessary low noise operation to achieve stable 1 μ V readouts. Proper layout is necessary for the LD122 and OP-07 front end circuitry to reduce stray RF and hum pickup. Having the OP-

07 included in the Auto-zero loop cancels front end amplifier bias-offsets, and more important drift with temperature. Reference drift is reduced by using an LM399 precision voltage reference with built in heater.

4½ DIGIT DVM CIRCUIT BENEFITS

- 1 μ V Resolution
- Overrange Blinking
- 0 $\rightarrow$ 19.999 mV Input Voltages
- Zero Adjust to Null Offset Introduced by PC Board Leakages and Comparator



Si7135

Precision 4 1/2 Digit

Single Chip CMOS A/D Converter



FEATURES

- Accuracy ± 1 Count over $\pm 20,000$ Counts
- 1 pA Input Current
- Auto Zero
- Differential Input
- 15 mW Power Consumption

BENEFITS

- Minimum External Components
- No External Zero Adjust
- Battery Operation

APPLICATIONS

- Precision DMM and DPM's
- Electronic Weighing
- Temperature Measuring Instruments

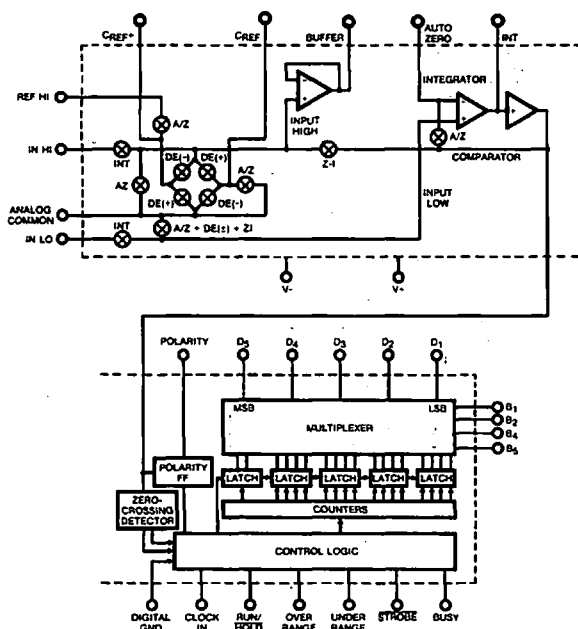
DESCRIPTION

The Si7135 is a precision 4 1/2 digit A/D converter system for use in display and microprocessor based data acquisition applications. Based on the reliable dual slope conversion technique, intrinsic features include 20,000 V full scale range, differential inputs, auto-polarity, auto-zero, and ratiometric operation to achieve a high level of versatility for the systems designer. The multiplexed BCD outputs, when connected to display drivers, make the Si7135 an ideal solution for visual display DVM/DPM applications.

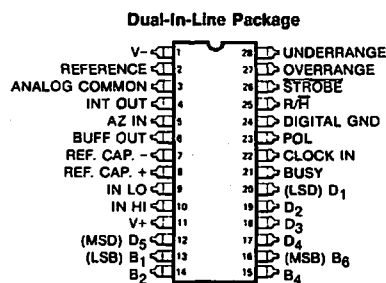
Manufactured on the Siliconix polysilicon gate CMOS process, Si7135 control functions include STROBE, OVER-RANGE, UNDER-RANGE, RUN/HOLD and BUSY.

Package options are the 28-pin plastic and ceramic DIP, and are rated for performance over the 0 to 70°C temperature range.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



Order Numbers:

Si7135CK

See Package 24

Si7135CJ

See Package 14

ABSOLUTE MAXIMUM RATINGS

Supply Voltage

V+	6 V
V-	-9 V
Analog Input Voltage (either input) ¹	V+ to V-
Reference Input Voltage (either input)	V+ to V-
Clock Input	GND to V+

Power Dissipation²

Ceramic Package	1000 mW
Plastic Package	800 mW
Operating Temperature	0 to 70°C
Storage Temperature	-65 to 125°C
Lead Temperature (Soldering, 10s)	300°C

ELECTRICAL CHARACTERISTICS³T_A = 25°C

	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: V+ = 5 V, V- = -5 V, f _{clock} = 120 kHz Full Scale = 2,0000 V	LIMITS			UNIT
				MIN ⁴	TYP ⁵	MAX	
ANALOG	Analog Input Range	V _{INPUT}		-2		2	V
	Zero Input Reading		See Figure 1 V _{in} = 0 V	-0.0000	±0.0000	0.0000	Digital Reading
	Ratiometric Reading		See Figure 1 V _{in} = V _{REF}	0.9998	0.9999	1.0000	
	Linearity Over ± Full Scale ⁶		See Figure 1 -2 V ≤ V _{in} ≤ 2 V		0.5	1	Digital Count Error
	Differential Linearity ⁷				±0.01		LSB
	Rollover Error ⁸		-2 V ≤ V _{in} ≤ 2 V		1.0	1.5	Digital Count Error
	Input Leakage Current	I _{ILK}	V _{in} = 0 V		1	10	pA
DIGITAL	Noise ⁹	E _N	See Figure 1, V _{in} = 0 V		15		μV
	Input High Voltage	V _{INH}	See Figure 2 CLOCK IN, RUN/HOLD	2.8	2.2		V
	Input Low Voltage	V _{INL}			1.6	0.8	
	Input Current With Input Voltage High	I _{INH}		V _{in} = 5 V	0.02	0.1	mA
	Input Current With Input Voltage Low	I _{INL}		V _{in} = 0 V	0.1	10	μA
	Output Voltage Low	V _{OL}	B ₁ , B ₂ , B ₃ , B ₄ , D ₁ , D ₂ , D ₃ , D ₄ , D ₅	I _{OL} = 1.6 mA	0.25	0.40	V
	Output Voltage High	V _{OH}	BUSY, STROBE, POLARITY, UNDERRANGE, OVERRANGE	I _{OH} = -1 mA	2.4	4.2	
				I _{OH} = -10 μA	4.9	4.99	
	+5 V Supply Range	V+		+4	+5	+6	mA
	-5 V Supply Range	V-			-5		
SUPPLY	+5 V Supply Range	I+	f _{clock} = 0		1.1	3.0	
	-5 V Supply Range	I-			0.8	3.0	
DYN	Power Dissipation Capacitance	C _{PD}	vs. Clock Frequency		40		pF
	Clock Frequency ¹¹			DC	120	200	kHz

NOTES:

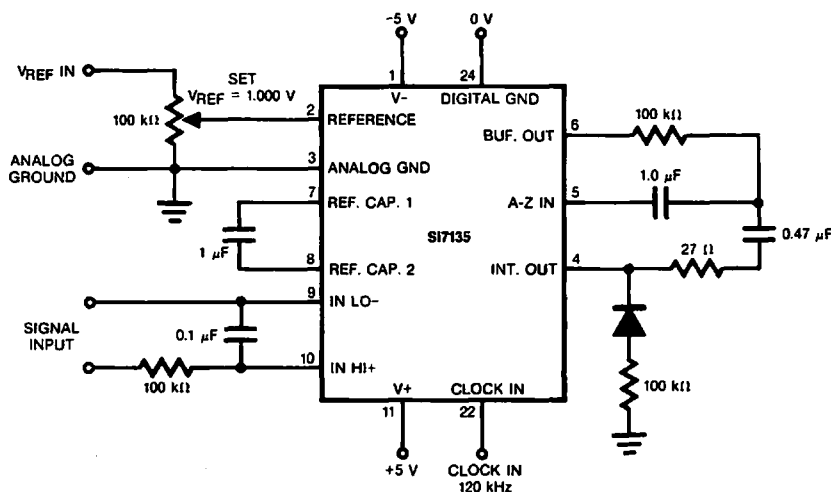
- Input voltages may exceed the supply voltages provided the input current is limited to 100 μA.
- Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.
- Refer to PROCESS OPTION FLOWCHART for additional information.
- The algebraic convention whereby the most negative value is a minimum, and the most positive value is a maximum, is used in this data sheet.
- Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- Error of reading from best straight line.
- Difference between worst case step of adjacent counts and ideal step.
- Difference in reading for equal positive and negative readings near full scale.
- Peak-to-peak value not exceeding 95% of the time.
- The temperature range can be extended beyond 70°C as long as the auto-zero and reference capacitors are increased to absorb the higher leakage of the Si7135.
- This specification relates to the clock frequency range over which the Si7135 will correctly perform its various functions. See the MAXIMUM CLOCK FREQUENCY section of the description for limitations on the clock frequency range in a system.

PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: V+ = 5 V, V- = -5 V, f _{clock} = 120 kHz Full Scale = 2.0000 V	LIMITS			UNIT
			MIN ⁴	TYP ⁵	MAX	
Zero Reading Drift		V _{in} = 0 V			2	μV/°C
Scale Factor Temperature Coefficient ¹⁰	TC	V _{in} = 2 V			5	ppm/°C

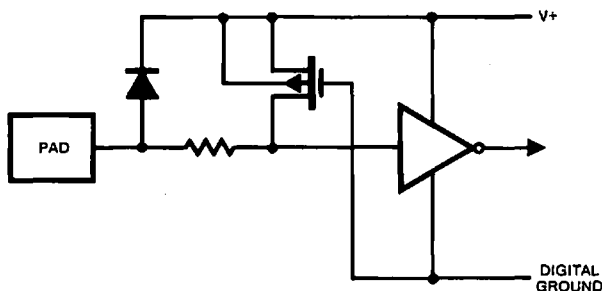
NOTES:

1. Input voltages may exceed the supply voltages provided the input current is limited to 100 μ A.
2. Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.
3. Refer to PROCESS OPTION FLOWCHART for additional information.
4. The algebraic convention whereby the most negative value is a minimum, and the most positive value is a maximum, is used in this data sheet.
5. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
6. Error of reading from best straight line.
7. Difference between worst case step of adjacent counts and ideal step.
8. Difference in reading for equal positive and negative readings near full scale.
9. Peak-to-peak value not exceeding 95% of the time.
10. The temperature range can be extended beyond 70°C as long as the auto-zero and reference capacitors are increased to absorb the higher leakage of the Si7135.
11. This specification relates to the clock frequency range over which the Si7135 will correctly perform its various functions. See the MAXIMUM CLOCK FREQUENCY section of the description for limitations on the clock frequency range in a system.

TEST CIRCUITS



SI7135 Test Circuit Figure 1



Logic Input Circuit
Figure 2

DETAILED DESCRIPTION

ANALOG SECTION

Figure 3 shows the Block Diagram of the Analog Section for the Si7135. Each measurement cycle is divided into four phases. They are (1) auto-zero (A-Z), (2) signal integrate (SI), (3) reference integrate (RI) and (4) zero integrator (ZI).

1. **AUTO-ZERO (A-Z) PHASE:** First, input high and low are disconnected from the pins and internally shorted to analog COMMON. Second, the reference capacitor is charged to the reference voltage. Third, a feedback loop is closed around the system to charge the auto-zero capacitor C_{AZ} to compensate for offset voltages in the buffer amplifier, integrator, and comparator. Since the comparator is included in the loop, the A-Z accuracy is limited only by the noise of the system. In any case, the offset referred to the input is less than $10\mu\text{V}$.
2. **SINGLE INTEGRATE (SI) PHASE:** During this phase, the auto-zero loop is opened, the internal short is removed, and the internal input high and low are connected to the external pins. The converter then integrates the differential voltage between IN HI and IN LO for a fixed time. This differential voltage can be within a wide common mode range within one volt of either supply. If the input signal has no return with respect to the converter power supply, IN LO can be tied to analog COMMON to establish the correct common-mode voltage. At the end of this phase, the polarity of the integrated signal is latched into the polarity F-F.
3. **REFERENCE INTEGRATE (RI) PHASE:** IN LO is internally connected to analog COMMON and IN HI is connected across the previously charged reference capacitor. Circuitry within the chip ensures that the capacitor will be connected with the correct polarity to cause the integrator output to return to zero. The time required for the output to return to zero is proportional to the input signal. Specifically the digital reading displayed is

$$10,000 \frac{V_{IN}}{V_{REF}}$$

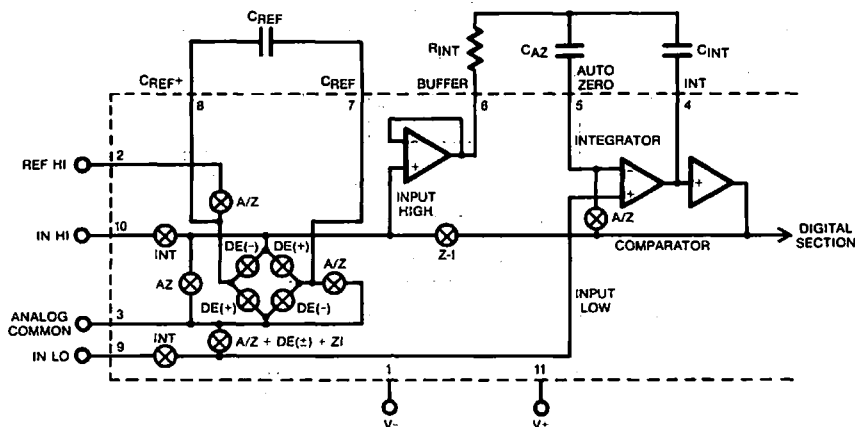
4. **ZERO INTEGRATOR (ZI) PHASE:** First, IN LOW is shorted to analog COMMON. Second, a feedback loop is closed around the system to IN HI to cause the integrator output to return to zero. Under normal condition, this phase lasts from 100 to 200 clock pulses, but after an overrange conversion, it is extended to 6200 clock pulses.

DIFFERENTIAL INPUT

The input can accept differential voltages anywhere within the common mode range of the input amplifier; or specifically from 0.5 volts below the positive supply to 1.0 volts above the negative supply. In this range the system has a typical CMRR of 86 dB. However, since the integrator also swings with the common mode voltage, care must be exercised to assure the integrator output does not saturate. A worst case condition would be a large positive common mode voltage with a near full scale negative differential input voltage. The negative input signal drives the integrator positive when most of its swing has been used up by the positive common mode voltage. For these critical applications the integrator swing can be reduced to less than the recommended 4 V full scale swing with some loss of accuracy. The integrator output can swing within 0.3 volts of either supply without loss of linearity.

ANALOG COMMON

Analog COMMON is used as the input low return during auto-zero and reference integrate. If IN LO is different from analog COMMON, a common mode voltage exists in the system and is taken care of by the excellent CMRR of the converter. However, in most applications IN LO will be set at a fixed known voltage (power supply common for instance). In this application, analog COMMON should be tied to the same point, thus removing the common mode voltage from the converter. The reference voltage is referenced to analog COMMON.



Analog Section of the Si7135
Figure 3

The reference input must be generated as a positive voltage with respect to COMMON, as shown in Figure 4.

Figure 5 shows the digital section of the Si7135. The Si7135 includes several pins which allow it to operate conveniently in more sophisticated systems. These include:

- 1. RUN/HOLD (R/H) (Pin 25):** When high (or open) the A/D converter (ADC) will free-run with equally spaced measurement cycles every 40,002 clock pulses. If taken low, the ADC will continue the full measurement cycle that it is doing and then hold this reading as long as R/H is held low. A short positive pulse (greater than 300 ns) will now initiate a new measurement cycle, beginning with between 1 and 10,001 counts of auto-zero. If the pulse occurs before the full measurement cycle (40,002 counts) is completed, it will not be recognized and the converter will simply complete the measurement it is doing. An external indication that a full measurement cycle has been completed is that the first strobe pulse

2. STROBE (Pin 26): This is a negative going output pulse that aids in transferring the BCD data to external latches for UARTs or microprocessors. There are 5 negative going STROBE pulses that occur in the center of each of the digit drive pulses and occur once and only once for each measurement cycle starting 101 pulses after the end of the full measurement cycle. Digit 5 (MSD) goes high at the end of the measurement cycle and stays on for 201 counts. In the center of this digit pulse (to avoid race conditions between changing BCD and digit drives) the first STROBE pulse goes negative for 1/2 clock pulse width. Similarly, after digit 5, digit 4 goes high (for 200 clock pulses) and 100 pulses later the STROBE pulse is sent. The digit drive will continue to scan (unless the previous signal was overrange) but no additional STROBE pulses will be sent until a new measurement is available.



DETAILED DESCRIPTION (Cont.)

DIGITAL SECTION (Cont.)

3. **BUSY (Pin 21):** BUSY goes high at the beginning of signal integrate and stays high until the first clock pulse after zero-crossing (or after end of measurement in the case of an overrange). The internal latches are enabled (i.e., loaded) during the first clock pulse after busy and are latched at the end of this clock pulse. The circuit automatically reverts to auto-zero when not BUSY, so it may also be considered a $(\overline{ZT} + \overline{AZ})$ signal. A very simple means for transmitting the data down a single wire pair from a remote location would be to AND BUSY with clock and subtract 10,001 counts from the number of pulses received — as mentioned previously there is one "NO-count" pulse in each reference integrate cycle.
4. **OVER-RANGE (Pin 27):** This pin goes positive when the input signal exceeds the range (20,000) of the converter. The output F-F is set at the end of BUSY and is reset to zero at the beginning of Reference integrate in the next measurement cycle.
5. **UNDER-RANGE (Pin 28):** This pin goes positive when the reading is 9% of range or less. The output F-F is set at the end of BUSY (if the new reading is 1800 or less) and is reset at the beginning of signal integrate of the next reading.
6. **POLARITY (POL) (Pin 23):** This pin is positive for a positive input signal. It is valid even for a zero reading. In other words, +0000 means the signal is positive but less than the least significant bit. The converter can be used as a null detector by forcing equal frequency of (+) and (-) readings. The null at this point should be less than 0.1 LSB. This output becomes valid at the beginning of reference integrate and remains correct until it is revalidated for the next measurement.
7. **DIGIT DRIVES (Pins 12, 17, 18, 19 and 20):** Each digit drive is a positive going signal that lasts for 200 clock pulses. The scan sequence is D₅ (MSD), D₄, D₃, D₂ and D₁ (LSD). All five digits are scanned and this scan is continuous unless an overrange occurs. Then all digit drives are blanked from the end of the strobe sequence until the beginning of Reference integrate when D₅ will start the scan again. This can give a blinking display as a visual indication of overrange.
8. **BCD (Pins 13, 14, 15 and 16):** The binary coded decimal bits B₈, B₄, B₂ and B₁ are positive logic signals that go on simultaneously with the digit driver signal.

COMPONENT VALUE SELECTION

For optimum performance of the analog section, care must be taken in the selection of values for the integrator capacitor and resistor, auto-zero capacitor, reference voltage, and conversion rate.

INTEGRATING RESISTOR

The integrating resistor is determined by the full scale input voltage and the output current of the buffer used to charge the integrator capacitor. Both the buffer amplifier and the integrator have a class A output stage with 100 μ A of quiescent current. They can supply 20 μ A of drive current with negligible non-linearity. Values of 5 to 40 μ A give good results, with nominal of 20 μ A, and the exact value of integrating resistor may be chosen by:

$$R_{INT} = \frac{\text{full scale voltage}}{20 \mu A}$$

INTEGRATING CAPACITOR

The product of integrating resistor and capacitor should be selected to give the maximum voltage swing which ensures that the tolerance build-up will not saturate the integrator swing (approximately 0.3 volts from either supply.) For ± 5 V supplies and analog COMMON tied to supply ground, a ± 3.5 to ± 4 V full scale integrator swing is fine, and 0.47 μ F is nominal. In general, the value of C_{INT} is given by:

$$C_{INT} = \frac{(10,000) \times (\text{clock period}) \times I_{INT}}{\text{integrator output voltage swing}} =$$

$$C_{INT} = \frac{(10,000) \times (\text{clock period}) \times (20 \mu A)}{\text{integrator output voltage swing}}$$

A very important characteristic of the integrating capacitor is that it has low dielectric absorption to prevent roll-over or ratiometric errors. A good test for dielectric absorption is to use the capacitor with the input tied to the reference.

This ratiometric condition should read half scale 0.9999, and any deviation is probably due to dielectric absorption. Polypropylene capacitors give undetectable errors at reasonable cost. Polystyrene and polycarbonate capacitors may also be used in less critical applications.

AUTO-ZERO AND REFERENCE CAPACITOR

The size of the auto-zero capacitor has some influence on the noise of the system, e.g. a large capacitor reduces noise. The reference capacitor should be large enough such that stray capacitance to ground from its nodes is negligible.

The dielectric absorption of the reference and auto-zero capacitors are only important at power-on or when the circuit is recovering from an overload. Thus, smaller or cheaper capacitors can be used here if accurate readings are not required for the first few seconds of recovery.

REFERENCE VOLTAGE

The analog input voltage (V_{IN}) required to generate a full-scale output is: V_{IN} = 2 V_{REF}.

The stability of the reference voltage is a major factor in the overall absolute accuracy of the converter. For this reason, it is recommended that a high quality reference be used where high-accuracy absolute measurements are being made.

COMPONENT VALUE SELECTION (Cont.)

MAXIMUM CLOCK FREQUENCY

The maximum conversion rate of most dual-slope A/D converters is limited by the frequency response of the comparator. The comparator in this circuit follows the integrator ramp with a 3 μ s delay, and at a clock frequency of 160 kHz (6 μ s period) half of the first reference integrate clock period is lost in delay. This means that the meter reading will change for 0 to 1 with a 50 μ V input, 1 to 2 with 150 μ V, 2 to 3 at 250 μ V, etc. This transition at mid-point is considered desirable by most users; however, if the clock frequency is increased appreciably above 160 kHz, the instrument will flash "1" on noise peaks even when the input is shorted.

For many dedicated applications where the input signal is always of one polarity, the delay of the comparator need not be a limitation. Since the non-linearity and noise do not increase substantially with frequency, clock rates of up to 1 MHz may be used. For a fixed clock frequency, the extra count or counts caused by comparator delay will be a constant and can be subtracted out digitally.

The clock frequency may be extended above 160 kHz without this error, however, by using a low value resistor in series with the integrating capacitor. The effect of the resistor is to introduce a small pedestal voltage on to the integrator output at the beginning of the reference integrate phase. By careful selection of the ratio between this resistor and the integrating resistor (a few tens of ohms in the recommended circuit), the comparator delay can be compensated and the maximum clock frequency extended by approximately a factor of 3. At higher frequencies, ringing and second order breaks will cause significant non-linearities in the first few counts of the instrument.

The minimum clock frequency is established by leakage on the auto-zero and reference capacitors. With most devices, measurement cycles as long as 10 seconds give no measurable leakage error.

To achieve maximum rejection of 60 Hz pickup, the signal integrate cycle should be a multiple of 60 Hz. Oscillator frequencies of 300 kHz, 200 kHz, 150 kHz, 120 kHz, 100 kHz, 40 kHz, 33 1/3 kHz, etc. should be selected. For 50 Hz rejection, oscillator frequencies of 250 kHz, 166 2/3 kHz, 125 kHz, 100 kHz, etc. would be suitable. Note that 100 kHz (2.5 readings/seconds) will reject both 50 and 60 Hz.

The clock used should be free from significant phase or frequency jitter. Several suitable low-cost oscillators are shown in the Applications section. If the multiplexed output display takes significant current from the logic supply, the clock should have good PSRR.

ZERO-CROSSING FLIP-FLOP

This flip-flop interrogates the data once every clock pulse after the transients of the previous clock pulse and half-

clock pulse have decayed. False zero-crossings caused by clock pulses are not recognized. The flip-flop delays the true zero-crossing by up to one count in every instance, and if a correction were not made, the display would always be one count too high. Therefore, the counter is disabled for one clock pulse at the beginning of phase 3. This one-count delay compensates for the delay of the zero-crossing flip-flop, and allows the correct number to be latched into the display. Similarly, a one-count delay at the beginning of phase 1 gives an overload display of 0000 instead of 0001. No delay occurs during phase 2, so that true ratiometric readings result.

EVALUATING THE ERROR SOURCES

Errors from the "ideal" cycle are caused by:

1. Capacitor voltage droop due to leakage.
2. Capacitor voltage change due to charge "drain-off" (the reverse of charge injection) when the switches turn off.
3. Non-linearity of buffer and integrator.
4. High-frequency limitations of buffer, integrator and comparator.
5. Integrating capacitor non-linearity (dielectric absorption.)
6. Charge lost by CREF in charging CSTRAY.
7. Charge lost by CAZ and CINT to charge CSTRAY.

NOISE

The peak-to-peak noise around zero is approximately 15 μ V (peak-to-peak value not exceeded 95% of the time.) Near full scale, this value increases to approximately 30 μ V. Much of the noise originates in the auto-zero loop, and is proportional to the ratio of the input signal to the reference.

ANALOG AND DIGITAL GROUNDS

Extreme care must be taken to avoid ground loops in the layout of Si7135 circuits, especially in high-sensitivity circuits. It is most important that return currents from digital loads are not fed into the analog ground line.

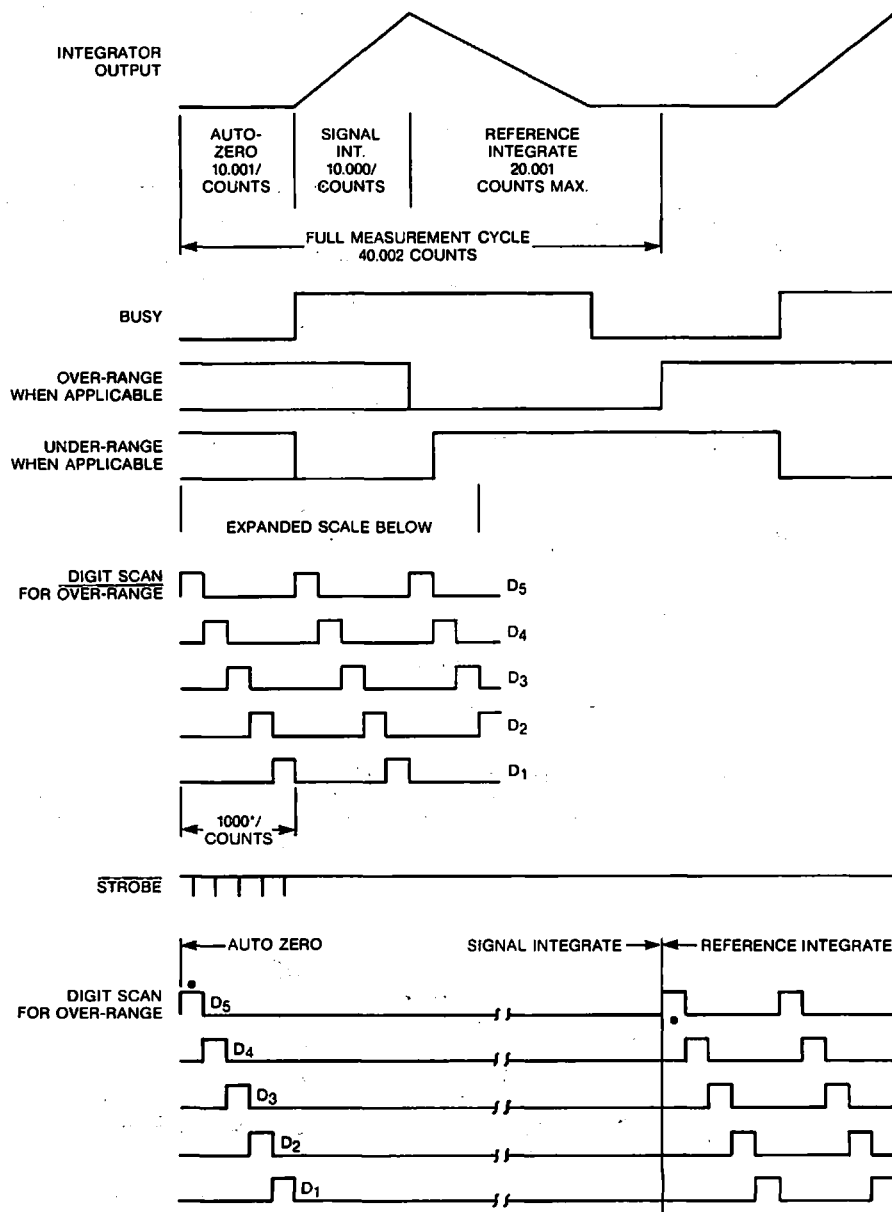
POWER SUPPLIES

The Si7135 is designed to work from ± 5 V supplies. However, in selected applications, no negative supply is required. The conditions to use a single +5 V supply are:

1. The input signal can be referenced to center of the common mode range of the converter.
2. The signal is less than ± 1.5 V.

See "DIFFERENTIAL INPUT" for a discussion of the effects this will have on the integrator swing without loss of linearity.

TIMING DIAGRAM



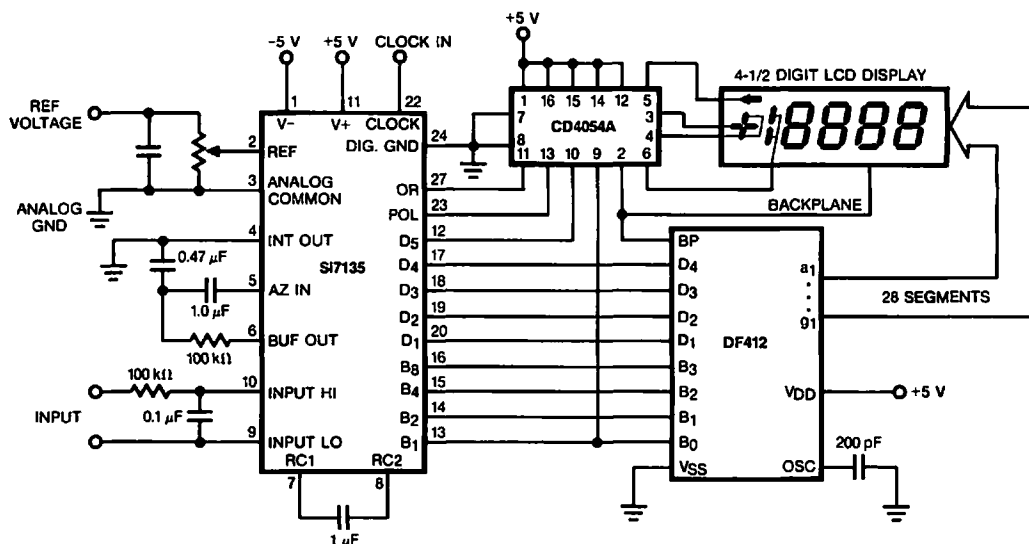
*FIRST D₅ OF AZ AND REF INT ONE COUNT LONGER

Timing Diagram
Figure 6

TYPICAL APPLICATIONS

The popular LCD displays can be interfaced to the output of the Si7135 with suitable display drivers, such as shown in Figure 7. A standard CMOS 4000 series LCD driver circuit is used for displaying the 1/2 digit, the polarity, and an 'overrange' flag. Of course, another full driver circuit

could be ganged to the one shown, if required. This would be useful if additional annunciators were needed. The Figure shows the complete circuit for a 4-1/2 digit (± 2.000 V) A/D.

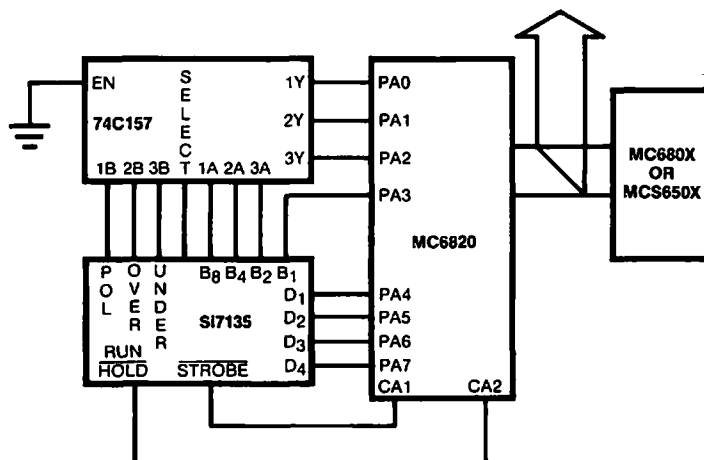


Si7135 Driving LCD Display
Figure 7

INTERFACING WITH MICROPROCESSORS

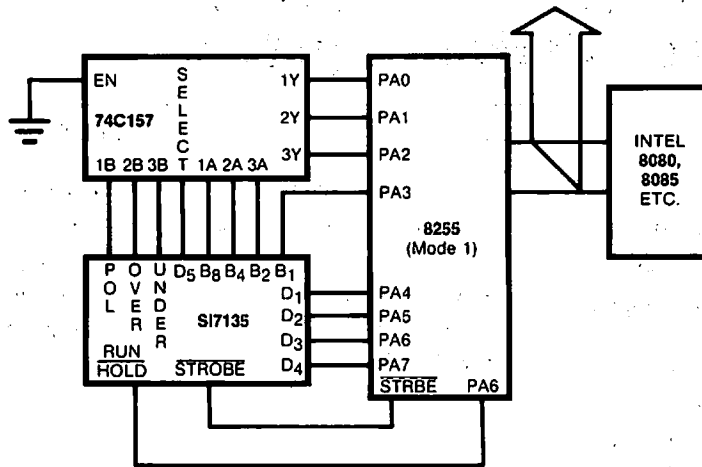
Circuits to interface the Si7135 directly with two popular microprocessors are shown in Figures 8 and 9. The 8080/8048 and the MC6800 families with 8-bit words need to have polarity, overrange and underrange multiplexed onto the digit 5 word. In each case the microprocessor can instruct the ADC when to begin a measurement and when to hold this measurement.

The Si7135 is designed to work from ± 5 volt supplies. However, if a negative supply is not available, it can be generated using 2 capacitors, and an inexpensive Si7660 or Si7661 I.C. (Figure 10).

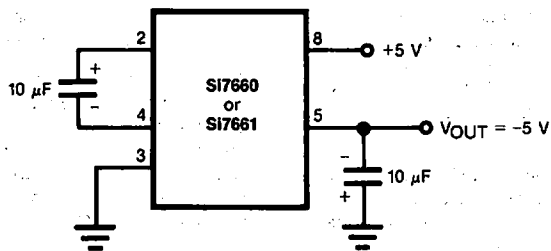


Interface to 680X and 650X Families
Figure 8

TYPICAL APPLICATIONS (Cont.)



Interface to 8080 Family
Figure 9



Generating a -5 V Supply From a +5 V Supply
Figure 10

Si520

8-Channel 8 Bit CMOS

Data Acquisition System



FEATURES

- 8-Bit Resolution $\pm \frac{1}{2}$ LSB
- 70 μ S Conversion Time
- No Missing Codes
- Latched Digital Inputs and Outputs
- 2.5 mW Power Consumption
- System Components Integrated in a Single Chip

BENEFITS

- Easily Interfaced to μ P
- Reduced Power Supply Requirements
- Accurate to 0.3% Over Temperature
- Better Reliability than Multi-Chip Designs

APPLICATIONS

- Data Acquisition Systems
- Portable Instruments
- Industrial Monitor and Control Systems
- Remote Data Collection

DESCRIPTION

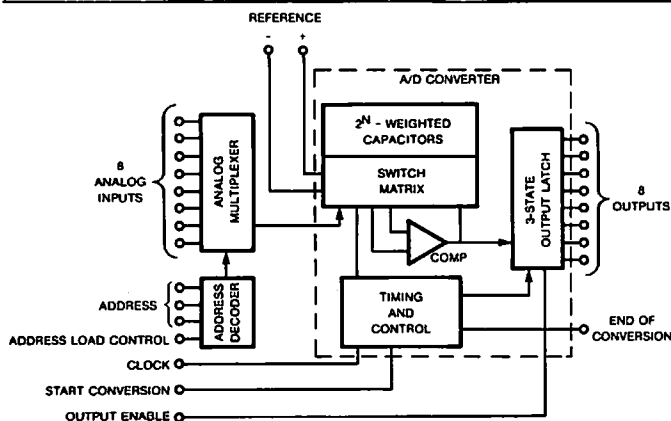
The Si520 is a CMOS Data Acquisition System combining an 8-channel multiplexer, a sample-hold function, an 8-bit A/D converter and microprocessor compatible control logic all on a single chip. Designed for use in general purpose data acquisition systems in process control, system diagnostics, or wherever multi-channel A/D conversions are required under the control of a microprocessor, Si520 offers an economical solution in general analog signal data collection applications.

The 8-channel multiplexer in Si520 can be controlled by a microprocessor using a 3-bit address to select any one of eight single-ended analog switches. The input signal is then 'sampled' and held stable then passed to the 8-bit A/D converter, which uses a binary weighted capacitor array in a successive-approximation algorithm to implement the conversion.

The design features of the Si520 make possible a pseudo-ratiometric conversion (i.e. the reference voltage can be selected to determine the analog input range), eliminate the need for zero or full scale adjustments for most applications, and insure 'no missing codes' performance.

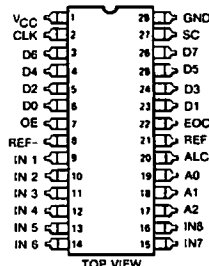
Also featured are latched 3-state outputs and latched address inputs to the multiplexer. Operation with a single 5 volt supply, low power requirements and moderately fast conversion time make Si520 especially useful for a wide range of industrial applications. Package options are the 28 pin plastic DIP and Cerdip. Both are specified over the -40°C to 85°C temperature range.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION

Dual-In-Line Package



Order Numbers

Si520DK
See Package 24
Si520DJ
See Package 14

ABSOLUTE MAXIMUM RATINGS

Reference Input Voltage Range, V_{ref}^{-1} -0.3 V to V_{ref}^{+}
 Reference Input Voltage Range, V_{ref}^{+} V_{ref}^{-} to $V_{CC} + 0.3$ V
 Supply Voltage, V_{CC}^{1} 6.5 V
 Input Voltage Range, All Inputs -0.3 V to $V_{CC} + 0.3$ V

Continuous Total Dissipation at or Below +55°C 1046 mW
 Operating Free Air Temperature Range -40 to +85°C
 Storage Temperature Range -65 to +150°C
 Lead Temperature 1/16 Inch (1.6 mm) from Case for 10 Sec. +260°C

ELECTRICAL CHARACTERISTICS³ $T_A = 25^{\circ}\text{C}$

	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: $V_{CC} = 4.75$ to 5.25 , $f_{clock} = 200$ kHz, $V_{ref}^{+} = V_{CC}$, $V_{ref}^{-} = 0$	LIMITS			UNIT
				MIN ⁴	TYP ⁵	MAX	
ANALOG MULTIPLEXER	Channel ON State Current ⁶	I_{on} (Peak)	$V_I = 2.5$ V $V_{CC} = 5$ V		-5		μA
	Channel OFF State Current ⁷	I_{Off}	$V_{CC} = 5$ V	$V_I = 5$ V		200	nA
				$V_I = 0$	-200		
DIGITAL	Analog Input Voltage ⁸	V_{ANALOG}		V_{ref}^{-}		V_{ref}^{+}	V
	High Level Input Voltage	V_{IH}	$V_{CC} = 5$ V	$V_{CC} - 1.5$			
	Low Level Input Voltage	V_{IL}	$V_{CC} = 5$ V			1.5	
	High Level Input Current	I_{IH}	$V_I = 5$ V			1	μA
	Low Level Input Current	I_{IL}	$V_I = 0$	-1			
	High Level Output Voltage	V_{OH}	$I_O = -360$ μA	4			V
	Low Level Output Voltage	V_{OL}	$I_O = 1.6$ mA	Data Outputs		0.4	
				End Of Conversion		0.4	
	OFF State Output Current	I_{OS}	$V_I = 5$ V			1	μA
			$V_I = 0$	-1			
SUPPLY	Supply Current ⁹	I_{CC}	V_{ref}^{+} & V_{ref}^{-} - Open, $V_{IL} = 0$ V, $V_{IH} = 5$ V		10	50	mA
	Supply Current Plus Reference Current ⁹	$I_{CC} + I_{ref}$	$V_{CC} = 5$ V, $V_{IL} = 0$ V, $V_{IH} = 5$ V			1	
	Supply Voltage ¹⁰	V_{CC}		3		5.5	
	Positive Reference Voltage ^{8, 10}	V_{ref}^{+}		3		V_{CC}	
	Negative Reference Voltage ⁸	V_{ref}^{-}		0		0.3	
	Voltage Between V_{CC} and V_{ref}^{+} Terminals ¹⁸	$V_{CC} - V_{ref}^{+}$		0		1	
DYNAMIC	Control Input Capacitance	C_i			2.5		pF
	Data Output Capacitance	C_O			5.5		
	Supply Voltage Sensitivity	k_{SVS}			0.05		
	Zero Error ¹¹		$f_{clock} = 372$ kHz		± 0.25		LSB
	Linearity Error ¹¹				± 0.25		
	Total Unadjusted Error ¹¹			-0.50	± 0.25	0.50	

NOTES

(See next page)

ELECTRICAL CHARACTERISTICS (Cont.)³ $T_A = 25^\circ\text{C}$ **Si520**

	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: $V_{CC} = 4.75$ to 5.25 , $f_{\text{clock}} = 200$ kHz, $V_{\text{ref}} + = V_{CC}$, $V_{\text{ref}} - = 0$	Si520DK/DJ			UNIT
				MIN ⁴	TYP ⁵	MAX	
TIMING	Clock Frequency ¹⁰	f_{clock}	$V_{CC} = 3$ V		100		kHz
			$V_{CC} = 5$ V			372	
	Start Pulse Width	t_{SC}		100			nS
	Address Load Control Pulse Width	t_{ALC}		200			
	Address Set Up Time	t_{SU}		50			
	Address Hold Time	t_H		50			
	Input Voltage Stable ¹⁰	t_{IS}		8			Clock Periods
	End Of Conversion Delay Time	t_{DEC}		0		200	nS
	Conversion Time ¹²	t_{CONV}	$f_{\text{clock}} = 372$ kHz, $t_{SC} = 100$ ns			70	μS
	Output Enable Time	t_{OE}	$C_L = 50$ pF		100	250	nS
	Output Disable Time	t_{OD}	$C_L = 10$ pF, $R_L = 10$ k Ω		100	250	

 $T_A = \text{Over Temperature Range}$

	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: $V_{CC} = 4.75$ to 5.25 , $f_{\text{clock}} = 200$ kHz, $V_{\text{ref}} + = V_{CC}$, $V_{\text{ref}} - = 0$	Si520DK/DJ			UNIT
				MIN ⁴	TYP ⁵	MAX	
ANALOG MULTIPLEXER	Channel ON State Current ⁹	$I_{on}(\text{Peak})$	$V_I = 2.5$ V $V_{CC} = 5$ V		-20		μA
	Channel OFF State Current ¹⁰	I_{Off}	$V_{CC} = 5$ V, $V_I = 5$ V			1	
			$V_I = 0$	-1			
DIGITAL	Analog Input Voltage ⁸	V_{ANALOG}		$V_{\text{ref}} -$		$V_{\text{ref}} +$	V
	High Level Input Voltage	V_{IH}	$V_{CC} = 5$ V	$V_{CC} - 1.5$			
	Low Level Input Voltage	V_{IL}				1.5	
	High Level Input Current	I_{IH}	$V_I = 5$ V			1	μA
	Low Level Input Current	I_{IL}	$V_I = 0$	-1			
	High Level Output Voltage	V_{OH}	$I_O = -360$ μA	4			V
	Low Level Output Voltage	V_{OL}	$I_O = 1.6$ mA	Data Outputs		0.4	
				End Of Conversion		0.4	
	OFF State Output Current	I_{OS}	$V_I = 5$ V			1	μA
			$V_I = 0$	-1			
SUPPLY	Supply Current ⁹	I_{CC}	$V_{\text{ref}} +$ & $V_{\text{ref}} -$ Open, $V_{IL} = 0$ V, $V_{IH} = 5$ V		10	50	mA
	Supply Current Plus Reference Current ⁹	$I_{CC} + I_{\text{ref}}$	$V_{CC} = 5$ V, $V_{IL} = 0$ V		0.5	1	
	Supply Voltage ¹⁰	V_{CC}		3		5.5	V
	Positive Reference Voltage ^{8, 10}	$V_{\text{ref}} +$		3		V_{CC}	
	Negative Reference Voltage ⁸	$V_{\text{ref}} -$		0		0.3	
	Voltage Between V_{CC} and $V_{\text{ref}} +$ Terminals ⁷	$V_{CC} - V_{\text{ref}} +$		0		1	

NOTES

(See next page)

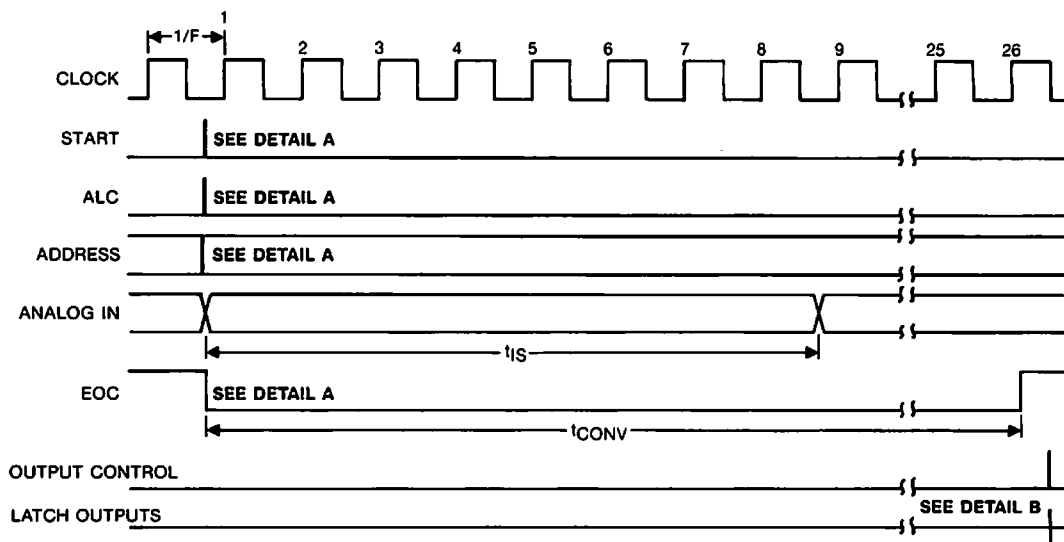
ELECTRICAL CHARACTERISTICS (Cont.)³ T_A = Over Temperature Range

	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: $V_{CC} = 4.75$ to 5.25 , $f_{clock} = 200$ kHz, $V_{ref} + V_{CC}$, $V_{ref} = 0$	Si520DK/DJ			UNIT
				MIN ⁴	TYP ⁵	MAX	
DYNAMIC	Control Input Capacitance	C_i			2.5		pF
	Data Output Capacitance	C_o			5.5		
	Supply Voltage Sensitivity	k _{svs}			0.05		%/V
	Zero Error ¹¹		$f_{clock} = 372$ kHz		±0.25		LSB
	Relative Accuracy Error ¹¹				±0.25		
	Total Unadjusted Error ¹¹			-0.75		0.75	
TIMING	Clock Frequency ¹⁰	f_{clock}	$V_{CC} = 5$ V			372	kHz
	Start Pulse Width	t_{SC}			130		nS
	Address Load Control Pulse Width	t_{ALC}			260		
	Address Set Up Time	t_{SU}			65		
	Address Hold Time	t_H			65		
	Input Voltage Stable ¹⁰	t_{IS}		8			Clock Periods
	End Of Conversion Delay Time	t_{DEC}			200		nS
	Conversion Time ¹²	t_{CONV}	$f_{clock} = 372$ kHz, $t_{SC} = 100$ ns			70	μS
	Output Enable Time	t_{OE}	$C_L = 50$ pF		130		nS
	Output Disable Time	t_{OD}	$C_L = 10$ pF, $R_L = 10$ kΩ		130		
	Operating Free Air Temperature	T_A		-40		85	°C

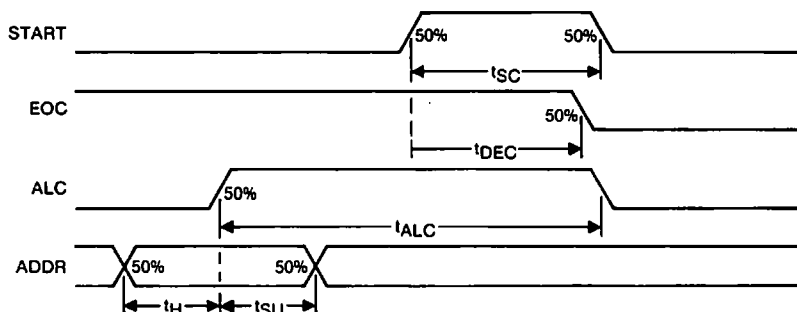
NOTES:

- All voltage values are with respect to ground terminal.
- For operation above 55°C free air temperature, derate from 1045 mW at 55°C to 716 mW at 85°C at the rate of 11.0 mW/°C.
- Refer to PROCESS OPTION FLOWCHART for additional information.
- The algebraic convention whereby the most negative value is a minimum, and the most positive value is a maximum, is used in this data sheet.
- Typical values are for DESIGN ONLY, not guaranteed nor subject to production testing.
- Decays exponentially during first clock high period.
- Channel addressed with clock off.
- Analog input voltage greater than $V_{ref} +$ converts as all ones and less than $V_{ref} -$ as all zeros.
- Current increases linearly with frequency of the clock at a rate of approximately 10% per 100 kHz.
- For proper operation the maximum clock rate must be lowered as the voltage across the reference terminals is lowered below 4.75 V. The maximum clock rate must be lowered by 0.68 f_{clock}/volt multiplication factor. $V_{ref} +$ must never be allowed to fall below 3.0 V or $V_{CC} - 1.0$ V, whichever is higher. Accuracy specifications degrade under these conditions.
- All errors are measured with reference to an ideal straight-line transfer curve from 9.8 mV to 4990 mV.
- Source resistance ≤ 1 kΩ.

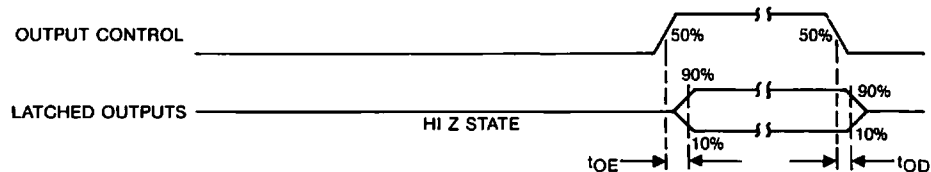
ELECTRICAL CHARACTERISTICS (Cont.)



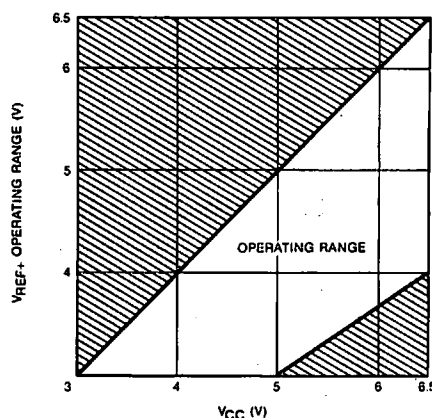
DETAIL A



DETAIL B

Timing Diagram
Figure 1

ELECTRICAL CHARACTERISTICS (Cont.)



Operating Range Of V_{REF+}
Figure 2

PIN OUT DESCRIPTION

Pin Number	Symbol	Description
1	V_{CC}	Input for the positive supply voltage.
2	CLK	Input for the CLOCK. The clock amplitude must conform to the V_{IH} and V_{IL} of the specifications and the rise time should be less than 10ns.
3-6	D_0, D_2, D_4, D_6	Digital DATA OUTPUTS. Bit 0 (Pin 6) is the LSB.
7	OE	Logic input for OUTPUT ENABLE. Connects the three-state output latches to the microprocessor BUS.
8	REF-	Input for the most negative voltage of the reference. It is normally grounded unless compressed mode operation is desired.
9-16	$IN_1 - IN_8$	ANALOG INPUTS of the 8-channel multiplexer (channel 1-Pin 9, channel 8-Pin 16).
17-19	$A_0 - A_2$	The three ADDRESS INPUTS that select the one-of-eight analog inputs to be converted.
20	ALC	ADDRESS LOAD CONTROL input that latches the input address into the multiplexer.
21	REF+	Input for the positive reference voltage. END OF CONVERSION output that goes high at the end of conversion.
22	EOC	END OF CONVERSION output that goes high at the end of conversion.
23-26	D_1, D_3, D_5, D_7	Digital DATA OUTPUTS. Bit 7 (Pin 26) is the MSB.
27	SC	START CONVERSION input that initiates the conversion process.
28	GND	Power supply and analog GROUND.

GENERAL PRECAUTIONS (For All Applications)

1. V_{REF+} must NEVER exceed V_{CC} by more than 50 mV.
2. V_{REF-} must NEVER be more negative than GND by more than 50 mV.
3. Under NO condition should the V_{REF+} be applied before V_{CC} (Prevents Latch-up).

PRINCIPLES OF OPERATION

The analog multiplexer selects 1 of 8 single-ended input channels as determined by the input address code. The address-load control transfers and latches the code into the decoder on the positive edge of the signal. The output latch is reset by the positive edge of the start pulse. Sampling starts with the positive edge of the start pulse and lasts for 8 clock periods from its falling edge. The conver-

sion process can be interrupted by a new start pulse before the end of 24 clock periods. Continuous conversion may be accomplished by connecting the end-of-conversion output to the start input. If used in this mode an external pulse should be applied after power up to assure start up.

MULTIPLEXER FUNCTION TABLE

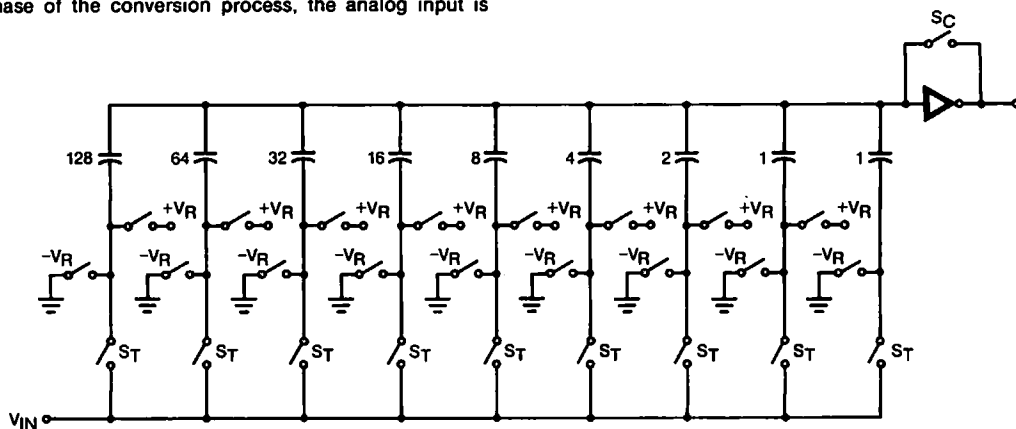
INPUTS				SELECTED ANALOG CHANNEL
ADDRESS			ADDRESS LOAD CONTROL*	
A ₂	A ₁	A ₀		
0	0	0	↑	1
0	0	1	↑	2
0	1	0	↑	3
0	1	1	↑	4
1	0	0	↑	5
1	0	1	↑	6
1	1	0	↑	7
1	1	1	↑	8

* ↑ = Low-to-High Transition

SWITCHED CAPACITOR A/D CONVERTER

The CMOS comparator in the successive-approximation system determines each bit by examining the charge on a series of binary-weighted capacitors (Figure 3). In the first phase of the conversion process, the analog input is

sampled by closing switch S_C and all S_T switches, and by simultaneously charging all the capacitors to the input voltage.



Simplified Successive Approximation A/D Converter
Figure 3

SWITCHED CAPACITOR A/D CONVERTER (Cont.)

In the next phase of the conversion process, all S_T and S_C switches are opened and the comparator begins identifying bits by identifying the charge on each capacitor relative to the reference voltage. In the switching sequence, all eight capacitors are examined separately until all 8 bits are identified, and then the charge-convert sequence is repeated. In the first step of the conversion phase, the comparator looks at the first capacitor (binary weight = 128). One pole of this capacitor is switched to the reference voltage, and the equivalent poles of all the other capacitors on the ladder are switched to ground. If the voltage at the summing node is greater than the trip-point of the comparator (approximately one-half the reference voltage), a bit is placed in the output register, and the 128-weight capacitor is switched to ground. If the voltage

at the summing node is less than the trip-point of the comparator, this 128-weight capacitor remains connected to the reference input through the remainder of the capacitor-sampling (bit-counting) process. The process is repeated for the 64-weight capacitor, the 32-weight capacitor, and so forth down the line, until all bits are tested.

As can be seen, with each step of the capacitor-sampling process, the initial charge is redistributed among the capacitors. The conversion process is successive-approximation, but relies on charge shifting rather than a successive-approximation register (and reference D/A) to count and weigh the bits from MSB to LSB.

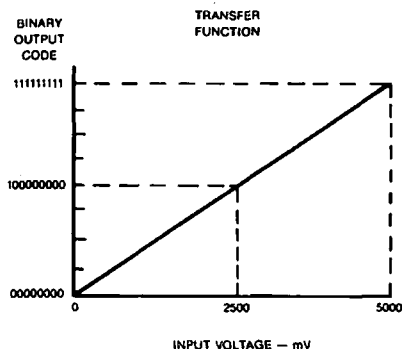
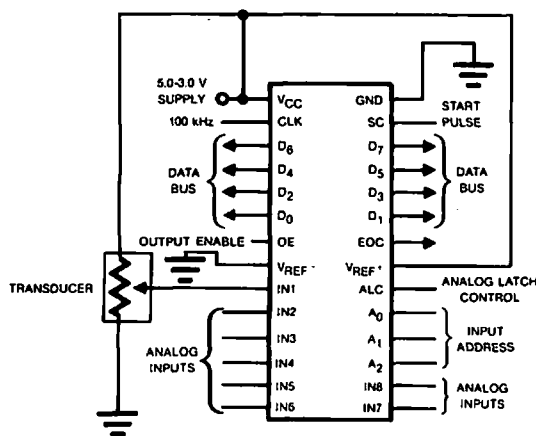
APPLICATIONS

The Si520 is a CMOS Data Acquisition System using charge redistribution to achieve A/D conversion. In typical applications, as a ratiometric conversion system for a microprocessor, V_{REF-} will be connected to ground and

V_{REF+} will be connected to V_{CC} . The output will then be a simple proportional ratio between analog input voltage and V_{CC} (Figure 4). The general relationship is:

$$\frac{DOUT}{2^8} = \frac{V_{IN}}{V_{REF+} - V_{REF-}}$$

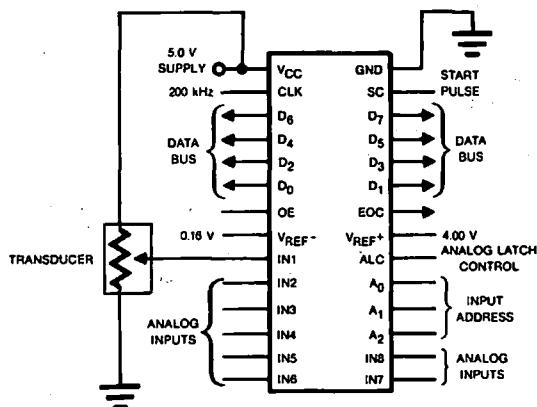
Where $DOUT$ = Digital Output
 V_{IN} = Analog Input
 V_{REF+} = Positive Reference Potential
 V_{REF-} = Negative Reference Potential



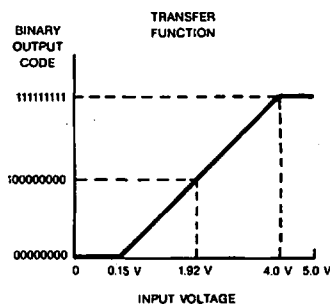
$V_{CC} = V_{REF+} = 5 \text{ V}$
 $GND = V_{REF-} = 0 \text{ V}$
 RESOLUTION = 19.5 mV

Ratiometric System
 Figure 4

APPLICATIONS (Cont.)



*Equivalent To 8.4-BIT Resolution over a 5-Volt range.



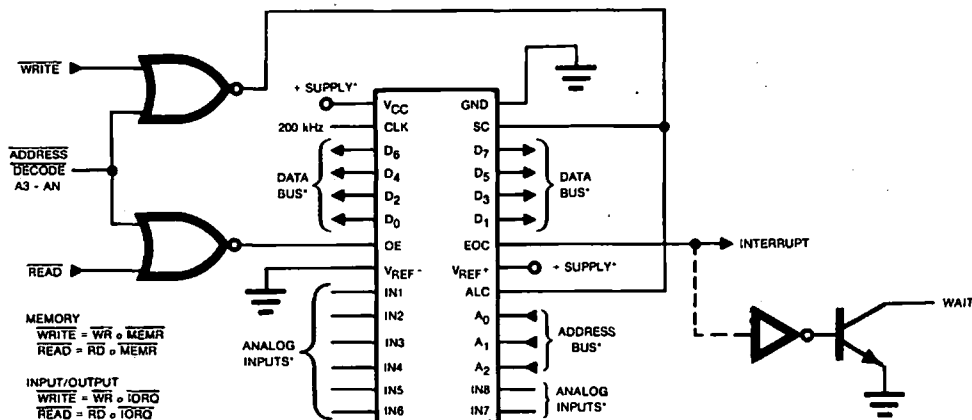
$V_{CC} = 5 \text{ V}$
 $V_{REF+} = 4.00 \text{ V}$
 $V_{REF-} = 0.16 \text{ V}$
 $GND = 0 \text{ V}$
 RESOLUTION = 15 mV*

NOTE: Input voltage below V_{REF-} converts as all zeros, input voltage above V_{REF+} converts as all ones.

Compressed System With TTL-Compatible I/O
 Figure 5

MICROPROCESSOR INTERFACE TABLE

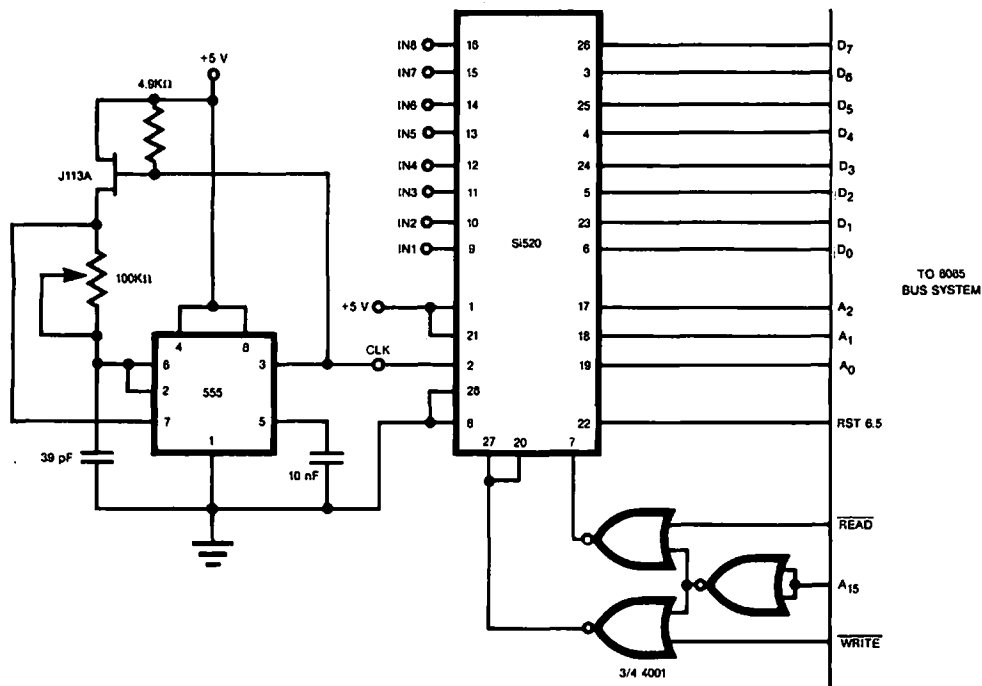
PROCESSOR	READ	WRITE	INTERRUPT (COMMENT)
8080	MEMR	MEMW	INTR (Thru RST Circuit)
8085	RD	WR	INTR (Thru RST Circuit)
Z-80	RD	WR	INT (Thru RST Circuit, Mode 0)
SC/MP	NRDS	NWDS	SA (Thru Sense A)
6800	VMA + 2 R/W	VMA + 2 R/W	IRQA Or IRQB (Thru PIA)



*NOTE: Range can be shifted between 3.0 V and 6.5 V by varying V_{REF-} and V_{CC} , but only 5 V allows TTL compatibility.

Typical Microprocessor Application
 Figure 6

map redundancy, a more sophisticated address decoding circuit would be needed. The NOR gates of the 4001 combine the address decoding READ, and WRITE signals to control the data acquisition system. The EOC pin is tied to RST 6.5 of the 8085 to notify the microprocessor when the conversion has been completed and when the data outputs are ready to be read.



Schematic Diagram of a Memory Mapped SI520 Interface
Figure 7

Si8601

8-Channel 8 Bit CMOS

Data Acquisition System



FEATURES

- 8-Bit Resolution $\pm \frac{1}{2}$ LSB
- 25 μ s Conversion Time
- No Missing Codes
- Latched Digital Inputs and Outputs
- 2.5 mW Power Consumption
- System Components Integrated in a Single Chip

BENEFITS

- Easily Interfaced to μ P
- Reduced Power Supply Requirements
- Accurate to 0.3% Over Temperature
- Better Reliability than Multi-Chip Designs

APPLICATIONS

- Data Acquisition Systems
- Portable Instruments
- Industrial Monitor and Control Systems
- Remote Data Collection

DESCRIPTION

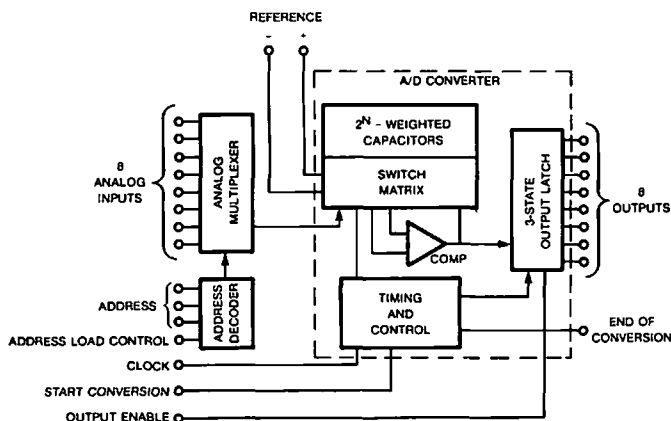
The Si8601 is a CMOS Data Acquisition System combining an 8-channel multiplexer, a sample-hold function, a 25 μ s 8-bit A/D converter and microprocessor compatible control logic, all on a single chip. Designed for use in general purpose data acquisition systems in process control, system diagnostics, or wherever multi-channel A/D conversions are required under the control of a microprocessor, Si8601 offers an economical solution to applications in general analog signal data collection.

The 8-channel multiplexer in Si8601 can be controlled by a microprocessor using a 3-bit address to select any one of eight single-ended analog switches. The input signal is then 'sampled' by a capacitor and passed to the high speed 8-bit A/D converter, which uses a binary weighted capacitor array in a successive-approximation algorithm to achieve a conversion in 25 μ s.

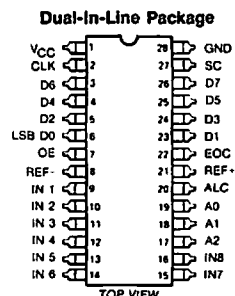
The design features of the Si8601 make possible a pseudo-ratiometric conversion (i.e. the reference voltage can be selected to determine the analog input range), eliminate the need for zero or full scale adjustments for most applications, and insure 'no missing codes' performance.

Also featured are latched 3-stated outputs and latched address inputs to the multiplexer. The single 5 volt supply, low power requirements and fast conversion time make Si8601 especially useful for a wide range of industrial applications. Package options are the 28 pin plastic or ceramic DIP which are specified over the -40 to 85°C temperature range.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



Order Numbers:
SI8601AK or **SI8601DK**
 See Package 24
SI8601DJ
 See Package 14

ABSOLUTE MAXIMUM RATINGS

Reference Input Voltage Range, V_{ref}^{-1} -0.3 V to V_{ref}^{+}
 Reference Input Voltage Range, V_{ref}^{+} V_{ref}^{-} to $V_{CC} + 0.3$ V
 Supply Voltage, V_{CC}^{1} 6.5 V
 Input Voltage Range, All Inputs -0.3 V to $V_{CC} + 0.3$ V

Continuous Total Dissipation at or Below 55°C² 1046 mW
 Operating Free Air Temperature Range
 (A Suffix) -55 to 125°C
 (D Suffix) -40 to 85°C
 Storage Temperature Range -65 to 150°C
 Lead Temperature 1/16 Inch (1.6 mm) from
 Case for 10 Sec 260°C

ELECTRICAL CHARACTERISTICS³ $T_A = 25^{\circ}\text{C}$

	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: $V_{CC} = 4.75$ to 5.25 , $f_{clock} = 200$ kHz, $V_{ref}^{+} = V_{CC}$, $V_{ref}^{-} = 0$	LIMITS			UNIT
				MIN ⁴	TYP ⁵	MAX	
ANALOG MULTIPLEXER	Analog Input Voltage ⁶	V_{ANALOG}		V_{ref}^{-}		V_{ref}^{+}	V
	Channel ON State Current ⁶	I_{ON} (Peak)	$V_I = 2.5$ V $V_{CC} = 5$ V		-5		μA
	Channel OFF State Current ⁷	I_{OFF}	$V_{CC} = 5$ V	$V_I = 5$ V		200	nA
				$V_I = 0$	-200		
DIGITAL	High Level Input Voltage	V_{IH}	$V_{CC} = 5$ V	$V_{CC} - 1.5$			V
	Low Level Input Voltage	V_{IL}	$V_{CC} = 5$ V			1.5	V
	High Level Input Current	I_{IH}	$V_I = 5$ V			1	μA
	Low Level Input Current	I_{IL}	$V_I = 0$	-1			μA
	High Level Output Voltage	V_{OH}	$I_O = -360$ μA	4			V
	Low Level Output Voltage	V_{OL}	$I_O = 1.6$ mA	Data Outputs		0.4	V
				End Of Conversion		0.4	
	OFF State Output Current	I_{OS}	$V_I = 5$ V $V_I = 0$	-1		1	μA
DYNAMIC	Control Input Capacitance	C_i			2.5		pF
	Data Output Capacitance	C_o			5.5		
	Supply Voltage Sensitivity	ksvs			0.05		%/V
	Zero Error ¹¹		$f_{clock} = 1.04$ MHz		± 0.25		LSB
	Linearity Error ¹¹				± 0.25		
	Total Unadjusted Error ¹¹			-0.50	± 0.25	0.50	
SUPPLY	Supply Current ⁹	I_{CC}	V_{ref}^{+} & V_{ref}^{-} Open, $V_{IL} = 0$ V, $V_{IH} = 5$ V	10		200	μA
	Supply Current Plus Reference Current ⁹	$I_{CC} + I_{ref}$	$V_{CC} = 5$ V, $V_{IL} = 0$ V, $V_{IH} = 5$ V			1	mA
	Supply Voltage ¹⁰	V_{CC}		3		5.5	V
	Positive Reference Voltage ^{8, 10}	V_{ref}^{+}		3		V_{CC}	
	Negative Reference Voltage ⁸	V_{ref}^{-}		0		0.3	
	Voltage Between V_{CC} and V_{ref}^{+} Terminals ¹⁰	$V_{CC} - V_{ref}^{+}$		0		1	

NOTES

(See next page)

ELECTRICAL CHARACTERISTICS³ (Cont.) $T_A = 25^\circ\text{C}$

	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: $V_{CC} = 4.75$ to 5.25 , $f_{clock} = 200$ kHz, $V_{ref+} = V_{CC}$, $V_{ref-} = 0$	LIMITS			UNIT
				MIN ⁴	TYP ⁵	MAX	
TIMING	Clock Frequency ¹⁰	f_{clock}	$V_{CC} = 3$ V $V_{CC} = 5$ V		100	1.04	MHz
	Start Pulse Width	t_{SC}		100			
	Address Load Control Pulse Width	t_{ALC}		200			ns
	Address Set Up Time	t_{SU}		50			
	Address Hold Time	t_H		50			
	Input Voltage Stable ¹⁰	t_{IS}		8			Clock Periods
	End Of Conversion Delay Time	t_{DEC}		0		200	ns
	Conversion Time ¹²	t_{CONV}	$f_{clock} = 1.04$ MHz, $t_{SC} = 100$ ns			25	μs
	Output Enable Time	t_{OE}	$C_L = 50$ pF		100	250	ns
	Output Disable Time	t_{OD}	$C_L = 10$ pF, $R_L = 10$ k Ω		100	250	

NOTES:

- All voltage values are with respect to ground terminal.
- For operation above 55°C free air temperature, derate from 1045 mW at 55°C to 716 mW at 85°C at the rate of 11.0 mW/ $^\circ\text{C}$.
- Refer to PROCESS OPTION FLOWCHART for additional information.
- The algebraic convention whereby the most negative value is a minimum, and the most positive value is a maximum, is used in this data sheet.
- Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- Decays exponentially during first clock high period.
- Channel addressed with clock off.
- Analog input voltage greater than V_{ref+} converts as all ones and less than V_{ref-} as all zeros.
- Current increases linearly with frequency of the clock at a rate of approximately 10% per 100 kHz.
- For proper operation the maximum clock rate must be lowered as the voltage across the reference terminals is lowered below 4.75 V. The maximum clock rate must be lowered by 0.68 f_{clock}/volt multiplication factor. V_{ref+} must never be allowed to fall below 3.0 V or $V_{CC} - 1.0$ V, whichever is higher. Accuracy specifications degrade under these conditions.
- All errors are measured with reference to an ideal straight-line transfer curve from 9.8 mV to 4990 mV.
- Source resistance ≤ 1 k Ω .

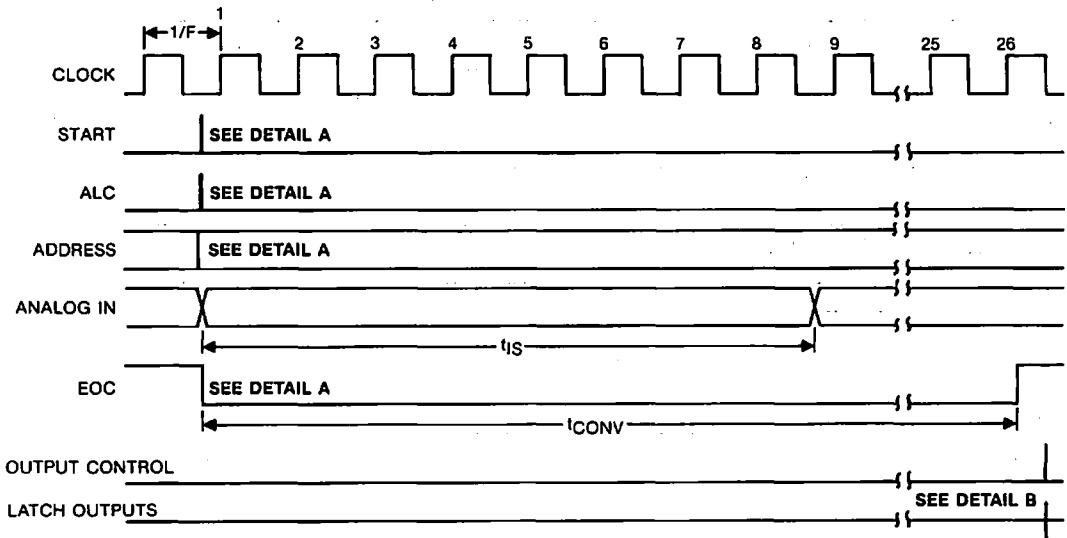
ELECTRICAL CHARACTERISTICS³ (Cont.) T_A = Over Temperature Range

	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: $V_{CC} = 4.75$ to 5.25 , $f_{clock} = 200$ kHz, $V_{ref+} = V_{CC}$, $V_{ref-} = 0$	LIMITS			UNIT
				MIN ⁴	TYP ⁵	MAX	
ANALOG MUX	Analog Input Voltage ⁸	V_{ANALOG}		V_{ref-}		V_{ref+}	V
	Channel OFF State Current ¹⁰	I_{OFF}	$V_{CC} = 5$ V	$V_I = 5$ V		1	μ A
				$V_I = 0$	-1		
DIGITAL	High Level Input Voltage	V_{IH}	$V_{CC} = 5$ V	$V_{CC} - 1.5$			V
	Low Level Input Voltage	V_{IL}				1.5	V
	High Level Input Current	I_{IH}	$V_I = 5$ V			1	μ A
	Low Level Input Current	I_{IL}	$V_I = 0$	-1			μ A
	High Level Output Voltage	V_{OH}	$I_O = -360$ μ A	4			V
	Low Level Output Voltage	V_{OL}	$I_O = 1.6$ mA	Data Outputs		0.4	V
				End Of Conversion		0.4	
	OFF State Output Current	I_{OS}	$V_I = 5$ V			1	μ A
DYNAMIC	Total Unadjusted Error ¹¹		$V_I = 0$	-1			
			$f_{clock} = 1.04$ MHz	-0.75		0.75	LSB
SUPPLY	Supply Current ⁹	I_{CC}	V_{ref+} & V_{ref-} Open, $V_{IL} = 0$ V, $V_{IH} = 5$ V			200	μ A
	Supply Current Plus Reference Current ⁹	$I_{CC} + I_{ref}$	$V_{CC} = 5$ V, $V_{IL} = 0$ V			1	mA
	Supply Voltage ¹⁰	V_{CC}		3		5.5	V
	Positive Reference Voltage ^{8, 10}	V_{ref+}		3		V_{CC}	
	Negative Reference Voltage ⁸	V_{ref-}		0		0.3	
	Voltage Between V_{CC} and V_{ref+} Terminals ⁷	$V_{CC} - V_{ref+}$		0		1	
TIMING	Clock Frequency ¹⁰	f_{clock}	$V_{CC} = 5$ V			1.04	MHz
	Input Voltage Stable ¹⁰	t_{IS}		8			Clock Periods
	Conversion Time ¹²	t_{CONV}	$f_{clock} = 372$ kHz, $t_{SC} = 100$ ns			70	μ s

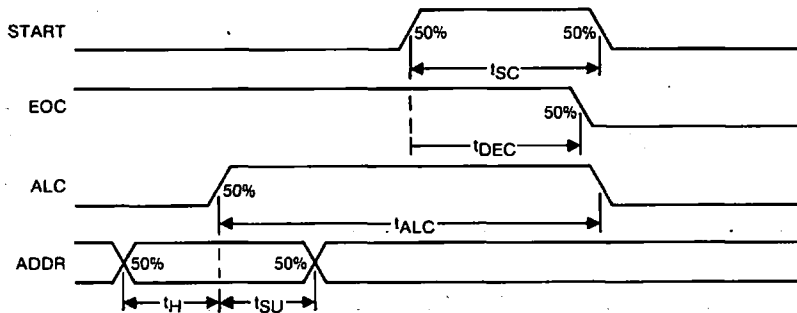
NOTES:

- All voltage values are with respect to ground terminal.
- For operation above 55°C free air temperature, derate from 1045 mW at 55°C to 716 mW at 85°C at the rate of 11.0 mW/°C.
- Refer to PROCESS OPTION FLOWCHART for additional information.
- The algebraic convention whereby the most negative value is a minimum, and the most positive value is a maximum, is used in this data sheet.
- Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- Decays exponentially during first clock high period.
- Channel addressed with clock off.
- Analog input voltage greater than V_{ref+} converts as all ones and less than V_{ref-} as all zeros.
- Current increases linearly with frequency of the clock at a rate of approximately 10% per 100 kHz.
- For proper operation the maximum clock rate must be lowered as the voltage across the reference terminals is lowered below 4.75 V. The maximum clock rate must be lowered by $0.68 f_{clock}/V_{OIT}$ multiplication factor. V_{ref+} must never be allowed to fall below 3.0 V or $V_{CC} - 1.0$ V, whichever is higher. Accuracy specifications degrade under these conditions.
- All errors are measured with reference to an ideal straight-line transfer curve from 9.8 mV to 4990 mV.
- Source resistance ≤ 1 k Ω .

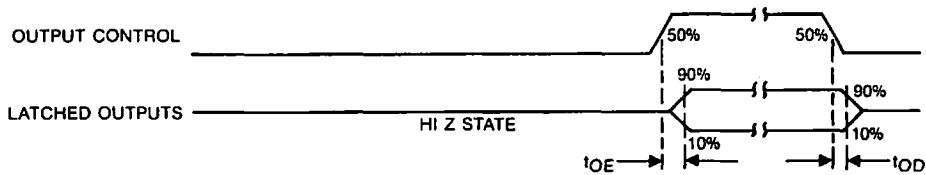
ELECTRICAL CHARACTERISTICS (Cont.)



DETAIL A



DETAIL B

Timing Diagram
Figure 1

ELECTRICAL CHARACTERISTICS (Cont.)

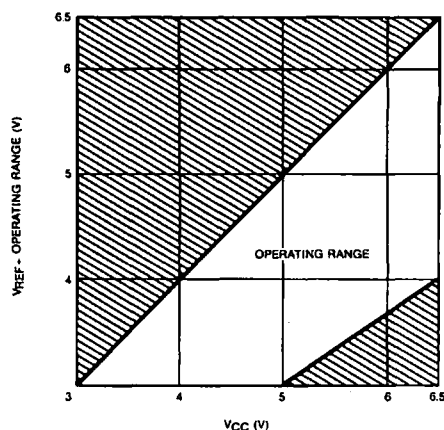
Operating Range Of V_{ref+}

Figure 2

PIN OUT DESCRIPTION

Pin Number	Symbol	Description
1	V_{CC}	Input for the positive supply voltage.
2	CLK	Input for the CLOCK. The clock amplitude must conform to the V_{IH} and V_{IL} of the specifications and the rise time should be less than 10ns.
3-6	D_0, D_2, D_4, D_6	Digital DATA OUTPUTS. Bit 0 (Pin 6) is the LSB.
7	OE	Logic input for OUTPUT ENABLE. Connects the three-state output latches to the microprocessor BUS.
8	REF-	Input for the most negative voltage of the reference. It is normally grounded unless compressed mode operation is desired.
9-16	IN_1 IN_8	ANALOG INPUTS of the 8-channel multiplexer (channel 1-Pin 9, channel 8-Pin 16).
17-19	$A_0 - A_2$	The three address inputs that select the one-of-eight analog inputs to be converted.
20	ALC	ADDRESS LOAD CONTROL input that latches the input address into the multiplexer.
21	REF+	Input for the positive reference voltage. END OF CONVERSION output that goes high at the end of conversion.
22	EOC	END OF CONVERSION output that goes high at the end of conversion.
23-26	D_1, D_3, D_5, D_7	Digital DATA OUTPUTS. Bit 7 (Pin 26) is the MSB.
27	SC	START CONVERSION input that initiates the conversion process.
28	GND	Power supply and analog GROUND.

GENERAL PRECAUTIONS (For All Applications)

1. V_{REF+} must NEVER exceed V_{CC} by more than 50 mV.
2. V_{REF-} must NEVER be more negative than GND by more than 50 mV.
3. Under NO condition should the V_{REF+} be applied before V_{CC} (Prevents Latch-up).

PRINCIPLES OF OPERATION

The analog multiplexer selects 1 of 8 single-ended input channels as determined by the input address code. The address-load control transfers and latches the code into the decoder on the positive edge of the signal. The output latch is reset by the positive edge of the start pulse. Sampling starts with the positive edge of the start pulse and lasts for 8 clock periods from its falling edge. The conver-

sion process can be interrupted by a new start pulse before the end of 24 clock periods. Continuous conversion may be accomplished by connecting the end-of-conversion output to the start input. If used in this mode an external pulse should be applied after power up to assure start up.

MULTIPLEXER FUNCTION TABLE

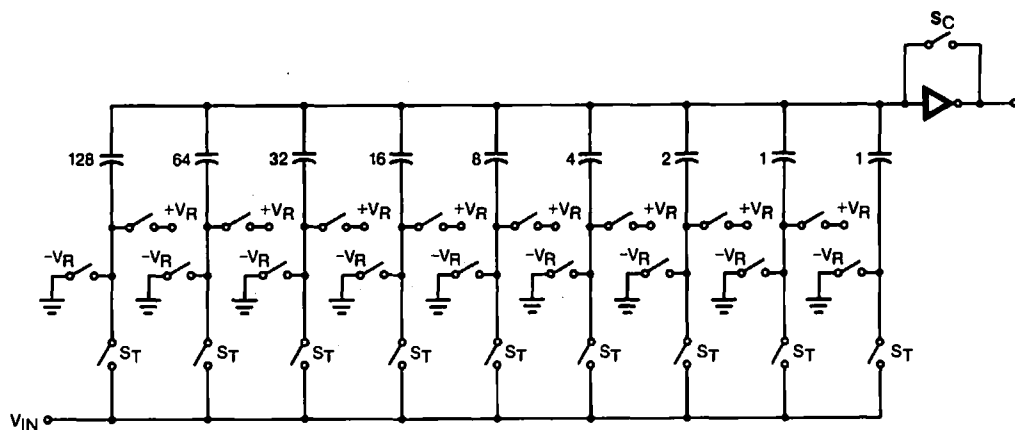
INPUTS				SELECTED ANALOG CHANNEL
ADDRESS			ADDRESS LOAD CONTROL*	
A ₂	A ₁	A ₀		
0	0	0	↑	1
0	0	1	↑	2
0	1	0	↑	3
0	1	1	↑	4
1	0	0	↑	5
1	0	1	↑	6
1	1	0	↑	7
1	1	1	↑	8

* ↑ = Low-to-High Transition

SWITCHED CAPACITOR A/D CONVERTER

The CMOS comparator in the successive-approximation system determines each bit by examining the charge on a series of binary-weighted capacitors (Figure 3). In the first phase of the conversion process, the analog input is

sampled by closing switch S_C and all S_T switches, and by simultaneously charging all the capacitors to the input voltage.



Simplified Successive Approximation A/D Converter
Figure 3

SWITCHED CAPACITOR A/D CONVERTER (Cont.)

In the next phase of the conversion process, all S_T and S_C switches are opened and the comparator begins identifying bits by identifying the charge on each capacitor relative to the reference voltage. In the switching sequence, all eight capacitors are examined separately until all 8 bits are identified, and then the charge-convert sequence is repeated. In the first step of the conversion phase, the comparator looks at the first capacitor (binary weight = 128). One pole of this capacitor is switched to the reference voltage, and the equivalent poles of all the other capacitors on the ladder are switched to ground. If the voltage at the summing node is greater than the trip-point of the comparator (approximately one-half the reference voltage), a bit is placed in the output register, and the 128-weight capacitor is switched to ground. If the voltage

at the summing node is less than the trip-point of the comparator, this 128-weight capacitor remains connected to the reference input through the remainder of the capacitor-sampling (bit-counting) process. The process is repeated for the 64-weight capacitor, the 32-weight capacitor, and so forth down the line, until all bits are tested.

As can be seen, with each step of the capacitor-sampling process, the initial charge is redistributed among the capacitors. The conversion process is successive-approximation, but relies on charge shifting rather than a successive-approximation register (and reference D/A) to count and weigh the bits from MSB to LSB.

APPLICATIONS

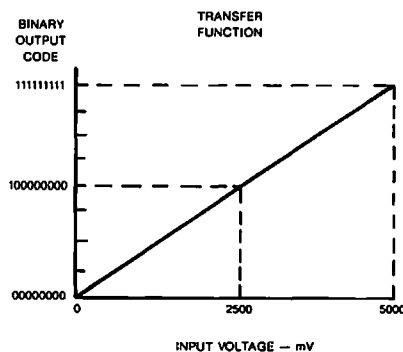
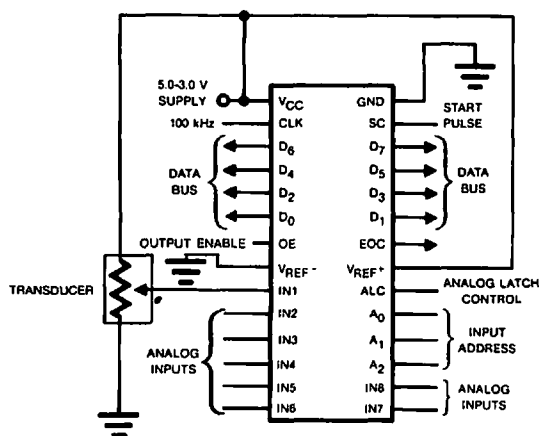
The Si8601 is a CMOS Data Acquisition System using charge redistribution to achieve A/D conversion. In typical applications, as a ratiometric conversion system for a microprocessor, V_{REF-} will be connected to ground and

V_{REF+} will be connected to V_{CC} . The output will then be a simple proportional ratio between analog input voltage and V_{CC} (Figure 4). The general relationship is:

$$\frac{D_{OUT}}{2^8} = \frac{V_{IN}}{V_{REF+} - V_{REF-}}$$

Where D_{OUT} = Digital Output
 V_{IN} = Analog Input
 V_{REF+} = Positive Reference Potential
 V_{REF-} = Negative Reference Potential

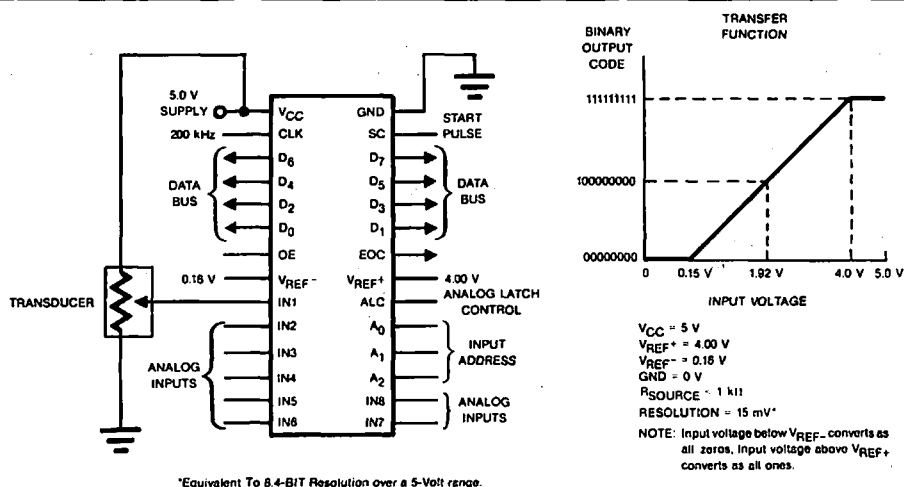
3



$V_{CC} = V_{REF+} = 5 \text{ V}$
 $GND = V_{REF-} = 0 \text{ V}$
 RESOLUTION = 19.5 mV
 $R_{SOURCE} = 1 \text{ k}\Omega$

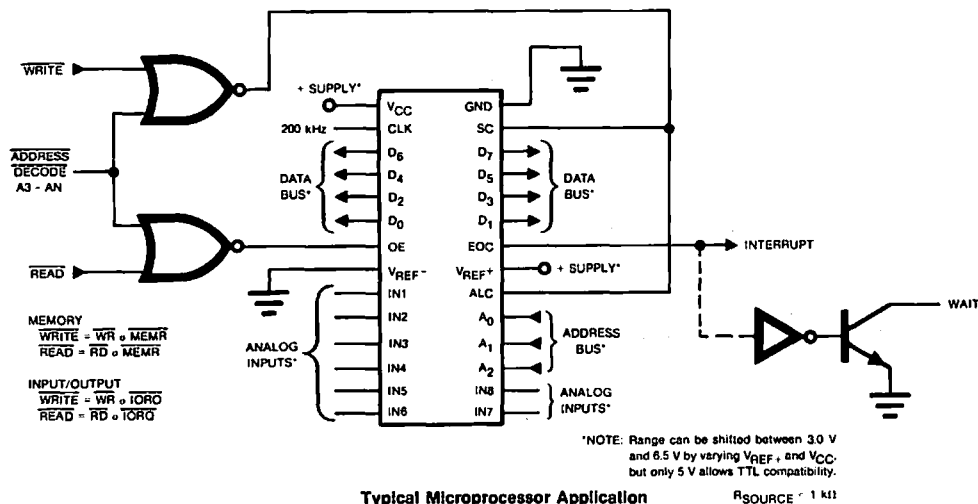
Ratiometric System
 Figure 4

APPLICATIONS (Cont.)

Compressed System With TTL-Compatible I/O
Figure 5

MICROPROCESSOR INTERFACE TABLE

PROCESSOR	READ	WRITE	INTERRUPT (COMMENT)
8080	MEMR	MEMW	INTR (Thru RST Circuit)
8085	RD	WR	INTR (Thru RST Circuit)
Z-80	RD	WR	INT (Thru RST Circuit, Mode 0)
SC/MP	NRDS	NWDS	SA (Thru Sense A)
6800	VMA + 2 R/W	VMA + 2 R/W	IRQA Or IRQB (Thru PIA)

Typical Microprocessor Application
Figure 6



Si8602

Fast 8-Channel 8 Bit CMOS

Data Acquisition System

FEATURES

- 8-Bit Resolution $\pm \frac{1}{2}$ LSB
- 25 μ s Conversion Time
- No Missing Codes
- True Sample/Hold Function
- 12.0 – 15.0 V Operation
- CMOS Compatible

BENEFITS

- Easily Interfaced to μ P
- Reduced Power Supply Requirements
- Accurate to 3/4 LSB Over Temperature
- Better Reliability than Multi-Chip Designs
- Power Consumption <30 mW

APPLICATIONS

- Data Acquisition Systems
- Portable Instruments
- Industrial Monitor and Control Systems
- Remote Data Collection

DESCRIPTION

The Si8602 is a CMOS Data Acquisition System combining an 8-channel multiplexer, a sample-hold function, a 25 μ s 8-bit A/D converter and microprocessor compatible control logic, all on a single chip. Designed for use in general purpose data acquisition systems in process control, system diagnostics, or wherever multi-channel A/D conversions are required under the control of a microprocessor, Si8602 offers an economical solution to applications in general analog signal data collection.

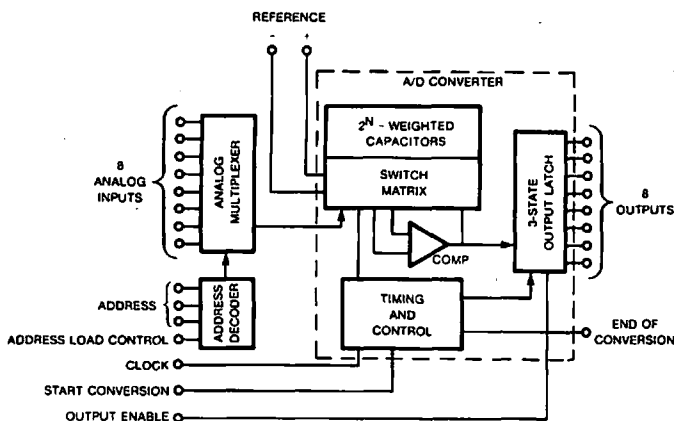
The 8-channel multiplexer in Si8602 can be controlled by a microprocessor using a 3-bit address to select any one of eight single-ended analog switches. The input signal is then 'sampled' by a capacitor sample-hold and passed to the high speed 8-bit A/D converter, which uses a binary weighted capacitor array in a successive-approximation algorithm to achieve a conversion in 25 μ s.

The design features of the Si8602 make possible a pseudo-ratiometric conversion (i.e. the reference voltage can be selected to determine the analog input range), eliminate the need for zero or full scale adjustments for most applications, and insure 'no missing codes' performance.

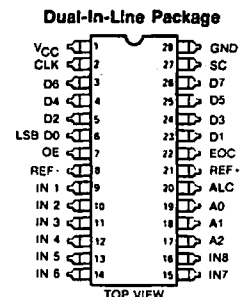
Also featured are latched 3-stated outputs and latched address inputs to the multiplexer. The single 15 volt supply, low power requirements and fast conversion time make Si8602 especially useful for a wide range of industrial applications. Package options are the 28 pin plastic or ceramic DIP which are specified over the -40 to 85°C temperature range.

3

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



Order Numbers:
Si8602DK
 See Package 24
Si8602DJ
 See Package 14

ABSOLUTE MAXIMUM RATINGS

Reference Input Voltage Range, V_{ref-} -0.3 V to V_{ref+}
 Reference Input Voltage Range, V_{ref+} V_{ref-} to $V_{CC} + 0.3$ V
 Supply Voltage, V_{CC} ¹ 6.5 V
 Input Voltage Range, All Inputs -0.3 V to $V_{CC} + 0.3$ V
 Continuous Total Dissipation at or Below 55°C² 1046 mW

Operating Temperature
 (A Suffix) -55 to 125°C
 (D Suffix) -40 to 85°C
 Storage Temperature Range -65 to 150°C
 Lead Temperature 1/16 Inch (1.6 mm) from Case for 10 Sec 260°C

ELECTRICAL CHARACTERISTICS¹ $T_A = 25^\circ\text{C}$

	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: $V_{CC} = 15$ V, $f_{clock} = 1.04$ MHz $V_{ref+} = 10$ V, $V_{ref-} = 0$ V	LIMITS			UNIT
				MIN ²	TYP ³	MAX	
ANALOG INPUT	Analog Input Voltage ⁵	V_{ANALOG}		V_{ref-}		V_{ref+}	V
	Channel ON State Current ⁵	$I_{on(Peak)}$	$V_I = 5$ V		-5		μA
	Channel OFF State Current ⁶	I_{Off}	$V_I = 15$ V $V_I = 0$		50 -50	100	nA
DYNAMIC	Control Input Capacitance	C_I			2.5		pF
	Data Output Capacitance	C_O			5.5		
	Supply Voltage Sensitivity	$ksvs$			0.05		%/V
	Zero Error ⁷		$f_{clock} = 372$ kHz or 1.04 MHz	$V_{CC} = 10.8$ $V_{CC} = 18.5$	-0.5 -0.5	0.5 0.5	LSB
	Full Scale Error ⁷			$V_{CC} = 10.8$ $V_{CC} = 18.5$	-0.75 -0.75	0.75 0.75	
	Relative Nonlinearity			$V_{CC} = 10.8$ $V_{CC} = 18.5$	-0.5 -0.5	0.5 0.5	
	Differential Nonlinearity			$V_{CC} = 10.8$ $V_{CC} = 18.5$	-0.5 -0.5	0.5 0.5	
TIMING	Clock Frequency	f_{clock}	$V_{CC} = 15$ V, $V_{ref} = 10$ V			1500	kHz
	Start Pulse Width	t_{SC}		50			ns
	Address Load Control Pulse Width	t_{ALC}		50			
	Address Set Up Time	t_{SU}		50			
	Address Hold Time	t_H		50			
	Input Voltage Stable	t_{IS}		8			Clock Period
	End of Conversion Delay Time	t_{DEC}		0		200	ns
	Conversion Time ⁹	t_{CONV}				25	μs
	Output Enable Time	t_{OE}	$C_L = 50$ pF		80	200	ns
	Output Disable Time	t_{OD}	$C_L = 10$ pF, $R_L = 10$ k Ω		80	200	
DIGITAL INPUT	High Level Input Voltage	V_{IH}		13.5			V
	Low Level Input Voltage	V_{IL}				1.5	
	High Level Input Current	I_{IH}	$V_I = 15.0$ V			1	μA
	Low Level Input Current	I_{IL}	$V_I = 0$	-1			
	High Level Output Voltage	V_{OH}	$I_O = 360$ μA	14	14.8		V
	Low Level Output Voltage	V_{OL}	$I_O = 1.6$ mA, All		0.16	0.4	
	OFF State Output Current	I_{OS}		-1		1	μA

NOTES:

- Refer to PROCESS OPTION FLOWCHART for additional information.
- The algebraic convention whereby the most negative value is a minimum, and the most positive value is a maximum, is used in this data sheet.
- Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- Current increase linearly with frequency of the clock at a rate of approximately 10% per 100 kHz.
- Decays exponentially during first clock high period.
- Channel addressed with clock off.
- Errors are measured with reference to an ideal straight line transfer curve from 19.6 mV to 9.98 V. See Figure below.
- Analog input voltage greater than V_{ref+} converts as all ones and less than V_{ref-} as all zeros.
- Source resistance ≤ 1 k Ω .

ELECTRICAL CHARACTERISTICS¹ (Cont.) $T_A = 25^\circ\text{C}$

	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: $V_{CC} = 15\text{ V}$, $f_{\text{clock}} = 1.04\text{ MHz}$ $V_{REF+} = 10\text{ V}$, $V_{REF-} = 0\text{ V}$	LIMITS			UNIT
				MIN ²	TYP ³	MAX	
SUPPLY	Supply Current ⁴	I_{CC}	$V_{IH} = 15\text{ V}$, $V_{IL} = 0\text{ V}$		0.6		mA
	Reference Current ⁴	I_{ref}			1.7		
	Supply Voltage	V_{CC}		10.8		16.5	
	Positive Reference Voltage ⁶	V_{ref+}		8		10	V
	Negative Reference Voltage ⁶	V_{ref-}		0		0.3	
	Voltage Between V_{CC} and V_{ref+} Terminals	V_{CC-} V_{ref+}		See Figure 1			

 $T_A = \text{Over Temperature Range}$

	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: $V_{CC} = 15\text{ V}$, $f_{\text{clock}} = 1.04\text{ MHz}$ $V_{\text{REF}+} = 10\text{ V}$, $V_{\text{REF}-} = 0\text{ V}$	LIMITS			UNIT
				MIN ²	TYP ³	MAX	
ANALOG INPUT	Analog Input Voltage ⁵	V_{ANALOG}	$V_I = 15\text{ V}$	$V_{\text{ref}-}$		$V_{\text{ref}+}$	V
	Channel OFF State Current ⁶	I_{Off}	$V_I = 0$	-1		1	nA
DYNAMIC	Zero Error ⁷		$f_{\text{clock}} = 372\text{ kHz}$ or 1.04 MHz	$V_{CC} = 10.8$ $V_{CC} = 16.5$	-0.5 -0.5	0.5 0.5	LSB
	Full Scale Error ⁷			$V_{CC} = 10.8$ $V_{CC} = 16.5$	-0.75 -0.75	0.75 0.75	
	Relative Accuracy Error ⁷			$V_{CC} = 10.8$ $V_{CC} = 16.5$	-0.5 -0.5	0.5 0.5	
	Differential Nonlinearity			$V_{CC} = 10.8$ $V_{CC} = 16.5$	-0.5 -0.5	0.5 0.5	
TIMING	Clock Frequency	f_{clock}	$V_{CC} = 15\text{ V}$, $V_{\text{ref}} = 10\text{ V}$			1500	kHz
	Input Voltage Stable	t_{IS}		8			Clock Period
	Conversion Time ⁹	t_{CONV}				25	μs
DIGITAL INPUT/OUTPUT	High Level Input Voltage	V_{IH}		13.5			V
	Low Level Input Voltage	V_{IL}				1.5	
	High Level Input Current	I_{IH}	$V_I = 15.0\text{ V}$			1	μA
	Low Level Input Current	I_{IL}	$V_I = 0$	-1			
	High Level Output Voltage	V_{OH}		14			V
	Low Level Output Voltage	V_{OL}	$I_O = 1.6\text{ mA}$, All			0.4	
	OFF State Output Current	I_{OS}		-1		1	μA

NOTES:

- Refer to PROCESS OPTION FLOWCHART for additional information.
- The algebraic convention whereby the most negative value is a minimum, and the most positive value is a maximum, is used in this data sheet.
- Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- Current increase linearly with frequency of the clock at a rate of approximately 10% per 100 kHz.
- Decays exponentially during first clock high period.
- Channel addressed with clock off.
- Errors are measured with reference to an ideal straight line transfer curve from 19.6 mV to 9.98 V. See Figure below.
- Analog input voltage greater than $V_{\text{ref}+}$ converts as all ones and less than $V_{\text{ref}-}$ as all zeros.
- Source resistance $\leq 1\text{ k}\Omega$.

ELECTRICAL CHARACTERISTICS¹ (Cont.)T_A = Over Temperature Range

	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: V _{CC} = 15 V, f _{clock} = 1.04 MHz V _{REF+} = 10 V, V _{REF-} = 0 V	LIMITS			UNIT
				MIN ²	TYP ³	MAX	
SUPPLY	Supply Current ⁴	I _{CC}	V _{IH} = 15 V, V _{IL} = 0 V			2	mA
	Supply Voltage	V _{CC}		10.8		16.5	V
	Positive Reference Voltage ⁸	V _{ref+}		8		10	
	Negative Reference Voltage ⁸	V _{ref-}		0		0.3	
	Voltage Between V _{CC} and V _{ref+} Terminals	V _{CC} - V _{ref+}		See Figure 1			

NOTES:

1. Refer to PROCESS OPTION FLOWCHART for additional information.
2. The algebraic convention whereby the most negative value is a minimum, and the most positive value is a maximum, is used in this data sheet.
3. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
4. Current increase linearly with frequency of the clock at a rate of approximately 10% per 100 kHz.
5. Decays exponentially during first clock high period.
6. Channel addressed with clock off.
7. Errors are measured with reference to an ideal straight line transfer curve from 19.6 MV to 9.98 V. See Figure below.
8. Analog input voltage greater than V_{ref+} converts as all ones and less than V_{ref-} as all zeros.
9. Source resistance ≤ 1 kΩ.

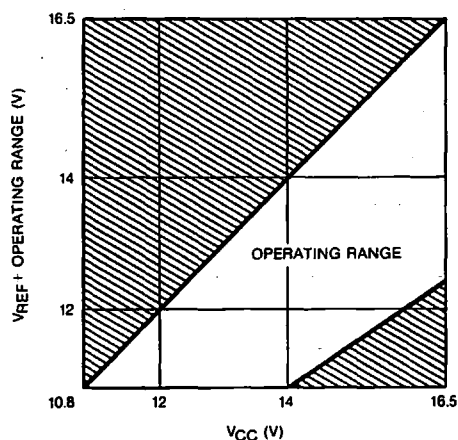
Operating Range Of V_{ref+}

Figure 1

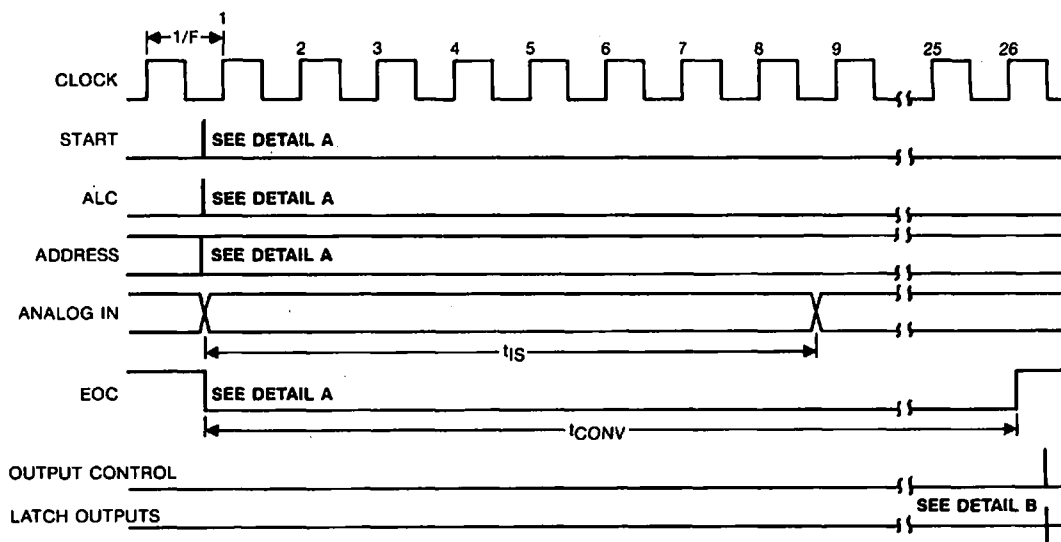
PIN DESCRIPTION

Pin Number	Symbol	Description
1	VCC	Input for the positive supply voltage.
2	CLK	Input for the CLOCK. The clock amplitude must conform to the V_{IH} and V_{IL} of the specifications and the rise time should be less than 10ns.
3-6	D ₀ , D ₂ , D ₄ , D ₆	Digital DATA OUTPUTS. Bit 0 (Pin 6) is the LSB.
7	OE	Logic input for OUTPUT ENABLE. Connects the three-state output latches to the microprocessor BUS.
8	REF-	Input for the most negative voltage of the reference. It is normally grounded unless compressed mode operation is desired.
9-16	IN ₁ IN ₈	ANALOG INPUTS of the 8-channel multiplexer (channel 1-Pin 9, channel 8-Pin 16).
17-19	A ₀ - A ₂	The three address inputs that select the one-of-eight analog inputs to be converted.
20	ALC	ADDRESS LOAD CONTROL input that latches the input address into the multiplexer.
21	REF+	Input for the positive reference voltage. END OF CONVERSION output that goes high at the end of conversion.
22	EOC	END OF CONVERSION output that goes high at the end of conversion.
23-26	D ₁ , D ₃ , D ₅ , D ₇	Digital DATA OUTPUTS. Bit 7 (Pin 26) is the MSB.
27	SC	START CONVERSION input that initiates the conversion process.
28	GND	Power supply and analog GROUND.

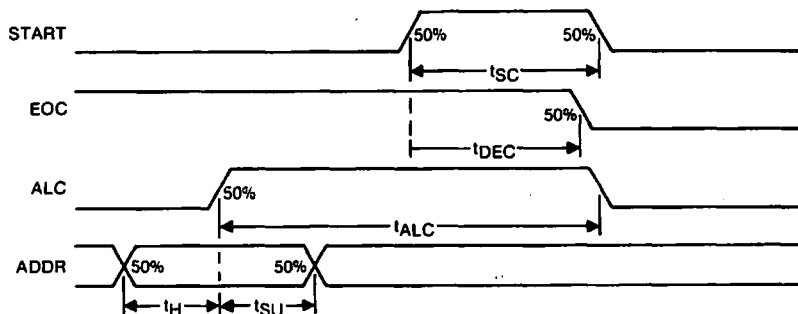
GENERAL PRECAUTIONS (For All Applications)

1. VREF+ must NEVER exceed VCC by more than 50 mV.
2. VREF- must NEVER be more negative than GND by more than 50 mV.
3. Under NO condition should the VREF+ be applied before VCC (Prevents Latch-up).

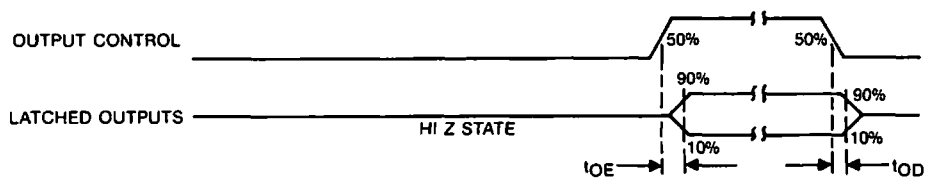
ELECTRICAL CHARACTERISTICS (Cont.)



DETAIL A



DETAIL B



Timing Diagram
Figure 2

PRINCIPLES OF OPERATION

The analog multiplexer selects 1 of 8 single-ended input channels as determined by the input address code. The address-load control transfers and latches the code into the decoder on the positive edge of the signal. The output latch is reset by the positive edge of the start pulse. Sampling starts with the positive edge of the start pulse and lasts for 8 clock periods from its falling edge. The conver-

sion process can be interrupted by a new start pulse before the end of 24 clock periods. Continuous conversion may be accomplished by connecting the end-of-conversion output to the start input. If used in this mode an external pulse should be applied after power up to assure start up.

MULTIPLEXER FUNCTION TABLE

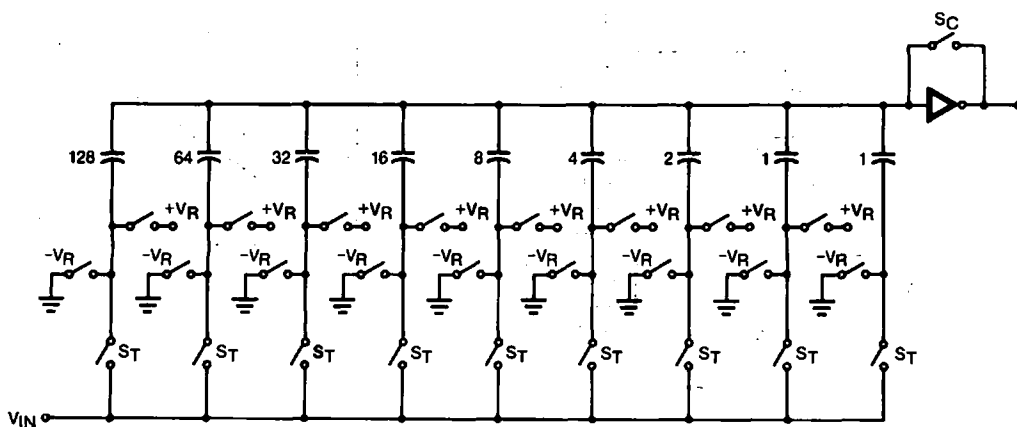
INPUTS				SELECTED ANALOG CHANNEL
ADDRESS			ADDRESS LOAD CONTROL*	
A ₂	A ₁	A ₀		
0	0	0	↑	1
0	0	1	↑	2
0	1	0	↑	3
0	1	1	↑	4
1	0	0	↑	5
1	0	1	↑	6
1	1	0	↑	7
1	1	1	↑	8

* ↑ = Low-to-High Transition

SWITCHED CAPACITOR A/D CONVERTER

The CMOS comparator in the successive-approximation system determines each bit by examining the charge on a series of binary-weighted capacitors (Figure 3). In the first phase of the conversion process, the analog input is

sampled by closing switch S_C and all S_T switches, and by simultaneously charging all the capacitors to the input voltage.



Simplified Successive Approximation A/D Converter
Figure 3

SWITCHED CAPACITOR A/D CONVERTER (Cont.)

In the next phase of the conversion process, all S_T and S_C switches are opened and the comparator begins identifying bits by identifying the charge on each capacitor relative to the reference voltage. In the switching sequence, all eight capacitors are examined separately until all 8 bits are identified, and then the charge-convert sequence is repeated. In the first step of the conversion phase, the comparator looks at the first capacitor (binary weight = 128). One pole of this capacitor is switched to the reference voltage, and the equivalent poles of all the other capacitors on the ladder are switched to ground. If the voltage at the summing node is greater than the trip-point of the comparator (approximately one-half the reference voltage), a bit is placed in the output register, and the 128-weight capacitor is switched to ground. If the voltage

at the summing node is less than the trip-point of the comparator, this 128-weight capacitor remains connected to the reference input through the remainder of the capacitor-sampling (bit-counting) process. The process is repeated for the 64-weight capacitor, the 32-weight capacitor, and so forth down the line, until all bits are tested.

As can be seen, with each step of the capacitor-sampling process, the initial charge is redistributed among the capacitors. The conversion process is successive-approximation, but relies on charge shifting rather than a successive-approximation register (and reference D/A) to count and weigh the bits from MSB to LSB.

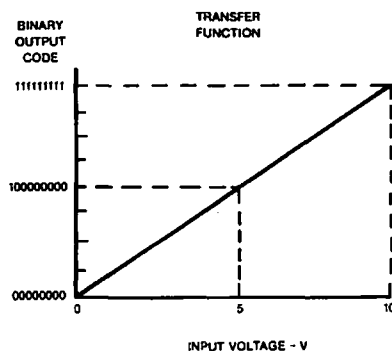
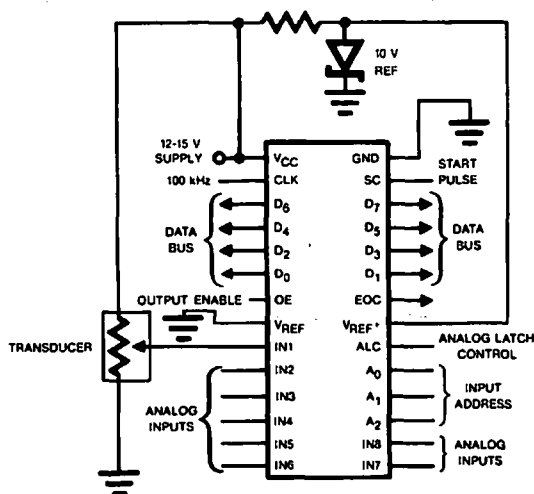
APPLICATIONS

The Si8601 is a CMOS Data Acquisition System using charge redistribution to achieve A/D conversion. In typical applications, as a ratiometric conversion system for a microprocessor, V_{REF-} will be connected to ground and

V_{REF+} will be connected to V_{CC} . The output will then be a simple proportional ratio between analog input voltage and V_{CC} (Figure 4). The general relationship is:

$$\frac{D_{OUT}}{2^8} = \frac{V_{IN}}{V_{REF+} - V_{REF-}}$$

Where D_{OUT} = Digital Output
 V_{IN} = Analog Input
 V_{REF+} = Positive Reference Potential
 V_{REF-} = Negative Reference Potential

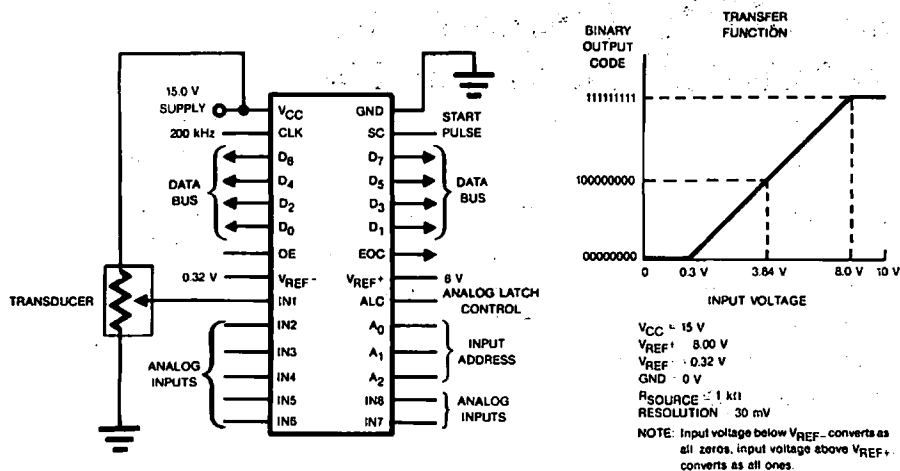


$V_{CC} = 15 \text{ V}$
 $V_{REF} = 10 \text{ V}$
 $GND = V_{REF-} = 0 \text{ V}$
 $\text{RESOLUTION} = 39 \text{ mV}$
 $R_{SOURCE} \leq 1 \text{ k}\Omega$

Ratiometric System

Figure 4

APPLICATIONS (Cont.)



Compressed System with CMOS-Compatible I/O
Figure 5

MICROPROCESSOR INTERFACE TABLE

PROCESSOR	READ	WRITE	INTERRUPT (COMMENT)
8080	MEMR	MEMW	INTR (Thru RST Circuit)
8085	RD	WR	INTR (Thru RST Circuit)
Z-80	RD	WR	INT (Thru RST Circuit, Mode 0)
SC/MP	NRDS	NWDS	SA (Thru Sense A)
6800	VMA + 2 R/W	VMA + 2 R/W	IRQA Or IRQB (Thru PIA)

Si25HC04

12 Bit CMOS Successive Approximation Register



FEATURES

- On Board Controlling Logic
- CMOS Technology
- Three State Outputs
- Expandable via Cascading
- Can be "Short-Cycled"

BENEFITS

- Ease of Interface
- Low Power Requirements
- Optimized Conversion Speed

APPLICATIONS

- Analog to Digital Converters
- Ring Counters
- Serial to Parallel Converters

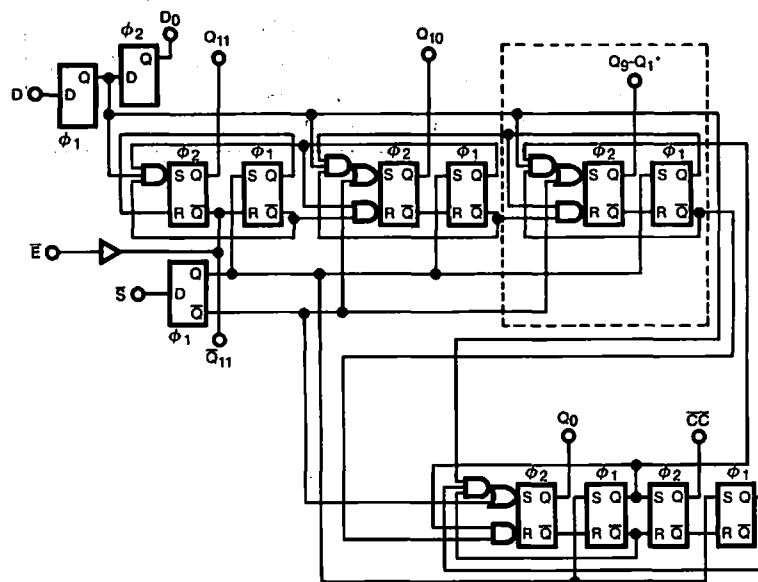
DESCRIPTION

The Si25HC04 is a 12-bit successive approximation register that contains all the digital control and storage necessary to build a successive approximation A/D converter. The Si25HC04 acts as a special purpose serial-to-parallel converter that accepts serial input data, moves it to the appropriate slave latch, and then to the register output (and the serial data out port). To facilitate 2's complement coding the complementary output of the most significant

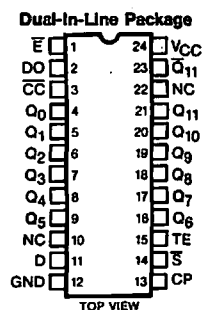
bit is made available. The register can be cascaded for applications requiring more than 12 bits, or short-cycled (truncated) if not all bits are required.

The Si25HC04 is available in a 24 lead ceramic or plastic DIP package, and is specified over the commercial (0 to 70°C) and military (-55 to 125°C) temperature ranges.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



Order Numbers:
 Si25HC04AK
 See Package 28
 Si25HC04CJ
 See Package 27

*Cell logic is repeated for register stages Q_9 to Q_1 .

ABSOLUTE MAXIMUM RATINGS

Supply Voltage

to Ground Potential (Continuous) -0.5 to 7.0 V

DC Voltage Applied

to Outputs for High Output State ... -0.5 to V_{CC} Max

DC Input Voltage -0.5 to 5.5 V

Output Current, Into Outputs 30 mA

DC Input Current -30 to 5.0 mA

Storage Temperature

(A Suffix) -65 to 150°C

(C Suffix) -65 to 125°C

Operating Temperature

(A Suffix) -55 to 125°C

(C Suffix) 0 to 70°C

ELECTRICAL CHARACTERISTICS¹ $T_A = 25^\circ\text{C}$

	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: $V_{CC} = 5.0\text{ V}$		LIMITS			UNIT
					MIN ²	TYP ³	MAX	
OUTPUT	Output High Voltage	V_{OH}	$V_{CC} = 4.5\text{ V}$, $V_{in} = 2.0\text{ V}$ or 0.8 V	$I_{OH} = -0.5\text{ mA}$	2.4			V
	Output Low Voltage	V_{OL}		$I_{OL} = 6.0\text{ mA}$			0.4	V
	Output Current in High Impedance State	I_{OC}	$V_O = 0\text{ V}$ $V_O = 5.0\text{ V}$		-1.0		1.0	μA
INPUT	Input High Voltage	V_{IH}			2.0			V
	Input Low Voltage	V_{IL}					0.8	V
	Input High Current	I_{IH}	$V_{CC} = V_{in} = 5.5\text{ V}$			1.0		mA
	Input Low Current	I_{IL}	$V_{CC} = 5.5\text{ V}$, $V_{in} = 0.4\text{ V}$			1.0		
SUPPLY	Power Supply Current	I_{CC}	$V_{CC} = 5.5\text{ V}$	A Suffix		2	3.0	mA
				C Suffix		2	3.0	
			All Inputs High or Low				0.15	
DYNAMIC	Turn-OFF Delay CP To Output High	t_{pd+}	$C_L = 50\text{ pF}$			3.0	55	ns
	Turn-OFF Delay CP To Output Low	t_{pd-}				3.0	55	
	Setup Time Data Input	t_{SD}			-10	0	10	
	Setup Time Start Input	t_{SS}			-15	-7	0	
	Turn-OFF Delay E to Q7(11) High	t_{pdE+}				20	35	
	Turn-On Delay E to Q7(11) Low	t_{pdE-}				30	55	
	Minimum Low Clock Pulse Width	t_{CPWL}				30	45	
	Minimum High Clock Pulse Width	t_{CPWH}				30	45	
	Maximum Clock Frequency	f_{MAX}			10	15		MHz

NOTES:

1. Refer to PROCESS OPTION FLOWCHART for additional information.
2. The algebraic convention whereby the most negative value is a minimum, and the most positive is a maximum, is used in this data sheet.
3. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

ELECTRICAL CHARACTERISTICS¹ (Cont.)T_A = Over Temperature Range

	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: V _{CC} = 5.0 V		LIMITS			UNIT
					MIN ²	TYP ³	MAX	
OUTPUT	Output High Voltage	V _{OH}	V _{CC} = 4.5 V, I _{OH} = -0.5 mA		2.4			V
	Output Low Voltage	V _{OL}	V _{in} = 2.0 V or 0.8 V, I _{OL} = 8.0 mA				0.4	
	Output Current in High Impedance State	I _{OC}	V _O = 0 V V _O = 5.0 V		-1.0		1.0	μA
INPUT	Input High Voltage	V _{IH}			2.0			V
	Input Low Voltage	V _{IL}					0.8	
	Input High Current	I _{IH}	V _{CC} = V _{in} = 5.5 V					
SUPPLY	Input Low Current	I _{IL}	V _{CC} = 5.5 V, V _{in} = 0.4 V					
	Power Supply Current	I _{CC}	V _{CC} = 5.5 V	A Suffix			3.0	mA
				C Suffix			3.0	
DYNAMIC	Turn-OFF Delay CP To Output High	t _{pd} +	C _L = 50 pF				5	ns
	Turn-OFF Delay CP To Output Low	t _{pd} -					5	
	Setup Time Data Input	t _{SD}			-10		10	
	Setup Time Start Input	t _{SS}			-15		0	
	Turn-OFF Delay E to Q ₇₍₁₁₎ High	t _{pdE} +					35	
	Turn-On Delay E to Q ₇₍₁₁₎ Low	t _{pdE} -					55	
	Minimum Low Clock Pulse Width	t _{CPWL}					45	
	Minimum High Clock Pulse Width	t _{CPWH}					45	
	Maximum Clock Frequency	f _{MAX}			10			MHz

NOTES:

1. Refer to PROCESS OPTION FLOWCHART for additional information.
2. The algebraic convention whereby the most negative value is a minimum, and the most positive is a maximum, is used in this data sheet.
3. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

TRUTH TABLE

Time	Inputs				Outputs													
t _n	D	S	E		D ₀	Q ₁₁	Q ₁₀	Q ₉	Q ₈	Q ₇	Q ₆	Q ₅	Q ₄	Q ₃	Q ₂	Q ₁	Q ₀	CC
0	X	L	L		X	X	X	X	X	X	X	X	X	X	X	X	X	X
1	D ₁₁	H	L		X	L	H	H	H	H	H	H	H	H	H	H	H	H
2	D ₁₀	H	L		D ₁₁	D ₁₁	L	H	H	H	H	H	H	H	H	H	H	H
3	D ₉	H	L		D ₁₀	D ₁₁	D ₁₀	L	H	H	H	H	H	H	H	H	H	H
4	D ₈	H	L		D ₉	D ₁₁	D ₁₀	D ₉	L	H	H	H	H	H	H	H	H	H
5	D ₇	H	L		D ₈	D ₁₁	D ₁₀	D ₉	D ₈	L	H	H	H	H	H	H	H	H
6	D ₆	H	L		D ₇	D ₁₁	D ₁₀	D ₉	D ₈	D ₇	L	H	H	H	H	H	H	H
7	D ₅	H	L		D ₆	D ₁₁	D ₁₀	D ₉	D ₈	D ₇	D ₆	L	H	H	H	H	H	H
8	D ₄	H	L		D ₅	D ₁₁	D ₁₀	D ₉	D ₈	D ₇	D ₆	D ₅	L	H	H	H	H	H
9	D ₃	H	L		D ₄	D ₁₁	D ₁₀	D ₉	D ₈	D ₇	D ₆	D ₅	D ₄	L	H	H	H	H
10	D ₂	H	L		D ₃	D ₁₁	D ₁₀	D ₉	D ₈	D ₇	D ₆	D ₅	D ₄	D ₃	L	H	H	H
11	D ₁	H	L		D ₂	D ₁₁	D ₁₀	D ₉	D ₈	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	L	H	H
12	D ₀	H	L		D ₁	D ₁₁	D ₁₀	D ₉	D ₈	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	L	H
13	X	H	L		D ₀	D ₁₁	D ₁₀	D ₉	D ₈	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	L
14	X	X	L		X	D ₁₁	D ₁₀	D ₉	D ₈	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	L
	X	X	H		X	H	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC

H = HIGH Voltage Level

L = LOW Voltage Level

X = Don't Care

NC = No Change

PIN DESCRIPTION

Pin Number	Symbol	Description
1	$\bar{E}$	Register ENABLE. This input is used to expand the length of the register and when high forces the Q ₁₁ register output high and inhibits conversion. When not used for expansion the enable is held at a LOW logic level (GND).
2	DO	The serial DATA OUTPUT.
3	$\overline{CC}$	CONVERSION COMPLETE output. This output remains HIGH during conversion and goes LOW when a conversion is complete.
4-9	Q ₀ -Q ₅	Register OUTPUTS. The six least significant bits of the register. Q ₀ is the LSB.
10	NC	No connection.
11	D	Serial DATA INPUT.
12	GND	Ground
13	CP	CLOCK INPUT.
14	$\bar{S}$	START input. Holding this input LOW for at least one clock period will reset the register to Q ₁₁ LOW and Q ₀ -Q ₁₀ HIGH. A LOW of one clock period is not necessary if it meets the set-up time requirements of the S input.
15	TE	THREE STATE ENABLE input. A HIGH on this input will disable the outputs putting them in a high impedance state. This input has an internal pull-down and needs no connection for normal operation.
16-21	Q ₆ -Q ₁₁	Register OUTPUTS. The six most significant bits of the register. Q ₁₁ is the MSB.
22	NC	No Connection.
23	$\bar{Q}_{11}$	Complementary output of the MSB register.
24	VCC	Positive power supply input.

OPERATION

The registers consist of a set of master-latches that act as the control elements in the device and change state when the input clock is LOW. A set of slave latches, that hold the register data and change on the input clock LOW-to-HIGH transition. Externally the device acts as a special purpose serial-to-parallel converter. It accepts data at the D input of the register and sends the data to the appropriate slave latch, this data appears at the register output and the DO output on the Si25HC04 when the clock goes from LOW-to-HIGH. There are no restrictions on the data input; it can change state at any time except during the set-up time just prior to the clock transition. At the same time that data enters the register bit the next less significant bit is set to a LOW ready for the next iteration and so on for each successive bit conversion cycle.

The register is reset by holding the $\bar{S}$ (Start) signal LOW during a full clock LOW-to-HIGH transition. The register synchronously resets to the state Q₁₁ LOW, (Note 2) and all the remaining register outputs HIGH. The $\overline{CC}$ (Conversion Complete) signal is also set HIGH at this time. After the clock has gone HIGH resetting the register, the S signal is removed. On the next clock LOW-to-HIGH transition the data on the D input is set into the Q₁₁ register bit. The Q₁₀ register bit is set to a LOW ready for the next

clock cycle. On the next clock LOW-to-HIGH transition data enters the Q₁₀ register bit and Q₉ is set to a LOW. This operation is repeated for each register bit in turn until the register has been filled. When the data goes into Q₀, the $\overline{CC}$ signal goes LOW, and the register is inhibited from further change until reset by a Start signal.

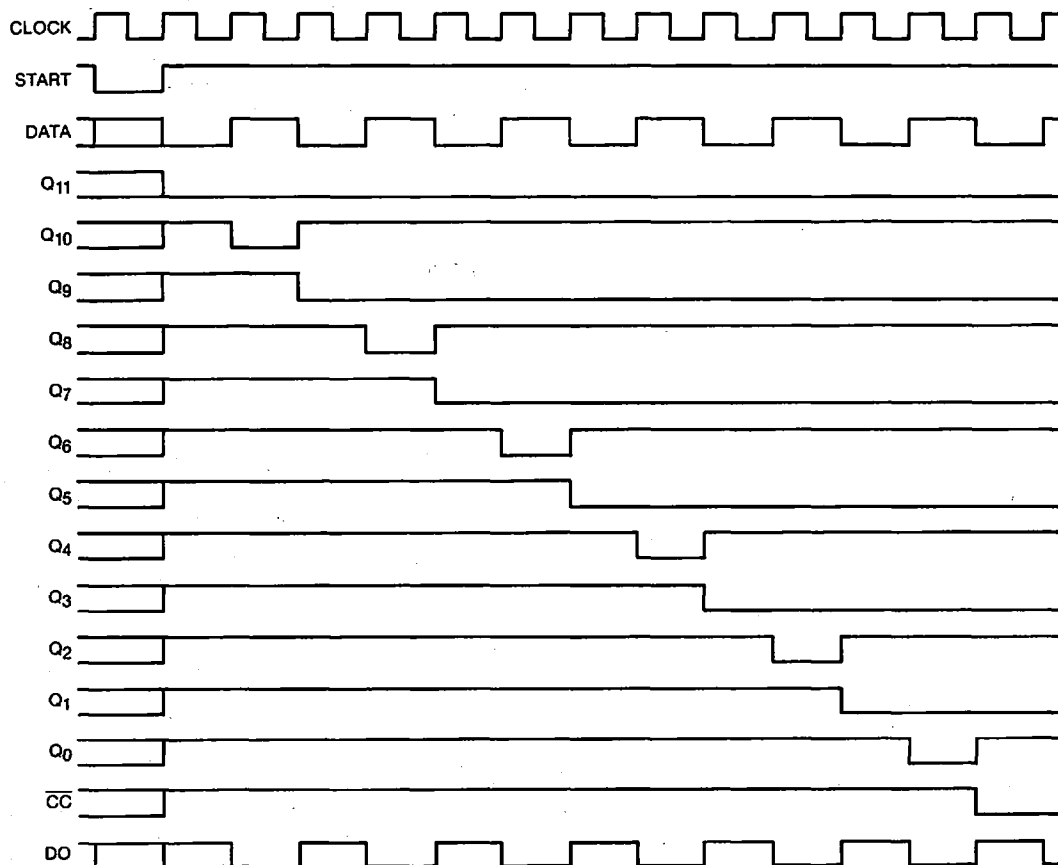
In order to allow ones or twos complement conversion, the complementary output of the most significant register bit is made available.

An active LOW enable input ($\bar{E}$) allows devices to be cascaded together to form a longer register. This is done by paralleling the clock, D, and $\bar{S}$ inputs and connecting the $\overline{CC}$ output to the $\bar{E}$ input of the next less significant device. When the Start signal resets the registers, the $\overline{CC}$ signals go HIGH, starting conversion in the MS Device and inhibiting the next less significant device from accepting data until the previous device is full and its $\overline{CC}$ goes LOW. If only one device is used the $\bar{E}$ input should be held at a LOW logic level. If all the bits are not required, the register may be truncated and conversion time saved by using a register output going LOW rather than the $\overline{CC}$ signal to indicate the end of conversion.

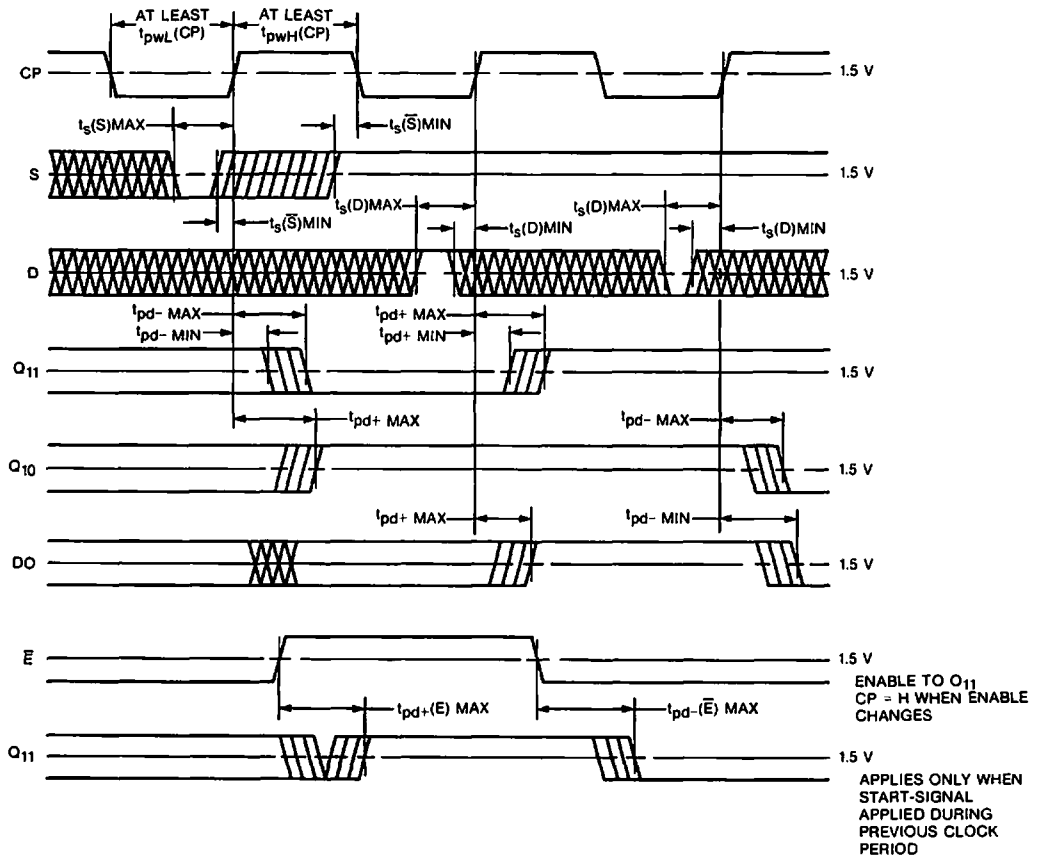
USER NOTES FOR A/D CONVERSION

1. The register can be used with either current switches that require a low voltage level to turn the switch on, or current switches that require a high voltage level to turn the current switch on. If current switches are used which turn on with a low logic level the resulting digital output from the register is active LOW. That is, a logic "1" is represented as a low voltage level. If current switches are used that turn on with a high logic level then the digital output is active HIGH; a logic "1" is represented as a high voltage level.
2. For a maximum digital error of $\pm 1/2$ LSB the comparator must be biased. If current switches that require a high voltage level to turn on are used, the comparator should be biased $+1/2$ LSB and if the current switches require a high logic level to turn on then the comparator must be biased $-1/2$ LSB.
3. The register, by suitable selection of resistor ladder network, can be used to perform either binary or BCD conversion. Additional data input gating should be used to eliminate the possibility of false BCD codes.
4. The register can be used to perform 2's complement conversion by offsetting the comparator $1/2$ full range $+1/2$ LSB and using the complement of the MSB Q_{11} as the sign bit.
5. If the register is truncated and operated in the continuous conversion mode a lock-up condition may occur on power-on. This situation can be overcome by making the START input the OR function of $\overline{CC}$ and the appropriate register output.

TIMING CHART



SWITCHING TIME WAVEFORMS



Key to Timing Diagram

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE: ANY CHANGE PERMITTED	CHANGING STATE UNKNOWN

Introduction	0
Interface	1
Analog Switches/Multiplexers	2
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DIGITAL-TO-ANALOG CONVERTERS

Title	Page
Introduction	4-3
Si8021/Si8020	4-5
DG515/DG516	4-11

Digital-To-Analog Converter Product Selector Guide¹

Function	Part No. Package Information	Specifications	Features
4-bit SPDT DAC switch	DG515 14 pin plastic, Sidebrazed, Ceramic	Binary weighted ON resistance 120 ns T_{on} time	Low ON resistance over temperature On chip drivers Used to configure up to 14 bit ADC or DAC with DG516
10-bit SPDT DAC switch	DG516 28 pin plastic, 28 pin ceramic, Ceramic	Binary weighted ON resistance 120 ns T_{on} time	Low ON resistance over temperature On chip drivers Used to configure up to 14 bit ADC or DAC with DG515
12-bit Monolithic CMOS Multiplying DAC	Si8021/8020² 28 pin plastic 28 pin ceramic	Guaranteed monotonicity to 12-bits Nonlinearity: .024% full scale—Si8021 .048% full scale—Si8020 Typical 1 μ s settling time	Multiplying DAC—accepts AC or DC reference Full four quadrant operation $\pm 25V$ reference (max rating) Double buffered Segmented bus for 4, 8, or 12-bit operation Onboard logic control circuitry

NOTE:

1. Devices shown in **boldface** are recommended for new designs.
2. Preliminary product. Specifications subject to change. Contact factory on availability.

INTRODUCTION

D/A Converter Products

Siliconix offers a number of circuit designs for use in developing D/A converter systems. The DG515 and DG516 are four and ten bit voltage switches, respectively, for use in building precision multiplying D/A converters. The switches include binary weighting in the most significant bits to reduce integral linearity errors. The Si8020 and Si8021 are twelve bit multiplying D/A converters with onboard latches and chip select logic to simplify interfacing with most microprocessors. They feature complementary current outputs to achieve bipolar output capability, or multiplication in all four quadrants. Both Si8020 and Si8021 also feature a segmented design to reduce glitches.

D/A Converters are devices that reconstitute analog signals from digital data. The basic converter consists of an arrangement of weighted resistance values, an analog reference or variable, and voltage or current switches that develop varying output voltages or steer currents in accordance with the digital input code. Although many converters have fixed references, there are many

applications calling for digital control of the gain (or attenuation) of an analog variable. Such devices are called *multiplying D/A converters*, because their the analog output is the product of the input digital code and the analog reference or variable input. These converters still can, of course, be used with fixed references.

Digital input registers are frequently recommended to both simplify the interface to microprocessors, and to hold the digital word constant at the input without having to tie up the microprocessor. While many D/A converters now include some form of input register, the Si8020 and Si8021 feature double buffering to simplify interfacing with most microprocessors. With its high, mid, and low byte enable features the user can load the D/A converter in three 4-bit bytes, one 4-bit and one 8-bit byte, or one 12-bit byte as determined by the bus architecture.

One important design feature of the Si8020 and Si8021 is the reduction of glitch energy at the major transition around the MSB. This is accomplished by using the segmented design approach.

GLOSSARY OF TERMS

Accuracy

May be specified in absolute and/or relative terms. Absolute accuracy is interpreted as a measure of the total error of the converter, and is expressed in terms of the difference between the actual analog output and the output expected for a given input digital code. Relative accuracy, on the other hand, is more an interpretation of the non-linearity of the converter and is specified in terms of the difference between the actual analog output and the output expected (based on the relative, or actual full scale output of the converter) for a given input code.

Absolute accuracy measurements should be made under a set of standard conditions, with the signal sources and measuring equipment traceable to some acceptable standard. Specified as LSB, or percent of full scale range.

Compliance Voltage

For a current output D/A converter, it is the maximum voltage range on the output terminal over which the current output of a DAC can vary for the DAC to meet an absolute accuracy as specified (usually $\pm 1/2$ LSB).

Differential Linearity (DNL)

The measured difference in output between any two adjacent digital codes should be exactly 1 LSB (or F.S. $\times 2^{-n}$ for an n-bit converter.) Any deviation from the ideal difference is called differential non-linearity, and is expressed in submultiples of an LSB. Differential linearity errors greater than 1 LSB can result in non-monotonic performance in a D/A converter, and missing codes in an A/D converter.

Feedthrough

An AC specification for a multiplying DAC which defines the frequency at which a specified (pk-pk) AC signal is seen at the DAC output with all bits in the "off" state. It is usually specified as %, ppm, or fractions of an LSB for a given set of input conditions.

Four Quadrant

For a multiplying D/A converter, "four quadrant" means that both the reference signal and the number represented by the digital input signal may be of either polarity. The converter is expected to obey the rules of multiplication for algebraic sign.

Gain

The gain of the converter is the analog scale factor that describes the nominal conversion relationship between the converter's full scale output and its analog (or reference) input. The gain is gen-

erally adjustable by the user (externally) to Full Scale $\times (1-2^{-n})$ with all bits on. For bipolar operation adjust output to F.S. $(1-2^{-(n-1)})$ with all bits on.

Least Significant Bit (LSB)

In a binary numerical system, the LSB is the bit that represents the least, or smallest, value. For example, in the natural binary number 1101 (decimal 13, or $2^3 + 2^2 + 0 \cdot 1 + 2^0$), the right-most digit is the LSB. It thus represents the smallest analog change that can be resolved in an n-bit converter and is equal to the full scale output range divided by 2^n where n = number of bits, $LSB = FS/2^n$.

Linearity

Linearity error of a converter, which implies the integral linearity error, is the deviation of the analog output from an ideal straight line, and is usually specified in % or ppm of the Full Scale range or submultiples of 1 LSB. The straight line can be either a "best straight line", or "end point." The former is derived empirically by manipulating the offset and/or gain of the converter to minimize the deviations of the actual analog output from the manipulated best line. The latter assumes the idealized line passes through the "end points" of the converter after it has been calibrated (zero and full scale.)

Monotonicity

A D/A converter is said to be monotonic if the output either increases or remains constant with increasing digital input codes. The statement monotonic (over temperature) is sometimes substituted for a differential non-linearity specification as a DNL specification of 1 LSB is not a sufficient condition for monotonic behavior.

Most-Significant Bit (MSB)

In a binary numerical system, the MSB is the bit that represents the largest value, or weight. For example, in the natural binary number 1101 (decimal 13, or $2^3 + 2^2 + 0 \cdot 1 + 2^0$), the leftmost digit (or "1") is the MSB. Its analog weight, relative to full scale, is $FS/2$. In bipolar applications the MSB also indicates the polarity of the number represented by the rest of the bits.

Offset (Zero Scale Error)

The measured analog output when the digital input code corresponds to an analog value of zero. Generally expressed as a percentage of Full Scale range but is also expressed in ppm, LSB's or in units of current or voltage.

GLOSSARY OF TERMS (Cont.)

Resolution

The number of states (2^n) that the Full Scale range may be divided into or resolved, where n = number of bits. This is usually expressed as a number of bits (n).

Settling Time

The elapsed time for the analog output to reach its final value within a specified error band after the corresponding digital input code has been changed. Usually specified as a Full Scale range change and measured from the 50% point of the digital input code change to the time the output reaches the final value within the specified error band.

Stability

The stability of a converter is usually related to changes in its characteristics as a function of temperature and time. While such measurements are difficult and time consuming, those related to temperature are often sufficiently critical to warrant their inclusion in the characteristic data. (See also Temperature Coefficient.)

Switching Time

In a D/A converter the switching time is the time it takes for the

logic and switches to change from one state (on or off) to the other. It includes delay and rise time, but does not include settling time, and is measured from the 50% point of the logic input to the 50% point of the changing analog input signal.

Temperature Coefficient

In general, temperature coefficients are expressed as fractions of an LSB/ $^{\circ}$ C, ppm/ $^{\circ}$ C, or as a %/ $^{\circ}$ C. Siliconix specifies the parameter at 25 $^{\circ}$ C and then over the rated temperature range. The temperature coefficient (or T.C.) can then be defined as the change in the parameter divided by the corresponding temperature change, and is usually specified for gain, offset and linearity parameters.

Zero and Gain-Adjustment Principles

For unipolar applications first adjust the D/A converter for zero output with all bits "off". Then with all bits "on", adjust the output for (Full Scale - 1 LSB), or F.S. ($1 - 2^{-(n-1)}$).

For bipolar applications, in offset binary, adjust the D/A converter's "zero" for -F.S. with all bits "off". Then with all bits "on" set the gain for F.S. ($1 - 2^{-(n-1)}$), or (Full Scale - 2 LSB'S.)

Siliconix

- ## APPLICATIONS

DESCRIPTION



ABSOLUTE MAXIMUM RATINGS

V _{DD} (to GND)	17 V
V _{REF} (to GND)	±25 V
Digital Input Voltage Range	V _{DD} to GND
Output Voltage (Pin 1, Pin 2)	-300 mV to V _{DD}
Storage Temperature	-65 to 150°C
Operating Temperature	
A Suffix	-55 to 125°C
B Suffix	-25 to 85°C

CAUTION

- Do not apply voltages higher than V_{DD} or less than GND potential on any terminal except V_{REF}.
- The digital control inputs are zener protected; however, permanent damage may occur on unconnected

C Suffix	0 to 70°C
Power Dissipation (Package)	
Up to 50°C:	
Plastic	1200 mW
Ceramic	1000 mW
Derate Above 50°C:	
Plastic	12 mW/°C
Ceramic	10 mW/°C

- units under high energy electrostatic fields. Keep unused inputs in conductive foam at all times.
- V_{DD1} should not exceed V_{DD2} by more than ±0.4V, especially during power on or off sequencing.

ELECTRICAL CHARACTERISTICS¹T_A = 25°C

	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: V _{DD1} = 10 to 16 V, V _{REF} = 10 V Unipolar Connection	LIMITS			UNITS
				MIN ²	TYP ³	MAX	
INPUT	Input Voltage Low Level	V _{INL}				0.8	V
	Input Voltage High Level	V _{INH}		2.4			
	Input Current	I _{IN}		-1		1	μA
TIMING	Data Set Up Time	t _{DS}	See Timing Diagram Figure 4	250			ns
	Data Hold Time	t _{DH}		0			
	Strobe Width (LBE, MBE & HBE)	t _{SW}		250			
	Strobe Hold Time	t _{SH}		10			
	Chip Enable Time	t _{CE}		250			
	Load DAC Time	t _{LD}		250			
	Data Output Time	t _{DO}			200	300	
REF.	Reference Input Voltage Range		AC or DC	-25		25	V
	Reference Input Impedance			5.0	10.0	15	kΩ
ANALOG OUTPUT	Analog Output Scale Factor				125	200	μA/V _{ref}
	Analog Output Leakage				<1	10	nA
	Analog Output Capacitance	C _{out1}	All Inputs High			52	pF
		C _{out2}	All Inputs Low			13	
STATIC	End Point Non-Linearity	Si8021				0.024	% F.S.
		Si8020				0.048	
	Monotonicity	Si8021		12			Bits
		Si8020		11			
	Gain Error		Using Internal Feedback Resistor	-0.4	±0.3	0.4	% F.S.
DYNAMIC	Full Scale Transition		Settling to 0.01% (Strobed)		1	2	μs
	Reference Feedthrough Error		V _{REF} = 20V _{pp} , f _i = 10kHz		1	2	mV
POWER SUPPLY	Power Supply Voltage Range			5		16	V
	Power Supply Current		V _I = 0 or 5V		0.5	2.5	mA
	Power Supply Rejection Ratio				.0005	0.002	% / %

S - Sample Tested G - Guaranteed By Design

ELECTRICAL CHARACTERISTICS¹ (Cont.) T_A = Over Operating Range

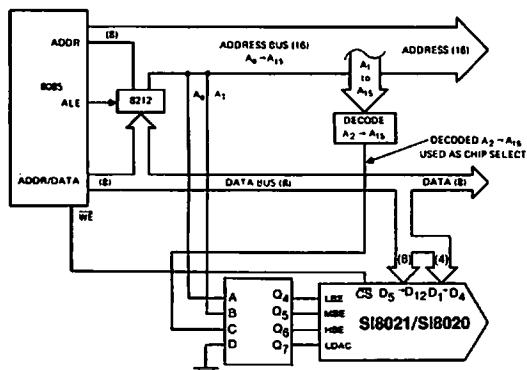
	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: $V_{DD1} = 10$ to 16 V, $V_{REF} = 10$ V Unipolar Connection	LIMITS			UNITS
				MIN ²	TYP ³	MAX	
INPUT	Input Voltage Low Level	V_{INL}				0.8	V
	Input Voltage High Level	V_{INH}		2.4			
	Input Current	I_{IN}		-1		1	μA
ANALOG OUTPUT	Analog Output Leakage				<1	200	nA
STATIC	End Point	Si8021				0.024	% F.S.
	Non-Linearity	Si8020				0.048	
	Monotonicity	Si8021		12			Bits
		Si8020		11			
STABILITY	Scale Factor TC				1	2	ppm/C
	Differential Nonlinearity TC				0.1	0.2	
POWER SUPPLY	Power Supply Voltage Range			5		16	V

NOTES:

1. Refer to PROCESS OPTION FLOWCHART for additional information.
2. The algebraic convention whereby the most negative value is a minimum, and the most positive is a maximum, is used in this data sheet.
3. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

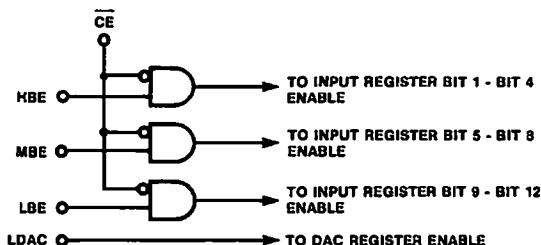
PIN NO	SYMBOL	PIN DESCRIPTION
1	FB4	Feedback path thru two internal series resistors of 4K ohms to the IO2 output. Used for low temperature drift bipolar operation.
2	LDTR	R-2R ladder termination resistor. Normally grounded for unipolar operation or connected to IO2 for bipolar operation.
3	FB3	Feedback path to the center tap of the two series resistors between IO2 and FB4. Used in conjunction with FB4 for low temperature drift bipolar operation. Provides divide by two gain (full scale equal to $V_{ref}/2$).
4	Vref	Reference voltage input - any AC or DC voltage with an instantaneous amplitude between -25V and +25V.
5	FB1	Feedback path thru an internal 8K ohm resistor to the IO1 output. Used for normal unity gain D/A conversion.
6	IO1	Current output of DAC.
7	IO2	Complementary current output of DAC.
8	ANALOG GND	Analog output ground.
9-20	Bits 1 - 12	Digital data inputs. Bit 1 is MSB and Bit 12 is LSB.
21	LDAC	Logic input to control the loading of DATA from the input register to the DAC register. Level triggered.
22	$\overline{CE}$	Logic input to enable the chip and allow the input DATA to be loaded into the input register. Level triggered.
23	LBE	Logic input to enable the lower bits register and load the 4 least significant bits. Level triggered.
24	MBE	Logic input to enable the middle bits register and load the 4 middle significant bits. Level triggered.
25	HBE	Logic input to enable the higher bits register and load the 4 most significant bits. Level triggered.
26	VDD1	Input for the positive power supply.
27	DIGITAL GND	Digital input and power supply ground.
28	VDD2	Input for the positive power supply. VDD1 and VDD2 must be connected to the positive supply for proper operation.

MEMORY MAPPED MICROPROCESSOR INTERFACE



NOTE: 1 of 8 Decoder (4028)
Figure 1

INTERNAL CONTROL LOGIC



NOTE: The transfer from input register to DAC register can be performed without Chip Enable

Figure 2

APPLICATION HINTS

The Si8021 is a precision 12-bit multiplying DAC designed for microprocessor system interface. To insure system performance consistent with Si8021/Si8020 specifications, careful attention must be given to the following points.

- GENERAL GROUND MANAGEMENT:** AC or transient voltages between ANALOG GND and DIGITAL GND can cause noise injection into the analog output. The simplest method of ensuring that voltages at ANALOG GND and DIGITAL GND are equal is to tie them together at the DAC. When using in complex systems that have the ANALOG GND and DIGITAL GND connected on the backplane, the connection of back-to-back diodes (1N914 or equiv.) between the Si8021 ANALOG GND and DIGITAL GND pins is recommended.
- OUTPUT AMPLIFIER OFFSET:** CMOS DAC's exhibit a code dependent output resistance which in turn can cause a code dependent error voltage at the amplifier output. The maximum amplitude of this offset, the adds to the DAC nonlinearity, is 0.33 Vos (Vos is the amplifier input offset voltage). To insure monotonic operation we recommend that the Vos of the amplifier be no greater than $12 \times 10^{-6} \times (V_{ref})$ over the temperature range. See NOTE for procedure to zero the external amplifiers.
- TEMPERATURE COEFFICIENTS:** The scale factor (gain temperature coefficient, of the DAC, is 2ppm/°C maximum. This corresponds to a worst case gain shift of 0.8 LSB over a 100°C temperature change. When a resistor is used to adjust full scale range a low temperature coefficient (ie <100ppm/°C) should be used.
- HIGH FREQUENCY CONSIDERATIONS:** The output capacitance of a CMOS DAC works in conjunction with the amplifier feedback resistance to add a pole to the open loop response. This can cause ringing or oscillation. Stability can be achieved by adding a phase compensation capacitor in parallel with the feedback resistor.

STROBE LOGIC

STROBE	FUNCTION
0	Data Latched (Held)
1	Data Changing (Transfer)

All Strobes are level triggered
Figure 3

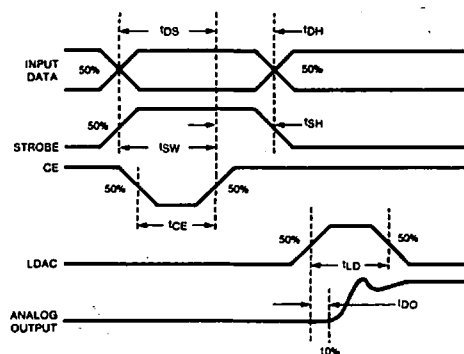
CONTROL OPERATIONS

INPUTS					OPERATION
HBE	MBE	LBE	LDAC	CE	
0	0	1	0	0	LB Data In
0	1	0	0	0	MB Data In
1	0	0	0	0	HB Data In
0	0	0	1	X	Load DAC Register
X	X	X	0	1	No Operation

X = Don't care

Table 1

TIMING DIAGRAM



*NOTE: LBE, MBE and HBE level triggered
Figure 4

TRANSFER FUNCTION (N=12)

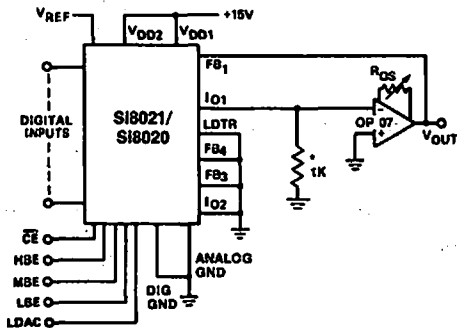
BINARY INPUT	UNIPOLAR OUTPUT	BIPOLAR OUTPUT
111 ... 111	$-V_{REF} (1 - 2^{-N})$	$-V_{REF} (1 - 2^{-(N-1)})$
100 ... 001	$-V_{REF} (1/2 + 2^{-N})$	$-V_{REF} (2^{-(N-1)})$
100 ... 000	$\frac{-V_{REF}}{2}$	0
011 ... 111	$-V_{REF} (1/2 - 2^{-N})$	$V_{REF} (2^{-(N-1)})$
000 ... 000	0	V_{REF}

Table 2

CONNECTIONS

SYMBOL	UNIPOLAR		BIPOLAR
	Binary See Fig 5	Compl Binary	Offset Binary
FB1	Output of Ext Op Amp	GND	See Figure 6 or 7
FB3	GND	Open	
FB4	GND	Output of Ext Op Amp	
LDTR	GND	GND	
IO1	Inv Input of Ext Op-Amp	GND	
IO2	GND	Inv Input of Ext Op-Amp	

Table 3

CONNECTION DIAGRAM,
UNIPOLAR OPERATION

*Add 1 k Ω and replace OP07 with very high speed op amp for 500 ns settling time to 0.01%.

Figure 6

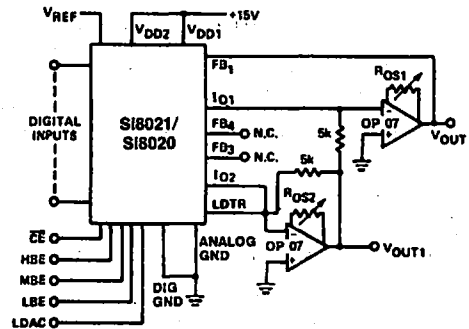
CONNECTION DIAGRAM,
BIPOLAR OPERATION

Figure 6

CONNECTION DIAGRAM,
BIPOLAR OPERATION

(for applications where bipolar offset temperature drift (~10 ppm/°C) is not critical)

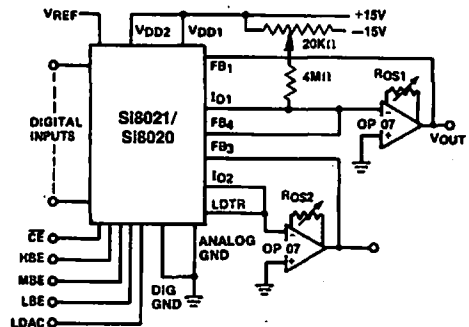


Figure 7

NOTE: To maintain specified linearity, external amplifiers must be zeroed. This is best done with VREF set to zero and,
Unipolar: load the DAC register with all bits at zero and adjust R_{OS} for $V_{OUT} = 0V$

Bipolar: load the DAC register with 10 ... 0 (MSB = 1) and set R_{OS2} for $V_{OUT} 1 = 0V$. Then set R_{OS1} for $V_{OUT} = 0V$

DG515/DG516 D/A Converter Switches



FEATURES

- Binary Weighting of ON Resistance
- 40 μ W Operating Power
- Single Supply Operation

BENEFITS

- Easily Interfaced
- Minimizes System Power Requirements
- Reduces System Cost

APPLICATIONS

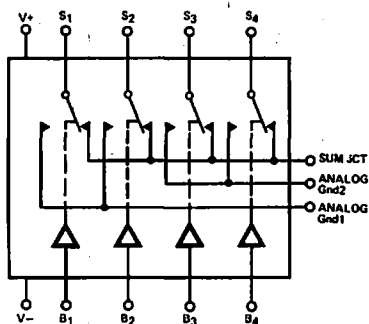
- 4, 10 or 14 Bit DAC's
- Multiplying DAC's
- Binary or BCD DAC's
- Frequency Synthesizers
- Virtual Ground Switches

DESCRIPTION

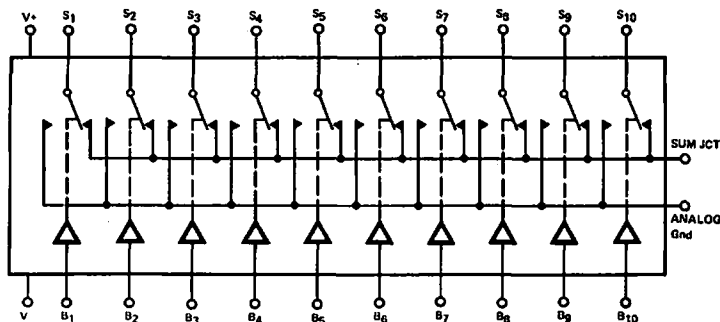
The DG515 and DG516 are 4 bit and 10 bit single-pole, double-throw switches designed specifically for building 4-bit to 14-bit binarily weighted D/A converters. These NMOS bidirectional analog switches feature binary weighted low channel ON resistance (continued from DG515 through bit 6 of DG516) to achieve monotic performance, CMOS compatible drivers, and low power consumption.

These switches are designed to steer the current output from a binary resistor ladder network to either the summing point of an operational amplifier or to ground. The DG515 is available in either the 14-lead plastic or side-braze package, while DG516 is supplied in the 28-lead Cerdip or plastic package. Both are available specified over three temperature ranges of 0 to 70°C, -25 to 85°C, and -55 to 125°C.

FUNCTIONAL BLOCK DIAGRAM



DG515

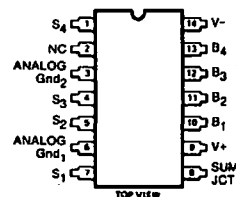


DG516

Switches Shown For Logic "1" Input

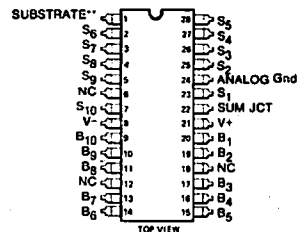
PIN CONFIGURATION

Dual In-Line Package



Order Numbers:
DG515AP or DG515BP
See Package 11
DG515CJ
See Package 7

Dual In-Line Package



Order Numbers:
DG516AR or DG516BR
See Package 13
DG516CJ
See Package 14

ABSOLUTE MAXIMUM RATINGS

V _S to Sum Jet or Analog Gnd	-200 mV
V _{IN} (Bit Logic Input)†	V- ≤ V _{IN} ≤ V+
ISWITCH	10 mA
Current (Any Terminal Except Switch)	30 mA
Storage Temperature (A & B Suffix)	-65 to 150°C
(C Suffix)	-65 to 125°C
Operating Temperature	
(A Suffix)	-55 to 125°C
(B Suffix)	-25 to 85°C
(C Suffix)	0 to 70°C
Power Dissipation (Package)*	
14 Pin Ceramic DIP**	825 mW
14 Pin Plastic DIP***	470 mW

28 Pin Ceramic DIP****	1200 mW
28 Plastic DIP****	625 mW

*Device mounted with all leads welded or soldered to PC board.

**Derate 11 mW/°C above 70°C

***Derate 6.3 mW/°C above 25°C

****Derate 10 mW/°C above 25°C

*****8.3 mW/°C above 25°C

†NOTE: Exceeding these voltage limits can result in a latch-up condition, excessive I+ and possible destruction to the device. Placing a 2 kΩ resistor in series with V+ will protect the device and allow recovery (without power supply cycling) after the overvoltage is removed.

ELECTRICAL CHARACTERISTICS¹

 $T_A = 25^\circ\text{C}$

PARAMETER		SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: V+ = 8 V, V- = 0 V	LIMITS												UNIT
				DG515A/B			DG515C			DG518A/B			DG516 C			
				MIN ²	TYP ³	MAX	MIN ²	TYP ³	MAX	MIN ²	TYP ³	MAX	MIN ²	TYP ³	MAX	
SWITCH	Switch 1	DG515	DS(on)	IS = 10 mA			6.25			7.8						
	Switch 2		DS(on)				12.5			15.6						
	Switch 3		DS(on)				25			31.2						
	Switch 4		DS(on)				50			62.5						
	Switch 1	DG516	DS(on)	IS = 1.0 mA							100			125	Ω	
	Switch 2		DS(on)						200			250				
	Switch 3		DS(on)						400			500				
	Switch 4		DS(on)						800			1000				
	Switch 5		DS(on)						1600			2000				
	Switch 6-10		DS(on)						3200			4000				
Switch To ANLG GND	JDS	VINH = 8 V, VINL = 0 V		20		20		20		20		20	%			
Switch To SUM JCT	(on)4,5															
INPUT	ANALOG Gnd (off)	ID(off)	VANALOG Gnd = 0 V, VS = -100 mV			40			40			40		40	nA	
	SUMMING Junction (off)	ID(off)	VSUMMING Jct = 0 V, VS = +100 mV	-40			-40			-40			-40			
	Threshold	VIN			4		4		4		4		4	V		
	Input Current, Input Voltage Low	IINL	VINL = 0 V	-1			-1			-1			-1		μA	
	Input Current, Input Voltage High	IINH	VINH = 8 V			1			1			1		1		
	Turn-ON Time	ton	See Switching Time Test Circuit			120			180			120			180	ns
	Turn-OFF Time	toff				170			250			170			250	
	Output Capacitance ANLG GND	CD	VINL = 0 V, f = 1 MHz		60		60			20			20		pF	
	Output Capacitance SUM JCT	CD			40		40			14			14			
	Output Capacitance ANLG GND	CD	VINH = 8 V, f = 1 MHz		40		40			14			14			
Output Capacitance SUM JCT	CD			60		60			20			20				
Positive Supply Current	I+	VINH = 8 V			5			5			5			5	μA	
Negative Supply Current	I-				-5			-5			-5					
Positive Supply Current	I+	VINL = 0 V			5			5			5			5		
Negative Supply Current	I-				-5			-5			-5					

NOTES:

1. Refer to PROCESS OPTION FLOWCHART for additional information.
2. The algebraic convention whereby the most negative value is a minimum, and the most positive is a maximum, is used in this data sheet.
3. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
4. $\Delta r_{DS(on)}$ as percent of maximum resistance.
5. This is the worst typical mismatch seen on a device.

ELECTRICAL CHARACTERISTICS¹ (Cont.)
 T_A = Over Temperature Range

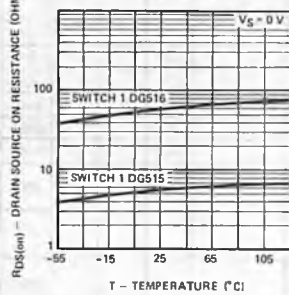
PARAMETER		SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: V+ = 8 V, V- = 0 V	LIMITS												UNIT
				DG515A/B			DG515C			DG516A/B			DG516 C			
				MIN ²	TYP ³	MAX	MIN ²	TYP ³	MAX	MIN ²	TYP ³	MAX	MIN ²	TYP ³	MAX	
SWITCH	Switch 1	DG515	rDS(on)	IS = 10 mA			9			11.2						
	Switch 2		rDS(on)				18			22.5						
	Switch 3		rDS(on)				36			45						
	Switch 4		rDS(on)				72			90						
	Switch 1	DG518	rDS(on)	IS = 1 mA								144		180		
	Switch 2		rDS(on)							288		360				
	Switch 3		rDS(on)							576		720				
	Switch 4		rDS(on)							1150		1440				
	Switch 5	rDS(on)	IS = 0.1 mA							2300		2880				
	Switch 6-10	rDS(on)							4600		5760					
	INPUT	ANALOG Gnd (off)	ID(off)	VANALOG Gnd = 0 V, VS = -100 mV									2000		2000	nA
				VANALOG Gnd = 0 V, VS = -20 mV			2000			2000						
SUMMING Junction (off)		ID(off)	VSUMMING Jct = 0 V, VS = +100 mV								2000		2000			
			VSUMMING Jct = 0 V, VS = +20 mV			2000			2000							
Input Current		INL	VINL = 0 V	-1			-1			-1			-1		μA	
Input Voltage Low																
Input Current		INH	VINH = 8 V			1			1			1		1		
Input Voltage High																
Positive Supply Current		I+	VINH = 8 V			150			150			150		150		
Negative Supply Current		I-		-150			-150			-150		-150				
Positive Supply Current		I+	VINL = 0 V			150			150			150		150		
Negative Supply Current		I-		-150			-150			-150		-150				

NOTES:

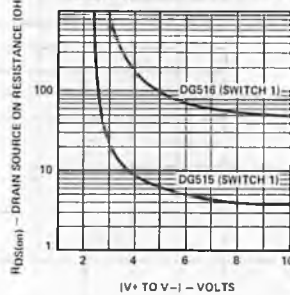
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5. This is the worst typical mismatch seen on a device.

TYPICAL CHARACTERISTICS

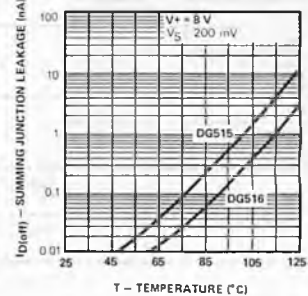
$R_{DS(on)}$ vs Temperature



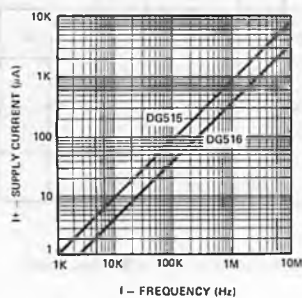
$R_{DS(on)}$ vs Supply Voltage



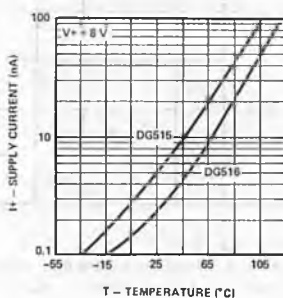
Leakage vs Temperature



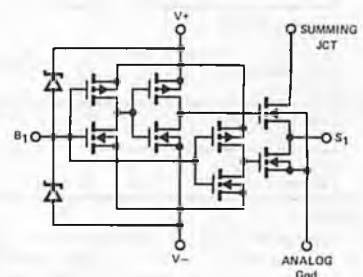
Supply Current vs Toggling Rate



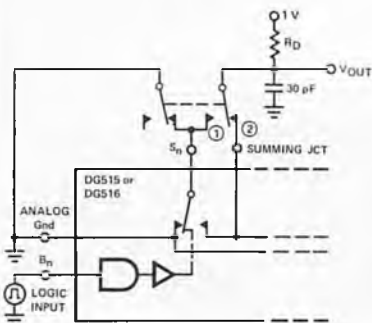
Quiescent Supply Current vs Temperature



Typical Channel (DG515 or DG516)

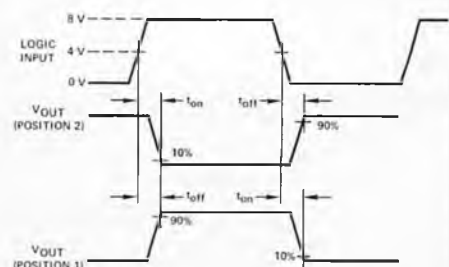


Switching Time Test Circuit



SWITCH	R_D (ohms)	
	DG515	DG516
1	50	300
2	100	300
3	200	300
4	200	510
5		510
6		1000
7		1000
8		1000
9		1000
10		1000

Switching Test Waveforms



The following Applications Circuits are intended to illustrate the following points:

1. A 2 k Ω resistor should be in series with V+ to limit supply current with negative ringing of the bit inputs.
2. Temperature compensation for R_{DS(on)} can be provided in the feedback path of the Op-Amp.
3. Bipolar reference voltages can be used in all configurations.

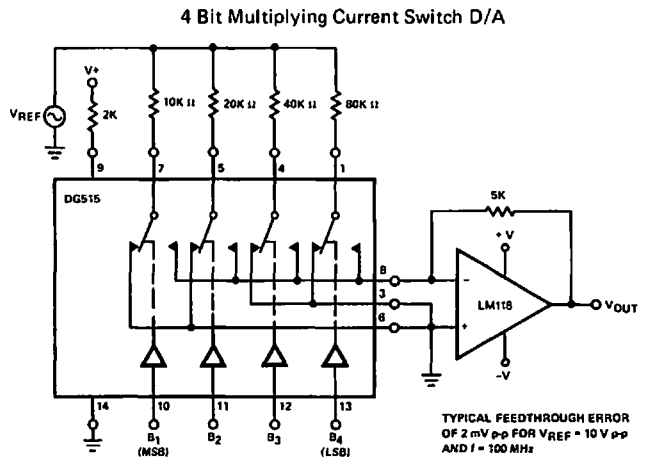


Figure 1

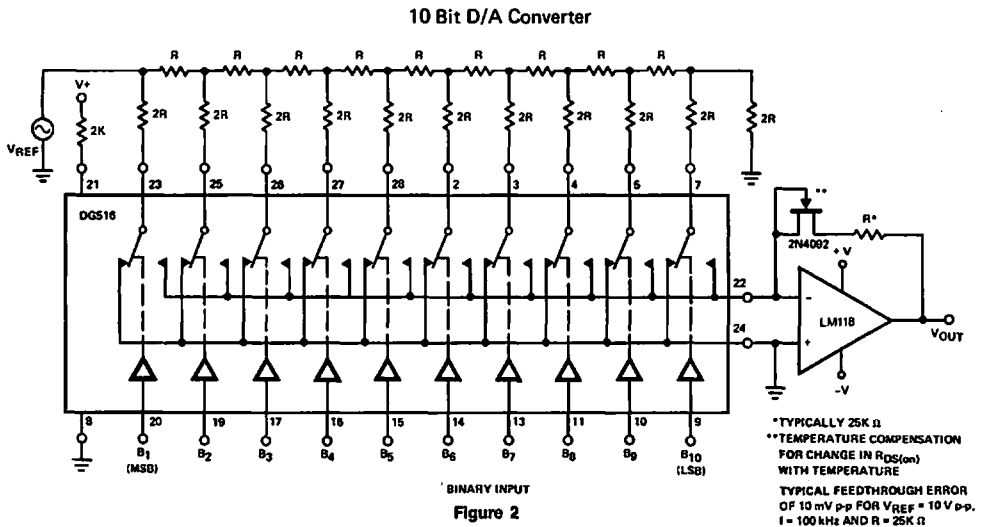


Figure 2

Unipolar Binary Operation

DIGITAL INPUT	ANALOG OUTPUT
1 1 1 1 1 1 1 1 1 1	$-V_{REF} (1 - 2^{-10})$
1 0 0 0 0 0 0 0 0 1	$-V_{REF} (1/2 + 2^{-10})$
1 0 0 0 0 0 0 0 0 0	$-V_{REF}/2$
0 1 1 1 1 1 1 1 1 1	$-V_{REF} (1/2 - 2^{-10})$
0 0 0 0 0 0 0 0 0 1	$-V_{REF} (2^{-10})$
0 0 0 0 0 0 0 0 0 0	0

Figure 3

10 Bit, 4 Quadrant Multiplying DAC (Offset Binary Coding)

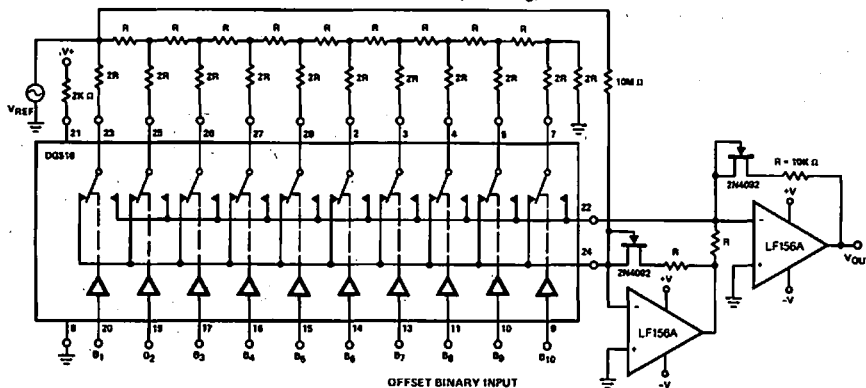


Figure 4

Bipolar (Offset Binary)* Operation

DIGITAL INPUT	ANALOG OUTPUT
1 1 1 1 1 1 1 1 1 1	$-V_{REF} (1 - 2^{-9})$
1 0 0 0 0 0 0 0 0 1	$-V_{REF} (2^{-9})$
1 0 0 0 0 0 0 0 0 0	0
0 1 1 1 1 1 1 1 1 1	$V_{REF} (2^{-9})$
0 0 0 0 0 0 0 0 0 1	$V_{REF} (1 - 2^{-9})$
0 0 0 0 0 0 0 0 0 0	V_{REF}

NOTE: 1 LSB = $2^{-9} V_{REF}$
 *Complementing B_1 (MSB) will give 2's complement coding.

Figure 5

Unipolar Binary Operation

DIGITAL INPUT	ANALOG OUTPUT
1 1 1 1 1 1 1 1 1 1 1 1	$-V_{REF} (1 - 2^{-14})$
1 0 0 0 0 0 0 0 0 0 0 0 1	$-V_{REF} (1/2 + 2^{-14})$
1 0 0 0 0 0 0 0 0 0 0 0 0	$-V_{REF}/2$
0 1 1 1 1 1 1 1 1 1 1 1	$-V_{REF} (1/2 - 2^{-14})$
0 0 0 0 0 0 0 0 0 0 0 0 1	$-V_{REF} (2^{-14})$
0 0 0 0 0 0 0 0 0 0 0 0 0	0

Figure 6

14 Bit Binary DAC (unipolar)

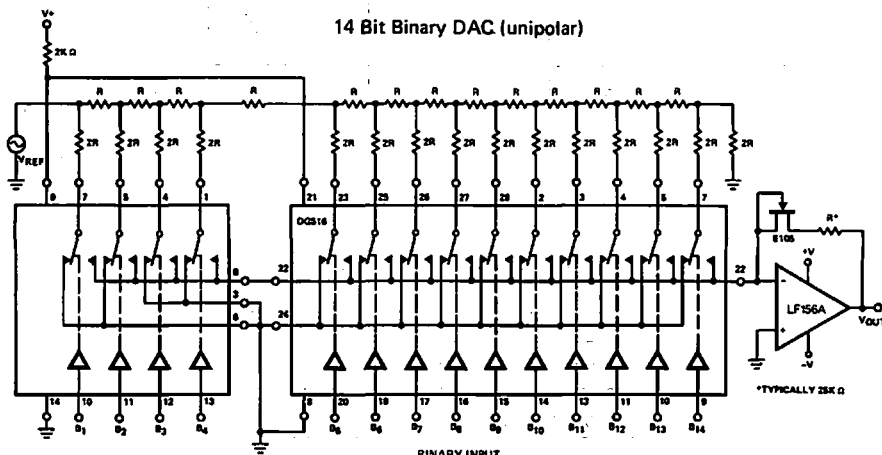


Figure 7

0	Introduction
1	Interface
2	Analog Switches/Multiplexers
3	A/D Converters
4	D/A Converters
5	Linear
6	Power Conversion
7	Telecommunications
8	Die Process & Topography
9	Package Data
10	Applications Information
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Index

LINEAR

Title	Page
Introduction	5-3
L144	5-5
L161	5-9
SI8901	5-19

Linear Product Selector Guide¹

Function	Part No. Package Information	Specifications	Features
Triple Op Amp	L144 14-pin plastic, ceramic, flat-pack	± 1.5 to ± 18 V supply Programmable supply current Internally compensated 0.4V/ μ s slew rate	80dB gain with 20k load Drives large capacitive loads ± 30 V differential input Monolithic construction
Quad Comparator	L161 16-pin plastic, ceramic, flat-pack	± 1.5 to ± 18 V supply Single supply operation Programmable supply current	Gain greater than 20V/mV Sensing near ground ± 30 V differential input CMOS Logic compatible
Ring Demodulator/ Balanced Mixer	SI8901² 8-pin metal can	+35 dB third order intercept point -55 dB input port isolation	Low ON resistance (50 ohms max.) Low Node Capacitances (7 pF max.) Very low power loss (<8dB)

INTRODUCTION

Operational Amplifiers

An operational amplifier is an open loop gain block that provides controlled amounts of gain and/or signal shaping when used in negative feedback circuits. Siliconix Bipolar-PMOS process was used to develop the L144, a triple operational amplifier that features micropower consumption for portable (battery powered) applications. The user can set the basic performance characteristics, bias current, slew rate and power supply consumption, with a single resistor.

Comparators

A comparator provides a logic output which indicates the amplitude relationship between two signals. The L161 is a quad comparator which was developed for micropower applications in cross-over detectors, pulse generators, DC to DC converters, or wherever comparator type action is required. Built on the Siliconix Bipolar-PMOS process, the user can program the basic operating conditions (input current, slew rate and power supply current) with a single resistor.

Ring Demodulator/Balanced Mixer

A ring of closely-matched MOSFETs may be used in a number of circumstances where it is necessary to mix, modulate, multiply or compare two RF signals. As a balanced mixer for example, the close approximation to square-law response available with MOSFETs minimizes harmonic distortion, while the essentially capacitive gates consume much less local oscillator power than is the case with other balanced mixers. As a multiplier, the low noise floor and high 1 dB compression point allow an exceptionally wide range of signals to be processed. As a modulator, the close matching of the four devices minimizes distortion and spurious harmonic products. In any application, the use of active devices minimizes losses through the stage, and in some cases allows actual gain to be achieved, thus increasing system efficiency. The S18901 is a quad MOS switch that has been configured as a ring demodulator.

DEFINITION OF TERMS

Common Mode Error Voltage (CMEV)

An operational amplifier (and differential input comparator) is designed to respond only to signals appearing between its input terminals and not to those in common with both. If the output error voltage, due to a known magnitude of common mode voltage (CMV), is referred to the input (by dividing by the closed loop gain), it reflects the equivalent input signal required to generate that output, and is thus called Common-Mode-Voltage-Error.

Common-Mode Range (CMR)

CMR is defined as the range of common mode voltage on the input terminals for which operation within specifications is assured.

Common-Mode Rejection Ratio (CMRR)

While CMRR is defined as the ratio of common-mode voltage (CMV) to Common Mode Error Voltage (CMEV), it is complicated by the fact that it is highly non-linear, and is also a function of frequency and temperature. Siliconix measures CMRR at DC and at the specified CMV limits, unless otherwise noted.

DC Open Loop Voltage Gain (A_{VOL})

Open loop gain is specified as the ratio of the change in output voltage (over a specified range) to the change in the differential input voltage producing it. As this parameter is very much frequency dependent, open loop gain is specified at DC and a typical open loop response curve is given for each type in the data sheet.

Input Bias Current (I_{BIAS})

Bias current is the input current required at either input terminal to drive the output to zero (assumes zero input voltage). Siliconix specifies the maximum value at either input terminal. Variations with temperature and supply voltage are specified separately.

Input Offset Current (I_{OS})

Offset current is defined as the difference between the currents into the two input terminals when the output is at zero volts.

Input Offset Voltage (V_{OS})

The input offset voltage is the DC input voltage required to provide zero voltage at the output of the amplifier when the input signal and input bias currents are at zero. The power supply and temperature dependent terms are specified separately.

Power-Supply Rejection Ratio (PSRR)

PSRR is the inverse ratio of the change in input offset voltage to the change in power supply voltage producing it. PSRR is specified in dB or V/V.

Response Time (t_r)

The interval between the application of an input step function and the time when the output crosses the logic threshold voltage. Logic threshold is defined as the voltage at the output of the comparator at which the loading logic circuitry changes its digital state, or, as 1.4 V when the loading logic circuitry is not used.

Slew Rate (S_r)

The maximum rate of change in the output voltage when supplying the rated output.

Unity Gain (Small-Signal) Bandwidth

Defined as the frequency at which the open-loop response becomes unity. It is specified for small signals as slew rate limits the frequency at which full output voltage swing can be obtained.

L144

Low-Power Triple Operational Amplifier



FEATURES

- 3 Amplifiers in One Package
- Programmable Supply Current
- Operates From ± 1.5 to ± 15 V
- Drives Large Capacitive Loads (< 1000 pF)
- Continuous Short Circuit Protection

BENEFITS

- Low Cost and Compact
- Easily Tailored to Optimize Circuit Performance
- Very Rugged

APPLICATIONS

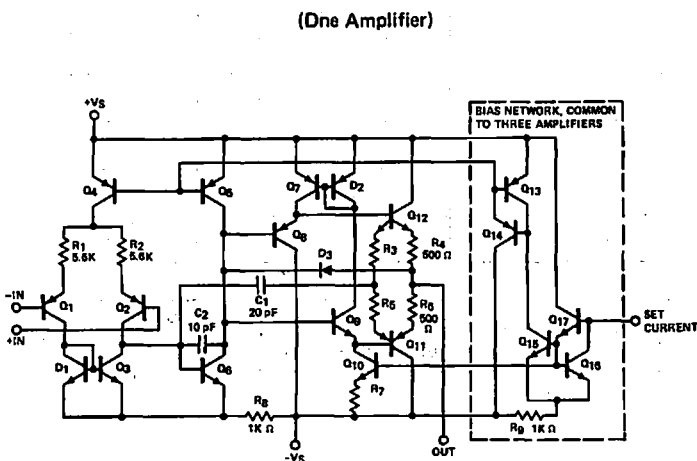
- Instrumentation Amplifiers
- Buffer Amplifiers
- Voltage Comparators
- Low-Drift Sample and Hold Circuits
- Active Filters
- Battery-Powered Circuits

DESCRIPTION

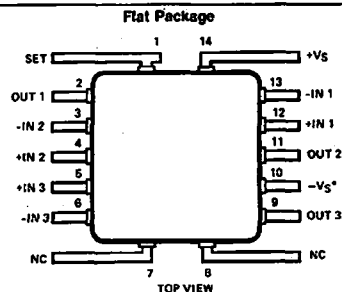
The Siliconix L144 is a low cost triple operational amplifier designed for general purpose applications where low-power is a primary consideration. Features include operation with supply voltages as low as ± 1.5 VDC, programmable supply current (with single resistor), and internal compensation to insure stability under all conditions of resistive feedback.

L144 will drive capacitive loads to 1000 pF and is short circuit protected. Package options include the popular 14 pin side braze and plastic DIP, and the flat pack. The L144A is specified for operation from -55°C to $+125^{\circ}\text{C}$, the L144B for -20°C to $+85^{\circ}\text{C}$, and the L144C for 0°C to $+70^{\circ}\text{C}$.

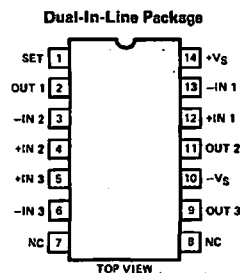
FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



*COMMON TO SUBSTRATE AND BASE OF PACKAGE
Order Numbers: L144AL or L144BL
See Package 5



Order Numbers: L144AP or L144BP
See Package 11
L144CJ
See Package 7

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	± 18 V
Differential Input Voltage	± 30 V
Input Voltage* (A Suffix)	± 18 V
(C Suffix)	± 15 V
Output Short Circuit Duration**	Indefinite
Operating Temperature (A Suffix)	-55 to 125°C
(B Suffix)	-25 to 85°C
(C Suffix)	0 to 70°C
Storage Temperature (A and B Suffix) ...	-65 to 150°C
(C Suffix)	-65 to 125°C
Lead Temperature (Soldering 60 Sec)	300°C
Power Dissipation (Package)***	

Flat Package	750 mW
14 Pin Ceramic DIP	825 mW
Plastic DIP	470 mW

*For supply voltages $< \pm 18$ V, maximum input voltage is equal to the supply voltage.

**Continuous short circuit is allowed for case temperatures to +125°C and ambient temperature to +70°C.

***All Leads welded or soldered to P.C. board. Derate 10 mW/°C for the flat package, 11 mW/°C for the 14 pin DIP above +75°C and 6.3 mW/°C above 25°C for the plastic DIP.

ELECTRICAL CHARACTERISTICS¹ $T_A = 25^\circ\text{C}$

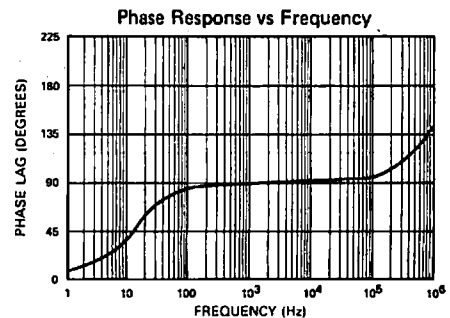
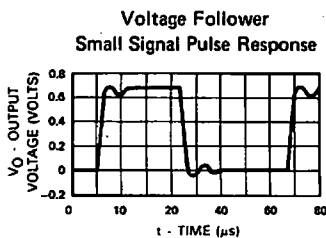
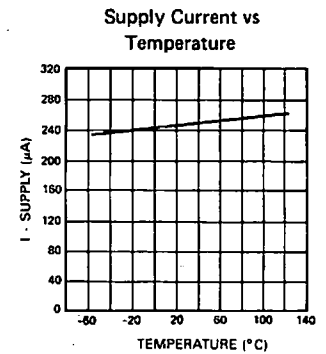
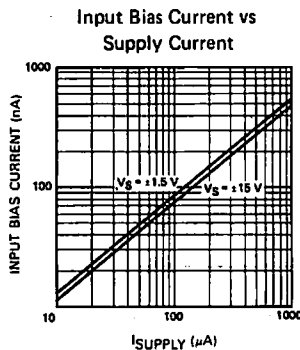
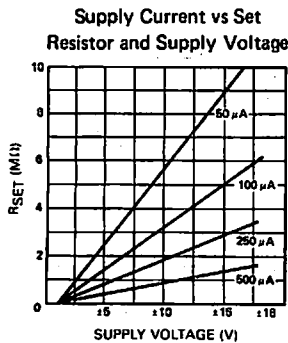
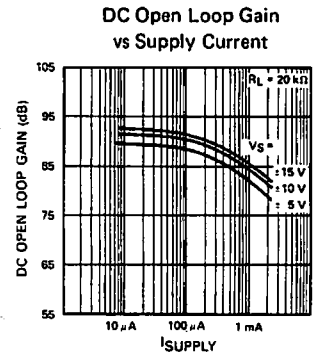
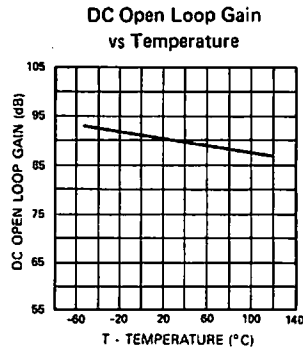
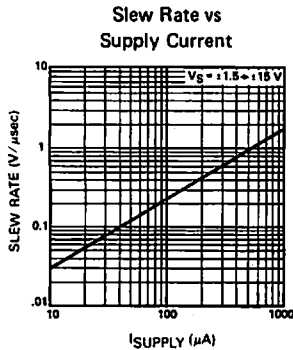
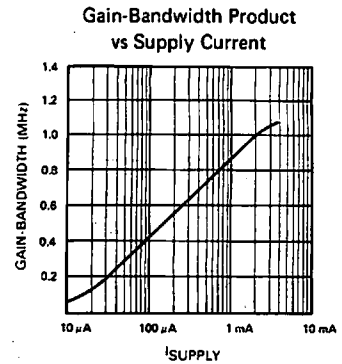
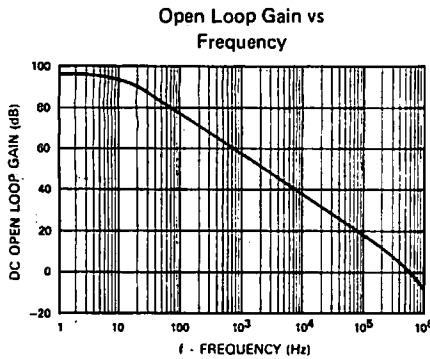
	PARAMETER	SYMBOL	TEST CONDITIONS ² UNLESS OTHERWISE NOTED: $V_S = \pm 15$ V, $R_L = 50$ k Ω , $R_{SET} = 3$ Ω (Pin 1 to 14)	A/B SUFFIX			C SUFFIX			UNIT
				MIN ³	TYP ⁴	MAX	MIN ³	TYP ⁴	MAX	
INPUT	Input Offset Voltage	V_{OS}	$R_S \leq 50$ k Ω		1	5		1	10	mV
	Average Temperature Coefficient Of Input Offset Voltage	dV_{OS}/dt			3.3			3.3		$\mu\text{V}/^\circ\text{C}$
	Input Offset Current	I_{OS}			2	50		5	70	nA
	Input Bias Current	I_{BIAS}		-200	-100		-250	-125		
OUTPUT	Output Voltage Swing	V_{OUT}		10	± 14	-10	10	± 14	-10	V
	Output Voltage Swing	V_{OUT}	$V_S = \pm 15$ V, $R_{SET} = 120$ k Ω		± 0.5			± 0.4		
	Output Short Circuit Current	I_{SC}	$R_L = 0$		1.5	15		1.5	15	mA
DYNAMIC	DC Open Loop Voltage Gain	A_{VOL}		3	30		1	30		V/mV
	Slew Rate	S_r			0.4			0.4		V/ μs
	Unity Gain Bandwidth				0.6			0.6		MHz
	Crosstalk		$f = 100$ Hz		-100			-100		
	Common Mode Rejection Ratio	CMRR	$V_{IN} = \pm 12$ V	80	90		70	80		dB
SUPPLY	Power Supply Rejection Ratio	PSRR		80	90		80	90		
	Source Current	I_S	Unity Gain $V_{IN} = 0$ On All Amps			350			400	μA

 $T_A = \text{Over Temperature Range}$

	PARAMETER	SYMBOL	TEST CONDITIONS ² UNLESS OTHERWISE NOTED: $V_S = \pm 15$ V, $R_L = 50$ k Ω , $R_{SET} = 3$ Ω (Pin 1 to 14)	A/B SUFFIX			C SUFFIX			UNIT
				MIN ³	TYP ⁴	MAX	MIN ³	TYP ⁴	MAX	
INPUT	Input Offset Voltage	V_{OS}	$R_S \leq 50$ k Ω			6				mV
	Input Bias Current	I_{BIAS}		-200			-250			nA
DYNAMIC	DC Open Loop Voltage Gain	A_{VOL}		3	30		1	30		V/mV

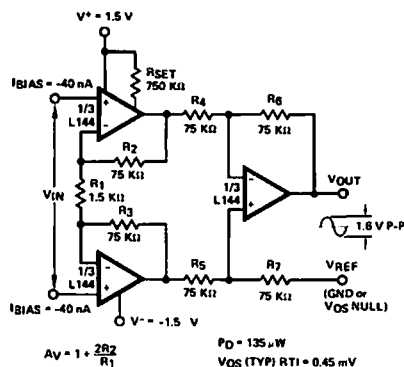
NOTES:

1. All DC parameters are 100% tested at 25°C. Lots are sample-tested for AC parameters and high and low temperature limits to assure conformance with specifications.
2. I_{SET} is adjustable. See typical characteristics.
3. The algebraic convention whereby the most negative value is a minimum, and the most positive value is a maximum, is used in this data sheet.
4. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

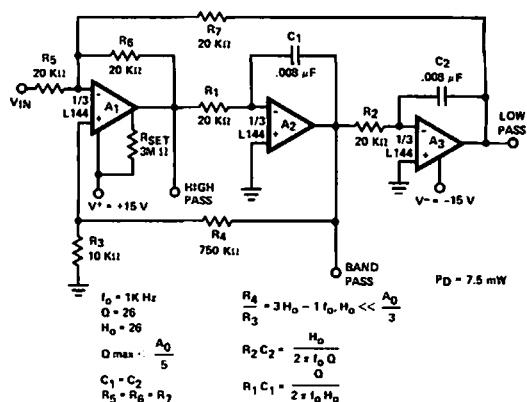


APPLICATIONS

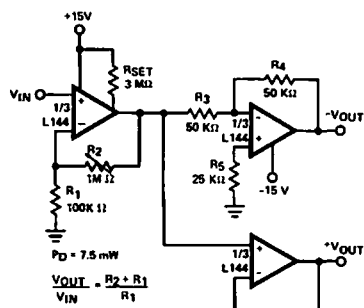
Instrumentation Amplifier



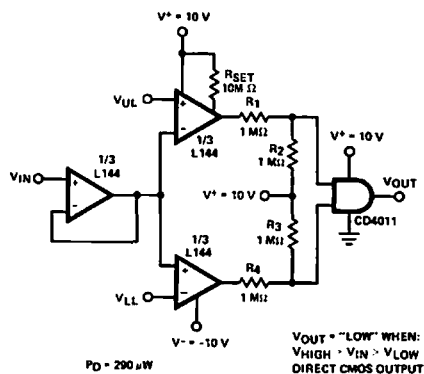
Active Filter



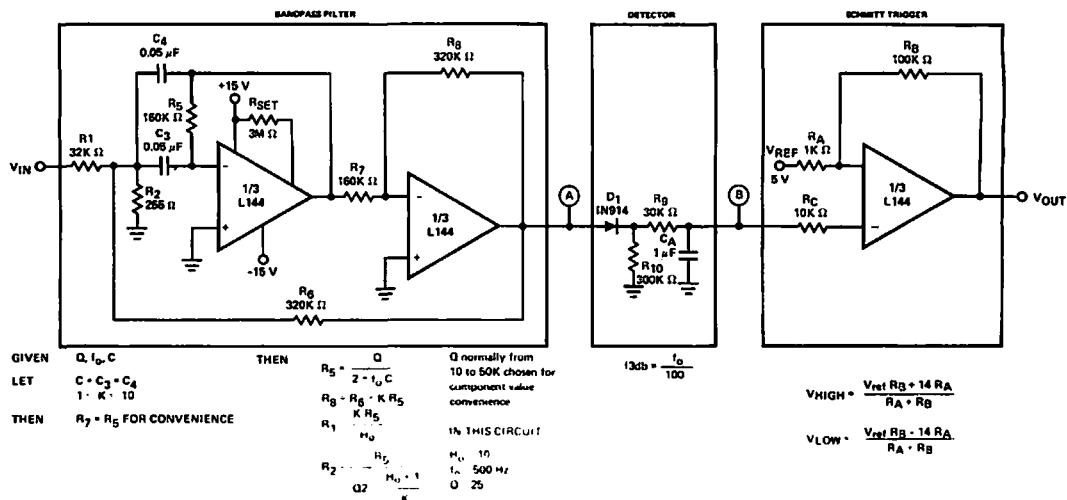
Precision Phase Splitter



Double-Ended Limit Comparator



500 Hz Tone Detector



L161

Micropower Quad Comparator



FEATURES

- Programmable Output Drive Capability
- Direct CMOS Logic Compatibility
- Low Power
- Direct Wire-OR of Output
- Input Sensing Near Ground

BENEFITS

- Minimizes System Power Requirements
- Reduces External Component Requirements
- Easily Tailored To Your System
- Minimizes Number of Supply Voltages in Your Systems

APPLICATIONS

- Voltage Comparators
- Window Comparators
- Level Detectors
- CMOS Line Receivers
- Oscillators
- Ramp Generators
- Phase Comparators
- Battery-Powered Circuits

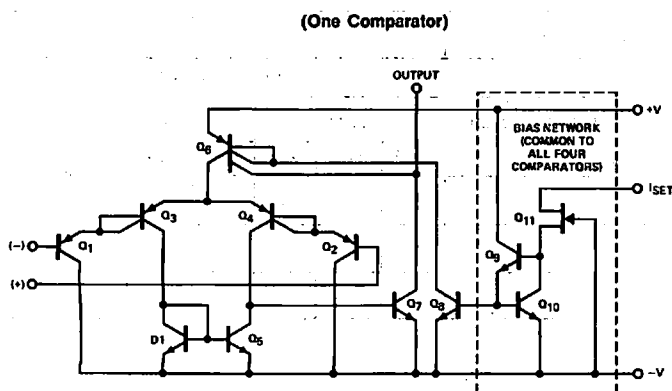
DESCRIPTION

The L161 is a monolithic quad comparator featuring direct control of both its DC and AC parameters with a single resistor. Operation at very small supply current and power dissipation (typically in the microwatt region) make possible battery operation; and the outputs can be hard wire OR'd for such unique applications as the double

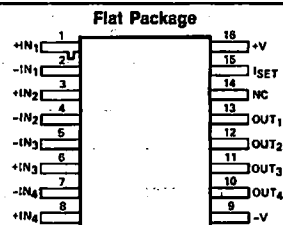
ended limit detector (see applications notes.)

L161 is available in the 16-pin plastic DIP for 0 to 70°C operation, the 16 lead side-braze for -25 to 85°C and -55 to 125°C operation, and the flat pack for -55 to 125°C applications.

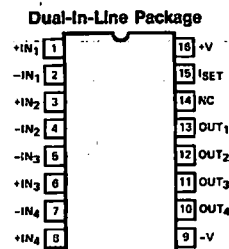
FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



TOP VIEW
Order Number:
L161AL
See Package 17



TOP VIEW
Order Numbers:
L161AP or L161BP
See Package 12
L161CJ
See Package 8

ABSOLUTE MAXIMUM RATINGS

Supply Voltage ± 18 V
 Differential Input Voltage ± 30 V
 Input Voltage* (A Suffix) ± 18 V
 (B Suffix) ± 18 V
 Output Short Circuit Duration** Indefinite
 Operating Temperature (A Suffix) -55 to $+125^{\circ}\text{C}$
 (B Suffix) -25 to 85°C
 (C Suffix) 0 to $+70^{\circ}\text{C}$
 Storage Temperature (A and B Suffix) -65 to 150°C
 (C Suffix) -65 to 125°C
 Power Dissipation (Package)***

Flat Package 750 mW

16 Pin DIP (Side Braze) 900 mW

16 Pin Plastic DIP 470 mW

*For supply voltages $< \pm 18$ V, maximum input voltage is equal to the supply voltage.

**Continuous short circuit current is allowed for case temperature to $+125^{\circ}\text{C}$ and ambient temperature to $+70^{\circ}\text{C}$.

***All Leads welded or soldered to P.C. board. Derate 10 mW/ $^{\circ}\text{C}$ above 75°C for the flat package, 12 mW/ $^{\circ}\text{C}$ above 75°C for the side braze DIP and 6.3 mW/ $^{\circ}\text{C}$ above 25°C for the plastic DIP.

LOW POWER ELECTRICAL CHARACTERISTICS¹

$T_A = 25^{\circ}\text{C}$

	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: $V_S = \pm 3$ V, $I_{SET} = 10$ μA , $R_L = 10$ M Ω , $C_L = 10$ pF	L161A			L161B/C			UNIT
				MIN ²	TYP ³	MAX	MIN ²	TYP ³	MAX	
INPUT	Input Offset Voltage	V_{OS}			1	3		1	6	mV
	Input Offset Current	I_{OS}			1	20		1	25	nA
	Input Bias Current	I_{BT}			20	100		20	200	
OUTPUT	DC Open Loop Voltage Gain	A_{VOL}		20	30		10	30		V/mV
	Low Output Voltage ⁴	V_{OL}	$R_L = 20$ k Ω		-2.95	-2.6		-2.95	-2.6	V
	High Output Voltage ⁴	V_{OH}	$R_L = 200$ k Ω	2.5	2.9		2.5	2.9		
DYNAMIC	Common Mode Range	CMR			+1.3/-3			+1.3/-3		
	Response Time	t	100 mV Overdrive, $C_L = 10$ pF		5			5		μs
	Common Mode Rejection Time	CMRR	$V_{IN} = \text{CMR}$	75	90		75	90		dB
SUPPLY	Power Supply Rejection Ratio	PSRR		65	80		65	80		
	Supply Current	I_S	All Inputs Grounded, $R_L = \infty$		210	300		210	300	μA

$T_A = \text{Over Temperature Range}$

	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: $V_S = \pm 3$ V, $I_{SET} = 10$ μA , $R_L = 10$ M Ω , $C_L = 10$ pF	L161A			L161B/C			UNIT
				MIN ²	TYP ³	MAX	MIN ²	TYP ³	MAX	
	Input Offset Voltage	V_{OS}				5				mV
	DC Open Loop Voltage Gain	A_{VOL}		10			5			V/mV
	Supply Current	I_S	All Inputs Grounded, $R_L = \infty$			350			350	μA

NOTES:

1. Refer to PROCESS OPTION FLOWCHART for additional information.
2. The algebraic convention whereby the most negative value is a minimum, and the most positive is a maximum, is used in this data sheet.
3. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
4. The output current drive of the L161 is non-symmetrical. This facilitates the wire-ORing of two comparator outputs. The output pull-down current capability is typically 75-150 times the pull-up current.

HIGH POWER ELECTRICAL CHARACTERISTICS

 $T_A = 25^\circ\text{C}$

	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: $V_S = \pm 15\text{ V}$, $I_{SET} = 100\text{ }\mu\text{A}$, $R_L = 2\text{ M}\Omega$, $C_L = 10\text{ pF}$	L161A			L161B/C			UNIT
				MIN ²	TYP ³	MAX	MIN ²	TYP ³	MAX	
INPUT	Input Offset Voltage	V_{OS}			1.5	3		1.5	6	mV
	Input Offset Current	I_{OS}			5	60		5	90	nA
	Input Bias Current	I_{BT}			100	400		100	800	
OUTPUT	DC Open Loop Voltage Gain	A_{VOL}		50	100		30	100		V/mV
	Low Output Voltage ⁴	V_{OL}	$R_L = 20\text{ k}\Omega$		-14.9	-14.6		-14.9	-14.6	V
	High Output Voltage ⁴	V_{OH}	$R_L = 200\text{ k}\Omega$	14.5	14.9		14.5	14.9		
DYNAMIC	Common Mode Range	CMR			+13/-15			+13/-15		
	Response Time	t	100 mV Overdrive, $C_L = 10\text{ pF}$		1			1		μs
	Common Mode Rejection Time	CMRR	$V_{IN} = \text{CMR}$	75	90		75	90		dB
SUPPLY	Power Supply Rejection Ratio	PSRR		65	80		65	80		
	Supply Current	I_S	All Inputs Grounded, $R_L = \infty$		2100	3500		2100	3500	μA

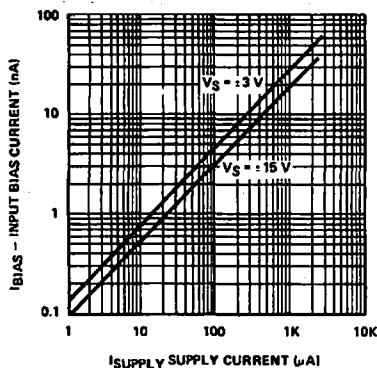
 $T_A = \text{Over Temperature Range}$

	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: $V_S = \pm 15\text{ V}$, $I_{SET} = 100\text{ }\mu\text{A}$, $R_L = 2\text{ M}\Omega$, $C_L = 10\text{ pF}$	L161A			L161B/C			UNIT
				MIN ²	TYP ³	MAX	MIN ²	TYP ³	MAX	
	Input Offset Voltage	V_{OS}				6				mV
	Input Bias Current	I_{BT}				500				nA
	DC Open Loop Voltage Gain	A_{VOL}		25			15			V/mV
	Supply Current	I_S	All Inputs Grounded, $R_L = \infty$			4000			4000	μA

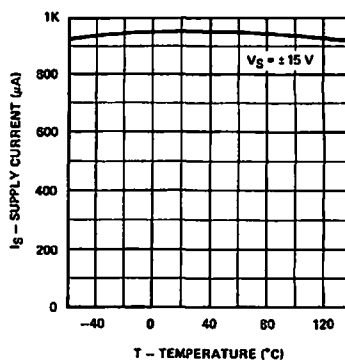
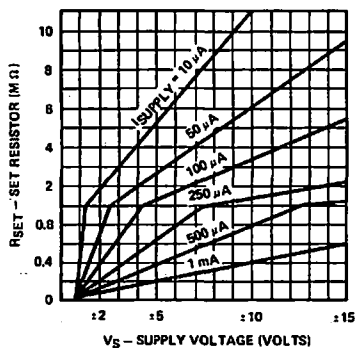
NOTES:

1. Refer to PROCESS OPTION FLOWCHART for additional information.
2. The algebraic convention whereby the most negative value is a minimum, and the most positive is a maximum, is used in this data sheet.
3. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
4. Set current (I_{SET}) and supply current (I_{SUPPLY}) can be determined by the following formulas: $I_{SET} = \frac{[(+V) - (2V_{BE}) - (-V)]}{R_{SET}}$; $I_{SUPPLY} = 21 \times I_{SET}$

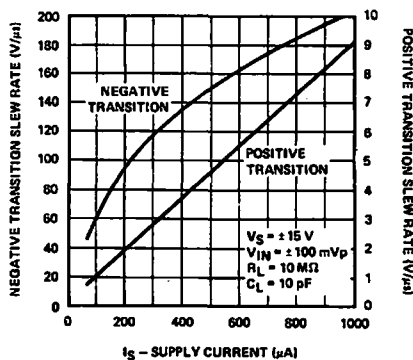
Input Bias Current vs Supply Current



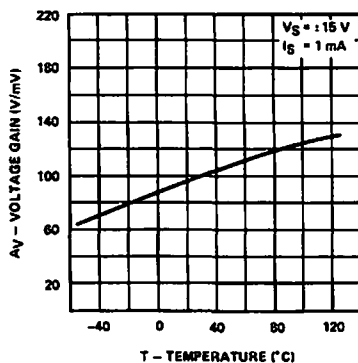
Supply Current vs Temperature

R_{SET} vs V_{SUPPLY} for Various SUPPLIES

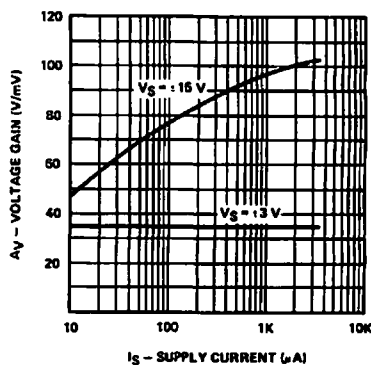
Slew Rate vs Supply Current



Voltage Gain vs Temperature

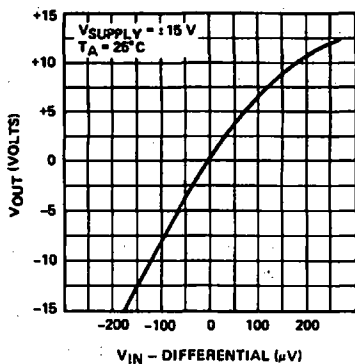
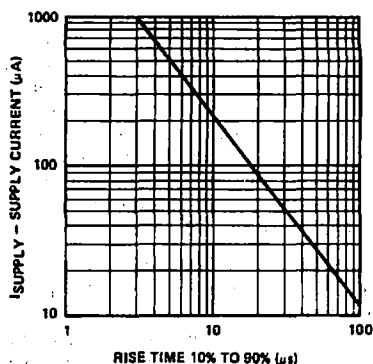
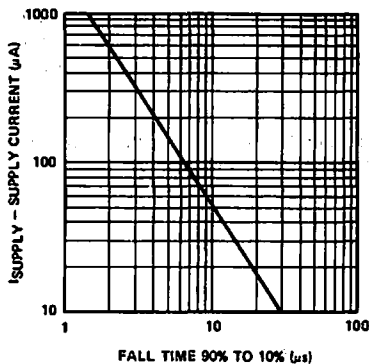
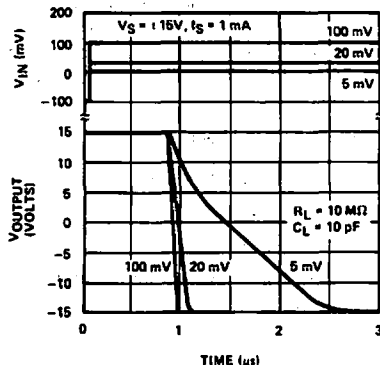
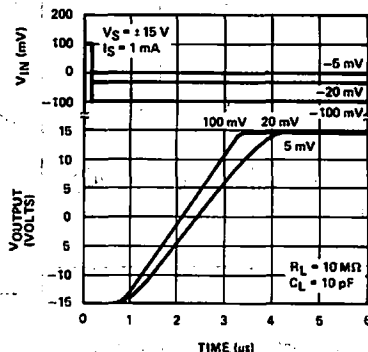


Voltage Gain vs Supply Current



NOTE:

The output current drive of each comparator in the L161 is non-symmetrical. The pull-up current is typically 2 [V₊ - (-V₋)/R_{SET}] and the pull-down current capability is typically from 75 to 150 times the pull-up current.

TYPICAL CHARACTERISTICS (Cont.)
 $(T_A = 25^\circ\text{C}, V_{\text{SUPPLY}} = \pm 15\text{ V unless otherwise noted})$
Transfer Characteristic

Rise Time vs Supply Current with One CMOS Load

Fall Time vs Supply Current with One CMOS Load

Response Time vs Input Overdrive Negative Transition

Response Time vs Input Overdrive Positive Transition

NOTE:

The output current drive of each comparator in the L161 is non-symmetrical. The pull-up current is typically $2(V_+ - 1 - (V_-)/R_{\text{SET}})$ and the pull-down current capability is typically from 75 to 150 times the pull-up current.

APPLICATIONS

DESCRIPTION

The L161 is a monolithic quad micropower comparator with an external control for varying its AC and DC characteristics. The variation of a single programming resistor will simultaneously alter parameters such as supply current, input bias current, slew rate, output drive capability, and gain. By making this resistor large, operation at very small supply current levels and power dissipations — typically in the low microwatt region — is possible. The L161 is therefore ideal for systems requiring minimum power drain, such as battery-powered instrumentation, aerospace systems, CMOS designs, and remote security systems.

The L161 is fabricated using standard bipolar processing. The circuit (Figure 1) is composed of five major blocks — four comparators and a common bias network. $Q_1 - Q_8$ and D_1 form a darlington differential amplifier with double-to-single ended conversion. Q_8 is a dual current source whose outputs are exactly twice the current flowing through Q_8 . The collector current of Q_8 is a function of the current supplied externally to $Q_9 - Q_{10}$, which in turn is known as the set current or I_{SET} . This set current is established by a resistor connected between the I_{SET} terminal and a voltage source, most commonly the positive supply. Q_{11} prevents excessive current from flowing through Q_9 and Q_{10} in the event the I_{SET} terminal is shorted to the positive supply; it has no effect on circuit operation under normal conditions.

SETTING THE SET CURRENT

The set current can be expressed as:

$$I_{SET} = \frac{[(+V) - (2 V_{BE}) - (-V)]}{R_{SET}} \quad (1)$$

where +V is the voltage to which the control resistor is

connected, -V is the negative supply voltage, V_{BE} is the base emitter drop of Q_9 or Q_{10} (about 0.7 V), and R_{SET} is the value of the external control resistor or set resistor. Equation 1 is simply a derivative of ohms law. There is also an analytical relationship between I_{SET} and the total supply current:

$$\begin{aligned} I_{SUPPLY} &= [I_{SET} \text{ (current sourced by } Q_6 \text{ to } Q_8) \\ &\quad + 2 I_{SET} \text{ (current sourced to the differential} \\ &\quad \text{amplifier by } Q_6) \\ &\quad + 2 I_{SET} \text{ (current sourced to the comparator} \\ &\quad \text{output by } Q_6)] \\ &\quad \times 4 \text{ (the total numbers of comparators)} \\ &\quad + I_{SET} \text{ (current sourced through } Q_{11}, Q_{10}, \\ &\quad \text{and } Q_9 \text{ to } -V) \\ &= [I_{SET} + 2 I_{SET} + 2 I_{SET}] \times 4 + I_{SET} \\ &= 21 I_{SET} \end{aligned}$$

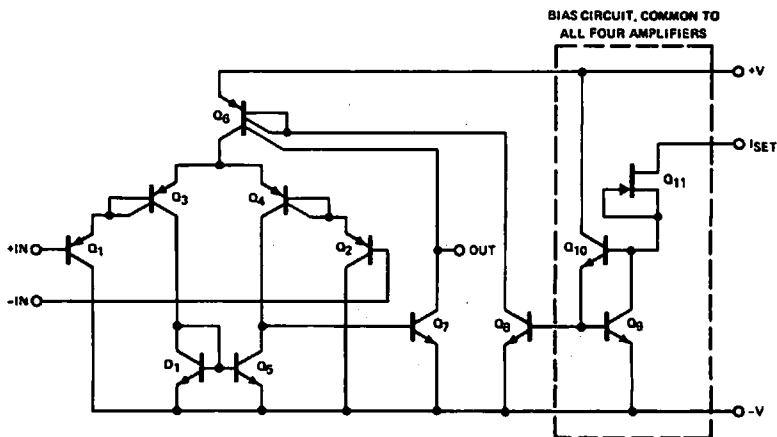
The output current pulldown capability (I_{OL}) of the L161 is about 2 orders of magnitude greater than the high output drive current, (I_{OH}), which allows wire-ORing the outputs. I_{OH} is simply the current sourced by Q_6 :

$$I_{OH} = 2 \times I_{SET} \quad (3)$$

I_{OL} is found by multiplying the current sourced by the collector of Q_6 by the gain Q_7 :

$$I_{OL} = \beta(Q_7) \times 2 I_{SET} \quad (4)$$

The beta of Q_7 is about 75-150.

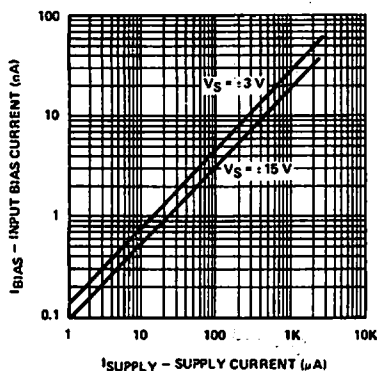


Schematic of One Channel of the L161
Plus the Common Bias Network
Figure 1

APPLICATIONS (Cont.)

INPUT BIAS CURRENT

Input bias current is a function of the betas of input devices Q_1 - Q_2 and I_{SET} . This is difficult to express analytically because β varies greatly with both processing and collector current; however it is roughly proportional to the set current and can easily be determined experimentally (see Figure 2).



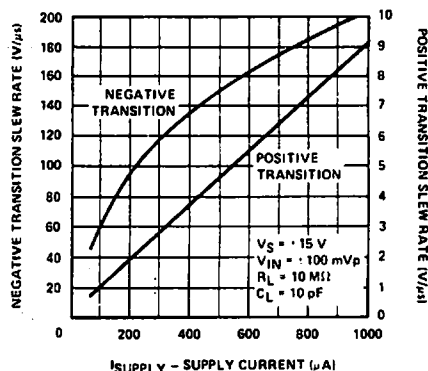
Input Bias Current vs Supply Current
Figure 2

GAIN

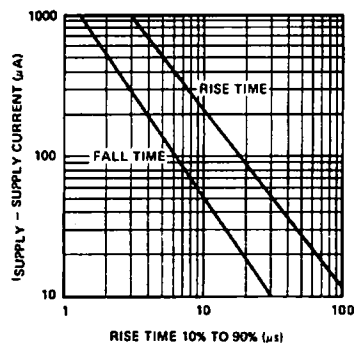
Gain varies logarithmically with changes in supply voltage and linearly with changes in set current. Primary causes are the decrease in output impedance of Q_7 with decreasing supply voltage and an increase in transistor betas with increasing set current. Other AC parameters such as slew rate and transition time are also effected by set current; however, current dependent parameters such as beta and chip capacitances make mathematical expressions imprecise. These relationships have been determined empirically and are presented in Figure 3 and 4.

The designer's ability to program the key parameters of the L161 enables him to program just enough supply current to meet his design objectives. This coupled with the L161's performance using only microwatts of power makes it

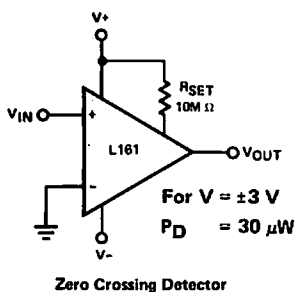
ideal for any micropower or battery-powered system, as well as a replacement for existing higher power comparators. The following applications illustrate the flexibility and unique capabilities of the L161.



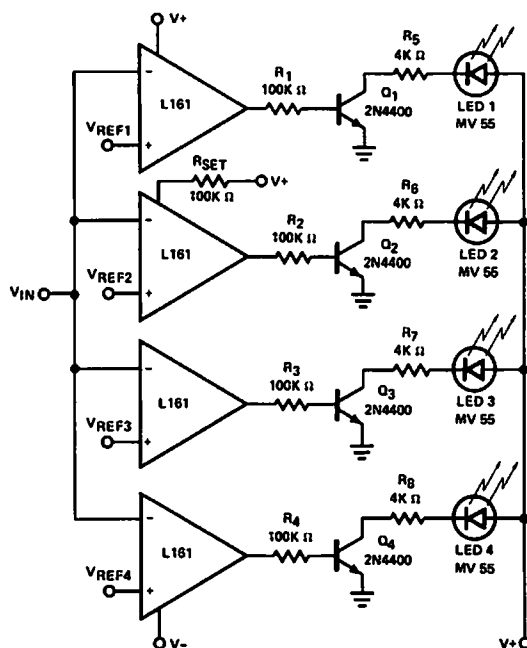
Slew Rate vs Supply Current
Figure 3



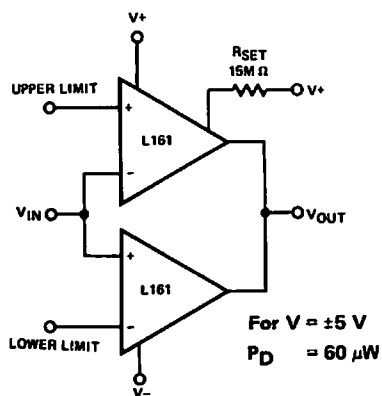
Rise and Fall Times vs Supply Current
With One CMOS Load
Figure 4



APPLICATIONS (Cont.)

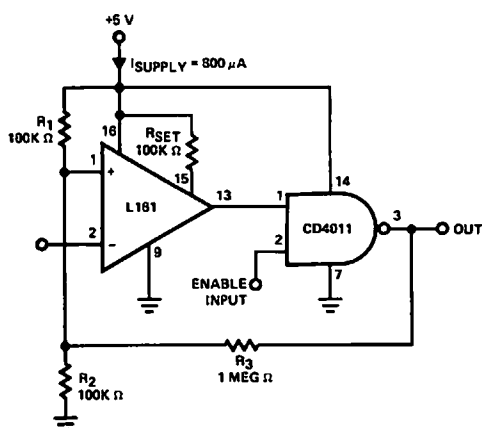


Voltage Level Detector



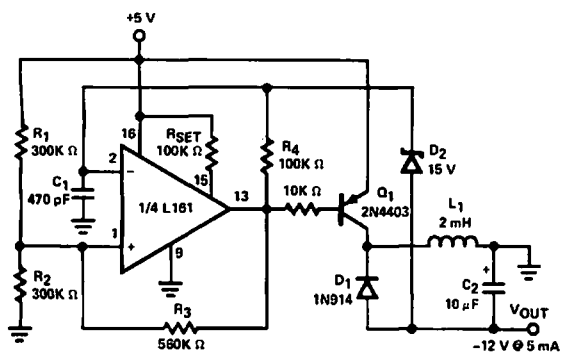
Double Ended Limit Detector

For $V = \pm 5\text{ V}$
 $P_D = 60\ \mu\text{W}$

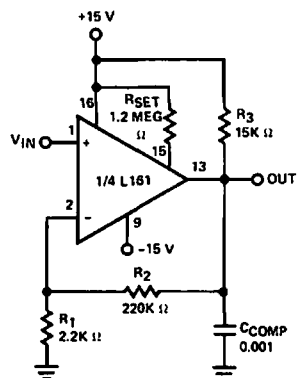


CMOS Line Receiver

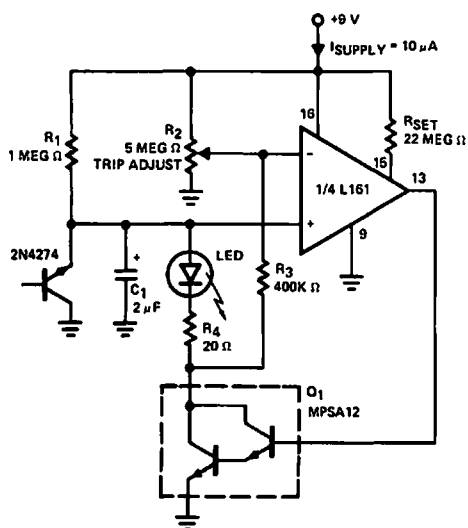
APPLICATIONS (Cont.)



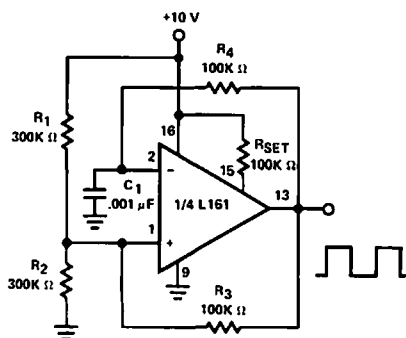
A Regulated DC to DC Converter



The L161 as an X100 Operational Amplifier

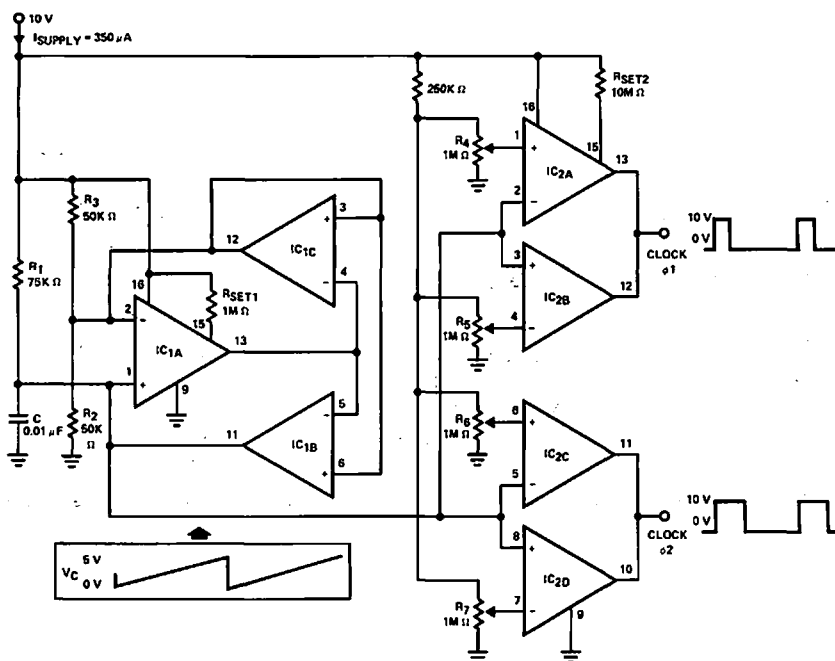


A Low Battery Indicator



Squarewave Oscillator

APPLICATIONS(Cont.)

A Versatile 2 ϕ Pulse Generator

Si8901

Ring Demodulator / Balanced Mixer



FEATURES

- Low ON Resistance
- Low Device Capacitance
<3 pF
- <2% Device Matching
Error
- High Third Order
Intercept Point (+35 dB)
- -55 dB Input Port Isolation

BENEFITS

- Useable to 1 GHz
- Low Harmonic Distortion
- Low Insertion Loss

APPLICATIONS

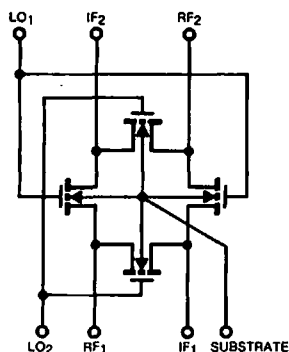
- RF Mixers
- CATV Encoders and
Decoders
- Modulators
- Demodulators
- Phase Sensitive
Detectors

DESCRIPTION

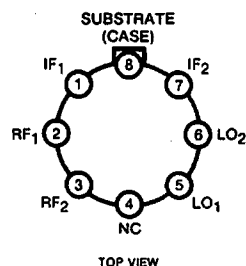
The Si8901 Ring Demodulator/Balanced Mixer offers significant improvements for RF mixer applications where low third order harmonic distortion has been a problem. Combining matching with very low junction capacitance, (<3 pF), low ON resistance (30 Ω) and very high OFF re-

sistance ($>10^9 \Omega$), the Si8901 accepts an RF and a local oscillator (LO) input and provides a high fidelity IF output with typical conversion loss of -8 dB at frequencies up to 1 GHz. Available in an 8 pin TO-99 package, this device is specified over -25 to 85°C operating temperature range.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



Order Numbers:
Si8901BA
See Package 26

ABSOLUTE MAXIMUM RATINGS

V_{DS} Drain to Source ± 15 V
 V_{DB} Drain to Substrate 22.5 V
 V_{SB} Source to Substrate 22.5 V
 V_{GS} Gate to Source -22.5 V to 30 V
 V_{GB} Gate to Substrate -0.3 V to 30 V
 V_{GD} Gate to Drain -22.5 V to 30 V

I_D Drain Current 50 mA
 Operating Temperature -25 to 85°C
 Storage Temperature -65 to 150°C
 Power Dissipation (Package)* 640 mW

*Derate 5 mW/C above 25°C

ELECTRICAL CHARACTERISTICS¹

$T_A = 25^\circ\text{C}$

	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED:	LIMITS			UNIT
				MIN ²	TYP ³	MAX	
STATIC	Drain-Source Breakdown Voltage	BV_{DS}	$V_{GS} = V_{SB} = -5$ V, $I_S = 10$ nA	15	25		V
	Source-Drain Breakdown Voltage	BV_{SD}	$V_{GD} = V_{DB} = -5$ V, $I_D = 10$ nA	15			
	Drain-Substrate Breakdown Voltage	BV_{DB}	Source Open, $V_{GB} = 0$ V, $I_D = 10$ nA	22.5			
	Source-Substrate Breakdown Voltage	BV_{DB}	Drain Open, $V_{GB} = 0$ V, $I_D = 10$ μ A	22.5			
	Threshold Voltage	V_{TH}	$V_{DS} = V_{GS} = V_{TH}$, $I_S = 1$ μ A, $V_{SB} = 0$ V	0.1	1	2.0	
	Gate Leakage Current	I_{GBS}	$V_{DB} = V_{SB} = 0$ V, $V_{GB} = 30$ V			2	μ A
	Drain-Source "ON" Resistance	$r_{DS(on)}$	$I_D = 10$ mA, $V_{SB} = 0$ V, $V_{GS} = 5$ V $I_D = 10$ mA, $V_{SB} = 0$ V, $V_{GS} = 10$ V		50 30	70	Ω
CAPACITANCE	Resistance Matching	$r_{DS(on)}$	$I_D = 10$ mA, $V_{SB} = 0$ V, $V_{GS} = 5$ V		1	5	
	Gate Node Capacitance	C_G	$V_{DS} = 10$ V, $V_{GS} = V_{BS} = -15$ V, $f = 1$ MHz See Capacitance Model in Figure 2		4.8		pF
	Drain Node Capacitance	C_D			2.6		
	Source Node Capacitance	C_S			7.0		
	Reverse Transfer Capacitance	C_{DG}			0.6		
DYNAMIC	Input Port Isolation	I_{IP}	See Figure 1		-55		dB
	Conversion Loss	L_C			8		
	Third Order Intercept	I_{3rd}			35		dBm
	Bandwidth	BW			1		GHz

NOTES:

1. Refer to PROCESS OPTION FLOWCHART for additional information.
2. The algebraic convention whereby the most negative value is a minimum, and the most positive is a maximum, is used in this data sheet.
3. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

DYNAMIC TEST CIRCUIT

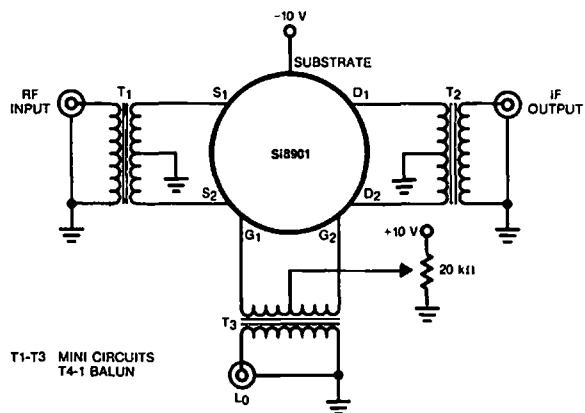


Figure 1

EQUIVALENT R AND C MODEL*

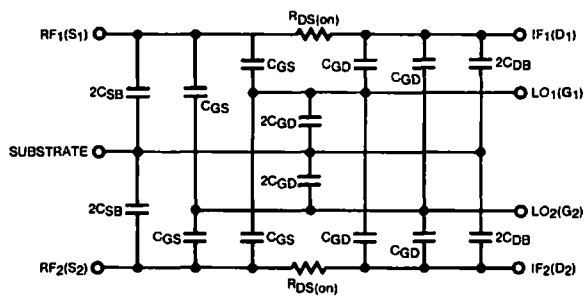


Figure 2

*Assuming one gate "ON" and one gate "OFF".

0	Introduction
1	Interface
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4	D/A Converters
5	Linear
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POWER CONVERSION

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Si7660	6-12
Si7661	6-18

Power Conversion Product Selector Guide¹

Pulse Width Modulators

Part Number	Function	Operating Frequency	Output Low Voltage @ Rated Current	Output High Voltage @ Rated Current	Supply Voltage
PWM25	Pulse Width Modulator for SMPS to drive NPN or N-channel Devices	200 Hz-300 kHz with Dead Time Adjust	0.4V @ 20mA 2.5V @ 100mA	V+ -2V @ 20mA V+ -3V @ 100mA	8.5V to 35V
PWM27	Pulse Width Modulator for SMPS to drive PNP or N-channel Devices	200 Hz-300 kHz with Dead Time Adjust	0.4V @ 20mA 2.5V @ 100mA	V+ -2V @ 20mA V+ -3V @ 100mA	8.5V to 35V
PWM125²	Pulse Width Modulator for SMPS to drive NPN or N-channel Devices	100 Hz-500 kHz with fixed 200 ns dead time	0.4V @ 20mA 2.5V @ 100mA	V+ -2V @ 20mA V+ -3V @ 100mA	8.5V to 35V
Si9100²	Switchmode Regulator subsystem for 1 W loads	40 kHz	N/A	N/A	10V to 65V

Voltage Converters

Si7660	Voltage Doubler/Inverter	1.5V to 10V	500µA Max.	-10V to 20V	-8.5V to 18.5V @ 20mA
Si7661²	Voltage Doubler/Inverter	4.5V to 20V	2mA Max.	-20V to 40V	-18V to 38V @ 20mA

NOTES:

1. Devices shown in **boldface** are recommended for new designs.
2. Preliminary product. Specifications subject to change. Contact factory on availability.

INTRODUCTION

Power Conversion IC's

Virtually every piece of electronic equipment in the world requires a DC power supply. This supply converts power from a battery or an AC line (sometimes both) into voltages and/or currents which are useful to the specific electronic equipment it serves. Usually the outputs must remain constant despite changes in input voltage, output load, ambient temperature, etc. In addition, the supply should have high conversion efficiency; inject a minimum of noise, ripple, or distortion onto its input and output; be small in volume, light in weight and low in cost.

Siliconix power conversion integrated circuits bring effective solutions to the problems of supplying power to electronic systems while meeting the above criteria. At present Siliconix manufactures three kinds of converter IC's: dual output pulse width modulators, single-ended monolithic switchmode power supplies, and charge pump voltage converters.

Pulse width modulators are controller systems which contain all the low-level electronic functions (clock, reference, error amplifier, comparator, etc) necessary for the construction of a switchmode power supply. Usually they are used to drive the power MOSFETs (not included) in such a supply. Monolithic switchmode power supplies are similar to pulse width modulators, but include a power MOSFET as part of the IC. Charge pump voltage converters are switching converters which are used to double or

invert an existing voltage. They may be used (for example) in systems where only a few parts require a negative supply.

The PWM25 is a regulating pulse width modulator that contains all the low-level control elements required to build a switchmode power supply: temperature compensated voltage reference, internal sawtooth oscillator, error amplifier, and pulse width modulator.

The PWM27 is equivalent to the PWM25 except that the outputs are logically inverted.

The PWM125 is equivalent to the PWM25 but offers an extended dynamic range and clock frequencies to 1 MHz.

The Si9100 is a one watt monolithic switchmode power supply which contains all the active components necessary to construct a one watt power supply. The power transformer, output rectification, and filtration are added by the user to fit the individual application.

The Si7660 is a charge pump voltage converter that inverts or doubles input voltages from +1.5 volts up to +10 volts. It features power conversion efficiencies up to 98%.

The Si7661 is a higher voltage version of the Si7660 intended for input voltages from +7.5 volts to +20 volts.

GLOSSARY OF TERMS

Clock

Pulse train produced by an on-chip oscillator.

Collector Supply Voltage (V_C)

Voltage applied to the PWM output drivers.

Common Mode Rejection

The ratio (in dB) of a voltage signal applied equally to both inputs of the error amplifier divided by its effect on the amplifier output.

Compensation

Terminal where a reactive network is connected to control the transient power supply response to a line or load disturbance; the method of tailoring such transient response.

Crossover Current

Current that flows across both totem pole output transistors during each coincident switching transition.

Current Mirror

Circuit effect by which the same current that flows through R_T is made available to charge C_T .

Dead Time

Time, at maximum duty cycle, during which both outputs of a PWM are off to prevent conduction overlap in the power switches.

Double Pulsing

Abnormal condition when two consecutive output pulses appear on the same output of a PWM instead of being alternated.

Duty Cycle

Ratio (in percent) of output pulse width divided by clock pulse period.

Flip Flop

Bistable circuit that alternately directs the output pulses to the two output drivers.

Gain-Bandwidth Product

Parameter that describes the open loop gain characteristic of the error amplifier. Frequency at which gain = 0 dB.

Input Supply Voltage ($+V_{IN}$)

Supply voltage that provides power to the PWM chip.

Junction Temperature

Temperature in the active regions of the semiconductor chip.

Latch

Protective circuit that ensures only one pulse is output for each clock cycle.

Line Regulation

Amount of output voltage change produced by a defined change of input voltage. Expressed as a ratio, either in dB or percent.

Load Regulation

Amount of output voltage change produced by a defined change in the output current.

Oscillator Charging Current

Current that flows through R_T . The same current will be used to charge C_T .

Output Source Resistance

A measure of load regulation. It is the ratio of change in output voltage divided by the corresponding change in output current.

Power Conversion Efficiency

Percentage ratio of power delivered to the load divided by input power.

Regulating Pulse Width Modulator

Integrated circuit that, using pulse width modulation, allows a switchmode power supply to regulate an output DC voltage.

Shut Down

Function that inhibits both outputs of a PWM to cause power supply turn off.

Soft Start

A feature that, at initial turn on, causes the output voltage to ramp up from zero to the desired voltage without creating high inrush currents.

Supply Voltage Rejection

Ratio (in dB) of a change in $+V_{IN}$ divided by its corresponding change in error amplifier output voltage.

GLOSSARY OF TERMS (Cont.)

Switch Mode Power Supply

Power supply that switches an unregulated DC input to produce high frequency current pulses before final rectification and/or regulation.

Switching Frequency

Rate at which all power switches in a power converter go through one complete cycle.

SYNC

Terminal where short pulses may be injected to synchronize multiple converters to each other or a single PWM to an external clock.

Thermal Resistance

Ratio of temperature difference between two surfaces and the amount of power dissipation being conducted through them.

Timing Capacitor (C_T)

Capacitor which determines the oscillator frequency.

Timing Resistor (R_T)

Resistor that determines the timing capacitor charging current and therefore the oscillator frequency.

Totem Pole

Configuration of output stage where two transistors are connected in series between the supply voltage and ground.

Undervoltage Lockout

Function on a PWM chip that inhibits both outputs if +V_{IN} falls below +8 volts.

Voltage Converter

Device that receives energy from a supply at a given voltage and delivers this energy to a load at a different voltage.

Voltage Reference

Very stable temperature compensated voltage source used as a standard to measure output voltage accuracy.

Voltage Regulator

Circuit that uses a pass transistor to produce the voltage reference.

PWM25/PWM27 Regulating Pulse Width Modulators



FEATURES

- High Frequency Operation
- Undervoltage Lockout
- Internal Soft Start
- Adjustable Dead Time
- Separate Oscillator Sync Terminal
- 8 to 35 V Operation

BENEFITS

- Industry Standard Pin Out
- Flexible Design for Power Control

APPLICATIONS

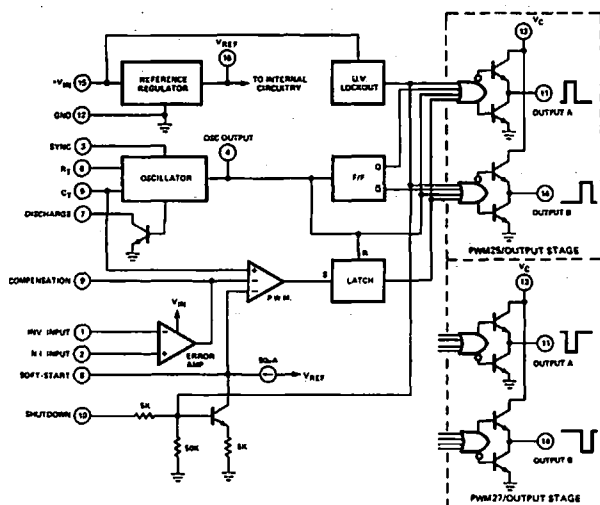
- High Frequency Switching Power Supplies
- Particularly Suitable for Driving MOSPOWER Transistors
- Low Parts Count

DESCRIPTION

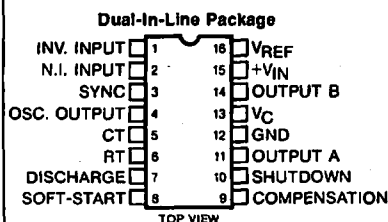
The PWM25/27 series of pulse width modulator integrated circuits are designed to offer improved performance and lowered external parts count when used to implement all types of switching power supplies. The on-chip +5.1 volt reference is trimmed to $\pm 1\%$ initial accuracy and the input common-mode range of the error amplifier includes the reference voltage, eliminating external potentiometers and divider resistors. A Sync input to the oscillator allows multiple units to be slaved together, or a single unit to be synchronized to an external system clock. A single resistor between the CT pin and the Discharge pin provides deadtime adjustment. These devices also feature built-in soft-start circuitry with only a timing capacitor required externally. A Shut-down pin controls both the soft-start

circuitry and the output stages, providing instantaneous turn-off with soft-start recycle for slow turn-on. These functions are also controlled by an undervoltage lockout which keeps the outputs off and the soft-start capacitor discharged for input voltages less than that required for normal operation. Another unique feature of these PWM circuits is a latch following the comparator. Once a PWM pulse has been terminated for any reason, the outputs will remain off for the duration of the period. The latch is reset with each clock pulse. The output stages are totem-pole designs capable of sourcing or sinking 100 mA. The PWM25 output stage features NOR logic, giving a LOW output for an OFF state. The PWM27 utilizes OR logic which results in a HIGH output level when OFF.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



Order Numbers:
 PWM25AK, PWM27AK
 PWM25BK, PWM27BK
 See Package 10
 PWM25CJ, PWM27CJ
 See Package 8

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (+V _{IN})	40 V
Collector Supply Voltage (V _C)	40 V
Logic Inputs	-0.3 to 5.5 V
Analog Inputs	-0.3 to V _{IN}
Output Current, Source or Sink	500 mA
Reference Output Current	50 mA
Oscillator Charging Current	5 mA
Power Dissipation at T _A = 25°C**	1000 mW
Thermal Resistance: junction to ambient	100°C/W
Power Dissipation at T _C = 25°C***	2000 mW
Thermal Resistance: junction to case	60°C/W
Operating Junction Temperature	150°C

Storage Temperature Range	-65 to 150°C
(A/B Suffix)	-65 to 125°C
(C Suffix)	-65 to 125°C
Operating Ambient Temperature Range	
(A Suffix)	-55 to 125°C
(B Suffix)	-25 to 85°C
(C Suffix)	-0 to 70°C
Lead Temperature (Soldering, 10 seconds)	300°C

**Derate at 10 mW/°C for ambient temperatures above 50°C.

***Derate at 16 mW/°C for case temperatures above 25°C.

RECOMMENDED OPERATING CONDITIONS*

Input Voltage (V _{IN})	8 to 35 V
Collector Supply Voltage (V _C)	4.5 to 35 V
Sink/Source Load Current	
(each output) Steady State	0 to 100 mA
Peak Current	0 to 400 mA

Reference Load Current	0 to 20 mA
Oscillator Frequency Range	100 Hz to 500 kHz
Oscillator Timing Resistor	1.5 to 210 kΩ
Oscillator Timing Capacitor	820 pF to 0.1 μF
*Range over which the device is functional.	

ELECTRICAL CHARACTERISTICS¹

T_A = 25°C

	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: $V_{in}^{+} = 20\text{ V}$	LIMITS						UNIT
				PWM25/PWM27A/B			PWM25/PWM27C			
				MIN ²	TYP ³	MAX	MIN ²	TYP ³	MAX	
REFERENCE	Output Voltage			5.05	5.10	5.15	5.00	5.10	5.20	V
	Line Regulation		$V_{in}^{+} = 8\text{ to }35\text{ V}$		4	20		4	20	mV
	Load Regulation		$I_L = 0\text{ to }20\text{ mA}$		20	50		20	50	
	Short Circuit Current		$V_{REF} = 0$		80	120		80	120	mA
	Output Noise Voltage		$10\text{ Hz} \leq f \leq 10\text{ kHz}$		40	200		40	200	$\mu\text{V(rms)}$
OSCILLATOR	Initial Accuracy ⁴				±2	±6		±2	±10	
	Voltage Stability ⁴		$V_{in}^{+} = 8\text{ to }35\text{ V}$		±0.1	±1		±0.1	±2	%
	Minimum Frequency		$R_T = 150\text{ k}\Omega$, $C_T = 0.1\text{ }\mu\text{F}$			200			200	Hz
	Maximum Frequency		$R_T = 2\text{ k}\Omega$, $C_T = 0.001\text{ }\mu\text{F}$	300	370			300	370	kHz
	Current Mirror		$I_{RT} = 2\text{ mA}$	1.7	2.0	2.2	1.7	2.0	2.2	mA
	Clock Amplitude ⁴			3.0	3.5		3.0	3.5		V
	Clock Width ⁴			0.3	0.5	1.3	0.3	0.5	1.3	μsec
	Sync Threshold			1.2	2.0	2.8	1.2	2.0	2.8	V
ERROR AMPLIFIER	Sync Input Current		Sync Voltage = 3.5 V		1.0	2.5		1.0	2.5	mA
	Input Offset Voltage		$V_{CM} = 5.1\text{ V}$		0.5	5		2	10	mV
	Input Bias Current				1	10		1	10	μA
	Input Offset Current					1			1	
	DC Open Loop Gain			$R_L \geq 10\text{ M}\Omega$	60	80		60	80	
	Gain-Bandwidth Product			$A_V = 0\text{ dB}$	60	80		60	80	
	Output Low Level				0.02	0.5		0.02	0.5	
	Output High Level				3.8	7		3.8	7	
	Common Mode Rejection			$V_{CM} = 1.5\text{ to }5.2\text{ V}$	60	85		60	85	
	COMPAR- ATOR	Supply Voltage Rejection		$V_{in}^{+} = 8\text{ to }35\text{ V}$, $V_{CM} = 5.1\text{ V}$	50	85		50	85	
Minimum Duty Cycle						0			0	
Maximum Duty Cycle				45	49		45	49	0	
Input Threshold ⁴			Zero Duty Cycle	0.6	0.9		0.6	0.9		
Input Threshold ⁴			Maximum Duty Cycle	3.3	3.6		3.3	3.6		V
Soft Start Current			$V_{SHUTDOWN} = 0\text{ V}$	25	50	100	25	50	100	μA
Soft Start Voltage			$V_{SHUTDOWN} = 2\text{ V}$		0.4	0.6		0.4	0.6	V
SOFT- START	Shutdown Input Current		$V_{SHUTDOWN} = 2.5\text{ V}$	0.4	1.0		0.4	1.0	mA	

NOTES:

1. Refer to PROCESS OPTION FLOWCHART for additional information.
2. The algebraic convention whereby the most negative value is a minimum, and the most positive value is a maximum is used in this data sheet.
3. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
4. Tested at f_{osc} = 40 kHz, R_T = 3.2 kΩ, C_T = 0.01 μF, R_D = 0 Ω.

ELECTRICAL CHARACTERISTICS¹ (Cont.)

	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: $V_{in}^{+} = 20\text{ V}$	LIMITS						UNIT
				PWM25/PWM27A/B			PWM25/PWM27C			
				MIN ²	TYP ³	MAX	MIN ²	TYP ³	MAX	
OUTPUT	Output Low Level		$I_{\text{SINK}} = 20\text{ mA}$		0.2	0.4		0.2	0.4	V
			$I_{\text{SINK}} = 100\text{ mA}$		1.0	2.5		1.0	2.5	
	Output High Level		$I_{\text{SOURCE}} = 20\text{ mA}$	18	19		18	19		
			$I_{\text{SOURCE}} = 100\text{ mA}$	17	18		17	18		
	Undervoltage Lockout		$V_{\text{COMP and } V_{\text{SS}}} = \text{high}$	6	7	8.5	6	7	8.5	ns
	Rise Time		$C_L = 1\text{ nF}$		100	600		100	600	
	Fall Time		$C_L = 1\text{ nF}$		50	300		50	300	
	Shutdown Delay		$V_{\text{SH}} = 3\text{ V}, C_B = 0$		0.2	0.5		0.2	0.5	
	Collector Leakage		$V_C = 35\text{ V}$			200			200	μA
SUPPLY	Supply Current		$V_{in}^{+} = 35\text{ V}$		14	20		14	20	mA

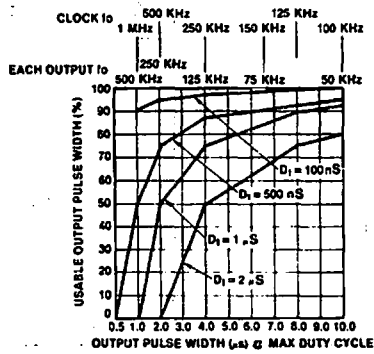
 T_A = Over Temperature Range

	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: $V_{in+} = 20\text{ V}$	LIMITS						UNITS	
				PWM25/PWM27A/B			PWM25/PWM27C				
				MIN ²	TYP ³	MAX	MIN ²	TYP ³	MAX		
REFERENCE	Line Regulation		$V_{in+} = 8\text{ to }35\text{ V}$			20			20	mV	
	Load Regulation		$I_L = 0\text{ to }20\text{ mA}$			50			50		
	Temperature Stability		Over Operating Range			50			50		
	Total Output Variation		Line, Load, and Temp	5.00		5.20	4.95		5.25	V	
	Long Term Stability					50			50	mV kHr	
OSCILLATOR	Voltage Stability ⁴		$V_{in+} = 8\text{ to }35\text{ V}$			± 1.0			± 2	%	
	Temperature Stability		Over Operating Range			± 6			± 6		
	Minimum Frequency		$R_T = 150\text{ k}\Omega$, $C_T = 0.1\text{ }\mu\text{F}$			200			200	Hz	
	Maximum Frequency		$R_T = 2\text{ k}\Omega$, $C_T = 0.001\text{ }\mu\text{F}$	300			300			kHz	
	Current Mirror		$I_{RT} = 2\text{ mA}$	1.7		2.2	1.7		2.2	mA	
ERROR AMPLIFIER	Clock Amplitude ⁴			3.0			3.0			V	
	Sync Threshold			1.2		2.8	1.2		2.8		
	Sync Input Current		Sync Voltage = 3.5 V			2.5			2.5	mA	
	Input Offset Voltage		$V_{CM} = 5.1\text{ V}$			5			10	mV	
	Input Bias Current					10			10	μA	
Input Offset Current					1			1			
DC Open Loop Gain		$R_L \geq 10\text{ M}\Omega$		60		60			dB		
COMPARATOR	Output Low Level					0.5			0.5	V	
	Output High Level			3.8			3.8				
	Common Mode Rejection		$V_{CM} = 1.5\text{ to }5.2\text{ V}$	60			60			dB	
	Supply Voltage Rejection		$V_{in+} = 8\text{ to }35\text{ V}$, $V_{CM} = 5.1\text{ V}$	50			50				
	Minimum Duty Cycle					0			0	%	
SOFT-START	Maximum Duty Cycle			45			45				
	Input Threshold ⁴		Zero Duty Cycle	0.6			0.6			V	
	Input Threshold ⁴		Maximum Duty Cycle			3.6			3.6		
	Input Bias Current									μA	
	Soft Start Current		$V_{SHUTDOWN} = 0\text{ V}$	25		100	25		100		
OUTPUT	Soft Start Voltage		$V_{SHUTDOWN} = 2\text{ V}$			0.6			0.6	V	
	Shutdown Input Current		$V_{SHUTDOWN} = 2.5\text{ V}$			1.0			1.0	mA	
	Output Low Level		$V_D = 20\text{ V}$	$I_{SINK} = 20\text{ mA}$			0.4			0.4	V
				$I_{SINK} = 100\text{ mA}$			2.5			2.5	
	Output High Level			$I_{SOURCE} = 20\text{ mA}$	18			18			
		$I_{SOURCE} = 100\text{ mA}$		17			17				
SUPPLY	Undervoltage Lockout			V_{COMP} and $V_{SS} = \text{high}$	6		8.5	6		8.5	
	Crossover Current			$V_C = 35\text{ V}$						mA	
	Collector Leakage						200			200	μA
	Supply Current		$V_{in+} = 35\text{ V}$			20			20	mA	

NOTES:

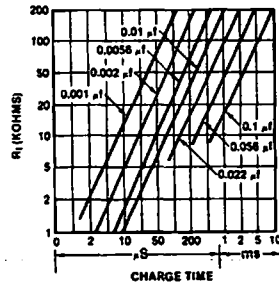
1. Refer to PROCESS OPTION FLOWCHART for additional information.
2. The algebraic convention whereby the most negative value is a minimum, and the most positive value is a maximum is used in this data sheet.
3. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
4. Tested at $f_{osc} = 40\text{ kHz}$, $R_T = 3.2\text{ k}\Omega$, $C_T = 0.01\text{ }\mu\text{F}$, $R_D = 0\text{ }\Omega$.

TYPICAL CHARACTERISTICS



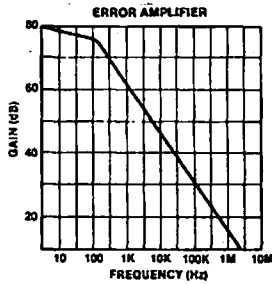
**Effect of Deadtime on
Output Pulse Range**
Figure 1

Figure 1 shows the relative amount of usable pulse width for a given amount of deadtime. Usable pulse width is that portion of the pulse used to adjust the output current. 500 nS is normal deadtime for the PWM25/27 but longer deadtimes can be realized by inserting a resistor between discharge at Pin 7 and C_T at Pin 5. As can be seen the smaller the deadtime the greater the adjustment range at higher speeds.

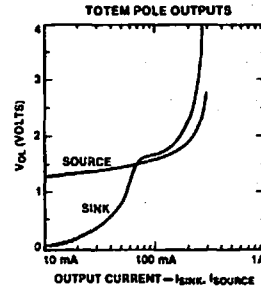


$V_t = 20 \text{ V}$
Figure 2

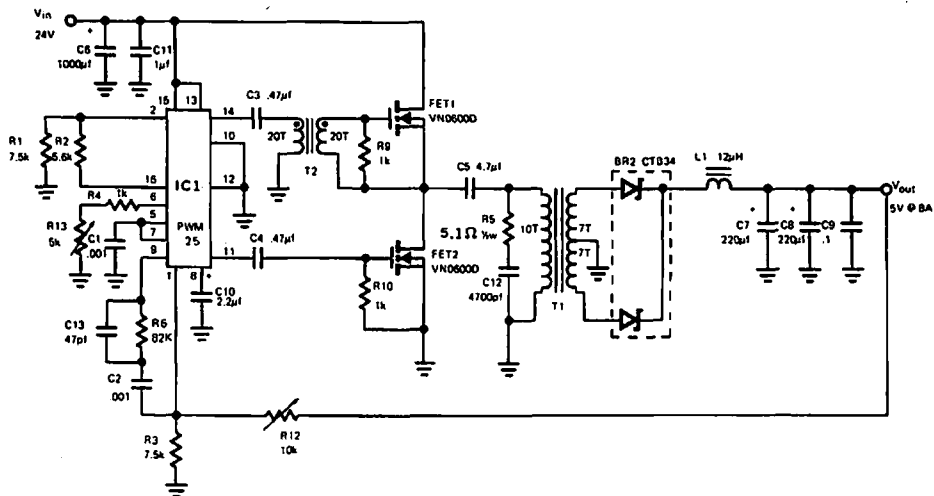
With Figure 2 the capacitor risetime for a given timing resistor value can be determined.



Gain vs. Frequency
Figure 3



Output Saturation
Figure 4





PWM 125

Regulating Pulse Width Modulator

FEATURES

- Fixed 200 ns Deadtime
- Operational to 500 kHz
- 8 to 35 V Operation
- Internal Soft-Start
- Input Undervoltage Lockout

BENEFITS

- Reduced Transients
- High Frequency Operation
- Military Temperature Range
- Versatile
- Lower Overall Parts Count

APPLICATIONS

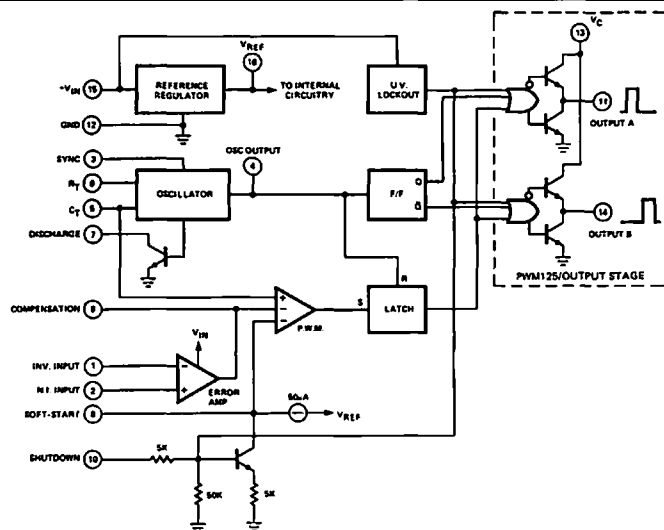
- Switched-Mode Power Supplies
- Power MOSFET Switching and Control

DESCRIPTION

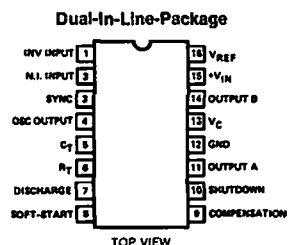
The PWM 125 pulse width modulator integrated circuit is designed to offer maximum performance and lowered external parts count when used to implement high speed switching power supplies. The on-chip +5.1 volt reference is trimmed to $\pm 1\%$ initial accuracy and the input common-mode range of the error amplifier includes the reference voltage, eliminating external potentiometers and divider resistors. A Sync input to the oscillator allows multiple units to be slaved together, or a single unit to be synchronized to an external system clock. These devices also feature built-in soft-start circuitry with only a timing capacitor required externally. A Shutdown pin controls both the soft-start circuitry and the output stages, providing instantaneous

turn-off with soft-start re-cycle for slow turn-on. These functions are also controlled by an undervoltage lockout which keeps the outputs off and the soft-start capacitor discharged for input voltages less than that required for normal operation. Another unique feature of these PWM circuits is a latch following the comparator. Once a PWM pulse has been terminated for any reason, the outputs will remain off for the duration of the period. The latch is reset with each clock pulse. The output stages are totem-pole designs capable of sourcing or sinking 100 mA. The PWM125 output stage features NOR logic, giving a LOW output for an OFF state.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION





Si9100

One Watt Switchmode Regulator Subsystem

FEATURES

- One Watt Power Conversion
- Operates from 10 to 65 V Input
- Uses either Voltage Mode or Current Mode Control
- One Resistor Sets Clock Frequency
- Fast Current Limiting
- External Synchronization Terminal
- Multi-Mode On/Off Control

BENEFITS

- Simplifies Power Converter Design
- Unique Starting Circuit Allows Easy Primary Side Control and Isolation
- High Conversion Efficiency Reduces System Losses
- Minimizes External Components
- Minimizes Converter Volume

APPLICATIONS

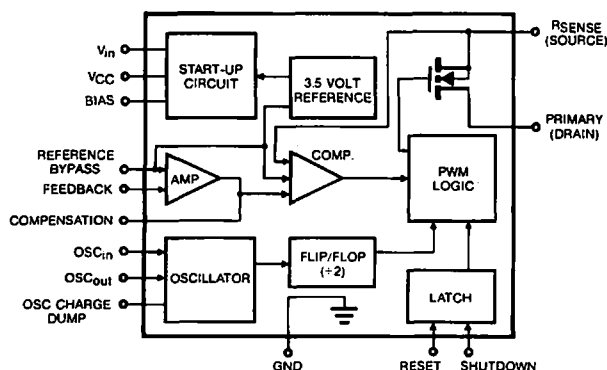
- DC/DC Converters
- Switchmode Power Supplies

DESCRIPTION

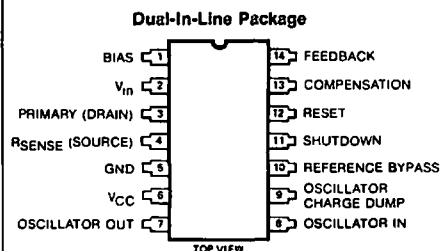
The Si9100 Switchmode Regulator Subsystem is a monolithic DMOS/CMOS integrated circuit which contains most of the components necessary to implement a one watt high efficiency DC to DC converter. The PWM subsystem includes high voltage start-up circuitry, oscillator, voltage

reference, and DMOS output transistor. Additional features include primary current sense, multimode on/off control, and external sync input. The Si9100 may be used with an appropriate magnetic to implement most single-ended power converter topologies.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



Si7660

Monolithic CMOS

Voltage Converter



FEATURES

- Conversion of +5 V Logic Supply to ± 5 V Supplies
- Voltage Multiplication ($V_{out} = nV_{in}$)
- 99.7% Typical Open Circuit Voltage Conversion Efficiency
- 95% Typical Power Efficiency
- Operating Voltage Range of 1.5 V to 10.0 V
- Requires Only 2 Capacitors and 1 Diode

BENEFITS

- Inexpensive Negative Supply from Positive Supply
- Easy to Use
- Minimum Parts Count

APPLICATIONS

- On Board Negative Supply for Dynamic RAMs
- Localized μ -Processor (8080 Type) Negative Supplies
- Inexpensive Negative Supplies
- Data Acquisition Systems

DESCRIPTION

The Siliconix Si7660 is a monolithic CMOS power supply circuit which offers unique performance advantages over previously available devices. The Si7660 performs a supply voltage conversion from positive to negative for an input range of +1.5 V to +10.0 V, resulting in a complementary output voltage of -1.5 V to -10.0 V with the addition of only 2 capacitors.

Contained on the chip are a voltage regulator, RC oscillator, voltage level translator, four power MOS switches, and a logic network. This logic network senses the most negative voltage in the device and ensures that the output N-channel switch substrates are not forward-biased.

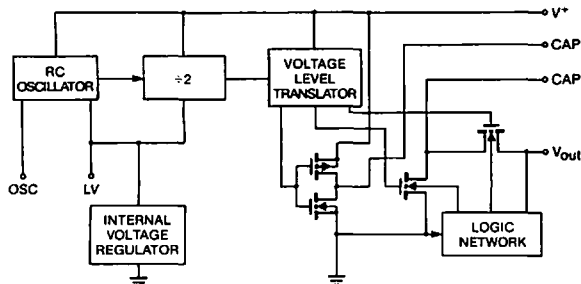
The oscillator, when unloaded, oscillates at a nominal frequency of 12 kHz for an input supply voltage of 1.5 to 10.0

volts. The "OSC" terminal may be connected to an external capacitor to lower the frequency or it may be driven by an external clock.

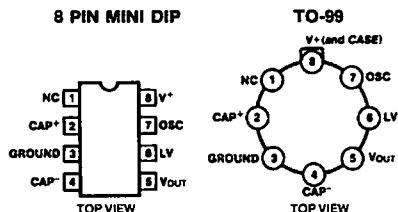
The "LV" terminal may be tied to GROUND to bypass the internal regulator and improve low voltage (LV) operation. At high voltages (+3.5 to +10 volts), the LV pin should be left disconnected.

Typical applications for the Si7660 are data acquisition and microprocessor based systems where a +5 volt supply is available for the digital functions, and an additional -5 volt supply is required for the analog functions. The Si7660 is also ideally suited for providing low current, -5 V body bias supply for dynamic RAMs.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



Order Number:
SI7660CJ
See Package 25

Order Numbers:
SI7660BA, SI7660CA
See Package 26

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	10.2 V	Operating Temperature (B Suffix)	-25 to 85°C
Oscillator Input Voltage ¹		(C Suffix)	0 to 70°C
-0.3 V to (V ⁺ + 0.3 V) for V ⁺ < 5.5 V		Power Dissipation ² :	
(V ⁺ - 8 V) to (V ⁺ + 0.3 V) for V ⁺ > 5.5 V		Metal Can Package	500 mW
LV	No connection for V ⁺ > 3.5 V	8 Pin Plastic DIP	300 mW
Storage Temperature (B Suffix)	-65 to 150°C		
(C Suffix)	-65 to 125°C		

ELECTRICAL CHARACTERISTICS³T_A = 25°C

	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED V ⁺ = 5 V, C _{osc} = 0	Si7660 B/C			UNITS
				MIN ⁴	TYP ⁵	MAX	
INPUT	Supply Voltage Range-Lo (DX out of Circuit)	V _L	R _L = 10 kΩ, LV = Ground	1.5		3.5	V
	Supply Voltage Range-Lo (DX in Circuit)			1.5		3.5	
	Supply Voltage Range-Hi ⁶ (DX out of Circuit)	V _H	R _L = 10 kΩ, LV = No Connection	3		6.5	
	Supply Voltage Range-Hi ⁶ (DX in Circuit)			3		10	
	Supply Current	I ₊	R _L = ∞ LV = Open		100	500	μA
OUTPUT	Output Source Resistance	R _{OUT}	LV = Open I _O = 20 mA		55	100	Ω
	Power Conversion Efficiency	P _{E1}	R _L = 5 kΩ	95	98		%
	Voltage Conversion Efficiency	V _{OUT} E1	R _L = ∞	97	99.9		
DYNAMIC	Oscillator Frequency	f _{osc}			12		kHz
	Oscillator Impedance	Z _{osc}	V ⁺ = 2 V, LV = GND V ⁺ = 5 V		1 100		MΩ kΩ

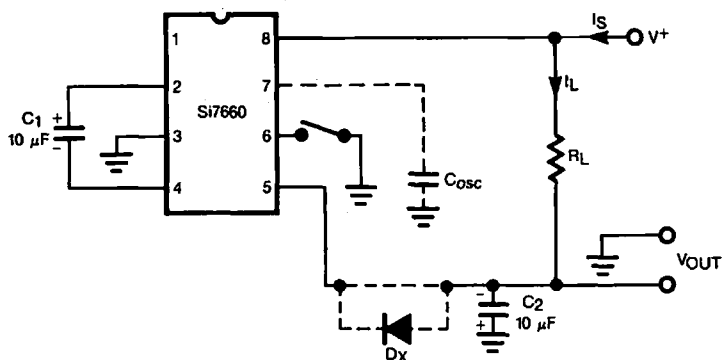
T_A = Over Temperature Range

	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED V ⁺ = 5 V, C _{osc} = 0	Si7660 B/C			UNITS
				MIN ⁴	TYP ⁵	MAX	
INPUT	Supply Voltage Range-Lo (DX out of Circuit)	V _L	R _L = 10 kΩ, LV = Ground	1.5		3.5	V
	Supply Voltage Range-Lo (DX in Circuit)			1.5		3.5	
	Supply Voltage Range-Hi ⁶ (DX out of Circuit)	V _H	R _L = 10 kΩ, LV = No Connection	3		5.0	
	Supply Voltage Range-Hi ⁶ (DX in Circuit)			3		10	
	Supply Current	I ₊	R _L = ∞ LV = Open			500	μA
OUTPUT	Output Source Resistance	R _{OUT}	V ⁺ = 2 V, LV = GND, I _O = 3 mA, DX In Circuit				Ω
			V ⁺ = 2 V, LV = GND I _O = 3 mA, DX out of Circuit			300	
			V ⁺ = 5 V, LV = Open I _O = 20 mA			120	

NOTES:

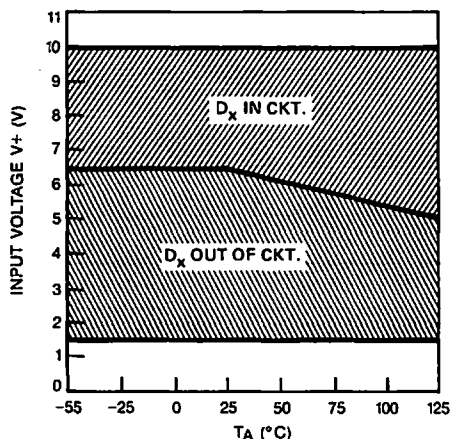
- For large value of C_{osc} (>1000 pF) the values of C₁ and C₂ should be increased to 100 μF.
- Derate 6 mW/°C above 75°C.
- All DC parameters are 100% tested at 25°C. Lots are sample-tested for AC parameters and high and low temperature limits to assure conformance with specifications.
- The algebraic convention whereby the most negative value is a minimum, and the most positive value is a maximum, is used in this data sheet.
- Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- DX is required for supply voltages greater than 6.5 V @ -55°C ≤ T_A ≤ 25°C; refer to performance curves (Fig. 1) for additional information.
- C₁ - Pump Capacitor
C₂ - Reservoir Capacitor

TEST CIRCUIT

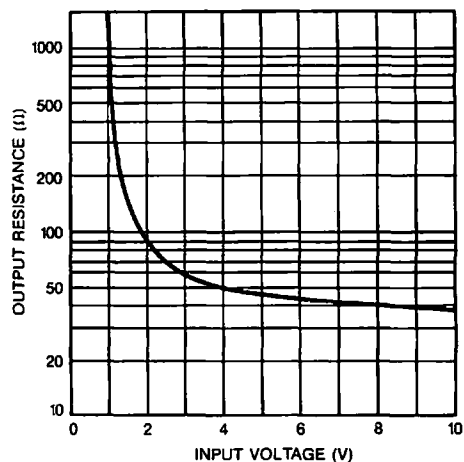


$V+ = 5\text{ V}$, $T_A = 25^\circ\text{C}$, $C_{osc} = 0$, Test Circuit Figure 1 unless otherwise specified. (See notes 6 and 7 on previous page)

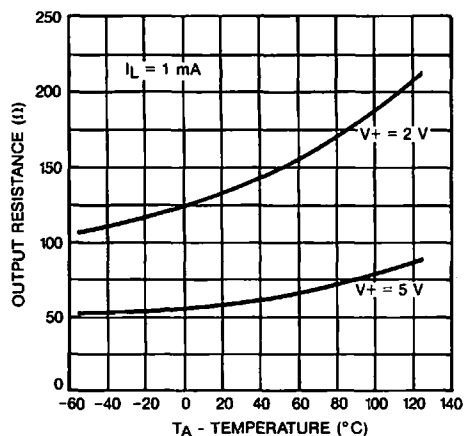
TYPICAL CHARACTERISTICS



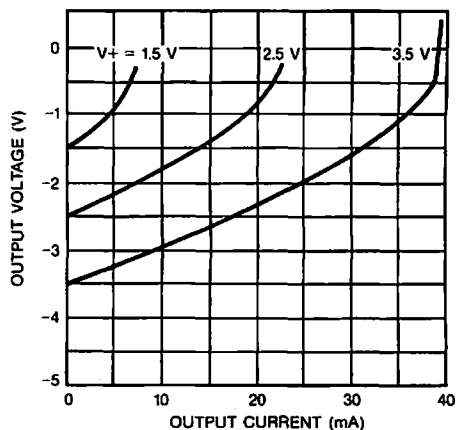
Operating Voltage as a Function of Temperature
Figure 1



Output Source Resistance as a Function of Supply Voltage
Figure 2



Output Source Resistance vs Temperature
Figure 3



Typical Si7660 Output LV = GND
Figure 4

TYPICAL CHARACTERISTICS (Cont.)

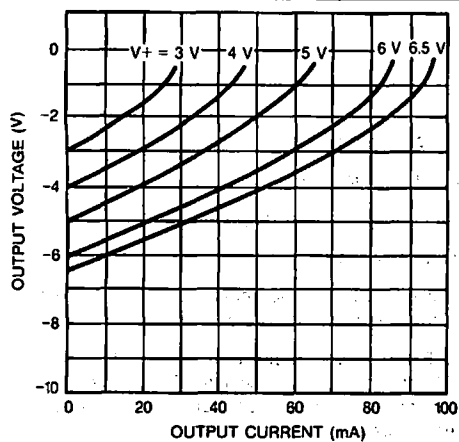


Figure 5

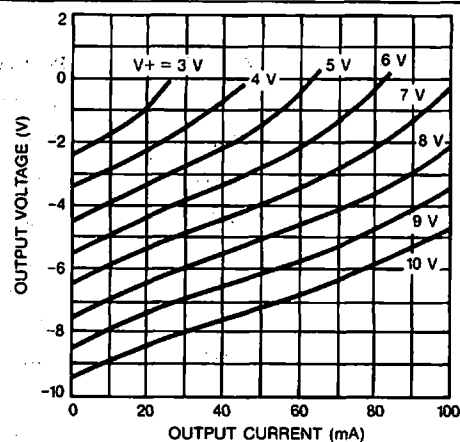


Figure 6

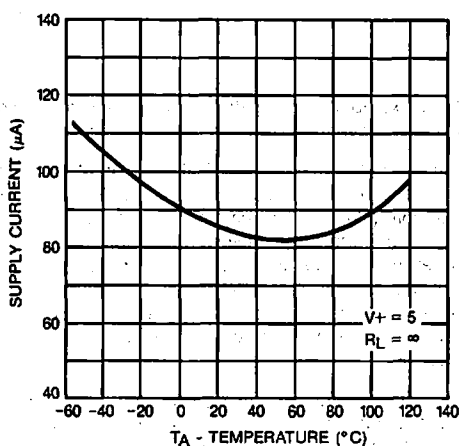


Figure 7

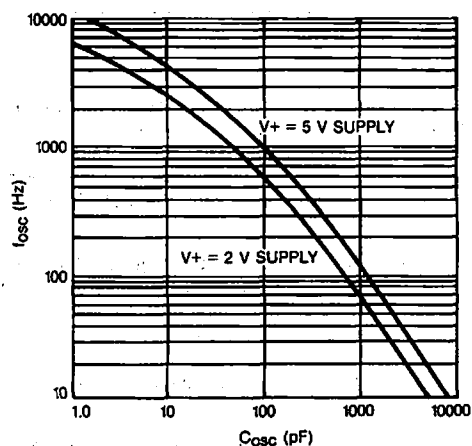


Figure 8

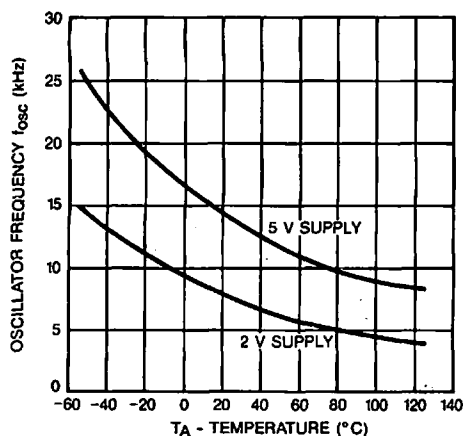


Figure 9

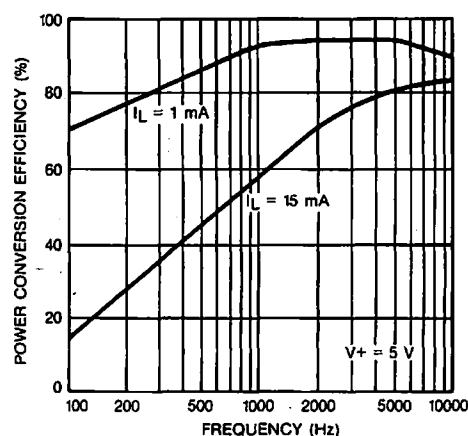


Figure 10

PIN DESCRIPTION

Pin Number	Symbol	Pin Description
1	—	No connection.
2	CAP+	Positive terminal connection for pump capacitor.
3	GND	Input and/or output ground reference.
4	CAP-	Negative terminal connection for pump capacitor.
5	VOUT	Output of the voltage converter.
6	LV	Low Voltage. Connection to ground shorts out internal power supply regulator for operation below 3.5 volts.
7	OSC	OSCillator input. External clock input to this pin will override the internal oscillator. The internal oscillator frequency can be slowed by connecting an external capacitor between this pin and ground. (See Figure 8)
8	V+	Input voltage connection.

APPLICATION HINTS

The Siliconix Si7660 is a VOLTAGE source, not a CURRENT source. Therefore, any heavy load current will either greatly reduce the output voltage (possibly out of the desired range) or cause the device to go into power shutdown. To avoid problems, keep the VOLTAGE conversion concept in mind.

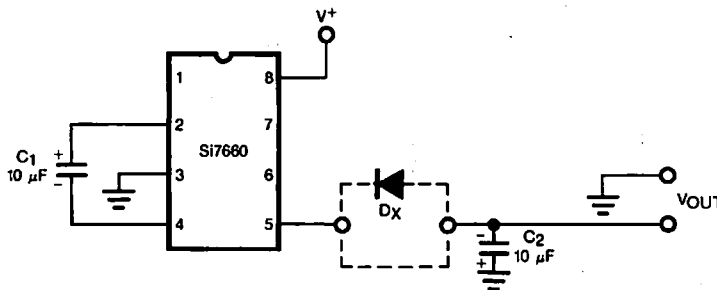
The Si7660 is intended for use as a voltage inverter. However, with a few added components, the inverter circuit can be rearranged to provide many different voltage levels. Some of the possibilities include voltage inversion, voltage multiplication, and even simultaneous inversion and multiplication. For more information refer to Application Note AN84-2.

There are many applications where a low current negative supply made with an Si7660 would do just as well as a full conventional negative supply or DC-to-DC converter module.

Some examples are negative power supplies for microprocessors, dynamic RAMs, or data acquisition systems.

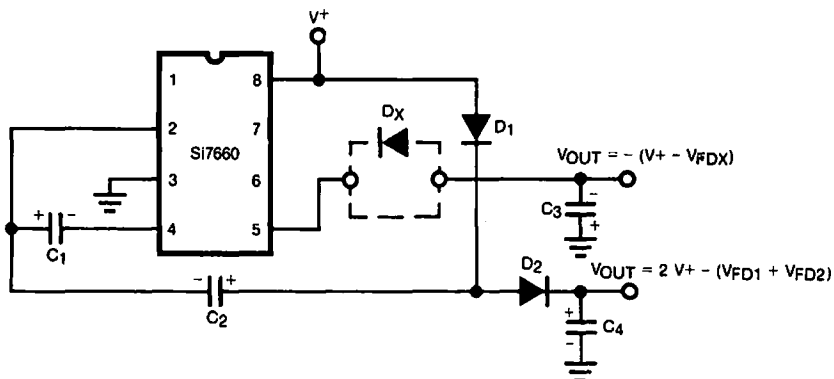
If the output ripple of the Si7660 is too great for a particular application, the value of the pump (C_1 , Fig. 11) and reservoir (C_2 , Fig. 11) capacitors can be increased to reduce this effect. However, it is important to note that increasing the capacitor size can lead to surge currents at turn-on. If the current is too great, the power dissipation of the device can be exceeded, causing destruction of the device. The maximum recommended capacitor size is 1000 μF .

To prevent device latchup, a diode (DX) should be placed in series with pin 5 when operating above 6.5 volts at room temperature. Refer to Figure 1 when operating the Si7660 at other temperatures.



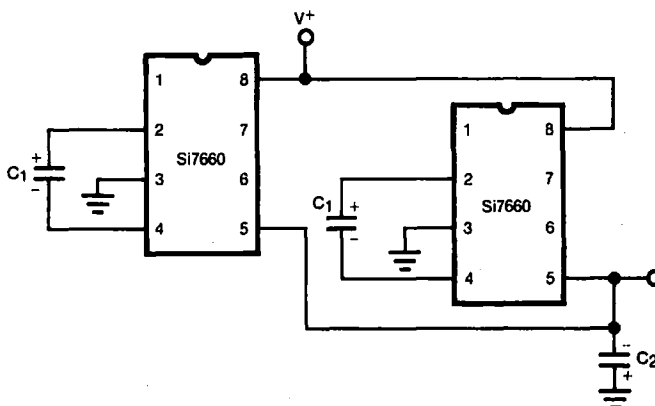
Basic Voltage Inverter Circuit
Figure 11

Figure 12 shows a circuit that will produce two output voltages utilizing both of the Si7660 features (i.e. inversion and doubling). The combined output current must be limited so the maximum device dissipation is not exceeded.



Combination Inverter/Multiplier Circuit
Figure 12

Two Si7660's can be paralleled to reduce the effective output resistance of the converter. The output voltage at a given current is increased since the voltage drop is halved when the devices are connected as shown in Figure 13.



Paralleling Two Si7660's to Reduce the Effective Output Resistance
Figure 13

Si7661

Monolithic CMOS

Voltage Converter



FEATURES

- Conversion of +4.5 V to +20 V Logic Supply to -4.5 V to -20 V Supplies
- Voltage Multiplication ($V_{out} = (-) nV_{in}$)
- 99.7% Typical Open Circuit Voltage Conversion Efficiency
- 95% Typical Power Efficiency
- Wide Operating Voltage Range 4.5 V to 20.0 V
- Requires Only 2 Capacitors

BENEFITS

- Inexpensive Negative Supply Generation
- Easy to Use
- Minimum Parts Count

APPLICATIONS

- On Board Negative Supply for Dynamic RAMs
- Localized μ -Processor (8080 Type) Negative Supplies
- Inexpensive Negative Supplies
- Data Acquisition Systems
- Up to -20 V for Op Amps, and other Linear Circuits

DESCRIPTION

The Siliconix Si7661 is a monolithic CMOS power supply circuit which offers unique performance advantages over previously available devices. The Si7661 performs a supply voltage conversion from positive to negative for an input range of +4.5 V to +20.0 V, resulting in a complementary output voltage of -4.5 V to -20.0 V with the addition of only 2 capacitors.

Contained on the chip are a voltage regulator, RC oscillator, voltage level translator, four power MOS switches, and a logic network. This logic network senses the most negative voltage in the device and ensures that the output N-channel switch substrates are not forward-biased.

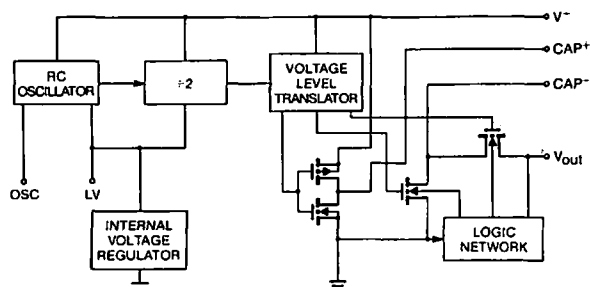
The oscillator, when unloaded, oscillates at a nominal frequency of 10 kHz for an input supply voltage of 4.5 to 20.0

volts. The "OSC" terminal may be connected to an external capacitor to lower the frequency or it may be driven by an external clock.

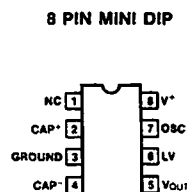
The "LV" terminal may be tied to GROUND to bypass the internal regulator and improve low voltage (LV) operation. At high voltages (+8 to +20.0 volts), the LV pin should be left disconnected.

Typical applications for the Si7661 are data acquisition and microprocessor based systems, where a +4.5 to +20 volt supply is available for the digital functions, and an additional -5 to -20 volts supply is required for analog devices, such as op amps. The Si7661 is also ideally suited for providing low current, -5 V body bias supply for dynamic RAMs.

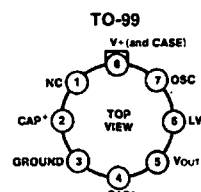
FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



Order Number:
SI7661CJ
See Package 25



Order Numbers:
SI7661BA, SI7661CA
See Package 26

ABSOLUTE MAXIMUM RATINGS

Supply Voltage 10.2 V
 Oscillator Input Voltage¹
 -0.3 V to ($V^+ + 0.3$ V) for $V^+ < 5.5$ V
 ($V^+ - 8$ V) to ($V^+ + 0.3$ V) for $V^+ > 5.5$ V
 LV No connection for $V^+ > 3.5$ V
 Storage Temperature (B Suffix) -65 to 150°C
 (C Suffix) -65 to 125°C

Operating Temperature (B Suffix) -25 to 85°C
 (C Suffix) 0 to 70°C
 Power Dissipation²:
 Metal Can Package 500 mW
 8 Pin Plastic DIP 300 mW

ELECTRICAL CHARACTERISTICS³ $T_A = 25^\circ\text{C}$

	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: $C_{osc} = 0$	Si7661 B/C			UNITS
				MIN ⁴	TYP ⁵	MAX	
INPUT	Supply Voltage Range-Lo	V_{+L}	$R_L = 10\text{ k}\Omega$, LV = Ground	4.5		9	V
	Supply Voltage Range-Hi	V_{+H}	$R_L = 10\text{ k}\Omega$, LV = No Connection	8		20	
	Supply Current	I^+	$V^+ = 4.5\text{ V}$, $R_L = \infty$, LV = GND $V^+ = 15\text{ V}$, $R_L = \infty$, LV = Open		100 0.7	500 2	μA mA
OUTPUT	Output Source Resistance	R_{OUT}	$V^+ = 4.5\text{ V}$, LV = GND $I_o = 3\text{ mA}$ $V^+ = 15\text{ V}$, LV = Open $I_o = 20\text{ mA}$		75 55		Ω
	Power Conversion Efficiency	P_{E1}	$V^+ = 15\text{ V}$, $P_L = 2\text{ k}\Omega$		92		%
	Voltage Conversion Efficiency	$V_{OUT\ E1}$	$V^+ = 15\text{ V}$, $R_L = \infty$	97	99.7		%
DYNAMIC	Oscillator Frequency	f_{osc}	$V^+ = 15\text{ V}$		10		kHz
	Oscillator Impedance	Z_{osc}	$V^+ = 4.5\text{ V}$, LV = GND $V^+ = 15\text{ V}$		1 100		M Ω k Ω

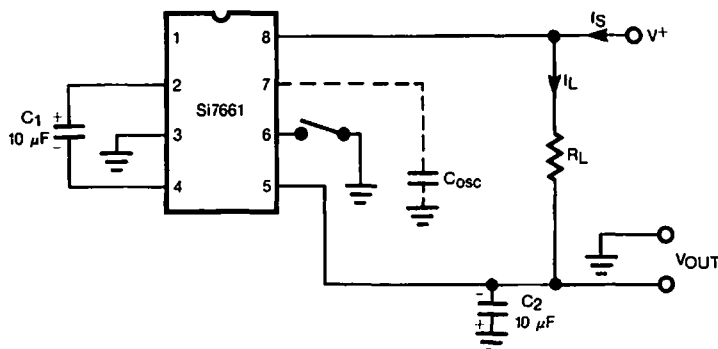
 $T_A = \text{Over Temperature Range}$

	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED:	Si7661 B/C			UNITS
				MIN ⁴	TYP ⁵	MAX	
INPUT	Supply Voltage Range-Lo	V_{+L}	$R_L = 10\text{ k}\Omega$, LV = Ground	4.5		9	V
	Supply Voltage Range-Hi	V_{+H}	$R_L = 10\text{ k}\Omega$, LV = No Connection	8		20	
OUTPUT	Output Source Resistance	R_{OUT}	$V^+ = 15\text{ V}$, LV = Open $I_o = 20\text{ mA}$			120	Ω

NOTES:

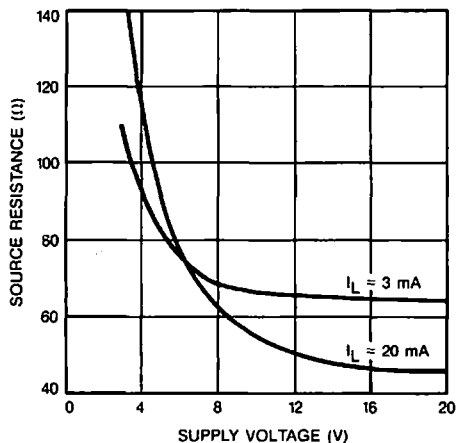
- For large value of C_{osc} (>1000 pF) the values of C_1 and C_2 should be increased to 100 μF .
- Derate 6 mW/°C above 75°C.
- Refer to PROCESS OPTION FLOWCHART for additional information.
- The algebraic convention whereby the most negative value is a minimum, and the most positive value is a maximum, is used in this data sheet.
- Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- C_1 - Pump Capacitor
 C_2 - Reservoir Capacitor

TEST CIRCUIT

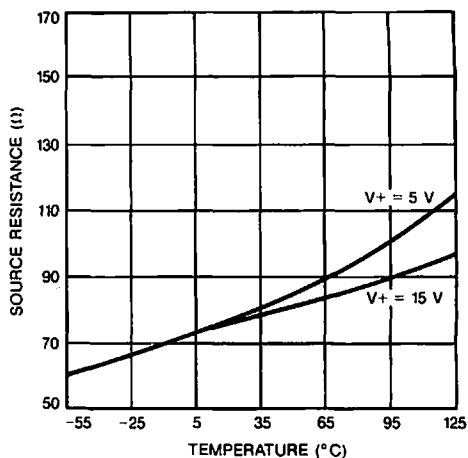


$V^+ = 15\text{ V}$, $T_A = 25^\circ\text{C}$, $C_{osc} = 0$, Test Circuit Figure 1 unless otherwise specified. (See note 6 on previous page)

TYPICAL CHARACTERISTICS



Output Source Resistance as a Function of Supply Voltage
Figure 1



Output Source Resistance as a Function of Temperature
Figure 2

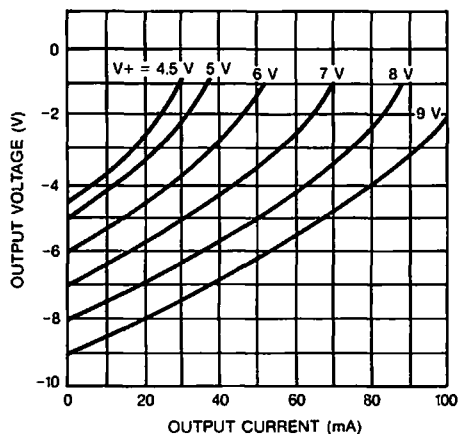


Figure 3

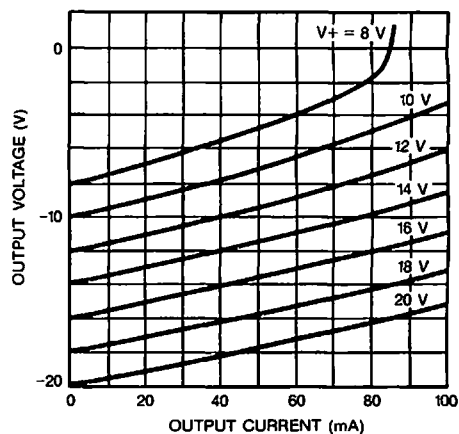
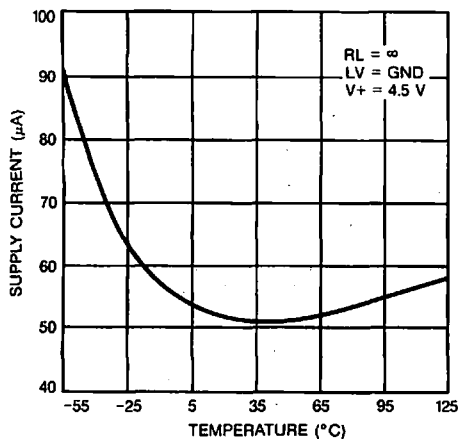
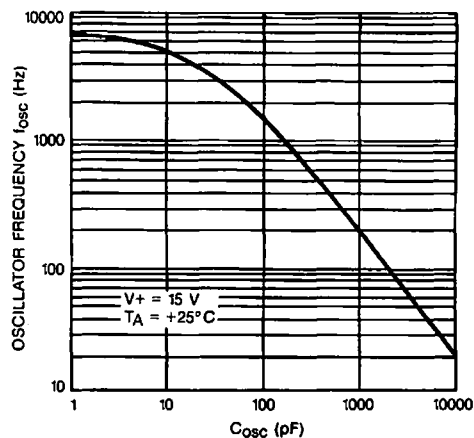


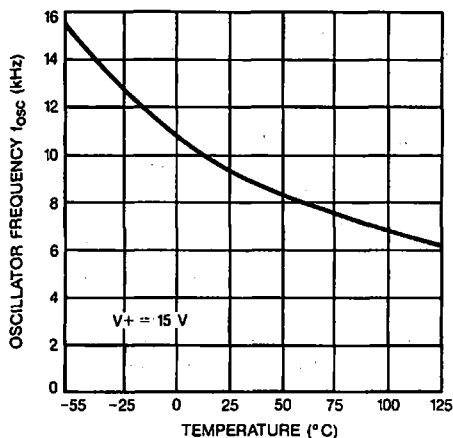
Figure 4



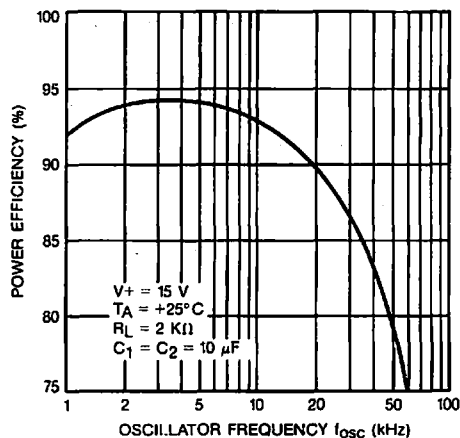
Supply Current vs Temperature
Figure 5



Frequency of Oscillation as a Function of
External Oscillator Capacitance
Figure 6



Unloaded Oscillator Frequency as a
Function of Temperature
Figure 7



Si7661 Power Efficiency vs Oscillator Frequency
Figure 8

PIN DESCRIPTION

Pin Number	Symbol	Pin Description
1	—	No connection.
2	CAP+	Positive terminal connection for pump capacitor.
3	GND	Input and/or output ground reference.
4	CAP-	Negative terminal connection for pump capacitor.
5	VOUT	Output of the voltage converter.
6	LV	Low Voltage. Connection to ground shorts out internal power supply regulator for operation below 9.0 volts.
7	OSC	OSCillator input. External clock input to this pin will override the internal oscillator. The internal oscillator frequency can be slowed by connecting an external capacitor between this pin and ground. (See Figure 6)
8	V+	Input voltage connection.

APPLICATION HINTS

The Siliconix Si7661 device is a **VOLTAGE** source, not a **CURRENT** source. Therefore, any heavy load current will either greatly reduce the output voltage (possibly out of the desired range) or will cause the device to go into power shutdown. To avoid problems, keep the **VOLTAGE** conversion concept in mind.

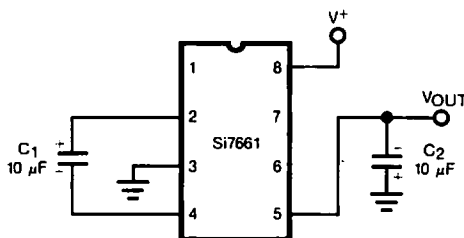
The Si7661 is intended for use as a voltage inverter. However, with a few added components, the inverter circuit can be rearranged to provide many different voltage levels. Some of the possibilities include voltage inversion, voltage multiplication, and even simultaneous inversion and multiplication. For more information refer to Application Note AN84-2.

There are many applications where a low current negative supply made with an Si7661 would do just as well as a

full conventional negative supply or DC-to-DC converter module. Some examples are negative power supplies for microprocessors, dynamic RAMs, or data acquisition systems.

In addition, the extended input voltage range of the Si7661 lends itself for use as a negative rail generator for most op-amp applications.

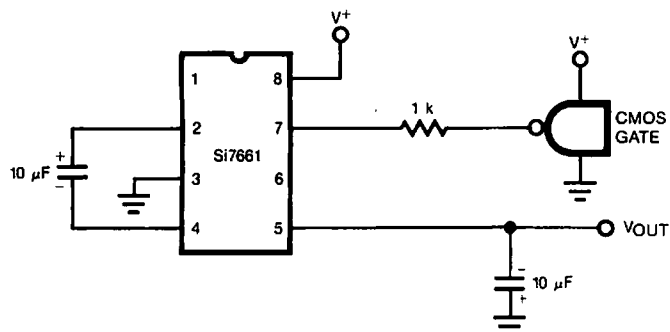
If the output ripple of the Si7661 is too great for a particular application, the value of the pump (C_1 , Fig. 9) and reservoir (C_2) capacitors can be increased to reduce this effect. However, it is important to note that increasing the capacitor size can lead to surge currents at turn-on. If the current is too great, the power dissipation of the device can be exceeded, causing destruction of the device. The maximum recommended capacitor size is 1000 μF .



Basic Inverter Circuit
Figure 9

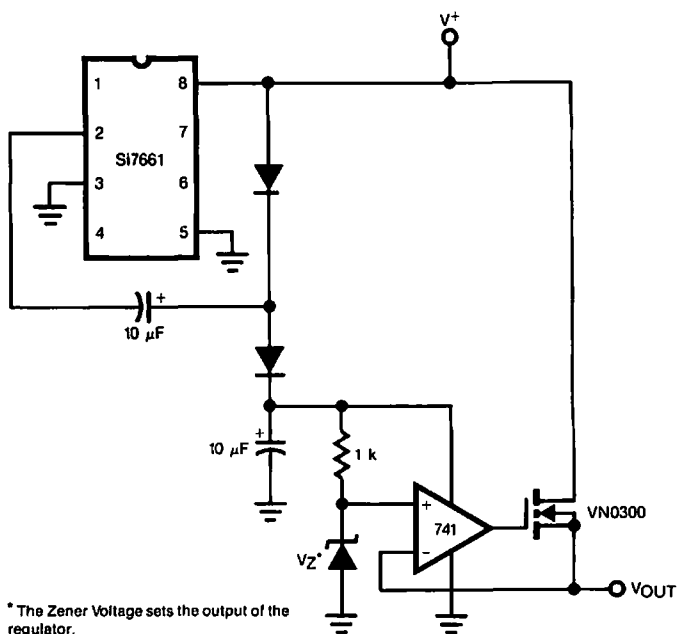
APPLICATION HINTS (Cont.)

When an external clock is used to drive the Si7661 a 1000 ohm resistor should be used between the clock source and the OSC input (pin 7) as shown in Figure 10.



Driving the Si7661 With an External Clock
Figure 10

Figure 11 shows a regulator that will operate with much less than 1 volt drop between V^+ and V_{OUT} at large output currents. Most three terminal voltage regulators would exhibit a drop of a volt or more under these conditions.



* The Zener Voltage sets the output of the regulator.

Low Loss Regulator Circuit
Figure 11

0 Introduction

1 Interface

2 Analog Switches/Multiplexers

3 A/D Converters

4 D/A Converters

5 Linear

6 Power Conversion

7 **Telecommunications**

8 Die Process & Topography

9 Package Data

10 Applications Information

11 Other Siliconix Products

12 Publications Index

13 Worldwide Sales Offices

Index

TELECOMMUNICATIONS

Title	Page
Introduction	7-3
DF320/DF320A/DG322A	7-5
DF820	7-15

Telecommunications Product Selector Guide¹

Function	Part No. Package Information	Specifications	Features
Loop Disconnect Dialer (pulse dialer)	DF320/320A/322A 18 pin plastic, 18 pin ceramic	Operation from 2.5 to 5V supply Low standby power dissipation: 3 μ W Low dynamic power consumption: 600 μ W On-chip oscillator for 3.579545 Mhz crystal	Redial capability Hold capability delays impulsing Post-impulsing pause of 33 ms Mask during impulsing and interdigit pause Selectable make-break ratio 10, 16, 20, 932 Hz impulsing rates Inter-digital pause of 800 ms
Loop Disconnect Dialer (pulse dialer)	DF820 18 pin plastic, 18 pin ceramic	Operation from -2.7 to -10V supply Off hook quiescent current 80 μ A (typ) On chip oscillator for 3.579545 Mhz crystal	24 digit last number redial Single and double contact keypad interface Multiple mode and dial pulse outputs Directory assistance

NOTES:

1. Devices shown in **boldface** are recommended for new designs.
2. Preliminary product. Specifications subject to change. Contact factory on availability.

INTRODUCTION

Telecom

The telephone appeared as a working instrument way back in 1876, but it was not until Strowger invented the two motion step by step switch in 1891 that an automatic system existed. The stepping of these two motion selectors was under the direct control of the subscriber. Movement of the Strowger switch is caused by interrupting the current flow in the telephone line by means of rotary dial. This was the start of the loop disconnect system.

Since then, crossbar and electronic (reed relay) exchanges have been developed and installed and these are also based on the loop disconnect principle.

Siliconix produced the first CMOS loop disconnect dialer in 1976 to replace the rotary dials on existing telephones and has sold over 5 million devices world-wide since its introduction.

There are still a high proportion of loop disconnect exchanges in

existence and with a lifespan of at least 20 years left in them, the loop disconnect telephone will be required for some time yet.

It is because of this future demand that in 1983 Siliconix introduced its latest in the range of loop disconnect dialers - the DF820. This has an improved feature set and reduces the number of interface components required for a telephone handset. In addition, the DF820 has the facility for entering a number string into the telephone without impulsing the line and then redialling this number at a later time - this can be used while talking to a telephone operator. The DF820 also has the capability to store a 4 digit and a 24 digit number simultaneously.

Both the DF320 and DF820 have versions available to meet most telephone specifications throughout the world today and as the loop disconnect system is going to be with us for quite a few years, the Siliconix range of dialers is waiting to meet your requirements.

GLOSSARY OF TERMS

A & B Legs

The pair of wires connecting the customer and the telephone exchange - see also tip and ring.

Break Period

The period in which the loop current falls to the lower of the two values used to represent signaling pulses.

Central Office/Switch

Main telephone exchange.

Exclusive Line

Link between the customer and the telephone exchange.

Inter-Digit Pause (IDP)

The interval between successive pulse trains.

Impulsing Ratio

The ratio between the make and break periods.

Line Break

The temporary disconnection of the telephone line when the subscriber is switched from a PABX to the main exchange.

Loop-Disconnect Signalling

A form of signalling by the apparatus connected to the line, where the basic network is repeatedly interrupted by signalling pulses during which the loop current falls to a very low value.

Make Period

The period in which the loop current returns to the higher of the two values used to represent signaling pulses.

Mute Switch

Relay contact or semiconductor device for muting the speech network during dialing to prevent objectionable clicks in the receiver.

Pre-Impulsing Pause (PIP)

The time delay between the disconnection of the speech network and the commencement of dialing.

Post Operative Impulsing Pause (POIP)

The time delay between the end of the dialing pulse train and the reconnection of the speech network.

Public Switched Telephone Network (PSTN)

Pulse Distortion

The effect on the impulsing ratio by the circuitry and telephone line when connected to an otherwise perfect dialling IC.

Sidetone

The reproduction of sounds in the earpiece of the telephone which are picked up by the associated telephone microphone.

Tip and Ring

The pair of wires connecting the subscriber to the central office —see also A & B Legs.

DF320/DF320A/DF322 CMOS Loop Disconnect Dialers



FEATURES

- 2.5 V to 5.5 V Operation
- 6 μ W Standby Dissipation
- Selectable M/S and Impulsing Speed
- Integrated Functions for Fewer External Components

BENEFITS

- Operates on Long and Short Loops
- Presents No Load to Voice
- Versatile
- Low Cost System Implementation

APPLICATIONS

- Push Button Telephones
- Repertory Dialers
- Telex
- Mobile Telephones
- Emergency Number Dialers

DESCRIPTION

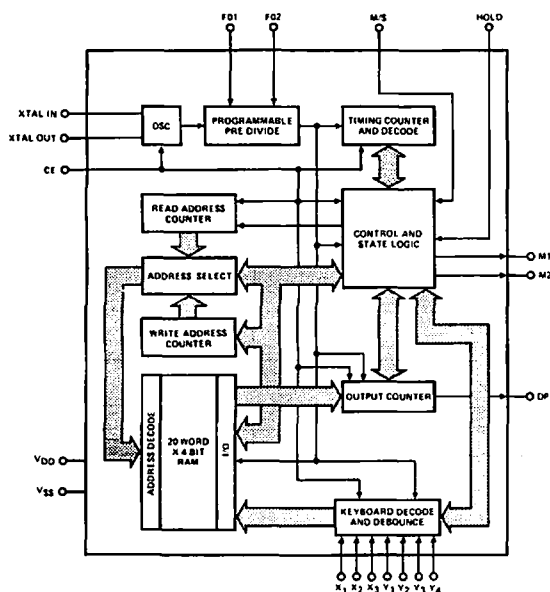
The DF320 series of monolithic CMOS Loop Disconnect Dialers each contain all the logic necessary to interface a standard double contact keyboard to a telephone system requiring loop disconnect signaling.

The DF320 provides the functions most commonly required in the push button telephone application. M1 is the masking option which remains at logic "1" throughout the dialing sequence. The DF322 is identical to the DF320 except that M2 is offered instead of M1. The M2 masking option is at logic "1" only during impulsing, allowing the telephone line to be monitored during the IDP. The DF320A has an extended post impulsing pause of 500 ms.

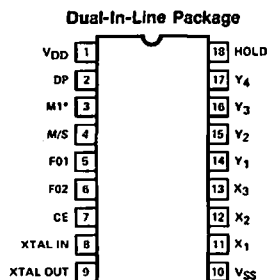
A dial pulsing output and two output options are provided to control the impulsing (loop disconnect) and muting functions. The circuit is capable of storing a number string of up to 20 digits and re-dialing this stored number automatically at a later time, initiated by a RE-DIAL input code. Impulsing mark/space ratio (M/S), and impulsing rate are pin programmable to meet most telephone authority specifications.

External component count is minimized by the inclusion of an on-chip clock oscillator, high impedance pull-down terminations to programming inputs as well as pull-up terminations to the keyboard giving direct interfacing.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



*M2 ON DF322DJ, DF322DK, DF322DP

Order Numbers:

DF320DJ, DF320ADJ, or DF322DJ
See Package 19

DF320DK, DF320ADK, or DF322DK
See Package 23

DF320DP, DF320ADP, DF322DP
See Package 20

ABSOLUTE MAXIMUM RATINGS

DF320/DF320A/DF322

V_{DD} - V_{SS} -0.3 V to 8 V
 Voltage on Any Pin V_{SS} - 0.3 V to V_{DD} + 0.3 V
 Current at Any Pin 10 mA
 Operating Temperature -40 to +85°C
 Storage Temperature (K Package) -65 to +150°C
 (J Package) -65 to +125°C

Power Dissipation (J and K Package)* 450 mW

*Derate 6.3 mW/°C above 25°C. All leads soldered to PC board.

ELECTRICAL CHARACTERISTICS^{1, 2}

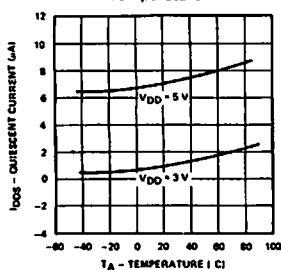
T_A = 25°C

PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: V _{DD} = 3.0 V, f _{CLK} = 3.579545 MHz	LIMITS			UNIT
			MIN ³	TYP ⁴	MAX	
Supply Voltage Operating Range	V _{DD}		2.5		5.5	V
Standby Supply Current	I _{DSS}	CE = V _{SS}		2	10	μA
Operating Supply Current	I _{DD}	C _{XTALOUT} = 12 pF		155	250	
Keypad Input Pull-Up Transistor Source Current	I _{ILK}	V _{IN} = V _{SS}	-10	-6	-0.5	
Keypad Input Leakage Current	I _{IHK}	V _{IN} = V _{DD}		0.1		nA
Programming Input Leakage Current	I _{ILP}	V _{IN} = V _{SS}		-0.1		
Programming Input Pull-Down Transistor Sink Current	I _{IHP}	V _{IN} = V _{DD}	0.5	3	10	μA
Input Logic "O" Level (All Inputs)	V _{IL}				0.65	V
Input Logic "I" Level (All Inputs)	V _{IH}		2.45			
Output Voltage Low Level (DP, M1, M2)	V _{OL}	No Load		0	0.01	
Output Voltage High Level (DP, M1, M2)	V _{OH}	No Load	2.99	3		mA
Output Current Low Level (DP, M1, M2)	I _{OL}	V _{OUT} = +2.3 V	0.5	1.5		
Output Current High Level (DP, M1, M2)	I _{OH}	V _{OUT} = +0.7 V		-1.5	-0.5	
Output Rise Time (DP, M1, M2)	t _r	C _L = 50 pF		1		μs
Output Fall Time (DP, M1, M2)	t _f			1		
Maximum Clock Frequency	f _{CLK}		3.58			MHz
Mark To Space Ratio	M/S	See Table 1	3:2		2:1	
Interdigit Pause	IDP	T = Selected Impulsing Period (See Table 1)		8T		ms
Impulsing Rate = 1T		See Table 1	10		932	Hz
Clock Start Up Time	t _{ON}	Timed From CE = Logic "I"		1.5	4	ms
Input Capacitance	C _{IN}	Any Input		5		pF
Post Impulsing Pause	POIP	DF320, DF322 DF320A		0.3T		ms
				5T		

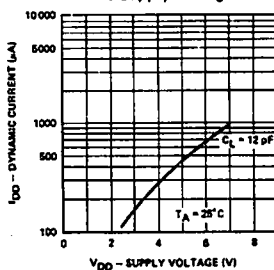
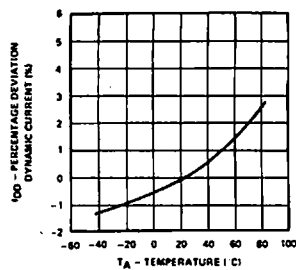
NOTES:

1. Refer to PROCESS OPTION FLOWCHART for additional information.
2. All voltages referenced to V_{SS} unless otherwise noted.
3. The algebraic convention whereby the most negative value is minimum, and the most positive value is maximum, is used in this data sheet.
4. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

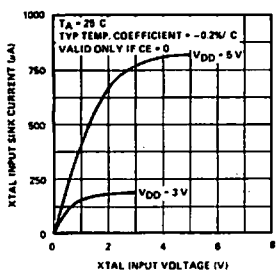
Typical Quiescent Current vs Temperature



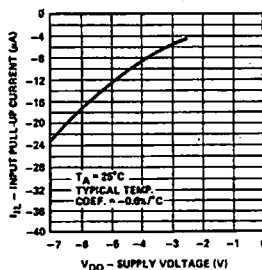
Typical Dynamic Current vs Supply Voltage

Typical Percentage Deviation of Dynamic Current vs Temperature (Normalized to $25^{\circ}C$)

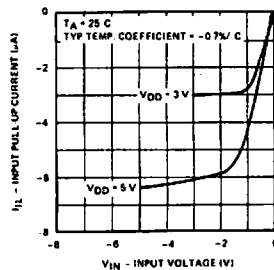
Typical XTAL IN Input Clamp Characteristics



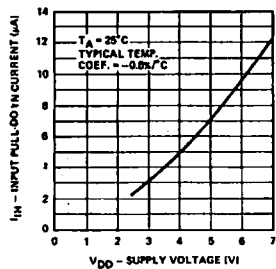
Typical Input Pull-Up Current vs Supply Voltage (X1, Y2, X3, Y1, Y2, Y3, Y4)



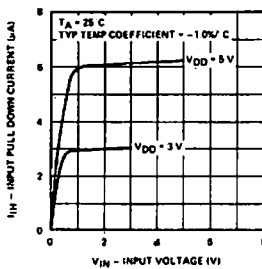
Typical Input Pull-Up Characteristics



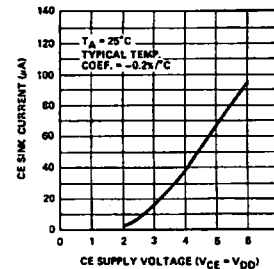
Typical Input Pull-Down Current vs Supply Voltage (M/S, FO1, FO2, Hold)



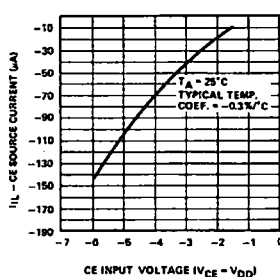
Typical Input Pull-Down Characteristics



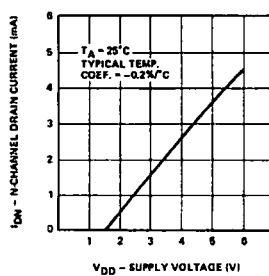
Typical CE Sink Current



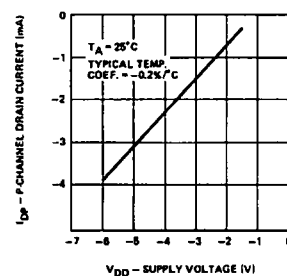
Typical CE Source Current



Typical N-Channel Output Drain Characteristics (DP, M1, M2)



Typical P-Channel Output Drain Characteristics (DP, M1, M2)

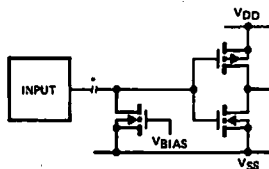
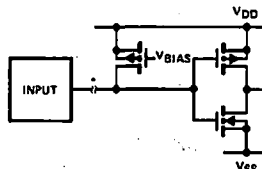
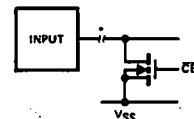
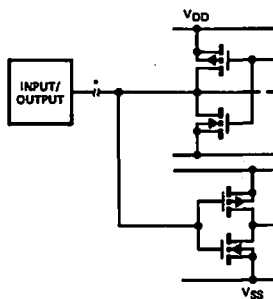
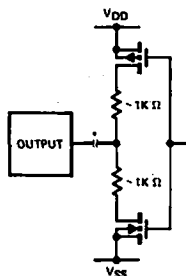
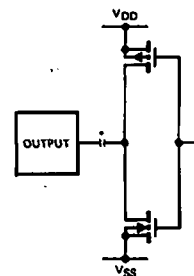


TYPICAL CHARACTERISTICS (Cont.)

Table 1

PIN FUNCTION	DESCRIPTION																									
VDD	Positive voltage supply																									
DP	Dial Pulsing Output Buffer																									
M1	Mask 1 (Buffered Output) = Logic "1" during Dialing Sequence																									
M2	Mask 2 (Buffered Output) = Logic "1" during Impulsing																									
M/S	Mask/Space (Break/Mask) Ratio select. On-chip active pull-down to V _{SS} . <table border="1"> <tr> <td>O C</td><td>2:1</td></tr> <tr> <td>VDD</td><td>3:2</td></tr> </table> Note: O C = Open circuit, see Figure 7	O C	2:1	VDD	3:2																					
O C	2:1																									
VDD	3:2																									
F01, F02	Impulsing Rate Selection. On-chip active pull-down to V _{SS} . <table border="1"> <thead> <tr> <th>F01</th><th>F02</th><th>Nominal Impulsing Rate</th><th>Actual* Impulsing Rate</th><th>System Clock Frequency</th></tr> </thead> <tbody> <tr> <td>O C</td><td>O C</td><td>10 Hz</td><td>10.13 Hz</td><td>303.9 Hz</td></tr> <tr> <td>O C</td><td>VDD</td><td>20 Hz</td><td>19.42 Hz</td><td>582.6 Hz</td></tr> <tr> <td>VDD</td><td>O C</td><td>932 Hz</td><td>932.17 Hz</td><td>27,965.1 Hz</td></tr> <tr> <td>VDD</td><td>VDD</td><td>16 Hz</td><td>15.54 Hz</td><td>466.1 Hz</td></tr> </tbody> </table> *Assumes f _{CLK} = 3.579545 MHz	F01	F02	Nominal Impulsing Rate	Actual* Impulsing Rate	System Clock Frequency	O C	O C	10 Hz	10.13 Hz	303.9 Hz	O C	VDD	20 Hz	19.42 Hz	582.6 Hz	VDD	O C	932 Hz	932.17 Hz	27,965.1 Hz	VDD	VDD	16 Hz	15.54 Hz	466.1 Hz
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O C	VDD	20 Hz	19.42 Hz	582.6 Hz																						
VDD	O C	932 Hz	932.17 Hz	27,965.1 Hz																						
VDD	VDD	16 Hz	15.54 Hz	466.1 Hz																						
CE	Chip Enable. Input/Output, left open it is internally controlled by keyboard decode logic. Can be externally forced for manually enabling chip.																									
XTAL IN	Crystal Input. Active, clamped low if CE = "0", high impedance if CE = "1".																									
XTAL OUT	Crystal Output. Buffer to drive crystal. Capacitive load on-chip.																									
VSS	System ground																									
X ₁ , X ₂ , X ₃	Column keyboard inputs having active pull-ups to VDD. Active LOW																									
Y ₁ , Y ₂ , Y ₃ , Y ₄	Row keyboard inputs having active pull-ups to VDD. Active LOW																									
HOLD	Prevents further impulsing. On-chip active pull-down to V _{SS} . <table border="1"> <tr> <td>O C</td><td>Normal Operation</td></tr> <tr> <td>VDD</td><td>No Impulsing. If activated during impulsing, hold occurs when the current digit is complete.</td></tr> </table>	O C	Normal Operation	VDD	No Impulsing. If activated during impulsing, hold occurs when the current digit is complete.																					
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INPUT OUTPUT SCHEMATICS

M/S, F01, F02, HOLD
Figure 1X₁, X₂, X₃, Y₁, Y₂, Y₃, Y₄
Figure 2XTAL IN
Figure 3CE
Figure 4DP, M1, M2
Figure 5XTAL OUT
Figure 6

*Circuit Protection Not Shown

FUNCTIONAL DESCRIPTION

1.0 Clock Oscillator — The on-chip oscillator amplifier is connected between the XTAL IN and XTAL OUT pins. The oscillator is completed by connecting a 3,579,545 Hz crystal in parallel with a 10M Ω resistor between XTAL IN and XTAL OUT. When CE = "0" an N-channel transistor clamp is activated, disabling oscillator operation. On the transition of CE to logic "1" a fast oscillator turn-on circuit kicks XTAL IN voltage to the amplifier bias point allowing oscillator operation within 4 ms. The basic clock frequency of 3.58 MHz is predivided by a programmable counter to provide the chip system clock.

As an alternative, an LC oscillator can be formed as shown in Figure 15. Selection of $f_{CLK} = 38.4$ kHz with F01 connected to V_{DD} will give an impulsing rate of 10 Hz.

It is also possible to control the DF320, DF320A, DF322 from an external clock applied to XTAL IN.

2.0 Chip Enable, CE — The Chip Enable pin is used to initialize the chip system. CE = "0" forces the chip into the static standby mode. In this mode the clock oscillator is OFF, internal registers are reset with the exception of the WRITE ADDRESS COUNTER and the circuit is ready to receive a new number or re-dial. While CE = "0" data cannot be received by the chip, but data previously entered and stored is maintained. When CE = "1" the clock oscillator is operating, the internal registers are enabled, and data can be entered from the keyboard up to a maximum of 20 digits.

CE is primarily controlled by a logic gate with function

$$F = \text{KEYBOARD INPUT} + M1 + \text{HOLD}$$

where + denotes logical OR.

To operate this gate, a resistor and capacitor should be connected in parallel between CE and V_{SS} . When the chip is used in the CE INTERNAL CONTROL MODE power ON reset occurs when V_{DD} is applied, since a logic "0" appears on the CE pin. The chip remains in the static standby condition until it receives the first valid keyboard input after V_{DD} is applied. This is statically decoded and causes CE = "1", hence enabling the clock oscillator. The debounce counter is then clocked by the system clock until the valid data condition is recognized. Data is then written into the on-chip RAM. CE is maintained at logic "1" by M1 during dialing.

The WRITE ADDRESS COUNTER is reset on recognition of the first valid debounced keyboard input provided that it is decoded during t_d of the pre-impulsing pause PIP (see Figure 8). In the CE INTERNAL CONTROL MODE this condition will always apply. When all keyed digits have been dialled, M1 goes to logic "0" and hence the chip returns to the static standby condition. If digits are sub-

sequently keyed during the same OFF-hook period, after a pause in dialling for example, the digit string will be recognized as a new number. This is not important provided RE-DIAL operation is not required.

The alternative to the CE INTERNAL CONTROL MODE is to override the internal logic gate with an externally derived signal. This mode of operation is referred to as the CE EXTERNAL CONTROL MODE. Figure 7 shows that if CE goes to logic "1" in the absence of a keyboard input, a single pulse of duration t_d is generated on M1. This pulse is intended to initialize a bistable latching relay used as shown in Figure 12. Immediately prior to M1 going to logic "1", the WRITE ADDRESS COUNTER is reset. All digits keyed subsequently are entered into consecutive RAM locations up to a maximum of 20. After the WRITE ADDRESS COUNTER has been reset, the RE-DIAL input code will not be recognized by the circuit. It is necessary that CE be maintained at logic "0" > 1 μ s after V_{DD} is applied in order to ensure correct system initializing. If CE is linked to V_{DD} by the method shown in Figure 12, adequate delay is obtained.

3.0 Data Entry — Data is entered to the circuit via a double contact keyboard connected as shown in Figure 10. Keyboard inputs are active low and encoded as shown in Table 2.

Keyboard Code
Table 2

No. of O/P Pulses	Digit	Y ₁	Y ₂	Y ₃	Y ₄	X ₁	X ₂	X ₃
1	1	0	1	1	1	0	1	1
2	2	0	1	1	1	1	0	1
3	3	0	1	1	1	1	1	0
4	4	1	0	1	1	0	1	1
5	5	1	0	1	1	1	0	1
6	6	1	0	1	1	1	1	0
7	7	1	1	0	1	0	1	1
8	8	1	1	0	1	1	0	1
9	9	1	1	0	1	1	1	0
10	0	1	1	1	0	1	0	1
RE-DIAL		1	1	1	0	1	1	0

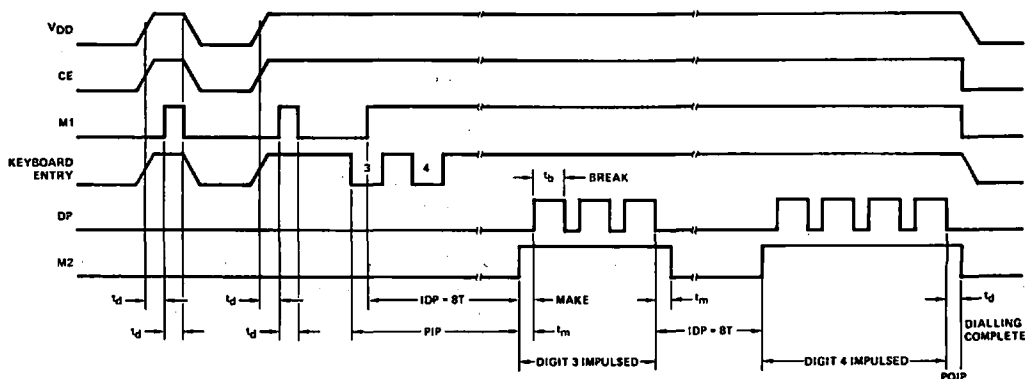
NOTE: "0" indicates pin taken low.

Keyboard inputs are fully decoded eliminating any possibility of invalid codes being recognized. A BCD format is used on-chip for data storage. Valid inputs have contact bounce removed via the debounce counter. Operation is illustrated in Figure 9. Input data is not written into the RAM until the input code has been present for a minimum of 3P and maximum of 4P (P = System Clock Period). The 1P uncertainty arises since data entry is not synchronized to the system clock. This is indicated by the shaded area on the keyboard entry waveform of Figure 9. The trailing edge of a keyboard entry is also debounced. The operation

of the debounce circuitry results in a maximum data entry rate of $\text{SYS CLK} \div 9$. Referring to Figure 9, data must remain stable during the RAM data entry period. Maximum contact bounce rejection is 10 ms at 10 Hz, 6.3 ms at 16 Hz or 5 ms at 20 Hz impinging rates. Minimum data valid time is 16.7 ms at 10 Hz, 10.4 ms at 16 Hz or 8.4 ms at 20 Hz impinging rates.

Upon recognition of the first keyboard input of a number string, the dial out sequence is initiated by a pre-impulsing pause (Figure 7). The WRITE ADDRESS COUNTER is

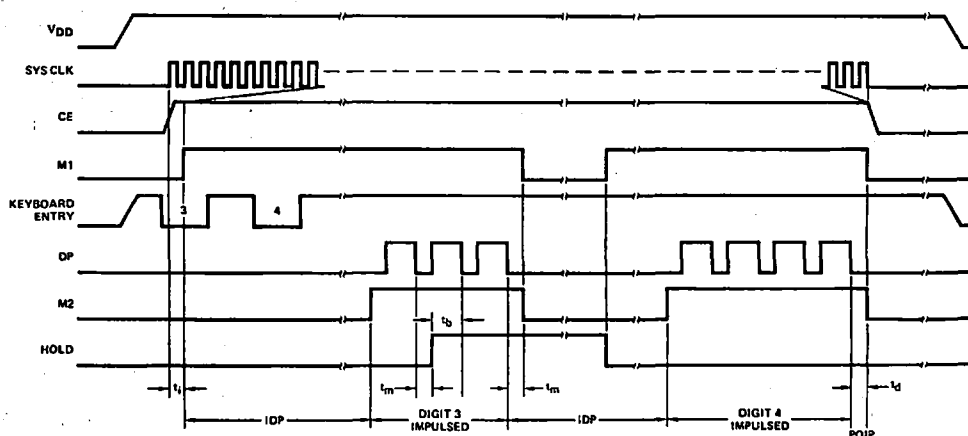
incremented on each digit entry. The contents of this counter indicate the length of the number to be dialed. The RE-DIAL code is recognized only if it is presented to the chip a maximum of 5P after $\text{CE} = "1"$. Decoding of RE-DIAL then inhibits the reset of the WRITE ADDRESS COUNTER, initiates the dialing sequence and the previous number string entered is dialed. If the circuit application is to utilize RE-DIAL, external CE control is necessary in some cases to ensure that $\text{CE} = "1"$ from the first keyboard entry throughout dialing in order to ensure all digits entered are stored consecutively should a delay occur during dialing.



NOTES:

- (1) $t_d = 10 \times P$
 $P = \text{System clock period} = T/30$
 $T = \text{selected impulsing period}$
- (2) Pre-Impulsing Pause (PIP) = $8T + t_d$
- (3) Post-Impulsing Pause (POIP) is equal to t_d ms on DF320, DF322 and $5T$ on DF320A.
- (4) t_b/t_m is the BREAK/MAKE RATIO. $T = (t_m + t_b)$ ms.
 $t_m = 10 \times P$ for 2:1 M/S ratio. $t_m = 12 \times P$ for 3:2 M/S ratio.

Loop Disconnect Dialer Timing CE-External Control
Figure 7



NOTE:

- (1) $t_i = t_{ON} + t_d$ where $t_{ON} = \text{Clock Start Up Time}$

Loop Disconnect Dialer Timing CE-Internal Control
Figure 8

FUNCTIONAL DESCRIPTION (Cont.)

4.0 Dialing Sequence - The dialing or impulsing sequence is initiated on recognition of the first keyboard entry after $CE = "1"$. The dialing sequence is identical for both internal and external control of CE . (See Figure 7 and 8).

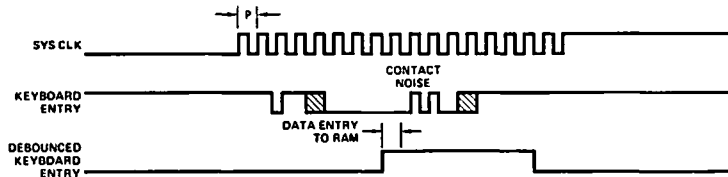
The basic impulsing pulse train is derived from the **TIMING COUNTER AND DECODE**. The IDP is timed by forcing a code on the **OUTPUT COUNTER** and inhibiting DP for the duration of IDP. The **READ ADDRESS COUNTER** then addresses the **RAM** and the first digit is used to program the decode of the **OUTPUT COUNTER**. A number of dial pulses is output via DP corresponding to the BCD data read from the **RAM**. At the completion of the digit, the **READ ADDRESS COUNTER** is incremented. The sequence continues until coincidence is recognized between the **READ ADDRESS COUNTER** contents and the **WRITE ADDRESS COUNTER** contents. The post-impulsing pause $POIP$, is then generated. The circuit then enters the dynamic standby condition if CE is maintained at logic "1" by external control, or the static standby condition if CE **INTERNAL CONTROL MODE** is used.

Impulsing rates, impulsing mark-to-space ratio and inter-digital pause are programmable as shown in Table 1.

The dialing sequence can be interrupted by applying logic "1" to **HOLD**. If $HOLD = "1"$ is applied during dialing of a digit, the circuit does not enter the **HOLD** mode until the digit is complete. In the **HOLD** mode $M1 = "0"$, allowing the telephone line to be monitored. When **HOLD** is released dialing continues preceded by an IDP. (See Figure 8). **HOLD** is used to extend the IDP allowing intermediate dial tone recognition if **RE-DIAL** is used in a **PABX** for example. Operation can be manual or via external control logic as shown in Figure 13.

NOTES:

- (1) The keyboard input decoding is mask programmable to suit different input codes.
- (2) The timing circuitry is mask programmable to give different M/S ratios and IDP values.
- (3) The clock predivision circuitry is mask programmable allowing use of different crystal or external clock frequencies.
- (4) The logic sense of DP , $M1$ and $M2$ outputs is mask programmable.



Keyboard Input Debounce Timing Diagram
Figure 9

APPLICATIONS

The circuit of Figure 10 shows a method of connecting the DF320 in parallel with the telephone network.

When the handset is lifted and power applied to the circuit Q_2 is fed base current through R_2 which in turn drives Q_1 . C_2 is charged via R_3 in series with D_1 to $(V_Z1 - 0.7)V$. When the minimum operating V_{DD} voltage is reached, power ON reset occurs via the CE network of C_1 and R_8 . Q_2 is maintained in the ON condition by G_1 while Q_3 , and hence Q_4 , are held OFF by G_2 . The DF320 network appears in parallel with the telephone as an impedance $> 10K \Omega$ in the standby condition with the telephone network connected in circuit through Q_1 .

On recognition of the first keyed digit, the DF320 clock is started. $M1$ then goes to logic "1" causing Q_2 , Q_1 to turn OFF, and Q_3 , Q_4 to turn ON. Hence the majority of the line loop current now flows through Q_4 , and Z_1 . When

impulsing occurs Q_3 and Q_4 are turned OFF by DP acting on G_2 . Line loop current is then reduced to approximately $50 \mu A$ taken through R_2 , R_4 and G_2 in series.

When dialing is complete $M1$ goes to logic "0" causing the telephone network to be reconnected. The DF320 then returns to the static standby condition. If the line loop is interrupted by the cradle switch during dialing, impulsing will continue until C_2 discharges to a voltage such that R_8 pulls CE to logic "0" causing the DF320 to reset.

The diode bridge protects the network from line polarity reversal.

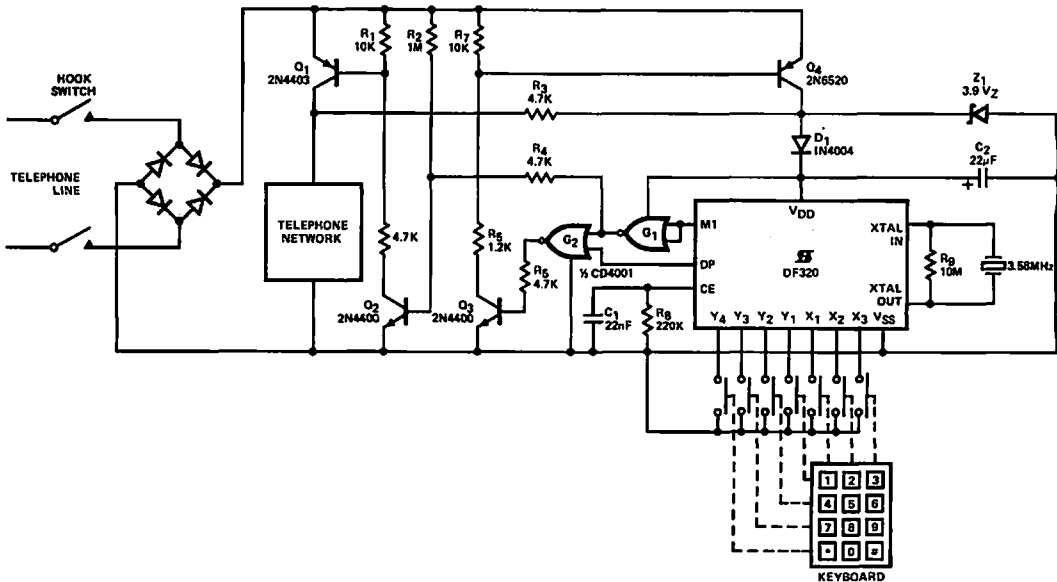
The circuit of Figure 11 shows a simple method of series connection of DF320 into the telephone set suitable for **PABX** or short line applications.

APPLICATIONS (Cont.)

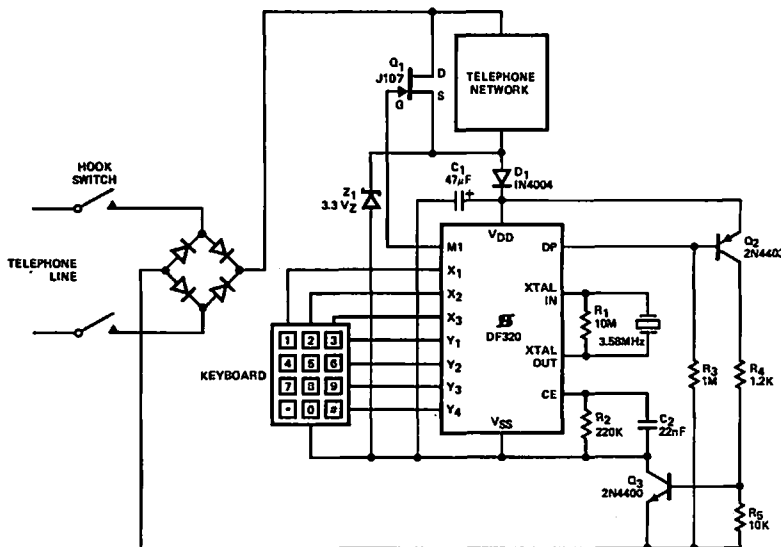
When the telephone handset is lifted, C_1 is charged via D_1 to $(V_{Z1} - 0.7)$ volts and DF320 power ON reset occurs. When the first keyed digit is recognized, M1 goes to logic "1" muting the telephone network by switching on the low ON resistance JFET Q_1 , and maximizing the line loop current for impulsing. Impulsing occurs through DP switching Q_2 , and hence Q_3 , OFF. Rapid discharge of C_1 through Z_1 is prevented during line break by the blocking diode D_1 .

When dialing is complete the circuit returns to the static standby condition and Q_1 is switched OFF. Circuit reset during a line interruption by the cradle switch is as for the parallel connection mode.

If a requirement exists that no semiconductor components should appear in the telephone loop during normal speech, the circuit of Figure 12 is required.



DF320 Parallel Telephone Connection
Figure 10



DF320 Series Telephone Connection
Figure 11

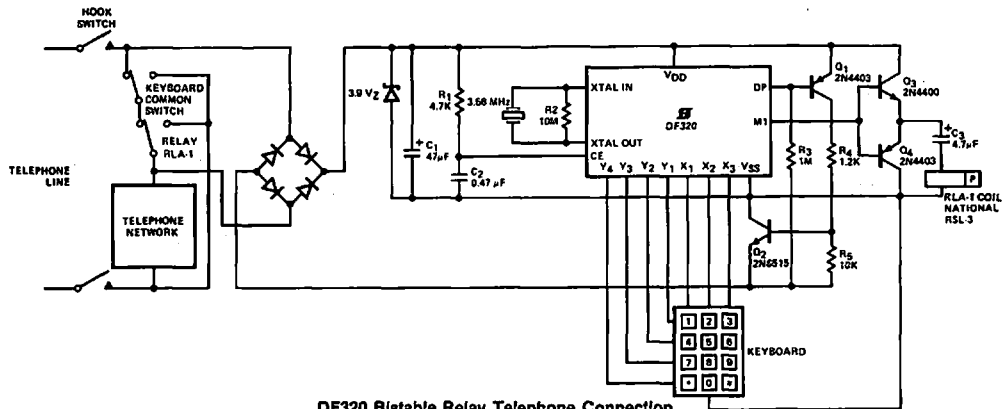
APPLICATIONS (Cont.)

While the circuits of Figures 10 and 11 did not require a common keyboard contact, it is necessary to have a common changeover switch in this case operating in conjunction with a bistable relay. In this application external control of CE is provided by the R₁, C₂ network. If, when the handset is lifted, the relay contact is such that the DF320 network is connected in circuit, it is necessary to initialize this relay to reconnect the telephone network. This is achieved by the single pulse which occurs on M1 if CE goes to logic "1" in the absence of a keyboard input (Figure 7).

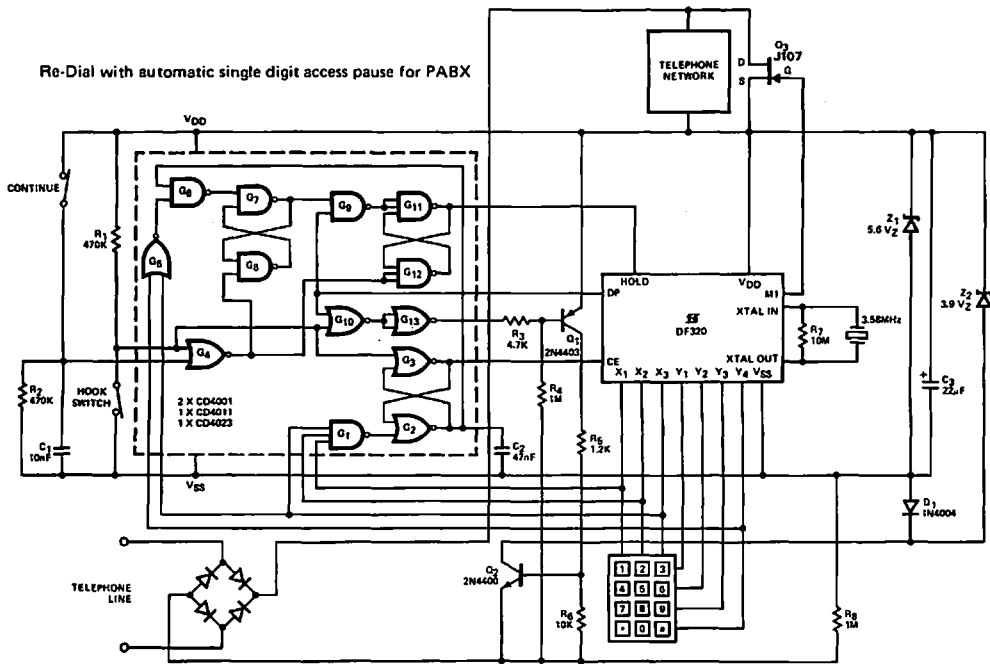
When the first digit is keyed, the DF320 network is connected into the telephone loop and the telephone network

short circuited by the keyboard common switch. M1 then goes to logic "1" switching the bistable relay hence maintaining the DF320 network in circuit. Impulsing occurs through DP switching Q₁ OFF which in turn switches Q₂. When dialing is complete the bistable relay is pulsed, switching the telephone network back in circuit and short circuiting the DF320 network.

The circuit of Figure 13 shows additional gating circuitry to provide an automatic access pause after the first digit is dialed, by controlling HOLD. This is useful in PABX applications, eliminating the need for a manual hold facility if RE-DIAL is used.



DF320 Bistable Relay Telephone Connection
Figure 12



DF320 Series Telephone Connection
Figure 13

The basic interface circuit is similar to that shown in Figure 11. Muting is achieved by Q₃ and line switching by Q₂ driven by Q₁.

In the ON-hook condition, Q₁ is held OFF by G₁₃ and standby current is supplied to the DF320 network by R_g; providing voltage limiting. CE is clamped to logic "0" by G₃. The DF320 is in the static standby mode and the previously dialed number is stored.

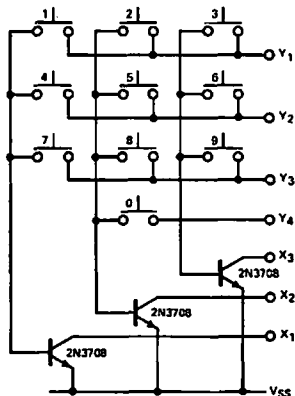
When the handset is lifted, G₁₃ goes to logic "0" switching Q₁, and hence Q₂, ON. The DF320 network V_{DD} is now given by (V_{Z2} - 0.7) volts. The DF320 remains in the static standby mode until the first key operation. G₁ decodes the common key function toggling the latch formed by G₂ and G₃ causing CE = "1". CE remains at logic "1" throughout the remainder of the OFF-hook condition ensuring that all digits keyed are stored by the DF320 as one number string. (See FUNCTIONAL DESCRIPTION, 3.0 DATA ENTRY).

If the first key operated is RE-DIAL, this condition is decoded by G₅, and via G₆ sets the latch formed by G₇

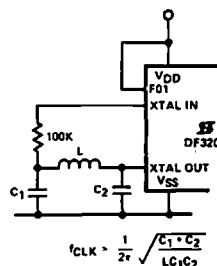
and G₈. G₉ is enabled and the first dial pulse causes the latch formed by G₁₁ and G₁₂ to be set taking HOLD to logic "1". When the first digit is complete M1 goes to logic "0" enabling the telephone network. When dial tone is recognized the CONTINUE switch is operated causing HOLD = "0" by resetting the latches formed by G₁₁, G₁₂ and G₇, G₈. The remainder of the number is then re-dialed. Subsequent operation of RE-DIAL is blocked by G₆.

Figure 14 shows a simple method of interfacing a single contact matrix-type keyboard to the DF320. Operation of a key causes the on-chip pull-up transistor of the Y input to provide base drive current to the corresponding X input external bipolar transistor, which sinks the X input pull-up current through its collector. Hence, a valid code is presented.

As an alternative to the crystal oscillator it is possible to operate the DF320 from an LC combination connected as shown in Figure 15. F01 is connected to V_{DD} selecting the 932 Hz impulsing condition. An oscillator frequency of 38.4kHz will give a 10 Hz impulsing rate.



Single Contact Keyboard Interface
Figure 14



LC Oscillator
Figure 15

DF820

Loop Disconnect Dialer



FEATURES

- 24 Digit Last Number Redial
- Number Entry Without Impulsing
- Single and Double Contact Keypad Interface
- Multiple Mute and Dial Pulse Outputs
- Directory Assistance

BENEFITS

- Operates on Long and Short Loops
- Versatile
- Presents a High Impedance to Voice

APPLICATIONS

- Push Button Telephones
- Reportory Dialers
- Telex
- Mobile Telephones
- Emergency Number Dialers

DESCRIPTION

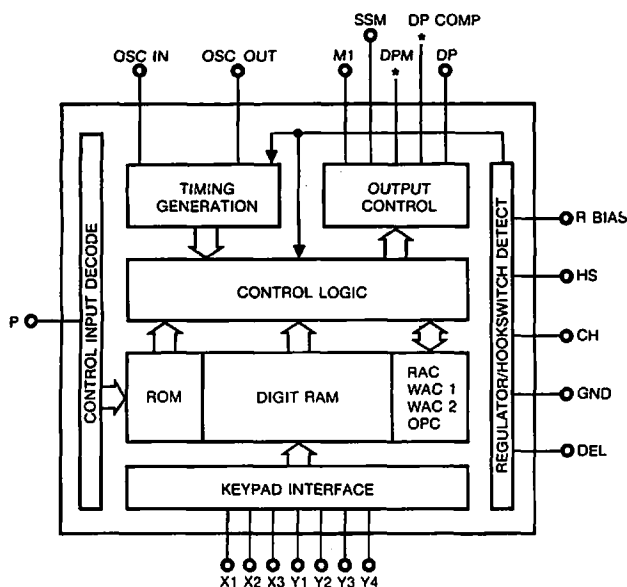
The DF820 is a monolithic CMOS Loop Disconnect Dialer containing all the logic necessary to interface a single or double contact keypad to the telephone line.

The DF820 provides the functions commonly required for push button telephone applications plus redial, PABX and

directory assistance features. The mark/space, POIP and hook switch delay are pin programmable with two options.

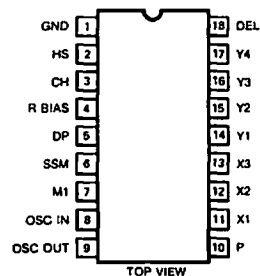
External component count is minimized due to the inclusion of an on-chip oscillator, regulator and hook switch processor.

FUNCTIONAL BLOCK DIAGRAM



*DPM and DP COMP Available as Bonding Option.

PIN CONFIGURATION



Order Number DF820DJ
See Package 19

Order Number DF820DK
See Package 23

ABSOLUTE MAXIMUM RATINGS

DF820

V_{GND} - V_{HS} -0.3 V to +12 V
 Current at GND, CH 50 mA
 (under power up conditions)
 Current at Other Pins 10 mA
 Voltage on Any Pin V_{HS} -0.3 V to V_{GND} +0.3 V
 Operating Temperature -40 to 85°C
 Storage Temperature (J Package) -65 to 125°C
 (K Package) -65 to 150°C

Power Dissipation*
 (J Package)** 450 mW
 (K Package)*** 1000 mW
 *All leads soldered to PC board.
 **Derate at 6.3 mW/°C above 25°C.
 ***Derate at 16 mW/°C above 25°C.

ELECTRICAL CHARACTERISTICS¹

T_A = 25°C

	PARAMETER		SYMBOL	TEST CONDITIONS UNLESS NOTED: V _{HS} = -4.5 V, f _{CLK} = 3.579545 MHz R _{BIAS} = 100 kΩ		LIMITS			UNIT
						MIN ²	TYP ³	MAX	
INPUT	Input Leakage Current		I _{LK}	V _{IN} = V _{CH}	Y ₁ , Y ₂ , Y ₃ , Y ₄		-0.1		nA
	Pull Down Transistor Sink Current		I _{IN}	V _{IN} = GND		0.5	5	15	
	Output Transistor Source Current		I _{IL}	V _{IN} = V _{CH}	X ₁ , X ₂ , X ₃ , Inputs/Outputs	-100			μA
	Output Transistor Sink Current		I _{IH}	V _{IN} = GND				15	
	Logic '0' Level		V _{IL}	X ₁ , X ₂ , X ₃ Y ₁ , Y ₂ , Y ₃ , Y ₄	V _{CH} + 0.5 V	V _{CH}			V
	Logic '1' Level		V _{IH}		-0.5	0			
OUTPUT	Voltage Levels DP	Low Level	V _{OL}	I _{OL} = -10 μA		V _{CH}			
		High Level	V _{OH}	I _{OH} = -250 μA DP		-0.2			
	Drive Current DPM, DPCOMP, SSM, M1	Sink	I _{OL}	V _{OUT} = -0.7 V	DPCOMP, DP, SSM, M1	100			μA
		Source	I _{OH}	V _{OUT} = -3.8 V		-100			
DYNAMIC	Clock Start Up Time ⁶		t _{ON}	V _{HS} = -3.2 V			10		
	Key Input Debounce Time		t _{DB}			5			ms
	Minimum Key Depression		t _{KD}					30	
	Off Hook To Key First Digit		t _{KF}					100	
	Output Rise Time		t _R	DPCOMP, DP, SSM, M1			1		μs
	Output Fall Time		t _F				1		
POWER	Start Up Voltage ⁴		V _{HS}			-3.2			V
	Operating Voltage Range ⁵		V _{HS}			-10		-2.7	
	Memory Retention Current Range		I _{MEM}			1			
	Off Hook Quiescent Current		I _{HS}				80	125	μA
	Operating Supply Current		I _{GND}	Hookswitch Open Circuit				150	
Output Open Circuit						300			

NOTES:

1. Refer to PROCESS OPTION FLOWCHART for additional information.
2. The algebraic convention whereby the most negative value is a minimum, and the most positive value is a maximum, is used in this data sheet.
3. Typical parametric values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
4. Start up voltage defines minimum voltage required to start oscillator within specified ON time.
5. Operating voltage range minimum defines minimum voltage required to guarantee oscillation.
6. Maximum stray capacitance of 10 pF at OSC in and OSC out pins.

PIN DESCRIPTION

Pin Function	Description
HS	Provides power to internal regulator circuit while keying in digits and dialing.
DEL	On and off hook operational states are sensed at this input pin.
GND	Standby and operating power ground.
CH	Connection for storage capacitor necessary to maintain power during line breaks and maintain memory contents while on hook.
R BIAS	Resistor bias. Pin to connect regulator biasing resistor.
OSC IN	Quartz Crystal Oscillator Input.
OSC OUT	Quartz Crystal Oscillator Output.
DP	Dial Pulsing Output - P Channel Open Drain.
DP COMP*	Dial Pulsing Output - Complementary Drive.
M1	Mute Switch Output - Complementary Drive.
DPM*	Dial Pulse Mute Output - Complementary Drive.
SSM	Mute Switch Output - Complementary Drive.
X1, X2, X3	Keypad Column Input/Outputs.
Y1, Y2, Y3, Y4	Keypad Row Inputs With Active Pull Downs.
P	Programming Pin For Selection Of: 1. Impulsing Rate - IR 2. Interdigit Pause - IDP 3. Hook Switch Delay - HSD 4. Break/Make Ratio - B/M Ratio 5. Post Impulsing Pause - POIP 6. Pre Impulsing Pause - PIP For various timing options, see Table 1. P pin should be connected to either logic '1' (GND, pin 1) or logic '0' (CH, pin 3).

*Available as bonding option.

TIMING OPTIONS

Timing Options
Table 1

	P	IR pps	IDP ms	B/M Ratio	POIP ms	HSD ms	
						Min.	Max.
DF820	0	10	800	60:40	33	225	250
	1	10	800	66:33	500	175	200

NOTES:

Positive logic is used: '1' = GND, '0' = CH.

P is Programming Pin 10.

Pre-Impulsing Pause (PIP) = Interdigit Pause (IDP).

TABLE 2 SINGLE CONTACT KEY PAD CODE

No. Of O/P Pulses	Key	Y ₁	Y ₂	Y ₃	Y ₄	X ₁	X ₂	X ₃
1	1	S	0	0	0	S	0	0
2	2	S	0	0	0	0	S	0
3	3	S	0	0	0	0	0	S
4	4	0	S	0	0	S	0	0
5	5	0	S	0	0	0	S	0
6	6	0	S	0	0	0	0	S
7	7	0	0	S	0	S	0	0
8	8	0	0	S	0	0	S	0
9	9	0	0	S	0	0	0	S
10	0	0	0	0	S	0	S	0
Redial	#	0	0	0	S	0	0	S
D/A	*	0	0	0	S	S	0	0

S = Inputs Shorted Together
 0 = Inputs Open Circuit

TABLE 3 DOUBLE CONTACT KEY PAD CODE

No. Of O/P Pulses	Key	Y ₁	Y ₂	Y ₃	Y ₄	X ₁	X ₂	X ₃
1	1	1	0	0	0	1	0	0
2	2	1	0	0	0	0	1	0
3	3	1	0	0	0	0	0	1
4	4	0	1	0	0	1	0	0
5	5	0	1	0	0	0	1	0
6	6	0	1	0	0	0	0	1
7	7	0	0	1	0	1	0	0
8	8	0	0	1	0	0	1	0
9	9	0	0	1	0	0	0	1
10	0	0	0	0	1	0	1	0
Redial	#	0	0	0	1	0	0	1
D/A	*	0	0	0	1	1	0	0

1= Inputs At Logic 1 = GND
 0 = Inputs At Logic 0 = V_{CH} Or Open Circuit

FUNCTIONAL DESCRIPTION

1. CLOCK OSCILLATOR

The on-chip oscillator amplifier is connected between the OSC IN and OSC OUT pins and has on-chip load capacitors. The oscillator is completed by connecting a 3.579545 MHz quartz crystal and 10 M Ω resistor between OSC IN and OSC OUT. Oscillation commences on depression of any key, and ceases after the post impulsing period. Any line breaks caused by change over from PABX to main exchange are processed by on-chip hookswitch timer. If the break exceeds max. HSD (see timing options) an on hook condition is recognized and the dialer resets to on hook quiescent state. Breaks less than min. HSD will be ignored. If, while timing a line break, the CH voltage should fall below the minimum required to sustain operation an internal reset circuit resets system to ON HOOK quiescent state.

2. REGULATOR CIRCUIT

Use of an on-chip regulator provides a number of important functions:

2.1 Regulates internal voltage applied to the oscillator and control logic which ensures consistent operation over a wide range of external voltages. Hence dynamic current consumption varies very little with the external voltage applied to the circuit. A capacitor connected from CH to GND maintains power to the circuit during line breaks.

2.2 Provides a supply to the digit stores and system registers (RAC, WAC 1 and WAC 2) so that information necessary for redial operation may be maintained indefinitely by connecting CH pin to the telephone line via a suitable resistor.

2.3 Hook Switch Signal Generation:

Hook Switch (HS) is a signal which indicates to the system control logic when power is applied to the chip, i.e. whether the phone is on or off hook. DEL is used to start up the operating system. It initiates clock operation and initiates the mute output to enable initialization of a bistable relay (if used) in the handset mute circuit.

Removing power from DEL when in signaling mode by line breaks or by replacing handset causes the circuit to shut down after a time given by HSD. When in the transmission mode, DEL prevents any glitches on the line (less than the time constant of the RC network) from initiating the operating system.

2.4 Eliminates need for external series regulation components normally needed in dialer circuits.

3. DATA ENTRY

All of the parts in the DF820 series interface directly with either a single contact keypad (X-Y type) or double contact keypad (2 of 7 type) without external programming. However, it is recommended that double contact types are wired with their common terminal unconnected to the supply, i.e. as a single contact type. This gives some operational advantages.

The keypad ROM and interface debounce logic ensure that only valid input codes are recognized. A key entry

must be bounce-free for a minimum of 9.05 msec (at 10 Hz IR) to guarantee entry to RAM. System is fully protected against key bounce provided that when bouncing it is not in one of the states for more than 5.075 msec (at 10 Hz IR).

The oscillator start up time enables the system to recognize a minimum key depression of 30 ms with 5 ms of bounce on leading and training edges.

The keypad interface debounce logic will correctly separate two overlapping key depressions provided the first key is depressed at least 8.23 ms before the second, and the second is released at least 13.2 ms after the first. (All times are with 10 Hz IR.) Note that with a double contact keypad, if the two keys are in the same row the second one will not be recognized.

Also, a second key depressed after the first and released before the first will be ignored. This occurs when a second key is accidentally caught while depressing intended key. Timing requirements are that either first key is depressed a minimum of 8.23 ms + bounce time before second; or first key is released at least 8.23 ms after the second.

The data entry system is highly immune to glitches coupled onto keypad inputs from line switches etc. by virtue of the debounce counter and also because valid inputs are latched on a clock edge before entry to the RAM. This removes the necessity to have keypad inputs stable for a whole clock period while data is being written into RAM.

Once a valid key entry is detected and debounced correctly, then the system is held in its operational state until all impulsing is completed or, if instructed, to reset by Hookswitch Timeout. Any digits entered in one off hook period will be stored as one number string, regardless of whether device goes into quiescent mode during sequence or not.

4. DIALING SEQUENCE

Any dialing sequence must be preceded by an OFF HOOK transition. This action forces the device to execute an initialization sequence comprising:

- Start clock oscillating.
- Decode control programming (defined by state of 'P' pin).
- Pulse mute outputs as shown in Timing Diagram. (This provides a method of initializing a latching bistable relay.)
- Internal circuitry is conditioned to look for key inputs.

The device is then looking for a valid keypad input to decide its next course of action.

The sequences of events for REDIAL and DIRECTORY ASSISTANCE are described in Sections 5 and 6 respectively.

The relevant waveform timings have been defined by action (c) of the initialization sequence.

In response to keypad entries, the device first causes the OUTPUT logic to time out a PRE-IMPULSING PAUSE (= to IDP selected). The mute outputs assume the states as shown in the timing waveform diagram.

FUNCTIONAL DESCRIPTION (Cont.)

On completion of the PRE-IMPULSING PAUSE, the output logic is loaded with the contents of the relevant RAM location defined by the READ ADDRESS COUNTER, and the READ ADDRESS COUNTER is incremented. The output logic then generates a pulse train numerically equivalent to the RAM contents, having a BREAK/MAKE ratio defined by action (b) of the initialization sequence.

On completion of impulsing a given digit, the READ and relevant WRITE ADDRESS COUNTERS are tested for equivalence. If they are not equal, a further IDP is forced on the output logic, followed by impulsing of the digit accessed. Locations of RAM, as defined by the READ ADDRESS COUNTER, are sequentially accessed until READ = WRITE, signifying all numbers entered have been impulsed. Under these circumstances, the last impulsing is followed by a POST IMPULSING PAUSE (POIP) as defined by action (b) in initialization sequence. Any further key inputs after this time will result in further writing of data into the RAM, and the incrementing of the WRITE ADDRESS COUNTER. This will result in READ not equal to WRITE and further sequential accesses of the RAM will occur until READ = WRITE.

Should a key input occur at the end of the POIP such that M1 output goes Low before data can be written to RAM, then M1 will remain Low for a count of 10 system clocks before going high again. The input data cannot be lost or corrupted by this action. This is specifically for use in relay muting applications, where voltage doubling capacitors require a certain pre-charge time.

The dialing sequence is completed by RAC = WAC, or by an ON HOOK transition.

An overflow facility is provided whereby in any OFF HOOK state, greater than 24 digits may be input and output. The 25th input overwrites location zero and so on. Once the 25th input has been written to RAM. Redial mode is inhibited until a new number string of ≤ 24 digits has been written in a successive OFF HOOK period.

5. REDIAL FACILITY

All devices have a main digit store of 24 digits and a buffer store of 4 digits. This enables any number of internal calls on a PABX system to be dialed (and redialed) and still retain the option to redial the last external call.

All devices may be used in telephones designed for both private and PABX extensions. Only the method of redial differs.

5.1 Private User

Redial # must be the first key depressed when in OFF HOOK Quiescent Mode, and cannot be re-

cognized by circuit at any other time. The circuit will always dial out the last number called regardless of length, up to the maximum of 24 digits.

e.g. possible sequence of operation

OFF HOOK
KEY IN NUMBER e.g. 0792 74681
ON HOOK
OFF HOOK
KEY IN REDIAL #
CIRCUIT DIALS OUT 0792 74681

5.2 PABX User

To redial an external call, the user must first re-enter access digit(s) (4 digits maximum), wait for dial tone, then key in Redial # when in OFF HOOK QUIESCENT mode, i.e. speech network connected to line. Circuit then redials last external call.

In between entering an external call and redialling it, the user is able to make use of the 4 digit buffer store to dial and redial internal calls. To redial an internal call, redial # must be the first key depressed, when in OFF HOOK QUIESCENT mode.

e.g. possible sequence of operation

OFF HOOK
KEY IN ACCESS DIGIT (e.g. 9)
WAIT FOR DIAL TONE
KEY IN 0792 74681
ON HOOK
OFF HOOK
KEY IN INTERNAL NUMBER e.g. 437
ON HOOK
OFF HOOK
KEY IN REDIAL KEY #
CIRCUIT DIALS OUT 437
ON HOOK
OFF HOOK
KEY IN ACCESS DIGIT 9
WAIT FOR DIAL TONE
KEY IN REDIAL KEY #
CIRCUIT DIALS OUT 0792 74681

Any number of internal calls can be made up to 4 digits in length without losing the external call. As soon as a number of over 4 digits is entered, this overwrites the previous external call. In countries that have intermediate dial tone (e.g. following area codes) then sequence of redial is: key in area code, wait for dial tone, depress # key.

6. DIRECTORY ASSISTANCE

This feature allows a digit string to be entered without outpulsing - typical use is entering a number given by directory assistance operators.

Entering a number is accomplished by first pressing * key when in OFF HOOK QUIESCENT mode, and then

FUNCTIONAL DESCRIPTION (Cont.)

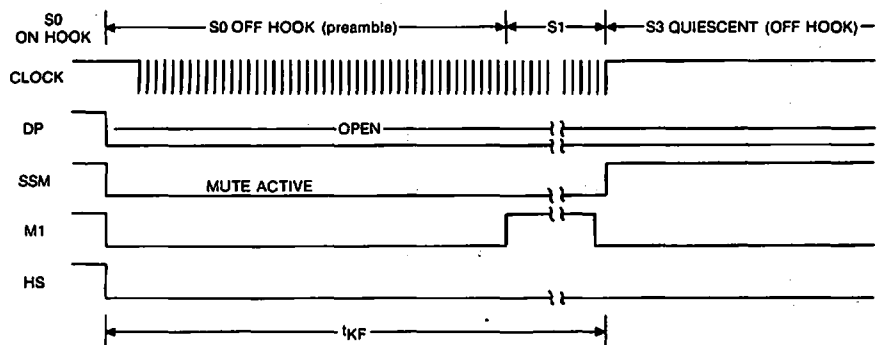
entering the number as per normal, including access digits and area codes. Redial code # will not be recognized once * key has been depressed. The speech network is only muted while the * key is depressed. This has an additional use as a privacy key while in the speech mode.

Dialing the number is accomplished by depressing

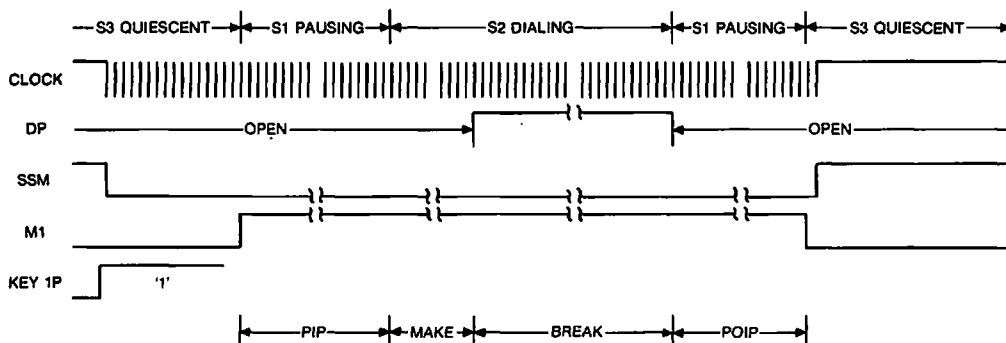
the hook switch, followed by the appropriate procedure for redial.

NOTE: Programming function of redial or directory assistance can be achieved by switching means other than by * and # on a 3×4 keyboard.

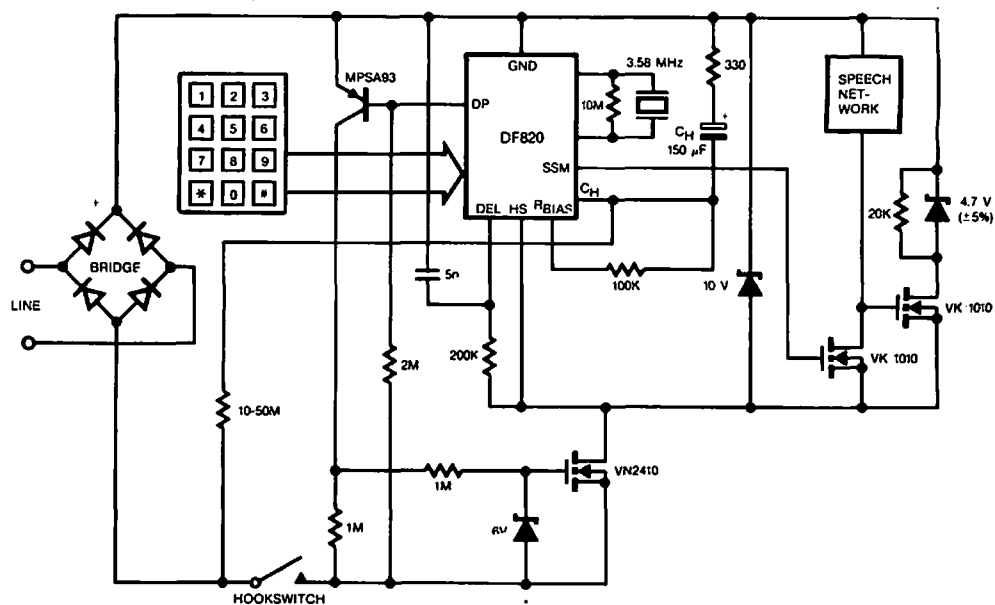
TIMING DIAGRAMS



Timing From Power Up



Timing From Standby



Typical Application Circuit for DF820

Introduction	0
Interface	1
Analog Switches/Multiplexers	2
A/D Converters	3
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DIE PROCESS AND TOPOGRAPHY

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DG300A	8-20	DG527	8-44
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DG302A	8-21	DG529	8-46
DG303A	8-21	G118	8-47
DG304A	8-22	G119	8-48
DG305A	8-22	L144	8-49
DG306A	8-23	L161	8-50
DG307A	8-23	Si7660	8-51
DG308A	8-24	CMJA1000	8-52
DG309	8-24	CMJB1000	8-53
DG381A	8-25	CMJC1000	8-54
DG384A	8-26	LODC1000	8-55
DG387A	8-27	LODF1000	8-56
DG390A	8-28	NC1000	8-57
DG501	8-29	NC2000	8-57
DG503	8-30	NIP1000	8-58

Die Process Information

Siliconix is a large-volume supplier of die to the hybrid industry. Screening includes 100% DC electrical probe and 100% visual inspection of each die.

PHYSICAL DATA

Physical layout and dimensions are presented in the Die Topography section. Dimensions are shown as $\frac{\text{inches}}{(\text{mm})}$. Die are supplied to length and width dimensions which have an accuracy of ± 3 mils. Thickness will be 15 ± 1 mils for integrated circuit die and 8 ± 2 mils for FETs.

Bonding pad location may be identified from the die topography shown. Contact factory for ordering information.

Each die or wafer is passivated with approximately 8000 Å of either silicon nitride or non-crystalline glass.

FET chips are supplied with gold backing; gold backing is available as an option for integrated circuits.

Die metallization is deposited aluminum approximately 12000 Å thick.

DIE SCREENING CRITERIA

Electrical Probe — All dice are 100% probed in wafer form at 25°C to DC parameters as shown on the respective chip data sheet in this section.

Visual Criteria — All die receives a visual inspection to MIL-STD-883, Method 2010, Condition B criteria. Siliconix QC Department samples each lot to an LTPD of 10%. Alternate visual criteria, including Method 2010, Condition A, or Siliconix Industrial criteria are available as options.

PACKAGING

Die are supplied in dust-proof, anti-static waffle packs (see illustration—Figure 1)

ASSEMBLY

The customer's interests will best be served if static sensitivity handling procedures are used.

PART NUMBER DESIGNATIONS

See ordering information.

OPTIONS

(Price will be quoted upon request.)

SEM — Scanning electron microscope examination and control in accordance with MIL-STD-883 Method 2018 can be ordered on die and wafers. SEM wafer qualification should be specified as a separate line item on a request for quote.

Wafer Qualification to Unprobed Parameters — Sample testing of purchased die to demonstrate capability to perform at data sheet temperature extremes or to switching time test limits by use of LTPD techniques can be provided at additional cost.

Visual inspection to customer generated specifications can be provided.

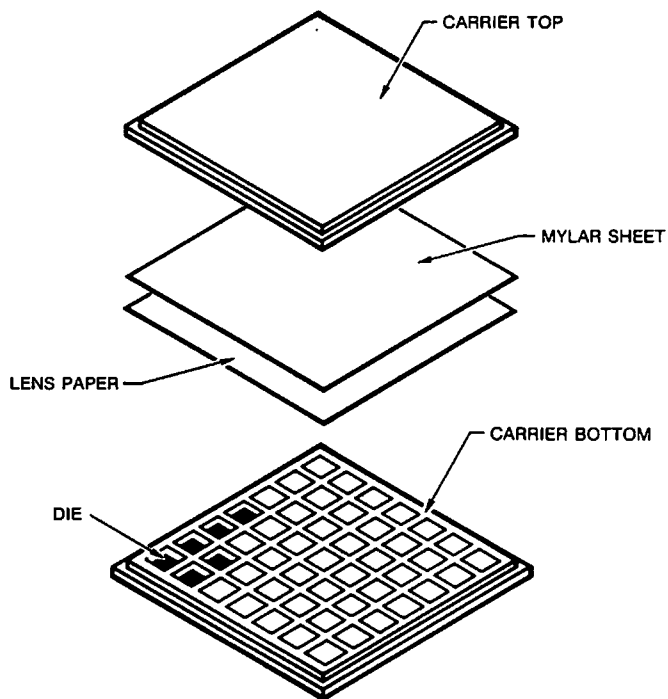
Gold Backing — Die may be purchased with gold alloyed to the backside. This is a special order item. Gold thickness would be as follows:

- FETs (NC, NIP) 7500 Å minimum
- IC's (all) 35000 Å minimum

Hot Probe — Siliconix has chip processing distributors with probe capability available.

CHIP PACKAGING

Chips are packaged as individual die in the flat waffle carrier illustrated in Figure 1. The carrier has a cavity size adequate to allow ease of loading/unloading and also prevents die from rotating within the cavity.



NOTE: Carrier top and bottom secured by clips

Figure 1

MULTICHIP DIE TOPOGRAPHY INFORMATION

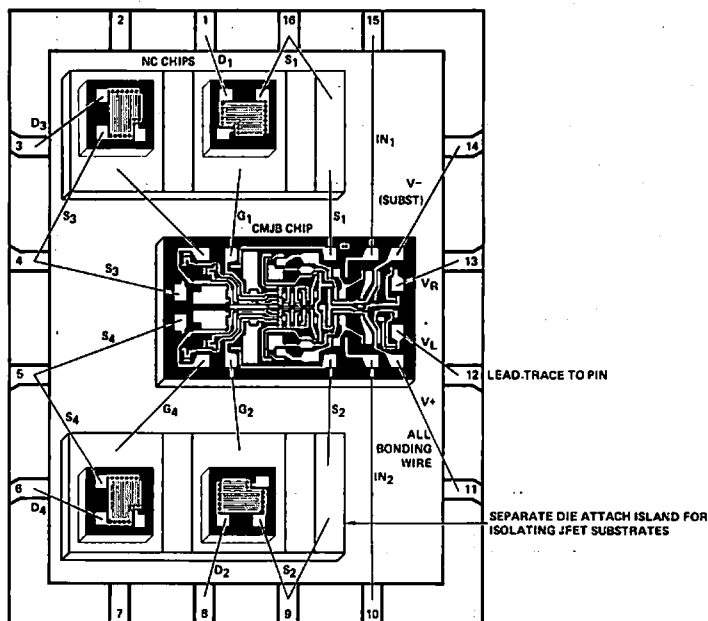
Some of Siliconix's analog switches are of multi-chip design with inter-chip connections. For example, the DG190 consists of a separate driver chip (CMJB) and four separate JFET transistors (NCB). Figure 1 illustrates the bonding diagram arrangement in the DIP package. The driver and the JFET switches are mounted so that the substrates are electrically isolated. The substrate of the driver is at the negative supply voltage while the substrate of the JFET switches is the gate connection. A bond wire connects the driver to the JFET gate.

The pin connections for the JFET switch chips can be determined from the chip section and switch pin-out in the data sheet.

Die Diagrams/Dimensions

The negative image photos show the metallization pattern. Scale is $\approx 32\times$. Bonding pads are 4 mil (0.10 mm) square, glass-free aluminum metallization. Pad identification numbers correspond to pin numbers for the dual-in-line package on data sheets.

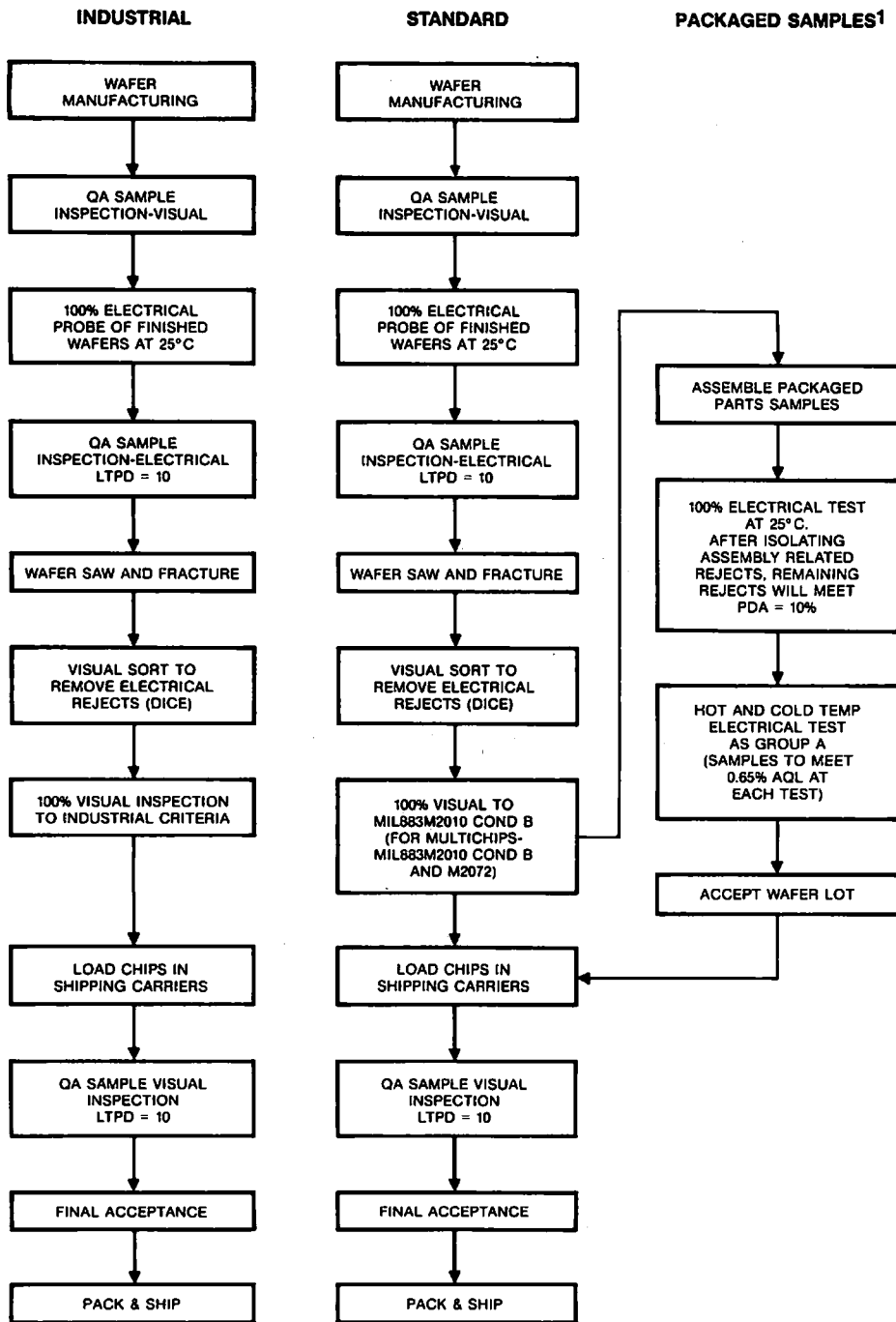
The following pages contain ordering information, layout, die dimensions and pad identification.



DG180 JFET Analog Switch
Figure 1

NOTE: Die Topography is for reference only

DIE SHIPMENT FLOW - INTEGRATED CIRCUITS

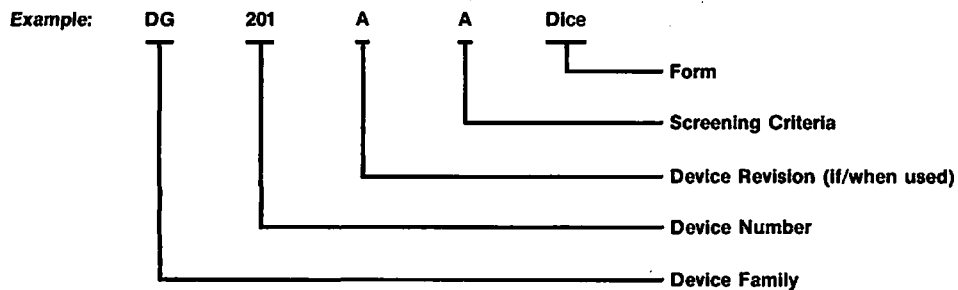


NOTES:

1. To demonstrate capability of performing at temperature extremes and switching time test limits by use of AQL, Packaged Samples flow is recommended.

Die Ordering Information

1. Monolithic Chips:



DEVICE FAMILY (1, 2 or 3 Letters)

- D — Drivers for FET Switches
- DG — Analog Switches
- G — Multi-Channel FETs
- L — Linear
- Si — Siliconix Second Source Part

DEVICE NUMBER (3 or 4 Digit Numbers)

SCREENING CRITERIA (1 Letter)

- A — Electrically probed @ 25°C; visual criteria screening to MIL-STD-883, Method 2010 Condition B.
- I — Electrically probed @ 25°C; visual criteria screening to Siliconix Specification 501B.

FORM (4 letters)

DICE — Chips waffle packed per Figure 4 in Die Process Information

2. Multichip

To order die which form multichip devices the driver chip and corresponding JFETs should be ordered using the geometry designations as shown in Table 1 below.

Example:

For DG190 die, order
CMJB1000
and NC1000

To determine number of JFETs required to go with each driver in a multichip device, see number in parenthesis following geometry codes as shown in table below.

Table 1

Siliconix Part No.	Geometry Code		Technology
	Driver	FET	
DG126	LODC1000	NC2000(4)	JFET Switch
DG129	LODC1000	NC1000(4)	JFET Switch
DG133	LODC1000	NC1000(2)	JFET Switch
DG134	LODC1000	NC2000(2)	JFET Switch
DG139	LODF1000	NC1000(4)	JFET Switch
DG140	LODC1000	NIP1000(4)	JFET Switch
DG141	LODC1000	NIP1000(2)	JFET Switch
DG142	LODF1000	NC2000(4)	JFET Switch
DG143	LODF1000	NC2000(2)	JFET Switch
DG144	LODF1000	NC1000(2)	JFET Switch
DG145	LODF1000	NIP1000(4)	JFET Switch
DG146	LODF1000	NIP1000(2)	JFET Switch
DG180	CMJB1000	NIP1000(2)	JFET Switch
DG181	CMJB1000	NC1000(2)	JFET Switch
DG182	CMJB1000	NC2000(2)	JFET Switch
DG183	CMJA1000	NIP1000(4)	JFET Switch
DG184	CMJA1000	NC1000(4)	JFET Switch
DG185	CMJA1000	NC2000(4)	JFET Switch
DG186	CMJC1000	NIP1000(2)	JFET Switch
DG187	CMJC1000	NC1000(2)	JFET Switch
DG188	CMJC1000	NC2000(2)	JFET Switch
DG189	CMJB1000	NIP1000(4)	JFET Switch
DG190	CMJB1000	NC1000(4)	JFET Switch
DG191	CMJB1000	NC2000(4)	JFET Switch

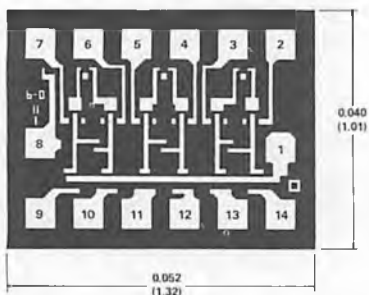
3. Options

The following options are considered "special" and a special part number will be assigned:

1. Die in wafer form
2. Gold backing on Integrated Circuit die
3. Class A visual
4. Customer visual criteria

Please identify as "similar to _____ with following additional conditions _____."

D125



PAD NO.	FUNCTION
1	V- (Substrate)
2	Input 1
3	Input 2
4	Input 3
5	Input 4
6	Input 5
7	Input 6
8	V _L
9	Output 6
10	Output 5
11	Output 4
12	Output 3
13	Output 2
14	Output 1

DC ELECTRICAL CHARACTERISTICS

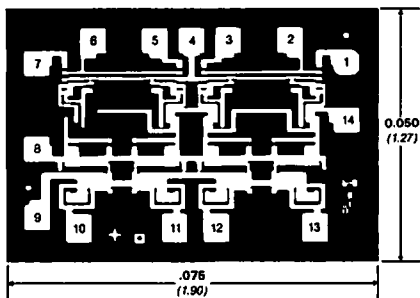
T_A = 25°C

	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED:	LIMITS		UNIT
				MIN ¹	MAX	
OUTPUT	Output Voltage Low	V _{OL}	V- = -20 V, V _L = 5 V, V _{in} = 1 V		-19.59	V
	Output Current High	I _{OH}	V- = -20 V, V _L = 5 V, V _{in} = 5 V		90	μA
INPUT	Input Current Input Voltage High	I _{INH}	V- = -21 V, V _L = 5 V, V _{in} = 4.6 V	-0.9		
	Input Current Input Voltage Low	I _{INL}	V- = -21 V, V _L = 5 V, V _{in} = 0 V	-0.6		
SUPPLY	Negative Supply Current	I-	V- = -21 V, V _L = 5 V, V _{in} = 4.6 V	-2		
	Logic Supply Current	I _L			1	

NOTES:

- The algebraic convention whereby the most negative value is a minimum, and the most positive value is a maximum, is used in this data sheet.

D129



PAD NO.	FUNCTION
1	Input 1
2	Input 2
3	Input 3
4	Input 4
5	Input 7
6	Input 8
7	Input 9
8	V_R
9	V_- (Substrate)
10	Output 4
11	Output 3
12	Output 2
13	Output 1
14	V_L

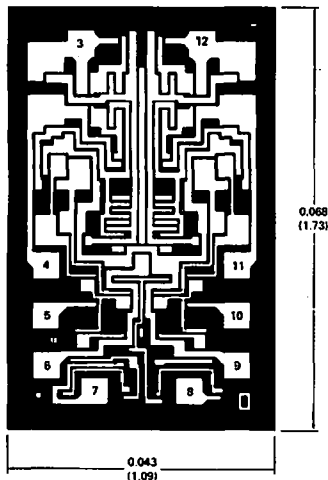
DC ELECTRICAL CHARACTERISTICS

$T_A = 25^\circ\text{C}$

	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: $V_- = -20\text{ V}$, $V_L = 5\text{ V}$, $V_R = 0\text{ V}$	LIMITS		UNIT
				MIN ¹	MAX	
OUTPUT	Output Voltage Low	V_{OL}	$V_L = 4.5\text{ V}$, $V_{in} = 2.2\text{ V}$, $I_O = 10\text{ mA}$		-19.2	V
	Output Current High	I_{OH}	$V_{in} = 0.7\text{ V}$	0.1		μA
INPUT	Input Current Input Voltage High	I_{INH}	$V_{in} = 5\text{ V}$		0.25	
	Input Current Input Voltage Low	I_{INL}	$V_L = 5.5\text{ V}$, $V_{in} = 0\text{ V}$	-200		
SUPPLY	Negative Supply Current	I_-	$V_L = 5.5\text{ V}$, One Channel ON	-2		mA
	Logic Supply Current	I_L			3	

NOTES:

1. The algebraic convention whereby the most negative value is a minimum, and the most positive value is a maximum, is used in this data sheet.



PAD NO.	FUNCTION
3	Out 1
4	Out 1
5	Input 1
6	V+
7	V _L
8	V _R
9	V- (Substrate)
10	Input 2
11	Out 2
12	Out 2

DC ELECTRICAL CHARACTERISTICS

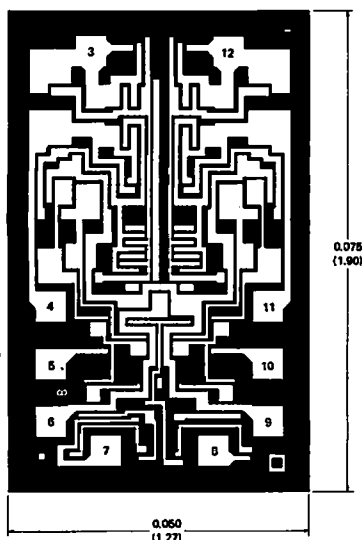
T_A = 25°C

	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: V ₊ = 10 V, V ₋ = -20 V, V _L = 5 V, V _R = 0 V	LIMITS		UNIT
				MIN ¹	MAX	
OUTPUT	Output Voltage High (V ₊ to V _O)	V _{OH} /V _{OH}	V _{IH} = 2 V for V _{OH} /V _{OL}	I _{OUT} = -1 mA	1.0	V
	Output Voltage Low (V _O to V ₋)	V _{OL} /V _{OL}	V _{IL} = 0.8 V for V _{OH} /V _{OL}	I _{OUT} = 1 mA	1.2	
INPUT	Input Current Input Voltage High	I _{INH}	V _{in} = 5 V		10	μA
	Input Current Input Voltage Low	I _{INL}	V _{in} = 0 V	-500		
SUPPLY	Positive Supply Current	I ₊	V _{in} = 0 V		100	mA
	Logic Supply Current	I _L	V _{in} = 0 V		4	
	Negative Supply Current	I ₋	V _{in} = 0 V	-3		
	Reference Supply Current Input Voltage High	I _{RH}	V _{in} = 2 V	-1.6		

NOTES:

- The algebraic convention whereby the most negative value is a minimum, and the most positive value is a maximum, is used in this data sheet.

D169



PAD NO.	FUNCTION
3	$\overline{\text{OUT}}_1$
4	OUT_1
5	IN_1
6	V_+
7	V_L
8	V_R
9	V_- (Substrate)
10	IN_2
11	OUT_2
12	$\overline{\text{OUT}}_2$

DC ELECTRICAL CHARACTERISTICS

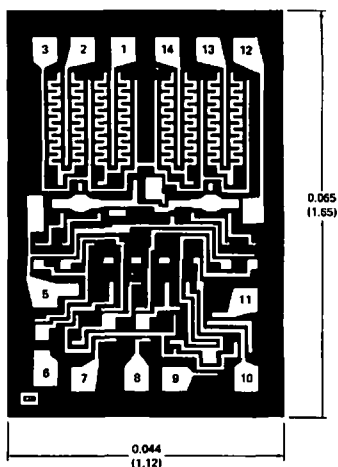
$T_A = 25^\circ\text{C}$

	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: $V_+ = 10\text{ V}$, $V_- = -20\text{ V}$, $V_L = 5\text{ V}$, $V_R = 0\text{ V}$		LIMITS		UNIT
					MIN ¹	MAX	
OUTPUT	Output Voltage High (V_+ to V_O)	V_{OH}/V_{OH}	$V_{IH} = 2\text{ V}$ for V_{OH}/V_{OL}	$I_{OUT} = -1\text{ mA}$		1.0	V
	Output Voltage Low (V_O to V_-)	V_{OL}/V_{OL}	$V_{IL} = 0.8\text{ V}$ for V_{OH}/V_{OL}	$I_{OUT} = 1\text{ mA}$		1.2	
INPUT	Input Current Input Voltage High	I_{INH}	$V_{in} = 5\text{ V}$			10	μA
	Input Current Input Voltage Low	I_{INL}			-500		
SUPPLY	Positive Supply Current	I_+	$V_{in} = 0\text{ V}$			100	mA
	Logic Supply Current	I_L				4	
	Negative Supply Current	I_-			-3		
	Reference Supply Current	I_R	$V_{in} = 2\text{ V}$		-1.6		

NOTES:

1. The algebraic convention whereby the most negative value is a minimum, and the most positive value is a maximum, is used in this data sheet.

DG172



PAD NO.	FUNCTION
1	Source 3
2	Source 4
3	Drain
5	V-(Substrate)
6	Input 4
7	Input 3
8	Input 2
9	Input 1
10	V _L
11	V _R
12	V+
13	Source 1
14	Source 2

ELECTRICAL CHARACTERISTICS

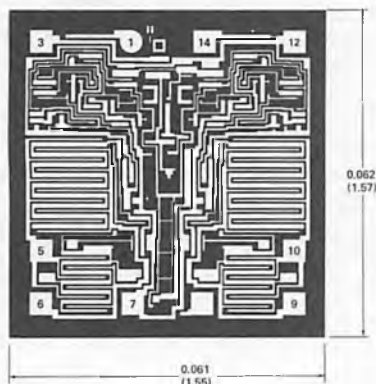
T_A = 25°C

	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: V ₊ = 10 V, V ₋ = -20 V, V _R = 0 V V _L = 5 V		LIMITS		UNIT
					MIN ¹	MAX	
SWITCH	Drain-Source ON Resistance	r _{DS(on)}	V _{in} = 0.8 V	I _S = 1 mA, V _D = -10 V		450	Ω
	Source OFF Leakage Current	I _{S(off)}		V _S = -10 V, V _D = 10 V	-100		nA
	Drain OFF Leakage Current	I _{D(off)}	V _{in} = 2 V, V _S = 10 V, V _D = -10 V		-100		
	Drain ON Leakage Current	I _{D(on)}	V _D = V _S = 10 V, V _{in} = 0.8 V			100	
INPUT	Input Current with Input Voltage High	I _{INH}	V _{in} = 5 V			100	
	Input Current with Input Voltage Low	I _{INL}	V _{in} = 0		-0.5		
SUPPLY	Positive Supply Current	I ₊	One Channel ON V _{in} = 0			3	mA
	Negative Supply Current	I ₋			-5.1		
	Logic Supply Current	I _L				5.7	
	Reference Supply Current	I _R				2.1	
			I _R = 0				
	Positive Supply Current	I ₊	All Channels OFF V _{in} = 5 V			10	μA
	Negative Supply Current	I ₋			-20		
	Logic Supply Current	I _L				4.5	
	Reference Supply Current	I _R				10	
			I _R = 0				
					-4.5		mA

NOTES:

- The algebraic convention whereby the most negative value is a minimum, and the most positive value is a maximum, is used in this data sheet.

DG200A



PAD NO.	FUNCTION
1	Input 2
3	Ground
5	Source 2
6	Drain 2
7	V-
9	Drain 1
10	Source 1
12	V+ (Substrate)
14	Input 1

DC ELECTRICAL CHARACTERISTICS

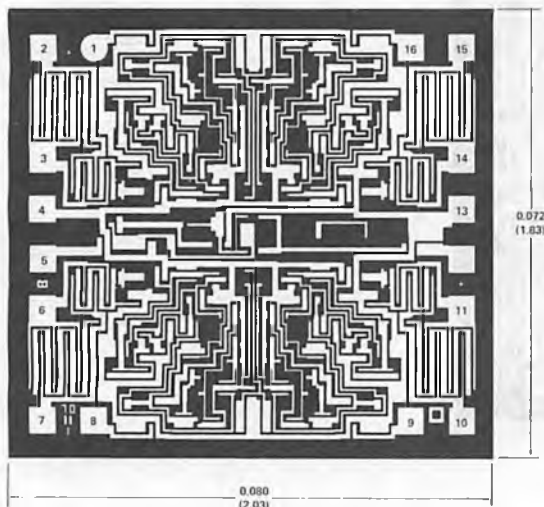
$T_A = 25^\circ\text{C}$

	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: $V_+ = 15\text{ V}$, $V_- = -15\text{ V}$, $GND = 0\text{ V}$	LIMITS		UNIT
				MIN ¹	MAX	
SWITCH	Drain-Source ON Resistance	$r_{DS(on)}$	$V_{in} = 0.8\text{ V}$, $I_S = -1\text{ mA}$	$V_D = 10\text{ V}$ $V_D = -10\text{ V}$	80 80	Ω
	Source OFF Leakage Current	$I_{S(off)}$	$V_{in} = 15\text{ V}$	$V_S = 14\text{ V}$, $V_D = -14\text{ V}$ $V_S = -14\text{ V}$, $V_D = 14\text{ V}$	1.2 -1.2	μA
	Drain OFF Leakage Current	$I_{D(off)}$		$V_D = 14\text{ V}$, $V_S = -14\text{ V}$ $V_D = -14\text{ V}$, $V_S = 14\text{ V}$	1.2 -1.2	
	Drain ON Leakage Current ²	$I_{D(on)}$		$V_D = V_S = 14\text{ V}$ $V_D = V_S = -14\text{ V}$	1.2 -1.2	
			$V_{in} = 0\text{ V}$			
INPUT	Input Current Input Voltage Low	I_{INH}	$V_{in} = 2.4\text{ V}$ $V_{in} = 15\text{ V}$	-1.0	1.0	μA
	Input Current Input Voltage High	I_{INL}	$V_{in} = 0\text{ V}$	-1.0		
SUPPLY	Positive Supply Current	I_+	Both Channels "ON" or "OFF" $V_{in} = 0\text{ or }2.4\text{ V}$		2.0	mA
	Negative Supply Current	I_-		-1.0		

NOTES:

- The algebraic convention whereby the most negative value is a minimum, and the most positive value is a maximum, is used in this data sheet.
- $I_{D(on)}$ is leakage from driver into "ON" switch.

DG201A/DG202



PAD NO.	FUNCTION
1	Input 1
2	Drain 1
3	Source 1
4	V-
5	GND
6	Source 4
7	Drain 4
8	Input 4
9	Input 3
10	Drain 3
11	Source 3
13	V+ (Substrate)
14	Source 2
15	Drain 2
16	Input 2

DC ELECTRICAL CHARACTERISTICS

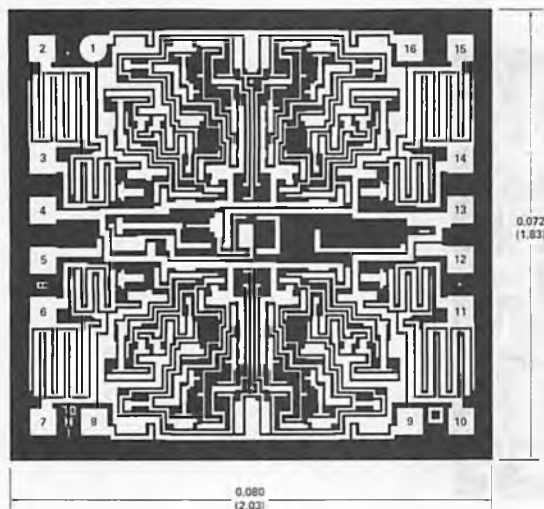
$T_A = 25^\circ\text{C}$

	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: $V_+ = 15\text{ V}$, $V_- = -15\text{ V}$, $GND = 0\text{ V}$	LIMITS		UNIT
				MIN ¹	MAX	
SWITCH	Drain-Source ON Resistance	$r_{DS(on)}$	$V_{in} = 0.8\text{ V}$, DG201A $V_{in} = 2.4\text{ V}$, DG202 $I_S = -1\text{ mA}$	$V_D = 10\text{ V}$	200	Ω
	Source OFF Leakage Current	$I_{S(off)}$	$V_{in} = 2.4\text{ V}$, DG201A $V_{in} = 0.8\text{ V}$, DG202	$V_S = 14\text{ V}$, $V_D = -14\text{ V}$ $V_S = -14\text{ V}$, $V_D = 14\text{ V}$	0.12	μA
	Drain OFF Leakage Current	$I_{D(off)}$		$V_D = 14\text{ V}$, $V_S = -14\text{ V}$ $V_D = -14\text{ V}$, $V_S = 14\text{ V}$	0.12	
	Drain ON Leakage Current	$I_{D(on)}$	$V_{in} = 0.8\text{ V}$, DG201A $V_{in} = 2.4\text{ V}$, DG202	$V_D = V_S = 14\text{ V}$ $V_D = V_S = -14\text{ V}$	0.12	
	Input Current Input Voltage High	I_{INH}	$V_{in} = 2.4\text{ V}$ $V_{in} = 15\text{ V}$	-10	10	
INPUT	Input Current Input Voltage Low	I_{INL}	$V_{in} = 0\text{ V}$	-10		
	Positive Supply Current	I_+	Both Channels "ON" or "OFF" $V_{in} = 0\text{ or }2.4\text{ V}$		2.0	mA
SUPPLY	Negative Supply Current	I_-		-1.0		

NOTES:

- The algebraic convention whereby the most negative value is a minimum, and the most positive value is a maximum, is used in this data sheet.

DG211/DG212



PAD NO.	FUNCTION
1	Input 1
2	Drain 1
3	Source 1
4	V-
5	Ground
6	Source 4
7	Drain 4
8	Input 4
9	Input 3
10	Drain 3
11	Source 3
12	V _L
13	V+ (Substrate)
14	Source 2
15	Drain 2
16	Input 2

DC ELECTRICAL CHARACTERISTICS

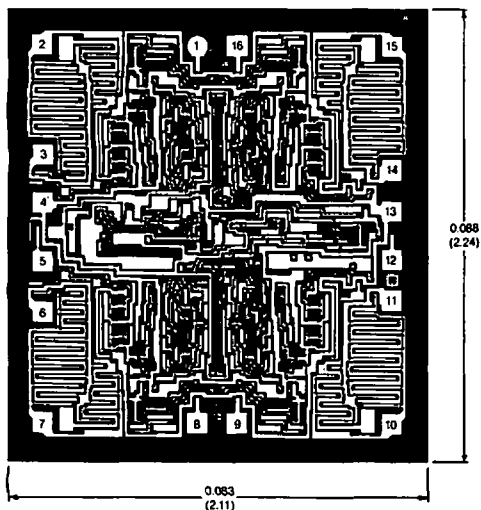
T_A = 25°C

	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: V ₊ = 15 V, V ₋ = -15 V, GND = 0 V, V _L = 5 V	LIMITS		UNIT
				MIN ¹	MAX	
SWITCH	Drain-Source ON Resistance	r _{DS(on)}	V _{in} = 0.8 V, DG211 V _{in} = 2.4 V, DG212	V _D = 10 V, I _S = -1.0 mA V _D = -10 V, I _S = 1.0 mA	175 175	Ω
	Source OFF Leakage Current	I _{S(off)}	V _{in} = 2.4 V, DG211 V _{in} = 0.8 V, DG212	V _S = 14 V, V _D = -14 V V _S = -14 V, V _D = 14 V	0.12 -0.12	μA
	Drain OFF Leakage Current	I _{D(off)}		V _D = 14 V, V _S = -14 V V _D = -14 V, V _S = 14 V	0.12 -0.12	
	Drain ON Leakage Current	I _{D(on)}	V _{in} = 0.8 V, DG211 V _{in} = 2.4 V, DG212	V _D = V _S = 14 V V _D = V _S = -14 V	0.12 -0.12	
INPUT	Input Current Input Voltage High	I _{INH}	V _{in} = 2.4 V	-1.0		
	Input Current Input Voltage Low	I _{INL}	V _{in} = 15 V		1.0	
SUPPLY	Positive Supply Current	I ₊	Both Channels ON or OFF V _{in} = 0 or 2.4 V		0.48	mA
	Negative Supply Current	I ₋		-0.48		
	Logic Supply Current	I _L			1.2	

NOTES:

1. The algebraic convention whereby the most negative value is a minimum, and the most positive value is a maximum, is used in this data sheet.

DG221



PAD NO.	FUNCTION
1	Input 1
2	Drain 1
3	Source 1
4	V-
5	GND
6	Source 4
7	Drain 4
8	Input 4
9	Input 3
10	Drain 3
11	Source 3
12	WR
13	V+ (Substrate)
14	Source 2
15	Drain 2
16	Input 2

DC ELECTRICAL CHARACTERISTICS

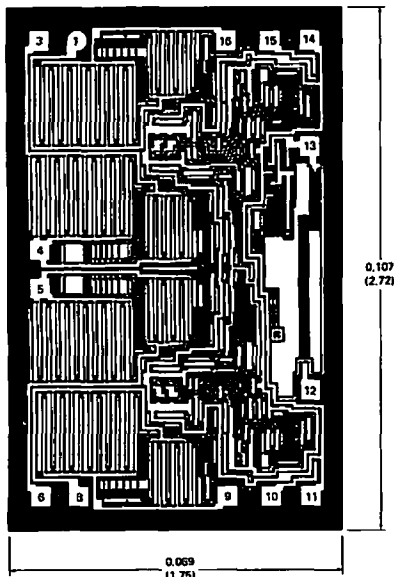
T_A = 25°C

	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: V ₊ = 15 V, V ₋ = -15 V, WR = GND = 0 V		LIMITS		UNIT
					MIN ¹	MAX	
SWITCH	Drain-Source ON Resistance	r _{DS(on)}	V _{in} = 0.8 V, I _S = -1 mA	V _D = 10 V V _D = -10 V		90 90	Ω
	Source OFF Leakage Current	I _{S(off)}	V _{in} = 2.4 V	V _S = 14 V, V _D = -14 V V _S = -14 V, V _D = 14 V		0.12 -0.12	μA
	Drain OFF Leakage Current	I _{D(off)}		V _D = 14 V, V _S = -14 V V _D = -14 V, V _S = 14 V		0.12 -0.12	
	Channel ON Leakage Current	I _{D(on)} + I _{S(on)}		V _D = V _S = 14 V V _D = V _S = -14 V		0.12 -0.12	
	Channel ON Leakage Current	I _{D(on)} + I _{S(on)}	V _{in} = 0.8 V				
INPUT	Input Current High	I _{I(H)}	V _{in} = 2.4 V		-1		
	Input Current Low	I _{I(L)}	V _{in} = 15 V			1	
	Input Current Low	I _{I(L)}	V _{in} = 0 V		-1		
SUPPLY	Positive Supply Current	I ₊	Both Channels "ON" or "OFF" V _{in} = 0 or 2.4 V			1.5	mA
	Negative Supply Current	I ₋			-1.0		

NOTES:

- The algebraic convention whereby the most negative value is a minimum, and the most positive value is a maximum, is used in this data sheet.

DG243



PAD NO.	FUNCTION
1	Drain 1
3	Drain 3
4	Source 3
5	Source 4
6	Drain 4
8	Drain 2
9	Source 2
10	Input 2
11	V+ (Substrate)
12	V _L
13	GND
14	V-
15	Input 1
16	Source 1

DC ELECTRICAL CHARACTERISTICS

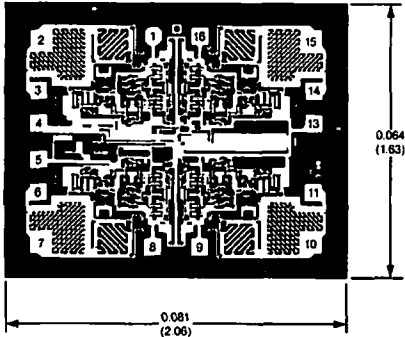
T_A = 25°C

	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: V ₊ = 15 V, V ₋ = -15 V, GND = 0 V, V _L = 5 V,	LIMITS		UNIT
				MIN ¹	MAX	
SWITCH	Drain-Source ON Resistance	r _{DS(on)}	V _D = 10 V, I _S = -10 mA, V _{in} = 2 V		50	Ω
			V _D = -10 V, I _S = 10 mA, V _{in} = 2 V		50	
	Source OFF Leakage Current	I _{S(off)}	V _{in} = 0.8 V	V _S = 14 V, V _D = -14 V	0.12	μA
	Drain OFF Leakage Current	I _{D(off)}		V _S = -14 V, V _D = 14 V	-0.12	
				V _D = 14 V, V _S = -14 V	0.12	
	Drain-Source ON Leakage Current	I _D + I _{S(on)}	V _{in} = 2.0 V	V _D = -14 V, V _S = 14 V	-0.12	
				V _D = V _S = 14 V	0.12	
INPUT	Input Current Input Voltage High	I _{INH}	V _{in} = 15 V		1.0	μA
	Input Current Input Voltage Low	I _{INL}	V _{in} = 0 V	-1.0		
SUPPLY	Positive Supply Current	I ₊	V _{in} = 0 or 2.4 V		300	μA
	Negative Supply Current	I ₋		-300		
	Logic Supply Current	I _L			300	
	Ground Supply Current	I _{GND}		-300		

NOTES:

- The algebraic convention whereby the most negative value is a minimum, and the most positive value is a maximum, is used in this data sheet.

DG271



PAD NO.	FUNCTION
1	Input 1
2	Drain 1
3	Source 1
4	V-
5	GND
6	Source 4
7	Drain 4
8	Input 4
9	Input 3
10	Drain 3
11	Source 3
13	V+ (Substrate)
14	Source 2
15	Drain 2
16	Input 2

ELECTRICAL CHARACTERISTICS

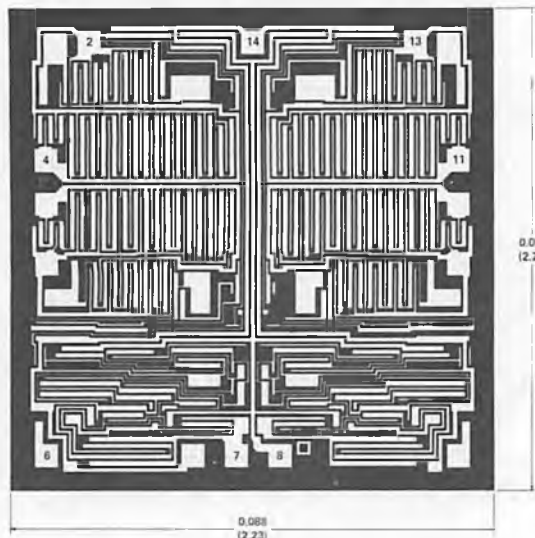
T_A = 25°C

	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: V ₊ = 15 V, V ₋ = -15 V, GND = 0 V	LIMITS		UNIT
				MIN ¹	MAX	
SWITCH	Drain-Source ON Resistance	r _{DS(on)}	V _{in} = 0.8 V	V _D = 10 V, I _S = -1 mA	50	Ω
				V _D = -10 V, I _S = -1 mA	50	
	Source OFF Leakage Current	I _{S(off)}	V _{in} = 2.0 V	V _D = 14 V, V _S = -14 V	120	nA
	Drain OFF Leakage Current	I _{D(off)}		V _D = -14 V, V _S = 14 V	-120	
	Channel ON Leakage Current	I _{D(on)} ⁺ I _{S(on)}		V _D = 14 V, V _S = -14 V	120	
INPUT	Input Current with Input Voltage High	I _{INH}	V _{in} = 2 V	-1		μA
			V _{in} = 15 V		1	
	Input Current with Input Voltage Low	I _{INL}	V _{in} = 0 V	-1		
SUPPLY	Positive Supply Current	I ₊	V _{in} = 0 V or 2 V		6	mA
	Negative Supply Current	I ₋		-4.5		

NOTES:

- The algebraic convention whereby the most negative value is a minimum, and the most positive value is a maximum, is used in this data sheet.

DG300A/DG301A



PAD NO.	FUNCTION
2	Drain 1
4	Source 1
6	Input 1
7	Ground
8	V-
11	Source 2
13	Drain 2
14	V+ (Substrate)

DC ELECTRICAL CHARACTERISTICS

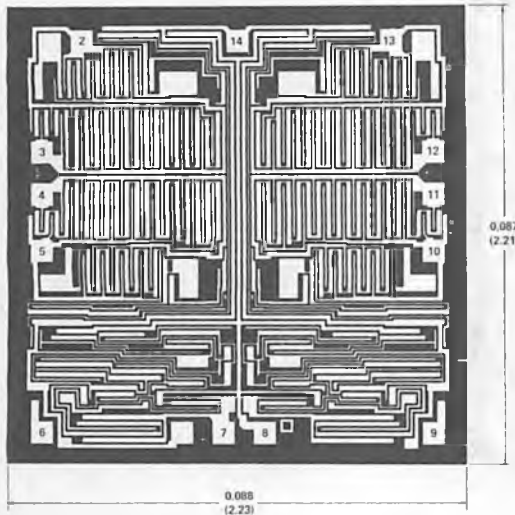
$T_A = 25^\circ\text{C}$

	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: $V_+ = 15\text{ V}$, $V_- = -15\text{ V}$, $\text{GND} = 0\text{ V}$	LIMITS		UNIT
				MIN ¹	MAX	
SWITCH	Drain-Source ON Resistance	$r_{DS(on)}$	$V_D = 10\text{ V}$, $I_S = -10\text{ mA}$		50	Ω
	Source OFF Leakage Current	$I_{S(off)}$	$V_{in} = 0.8\text{ V}$, DG300A $V_S = -14\text{ V}$, $V_D = 14\text{ V}$	-0.12	0.12	μA
	Drain OFF Leakage Current	$I_{D(off)}$	$V_{in} = 0.8\text{ V}$ or 4 V , DG301A ² $V_D = 14\text{ V}$, $V_S = -14\text{ V}$	-0.12	0.12	
	Drain ON Leakage Current	$I_{D(on)}$	$V_{in} = 4\text{ V}$, DG300A $V_{in} = 0.8\text{ V}$ or 4 V , DG301A ²	$V_D = V_S = 14\text{ V}$ $V_D = V_S = -14\text{ V}$	-0.12	0.12
INPUT	Input Current Input Voltage High	I_{INH}	$V_{in} = 15\text{ V}$		1.0	μA
	Input Current Input Voltage Low	I_{INL}	$V_{in} = 0\text{ V}$	-1.0		
SUPPLY	Positive Supply Current	I_+	$V_{in} = 4\text{ V}$ $V_{in} = 0.8\text{ V}$		500 -10	μA
	Negative Supply Current	I_-	$V_{in} = 4\text{ V}$ $V_{in} = 0.8\text{ V}$		-10	

NOTES:

- The algebraic convention whereby the most negative value is a minimum, and the most positive value is a maximum, is used in this data sheet.
- V_{in} = input voltage to perform proper function.

DG302A/DG303A



PAD NO.	FUNCTION
2	Source 3
3	Drain 3
4	Drain 1
5	Source 1
6	Input 1
7	Ground
8	V-
9	Input 2
10	Source 2
11	Drain 2
12	Drain 4
13	Source 4
14	V- (Substrate)

DC ELECTRICAL CHARACTERISTICS

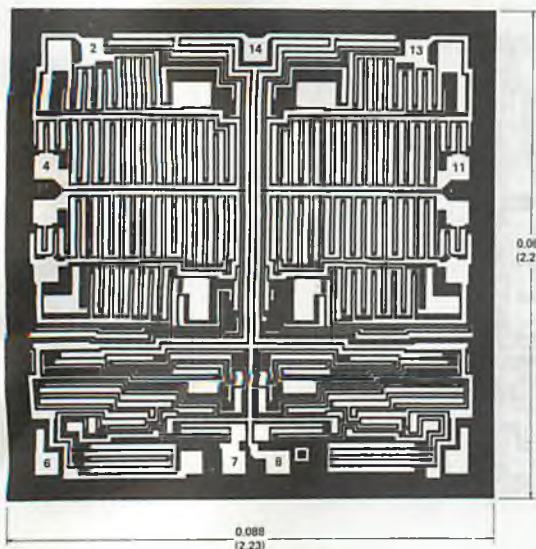
T_A = 25°C

	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: V _r = 15 V, V ₋ = -15 V, GND = 0 V	LIMITS		UNIT
				MIN ¹	MAX	
SWITCH	Drain-Source ON Resistance	r _{DS(on)}	V _D = 10 V, I _S = -10 mA		50	Ω
			V _D = -10 V, I _S = 10 mA			
	Source OFF Leakage Current	I _{S(off)}	V _{in} = 0.8 V, DG302A	V _S = 14 V, V _D = -14 V	0.12	μA
				V _S = -14 V, V _D = 14 V	-0.12	
SWITCH	Drain OFF Leakage Current	I _{D(off)}	V _{in} = 0.8 V or 4 V, DG303A ²	V _D = 14 V, V _S = -14 V	0.12	
				V _D = -14 V, V _S = 14 V	-0.12	
	Drain ON Leakage Current	I _{D(on)}	V _{in} = 4 V, DG302A	V _D = V _S = 14 V	0.12	μA
			V _{in} = 0.8 V or 4 V, DG303A ²	V _D = V _S = -14 V	-0.12	
INPUT	Input Current	I _{INH}	V _{in} = 15 V		1.0	
	Input Voltage High					
	Input Current	I _{INL}	V _{in} = 0 V	-1.0		
SUPPLY	Input Voltage Low					
	Positive Supply Current	I ₊	V _{in} = 4 V		500	μA
			V _{in} = 0.8 V	-10		
SUPPLY	Negative Supply Current	I ₋	V _{in} = 4 V		10	
			V _{in} = 0.8 V	-10		

NOTES:

- The algebraic convention whereby the most negative value is a minimum, and the most positive value is a maximum, is used in this data sheet.
- V_{in} = input voltage to perform proper function.

DG304A/DG305A



PAD NO.	FUNCTION
2	Drain 1
4	Source 1
6	Input 1
7	Ground
8	V-
11	Source 2
13	Drain 2
14	V+ (Substrate)

DC ELECTRICAL CHARACTERISTICS

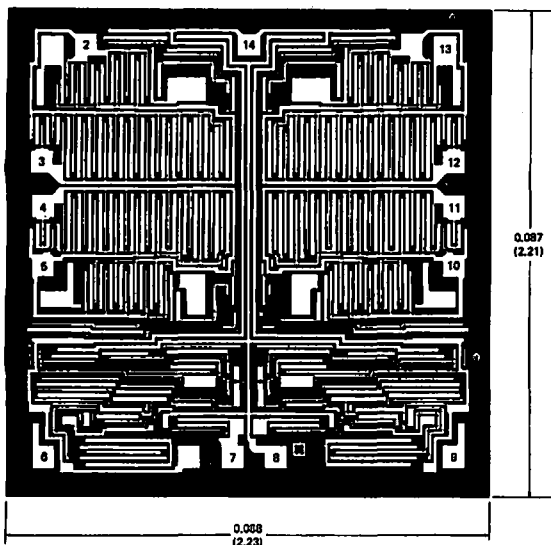
$T_A = 25^\circ\text{C}$

	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: $V_+ = 15\text{ V}$, $V_- = -15\text{ V}$, $\text{GND} = 0\text{ V}$	LIMITS		UNIT
				MIN ¹	MAX	
SWITCH	Drain-Source ON Resistance	$r_{DS(on)}$	$V_D = 10\text{ V}$, $I_S = -10\text{ mA}$		50	Ω
			$V_D = -10\text{ V}$, $I_S = 10\text{ mA}$			
	Source OFF Leakage Current	$I_{S(off)}$	$V_{in} = 3.5\text{ V}$, DG304A $V_S = 14\text{ V}$, $V_D = -14\text{ V}$	-0.12	0.12	
	Drain OFF Leakage Current	$I_{D(off)}$	$V_{in} = 11\text{ V}$ or 3.5 V , DG305A ² $V_D = 14\text{ V}$, $V_S = -14\text{ V}$	-0.12	0.12	
	Drain ON Leakage Current	$I_{D(on)}$	$V_{in} = 11\text{ V}$, DG304A $V_{in} = 3.5\text{ V}$ or 11 V , DG305A ²	-0.12	0.12	
INPUT	Input Current Input Voltage High	I_{INH}	$V_{in} = 15\text{ V}$		1.0	μA
	Input Current Input Voltage Low	I_{INL}	$V_{in} = 0\text{ V}$	-1.0		
SUPPLY	Positive Supply Current	I_+	$V_{in} = 15\text{ V}$		10	
	Negative Supply Current	I_-	$V_{in} = 0\text{ V}$		10	
			$V_{in} = 15\text{ V}$	-10		
			$V_{in} = 0\text{ V}$	-10		

NOTES:

- The algebraic convention whereby the most negative value is a minimum, and the most positive value is a maximum, is used in this data sheet.
- V_{in} = input voltage to perform proper function.

DG306A/DG307A



PAD NO.	FUNCTION
2	Source 3
3	Drain 3
4	Drain 1
5	Source 1
6	Input 1
7	Ground
8	V-
9	Input 2
10	Source 2
11	Drain 2
12	Drain 4
13	Source 4
14	V+ (Substrate)

DC ELECTRICAL CHARACTERISTICS

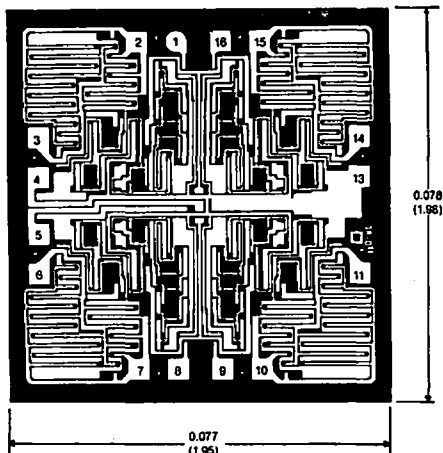
$T_A = 25^\circ\text{C}$

	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: $V_+ = 15\text{ V}$, $V_- = -15\text{ V}$, $GND = 0\text{ V}$	LIMITS		UNIT
				MIN ¹	MAX	
SWITCH	Drain-Source ON Resistance	$r_{DS(on)}$	$V_D = 10\text{ V}$, $I_S = -10\text{ mA}$ $V_D = -10\text{ V}$, $I_S = 10\text{ mA}$		50	Ω
	Source OFF Leakage Current	$I_{S(off)}$	$V_{in} = 3.5\text{ V}$, DG306A $V_S = 14\text{ V}$, $V_D = -14\text{ V}$ $V_S = -14\text{ V}$, $V_D = 14\text{ V}$	-0.12	0.12	
	Drain OFF Leakage Current	$I_{D(off)}$	$V_{in} = 11\text{ V}$ or 3.5 V , DG307A ² $V_D = 14\text{ V}$, $V_S = -14\text{ V}$ $V_D = -14\text{ V}$, $V_S = 14\text{ V}$	-0.12	0.12	
	Drain ON Leakage Current	$I_{D(on)}$	$V_{in} = 11\text{ V}$, DG306A $V_D = V_S = 14\text{ V}$ $V_{in} = 3.5\text{ V}$ or 11 V , DG307A ² $V_D = V_S = -14\text{ V}$	-0.12	0.12	
INPUT	Input Current Input Voltage High	I_{INH}	$V_{in} = 15\text{ V}$		1.0	μA
	Input Current Input Voltage Low	I_{INL}	$V_{in} = 0\text{ V}$	-1.0		
	Positive Supply Current	I_+	$V_{in} = 15\text{ V}$ $V_{in} = 0\text{ V}$		10 10	
SUPPLY	Negative Supply Current	I_-	$V_{in} = 15\text{ V}$ $V_{in} = 0\text{ V}$	-10 -10		

NOTES:

- The algebraic convention whereby the most negative value is a minimum, and the most positive value is a maximum, is used in this data sheet.
- V_{in} = input voltage to perform proper function.

DG308A/DG309



PAD NO.	FUNCTION
1	Input 1
2	Drain 1
3	Source 1
4	V-
5	Ground
6	Source 4
7	Drain 4
8	Input 4
9	Input 3
10	Drain 3
11	Source 3
13	V+ (Substrate)
14	Source 2
15	Drain 2
16	Input 2

DC ELECTRICAL CHARACTERISTICS

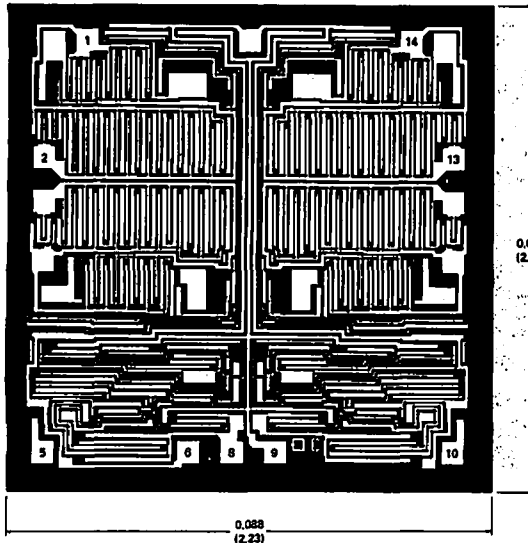
$T_A = 25^\circ\text{C}$

	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: $V_+ = 15\text{ V}$, $V_- = -15\text{ V}$, $GND = 0\text{ V}$	LIMITS		UNIT
				MIN ¹	MAX	
SWITCH	Drain-Source ON Resistance	$r_{DS(on)}$	$V_D = 10\text{ V}$, $I_S = -10\text{ mA}$		100	Ω
			$V_D = -10\text{ V}$, $I_S = 10\text{ mA}$			
	Source OFF Leakage Current	$I_{S(off)}$	$V_{in} = 3.5\text{ V}$, DG308A	$V_S = 14\text{ V}$, $V_D = -14\text{ V}$	0.12	
			$V_{in} = 11\text{ V}$, DG309	$V_S = -14\text{ V}$, $V_D = 14\text{ V}$	-0.12	
	Drain OFF Leakage Current	$I_{D(off)}$		$V_D = 14\text{ V}$, $V_S = -14\text{ V}$	0.12	
INPUT	Drain ON Leakage Current	$I_{D(on)}$	$V_{in} = 11\text{ V}$, DG308A	$V_D = -14\text{ V}$, $V_S = 14\text{ V}$	-0.12	
			$V_{in} = 0\text{ V}$, DG309	$V_D = 14\text{ V}$, $V_S = -14\text{ V}$	0.12	
	Input Current Input Voltage High	I_{INH}	$V_{in} = 15\text{ V}$		1.0	μA
	Input Current Input Voltage Low	I_{INL}	$V_{in} = 0\text{ V}$	-1.0		
	Positive Supply Current	I_+	$V_{in} = 15\text{ V}$		10	
SUPPLY	Negative Supply Current	I_-	$V_{in} = 0\text{ V}$		10	
			$V_{in} = 15\text{ V}$		-10	
			$V_{in} = 0\text{ V}$		-10	

NOTES:

1. The algebraic convention whereby the most negative value is a minimum, and the most positive value is a maximum, is used in this data sheet.

DG381A



PAD NO.	FUNCTION
1	Source 1
2	Drain 1
5	Input 1
6	V+ (Substrate)
8	V _R
9	V-
10	Input 2
13	Drain 2
14	Source 2

DC ELECTRICAL CHARACTERISTICS

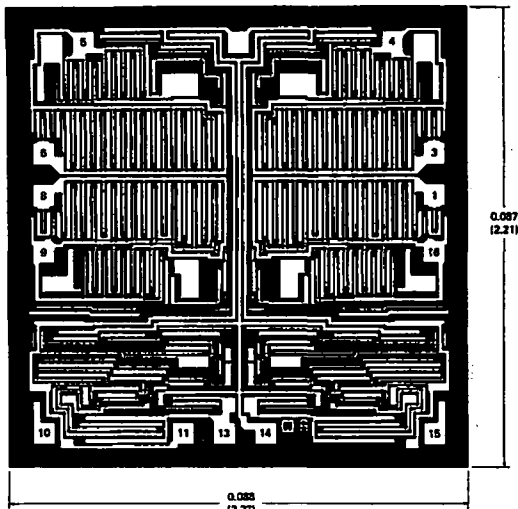
T_A = 25°C

	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: V ₊ = 15 V, V ₋ = -15 V, GND = 0 V	LIMITS		UNIT
				MIN ¹	MAX	
SWITCH	Drain-Source ON Resistance	r _{DS(on)}	V _D = 10 V, I _S = -10 mA V _D = -10 V, I _S = 10 mA		50	Ω
	Source OFF Leakage Current	I _{S(off)}	V _{in} = 4 V	V _S = 14 V, V _D = -14 V V _S = -14 V, V _D = 14 V	-0.12	μA
	Drain OFF Leakage Current	I _{D(off)}		V _D = 14 V, V _S = -14 V V _D = -14 V, V _S = 14 V	-0.12	
	Drain ON Leakage Current	I _{D(on)}		V _D = V _S = 14 V V _D = V _S = -14 V	-0.12	
			V _{in} = 0.8 V			
INPUT	Input Current Input Voltage High	I _{INH}	V _{in} = 15 V		1.0	μA
	Input Current Input Voltage Low	I _{INL}	V _{in} = 0 V	-1.0		
SUPPLY	Positive Supply Current	I ₊	V _{in} = 4 V V _{in} = 0.8 V		500 10	μA
	Negative Supply Current	I ₋	V _{in} = 4 V V _{in} = 0.8 V	-10 -10		

NOTES:

1. The algebraic convention whereby the most negative value is a minimum, and the most positive value is a maximum, is used in this data sheet.

DG384A



PAD NO.	FUNCTION
1	Drain 1
3	Drain 3
4	Source 3
5	Source 4
6	Drain 4
8	Drain 2
9	Source 2
10	Input 2
11	V+ (Substrate)
13	GND
14	V-
15	Input 1
16	Source 1

DC ELECTRICAL CHARACTERISTICS

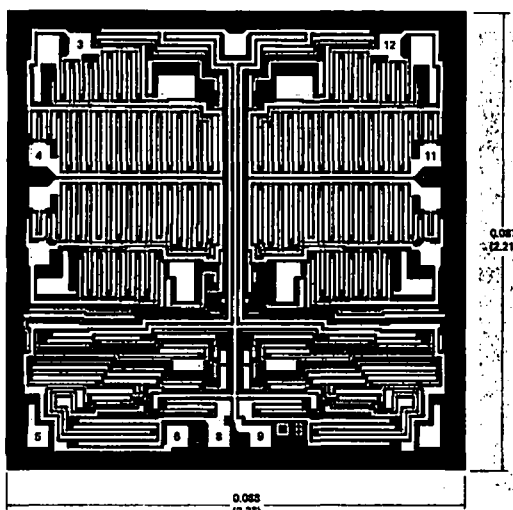
$T_A = 25^\circ\text{C}$

	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: $V_+ = 15\text{ V}$, $V_- = -15\text{ V}$, GND = 0 V	LIMITS		UNIT
				MIN ¹	MAX	
SWITCH	Drain-Source ON Resistance	$r_{DS(on)}$	$V_D = 10\text{ V}$, $I_S = -10\text{ mA}$ $V_D = -10\text{ V}$, $I_S = 10\text{ mA}$		50	Ω
	Source OFF Leakage Current	$I_{S(off)}$	0.8 V	$V_S = 14\text{ V}$, $V_D = -14\text{ V}$	0.12	μA
	Drain OFF Leakage Current	$I_{D(off)}$		$V_D = -14\text{ V}$, $V_S = 14\text{ V}$	-0.12	
	Drain ON Leakage Current	$I_{D(on)}$		$V_D = 14\text{ V}$, $V_S = -14\text{ V}$	0.12	
				$V_D = -14\text{ V}$, $V_S = 14\text{ V}$	-0.12	
			$V_{in} = 4\text{ V}$	$V_D = V_S = 14\text{ V}$	0.12	
INPUT	Input Current Input Voltage High	I_{INH}	$V_{in} = 15\text{ V}$		1.0	μA
	Input Current Input Voltage Low	I_{INL}	$V_{in} = 0\text{ V}$	-1.0		
SUPPLY	Positive Supply Current	I_+	$V_{in} = 4\text{ V}$		500	μA
			$V_{in} = 0.8\text{ V}$		10	
	Negative Supply Current	I_-	$V_{in} = 4\text{ V}$	-10		
			$V_{in} = 0.8\text{ V}$	-10		

NOTES:

1. The algebraic convention whereby the most negative value is a minimum, and the most positive value is a maximum, is used in this data sheet.

DG387A



PAD NO.	FUNCTION
3	Drain 1
4	Source 1
5	Input 1
6	V+ (Substrate)
8	V _R
9	V-
11	Source 2
12	Drain 2

DC ELECTRICAL CHARACTERISTICS

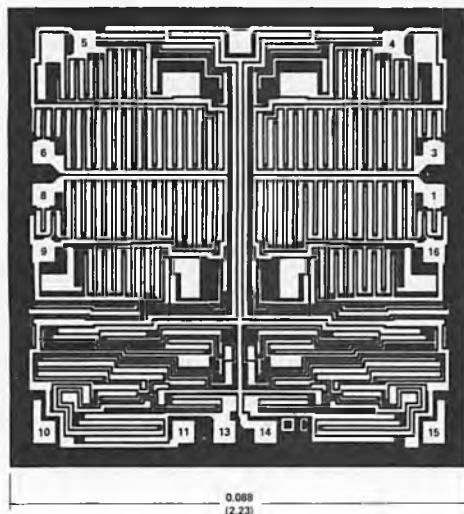
T_A = 25°C

	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: V ₊ = 15 V, V ₋ = -15 V, GND = 0 V	LIMITS		UNIT
				MIN ¹	MAX	
SWITCH	Drain-Source ON Resistance	r _{DS(on)}	V _D = 10 V, I _S = -10 mA		50	Ω
			V _D = -10 V, I _S = 10 mA			
	Source OFF Leakage Current	I _{S(off)}	V _{in} = 0.8 V, SW 1		0.12	
			V _S = 14 V, V _D = -14 V			
			V _S = -14 V, V _D = 14 V	-0.12		
SWITCH	Drain OFF Leakage Current	I _{D(off)}	V _{in} = 4 V, SW 2		0.12	
			V _D = 14 V, V _S = -14 V			
			V _D = -14 V, V _S = 14 V	-0.12		
SWITCH	Drain ON Leakage Current	I _{D(on)}	V _{in} = 4 V, SW 1		0.12	
			V _{in} = 0.8 V, SW 2			
INPUT	Input Current	I _{IN}	V _{in} = 15 V		1.0	μA
	Input Voltage High	I _{INH}	V _{in} = 0 V	-1.0		
	Input Voltage Low	I _{INL}				
SUPPLY	Positive Supply Current	I ₊	V _{in} = 4 V		500	
			V _{in} = 0.8 V		10	
	Negative Supply Current	I ₋	V _{in} = 4 V	-10		
			V _{in} = 0.8 V	-10		

NOTES:

- The algebraic convention whereby the most negative value is a minimum, and the most positive value is a maximum, is used in this data sheet.

DG390A



PAD NO.	FUNCTION
1	Input 1
3	Drain 3
4	Source 3
5	Source 4
6	Drain 4
8	Drain 2
9	Source 2
10	Input 2
11	V+ (Substrate)
13	GND
14	V-
15	Input 1
16	Source 1

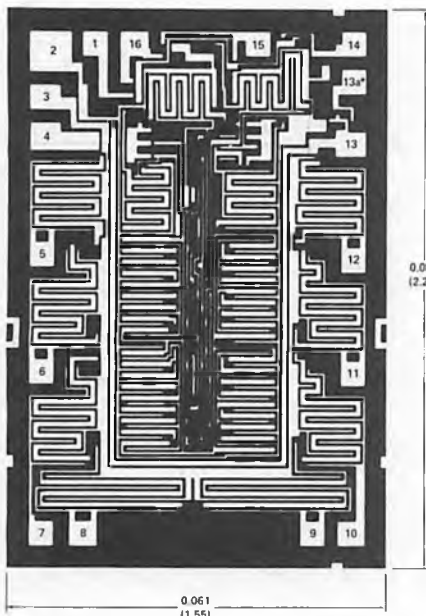
DC ELECTRICAL CHARACTERISTICS

$T_A = 25^\circ\text{C}$

	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: $V_+ = 15\text{ V}$, $V_- = -15\text{ V}$, $GND = 0\text{ V}$	LIMITS		UNIT
				MIN ¹	MAX	
SWITCH	Drain-Source ON Resistance	$r_{DS(on)}$	$V_D = 10\text{ V}$, $I_S = -10\text{ mA}$		50	Ω
			$V_D = -10\text{ V}$, $I_S = 10\text{ mA}$			
	Source OFF Leakage Current	$I_{S(off)}$	$V_{in} = 0.8\text{ or }4\text{ V}$	$V_S = 14\text{ V}$, $V_D = -14\text{ V}$	0.12	μA
				$V_S = -14\text{ V}$, $V_D = 14\text{ V}$	-0.12	
	Drain OFF Leakage Current	$I_{D(off)}$	$V_{in} = 4\text{ or }0.8\text{ V}$	$V_D = 14\text{ V}$, $V_S = -14\text{ V}$	0.12	
INPUT	Drain ON Leakage Current	$I_{D(on)}$		$V_D = -14\text{ V}$, $V_S = 14\text{ V}$	-0.12	
				$V_D = V_S = 14\text{ V}$	0.12	
				$V_D = V_S = -14\text{ V}$	-0.12	
	Input Current Input Voltage High	I_{INH}	$V_{in} = 15\text{ V}$		1.0	
	Input Current Input Voltage Low	I_{INL}	$V_{in} = 0\text{ V}$	-1.0		
SUPPLY	Positive Supply Current	I_+	$V_{in} = 4\text{ V}$		500	μA
			$V_{in} = 0.8\text{ V}$		10	
	Negative Supply Current	I_-	$V_{in} = 4\text{ V}$	-10		
			$V_{in} = 0.8\text{ V}$	-10		

NOTES:

1. The algebraic convention whereby the most negative value is a minimum, and the most positive value is a maximum, is used in this data sheet.



PAD NO.	FUNCTION
1	Enable
2†	V+ (Substrate)
3	Drain
4†	V+ (Substrate)
5	Source 8
6	Source 7
7	Source 6
8	Source 5
9	Source 4
10	Source 3
11	Source 2
12	Source 1
13	V-
14	Address 0
15	Address 1
16	Address 2

* Pad 13a is connected to V-
† Pads 2 and 4 are interconnected, either one may be used

DC ELECTRICAL CHARACTERISTICS

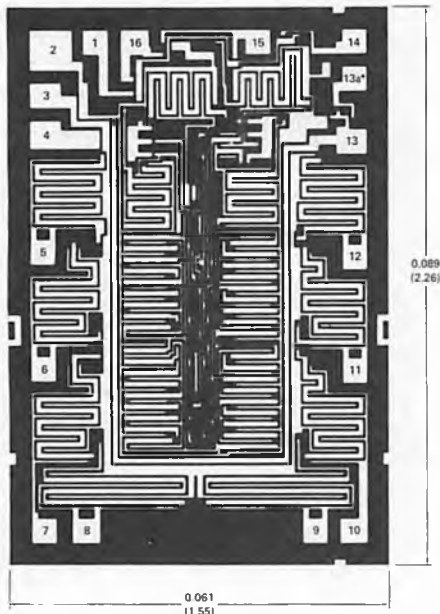
T_A = 25°C

	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: V _D = 5 V, V _S = -20 V, V _{EN} = 3.5 V, V _{AL} = 0.6 V, V _{AH} = 3.5 V	LIMITS		UNIT
				MIN ¹	MAX	
SWITCH	Drain-Source ON Resistance	r _{DS(on)}	I _S = -100 μA	V _D = 5 V	200	Ω
				V _D = 0 V	250	
				V _D = -5 V	800	
	Source OFF Leakage Current	I _{S(off)}	V _D = 0 V, V _{EN} = 0.6 V, V _S = 10 V	-0.12		μA
INPUT	Drain OFF Leakage Current	I _{D(off)}	V _D = 10 V, V _{EN} = 0.6 V, V _S = 0 V	-0.12		
	Channel ON Leakage Current	I _{D(on)} + I _{S(on)}	V _D = V _S = 0 V		0.12	
SUPPLY	Input Current Input Voltage Low	I _{INL}	V _{AL} = 0 V	-1200		mA
	Input Current Input Voltage High	I _{INH}	V _{AH} = 3.5 V		-150	
SUPPLY	Drain Supply Current	I ₋	V _A = 0 V	V _{EN} = 0 V	-6.0	mA
				V _{EN} = 0 V	-6.0	
	Source Supply Current	I ₊		V _{EN} = 0 V	7.0	
					8.0	

NOTES:

1. The algebraic convention whereby the most negative value is a minimum, and the most positive value is a maximum, is used in this data sheet.

DG503



PAD NO.	FUNCTION
1	Enable
2†	V+ (Substrate)
3	Drain
4†	V+ (Substrate)
5	Source 8
6	Source 7
7	Source 6
8	Source 5
9	Source 4
10	Source 3
11	Source 2
12	Source 1
13	V-
14	Address 0
15	Address 1
16	Address 2

*Pad 13a is connected to V-.

†Pads 2 and 4 are interconnected, either one may be used.

DC ELECTRICAL CHARACTERISTICS

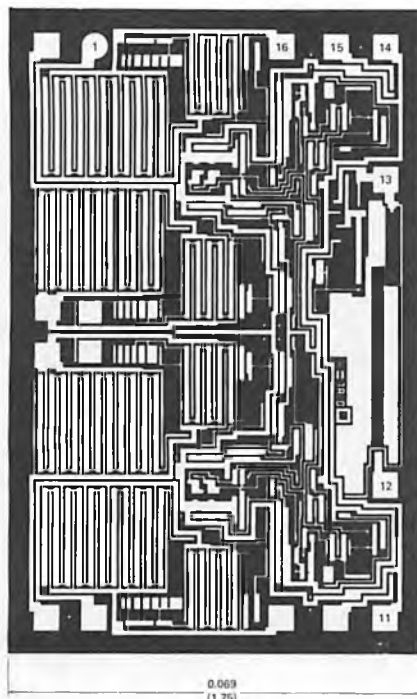
T_A = 25°C

	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: V ₋ = 10 V, V ₋ = -20 V, V _{EN} = 8.5 V, V _{AL} = 0.6 V, V _{AH} = 8.5 V	LIMITS		UNIT
				MIN ¹	MAX	
SWITCH	Drain-Source ON Resistance	r _{DS(on)}	I _S = -100 μA, V _D = 10 V		150	Ω
			I _S = 1.0 mA	V _D = 0 V	250	
				V _D = -10 V	800	
	Source OFF Leakage Current	I _{S(off)}	V _D = 10 V, V _{EN} = 0.6 V, V _S = -10 V	-0.12		μA
INPUT	Drain OFF Leakage Current	I _{D(off)}	V _D = -10 V, V _{EN} = 0.6 V, V _S = 10 V	-0.12		
	Channel ON Leakage Current	I _{D(on)} + I _{S(on)}	V _D = V _S = 10 V		0.12	
	Input Current Input Voltage Low	I _{INL}	V _{AL} = 0 V	-1.0		
SUPPLY	Drain Supply Current	I ₋	V _A = 0 V	V _{EN} = 0 V	-6.0	mA
				V _{EN} = 0 V	-6.0	
	Source Supply Current	I ₊		V _{EN} = 0 V	7.0	
					8.0	

NOTES:

1. The algebraic convention whereby the most negative value is a minimum, and the most positive value is a maximum, is used in this data sheet.

DG5040



PAD NO.	FUNCTION
1	Drain 1
11	V+ (Substrate)
12	V _L
13	GND
14	V-
15	Input 1
16	Source 1

DC ELECTRICAL CHARACTERISTICS

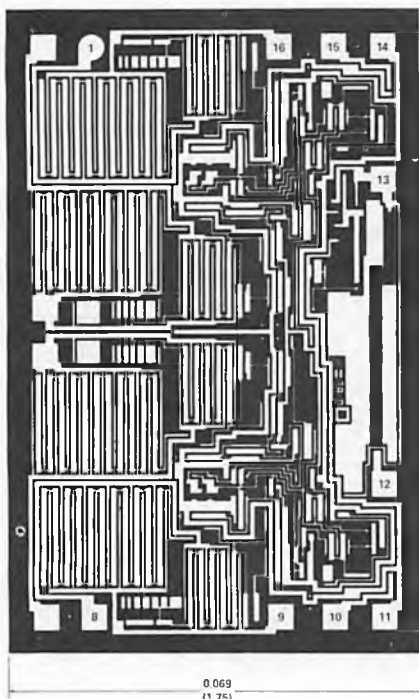
T_A = 25°C

	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: V _T = 15 V, V ₋ = -15 V, V _L = 5 V, GND = 0 V	LIMITS		UNIT
				MIN ¹	MAX	
SWITCH	Drain-Source ON Resistance	r _{DS(on)}	V _D = 10 V, I _S = -10 mA		50	Ω
			V _D = -10 V, I _S = 10 mA			
	Source OFF Leakage Current	I _{S(off)}	V _{in} = 0 V	V _S = 14 V, V _D = -14 V	0.12	
				V _S = -14 V, V _D = 14 V	-0.12	
	Drain OFF Leakage Current	I _{D(off)}	V _{in} = 2.0 V	V _D = 14 V, V _S = -14 V	0.12	
INPUT				V _D = -14 V, V _S = 14 V	-0.12	
	Drain ON Leakage Current	I _{D(on)}	V _{in} = 2.0 V	V _D = V _S = 14 V	0.12	
				V _D = V _S = -14 V	-0.12	
	Input Current Input Voltage High	I _{INH}	V _{in} = 15 V		1	
	Input Current Input Voltage Low	I _{INL}	V _{in} = 0 V	-1		μA
SUPPLY	Positive Supply Current	I ₊	V _{in} = 2.4 V		300	
			V _{in} = 0 V		300	
	Negative Supply Current	I ₋	V _{in} = 2.4 V	-300		
			V _{in} = 0 V	-300		
	Logic Supply Current	I _L	V _{in} = 2.4 V		300	
			V _{in} = 0 V			
	Ground Supply Current	I _{GND}	V _{in} = 2.4 V	-300		
			V _{in} = 0 V	-300		

NOTES:

1. The algebraic convention whereby the most negative value is a minimum, and the most positive value is a maximum, is used in this data sheet.

DG5041



PAD NO.	FUNCTION
1	Drain 1
8	Drain 2
9	Source 2
10	Input 2
11	V- (Substrate)
12	V _L
13	GND
14	V-
15	Input 1
16	Source 1

DC ELECTRICAL CHARACTERISTICS

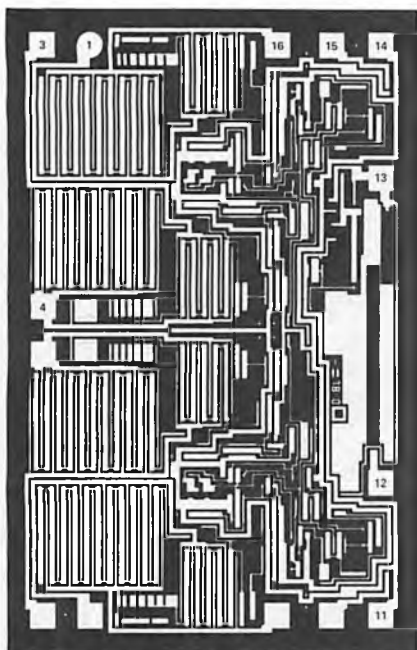
T_A = 25°C

	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: V ₊ = 15 V, V ₋ = -15 V, V _L = 5 V, GND = 0 V	LIMITS		UNIT
				MIN ¹	MAX	
SWITCH	Drain-Source ON Resistance	r _{DS(on)}	V _D = 10 V, I _S = -10 mA V _D = -10 V, I _S = 10 mA		50	Ω
	Source OFF Leakage Current	I _{S(off)}	V _{in} = 0 V	V _S = 14 V, V _D = -14 V V _S = -14 V, V _D = 14 V	0.12 -0.12	μA
	Drain OFF Leakage Current	I _{D(off)}		V _D = 14 V, V _S = -14 V V _D = -14 V, V _S = 14 V	0.12 -0.12	
	Drain ON Leakage Current	I _{D(on)}		V _D = V _S = 14 V V _D = V _S = -14 V	0.12 -0.12	
			V _{in} = 2.0 V			
INPUT	Input Current Input Voltage High	I _{INH}	V _{in} = 15 V		1	μA
	Input Current Input Voltage Low	I _{INL}	V _{in} = 0 V	-1		
SUPPLY	Positive Supply Current	I ₊	V _{in} = 2.4 V V _{in} = 0 V		300 300	μA
	Negative Supply Current	I ₋	V _{in} = 2.4 V V _{in} = 0 V	-300 -300		
	Logic Supply Current	I _L	V _{in} = 2.4 V V _{in} = 0 V		300 300	
	Ground Supply Current	I _{GND}	V _{in} = 2.4 V V _{in} = 0 V	-300 -300		

NOTES:

1. The algebraic convention whereby the most negative value is a minimum, and the most positive value is a maximum, is used in this data sheet.

DG5042



0.107
(2.72)

0.069
(1.76)

PAD NO.	FUNCTION
1	Drain 1
3	Drain 2
4	Source 2
11	V+ (Substrate)
12	V _L
13	GND
14	V-
15	Input 1
16	Source 1

Order Number:
DG5042A Dice

DC ELECTRICAL CHARACTERISTICS

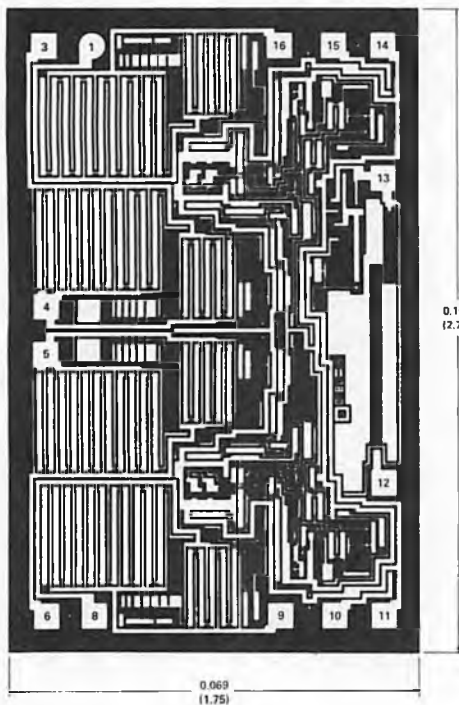
T_A = 25°C

	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: V ₊ = 15 V, V ₋ = -15 V, V _L = 5 V, GND = 0 V	LIMITS		UNIT
				MIN ¹	MAX	
SWITCH	Drain-Source ON Resistance	r _{DS(on)}	V _D = 10 V, I _S = -10 mA		50	Ω
	Source OFF Leakage Current	I _{S(off)}	V _{in} = 0 V, SW 1		0.12	
	Drain OFF Leakage Current	I _{D(off)}	V _{in} = 2.0 V, SW 2		0.12	
	Drain ON Leakage Current	I _{D(on)}	V _{in} = 2.0 V, SW 1		0.12	
			V _{in} = 0 V, SW 2		0.12	
INPUT	Input Current Input Voltage High	I _{INH}	V _{in} = 15 V		1	
	Input Current Input Voltage Low	I _{INL}	V _{in} = 0 V	-1		μA
SUPPLY	Positive Supply Current	I ₊	V _{in} = 2.4 V		300	
			V _{in} = 0 V		300	
	Negative Supply Current	I ₋	V _{in} = 2.4 V	-300		
			V _{in} = 0 V	-300		
	Logic Supply Current	I _L	V _{in} = 2.4 V		300	
			V _{in} = 0 V		300	
	Ground Supply Current	I _{GND}	V _{in} = 2.4 V	-300		
			V _{in} = 0 V	-300		

NOTES:

1. The algebraic convention whereby the most negative value is a minimum, and the most positive value is a maximum, is used in this data sheet.

DG5043



PAD NO.	FUNCTION
1	Drain 1
3	Drain 3
4	Source 3
5	Source 4
6	Drain 4
8	Drain 2
9	Source 2
10	Input 2
11	V+ (Substrate)
12	V _L
13	GND
14	V-
15	Input 1
16	Source 1

DC ELECTRICAL CHARACTERISTICS

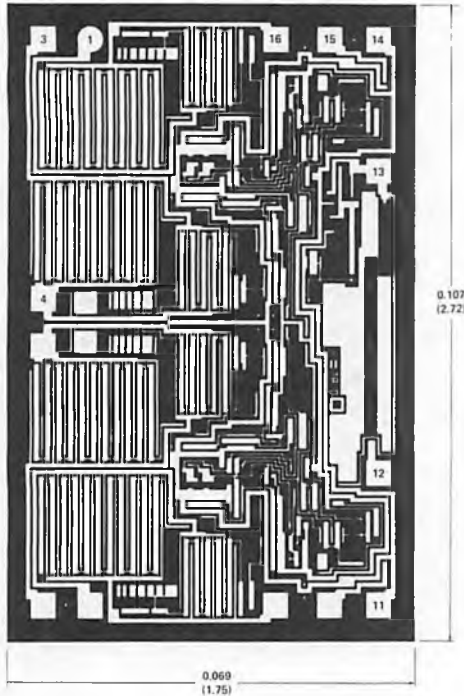
T_A = 25°C

	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: V ₊ = 15 V, V ₋ = -15 V, V _L = 5 V, GND = 0 V	LIMITS		UNIT
				MIN ¹	MAX	
SWITCH	Drain-Source ON Resistance	r _{DS(on)}	V _D = 10 V, I _S = -10 mA		50	Ω
	Source OFF Leakage Current	I _{S(off)}	V _D = -10 V, I _S = 10 mA			
	Drain OFF Leakage Current	I _{D(off)}	V _{in} = 0 V, SW 1 & 2		0.12	
			V _S = 14 V, V _D = -14 V			
			V _S = -14 V, V _D = 14 V	-0.12		
INPUT	Drain ON Leakage Current	I _{D(on)}	V _{in} = 2.0 V, SW 3 & 4		0.12	
			V _D = -14 V, V _S = -14 V			
			V _D = -14 V, V _S = 14 V	-0.12		
	Drain ON Leakage Current	I _{D(on)}	V _{in} = 2.0 V, SW 1 & 2		0.12	
			V _{in} = 0 V, SW 3 & 4			
SUPPLY	Input Current Input Voltage High	I _{INH}	V _{in} = 15 V		1	
	Input Current Input Voltage Low	I _{INL}	V _{in} = 0 V	-1		μA
	Positive Supply Current	I ₊	V _{in} = 2.4 V		300	
			V _{in} = 0 V		300	
	Negative Supply Current	I ₋	V _{in} = 2.4 V	-300		
SUPPLY			V _{in} = 0 V	-300		
	Logic Supply Current	I _L	V _{in} = 2.4 V		300	
			V _{in} = 0 V		300	
	Ground Supply Current	I _{GND}	V _{in} = 2.4 V	-300		
			V _{in} = 0 V	-300		

NOTES:

1. The algebraic convention whereby the most negative value is a minimum, and the most positive value is a maximum, is used in this data sheet.

DG5044



PAD NO.	FUNCTION
1	Drain 1
3	Drain 2
4	Source 2
11	V+ (Substrate)
12	V _L
13	GND
14	V-
15	Input 1
16	Source 1

DC ELECTRICAL CHARACTERISTICS

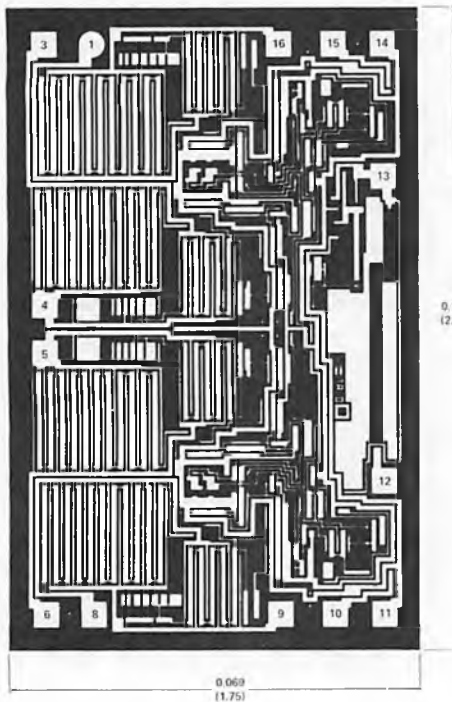
T_A = 25°C

	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: V ₊ = 15 V, V ₋ = -15 V, V _L = 5 V, GND = 0 V	LIMITS		UNIT
				MIN ¹	MAX	
SWITCH	Drain-Source ON Resistance	r _{DS(on)}	V _D = 10 V, I _S = -10 mA		50	Ω
	Source OFF Leakage Current	I _{S(off)}	V _D = -10 V, I _S = 10 mA			
	Drain OFF Leakage Current	I _{D(off)}	V _{in} = 0 V			
	Drain ON Leakage Current	I _{D(on)}	V _{in} = 2.4 V			
INPUT	Input Current Input Voltage High	I _{INH}	V _{in} = 2.4 V		1	
	Input Current Input Voltage Low	I _{INL}	V _{in} = 0 V	-1		μA
SUPPLY	Positive Supply Current	I ₊	V _{in} = 2.4 V		300	
			V _{in} = 0 V		300	
	Negative Supply Current	I ₋	V _{in} = 2.4 V	-300		
			V _{in} = 0 V	-300		
	Ground Supply Current	I _{GND}	V _{in} = 2.4 V	-300		
			V _{in} = 0 V	-300		
	Logic Supply Current	I _L	V _{in} = 0 or 2.4		300	

NOTES:

1. The algebraic convention whereby the most negative value is a minimum, and the most positive value is a maximum, is used in this data sheet.

DG5045



PAD NO.	FUNCTION
1	Drain 1
3	Drain 3
4	Source 3
5	Source 4
6	Drain 4
8	Drain 2
9	Source 2
10	Input 2
11	V+ (Substrate)
12	V _L
13	GND
14	V-
15	Input 1
16	Source 1

DC ELECTRICAL CHARACTERISTICS

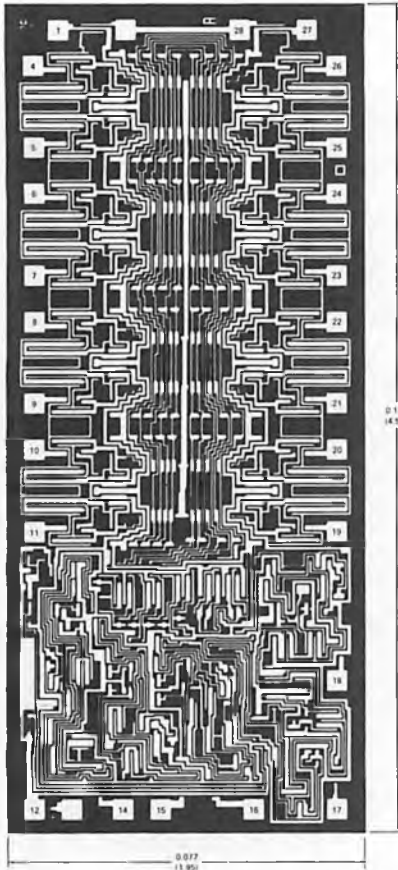
T_A = 25°C

	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: V ⁺ = 15 V, V ⁻ = -15 V, V _L = 5 V, GND = 0 V	LIMITS		UNIT	
				MIN ¹	MAX		
SWITCH	Drain-Source ON Resistance	r _{DS(on)}	V _D = 10 V, I _S = -10 mA V _D = -10 V, I _S = 10 mA		50	Ω	
	Source OFF Leakage Current	I _{S(off)}	V _{in} = 0 V	V _S = 14 V, V _D = -14 V V _S = -14 V, V _D = 14 V	-0.12	0.12	
	Drain OFF Leakage Current	I _{D(off)}		V _D = 14 V, V _S = -14 V V _D = -14 V, V _S = 14 V	-0.12	0.12	
	Drain ON Leakage Current	I _{D(on)}		V _{in} = 2.4 V	V _D = V _S = 14 V V _D = V _S = -14 V	-0.12	0.12
	INPUT	Input Current Input Voltage High	I _{INH}	V _{in} = 2.4 V		1	μA
		Input Current Input Voltage Low	I _{INL}	V _{in} = 0 V	-1		
SUPPLY	Positive Supply Current	I ⁺	V _{in} = 2.4 V V _{in} = 0 V		300 300		
	Negative Supply Current	I ⁻	V _{in} = 2.4 V V _{in} = 0 V	-300 -300			
	Ground Supply Current	I _{GND}	V _{in} = 0 or 2.4 V	-300			
	Logic Supply Current	I _L			300		

NOTES:

1. The algebraic convention whereby the most negative value is a minimum, and the most positive value is a maximum, is used in this data sheet.

DG506A



PAD NO.	FUNCTION
1	V+ (Substrate)
4	Source 16
5	Source 15
6	Source 14
7	Source 13
8	Source 12
9	Source 11
10	Source 10
11	Source 9
12	Ground
14	Address 3
15	Address 2
16	Address 1
17	Address 0
18	Enable
19	Source 1
20	Source 2
21	Source 3
22	Source 4
23	Source 5
24	Source 6
25	Source 7
26	Source 8
27	V-
28	Drain

DC ELECTRICAL CHARACTERISTICS

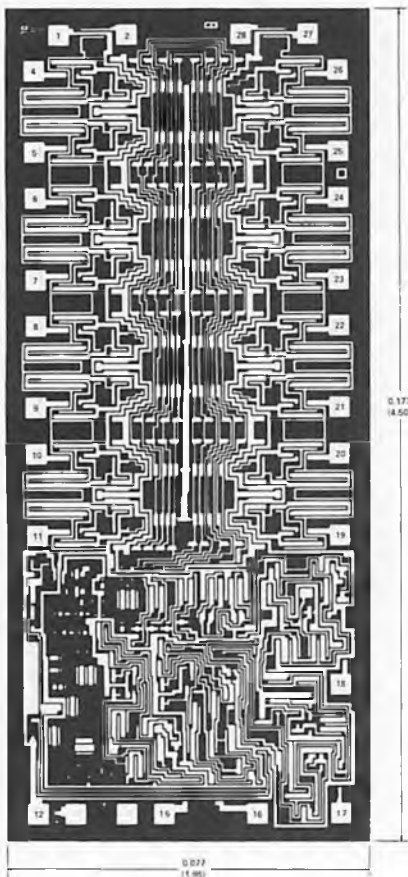
$T_A = 25^\circ\text{C}$

	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: $V_+ = 15\text{ V}$, $V_- = -15\text{ V}$, $\text{GND} = 0\text{ V}$, $V_{\text{REF}} = 2\text{ Open}$	LIMITS		UNIT
				MIN ¹	MAX	
SWITCH	Drain-Source ON Resistance	$r_{\text{DS(on)}}$	$V_D = \pm 10\text{ V}$, $I_S = -200\text{ }\mu\text{A}$, $V_{\text{AL}} = 76\text{ mV}$, $V_{\text{AH}} = 2.4\text{ V}$		450	Ω
	Source OFF Leakage Current	$I_{\text{S(off)}}$	$V_{\text{EN}} = 0$	$V_S = 15\text{ V}$, $V_D = -15\text{ V}$	0.12	μA
	Drain OFF Leakage Current	$I_{\text{D(off)}}$		$V_S = -15\text{ V}$, $V_D = 15\text{ V}$	-0.12	
	Drain ON Leakage Current	$I_{\text{D(on)}}$		$V_S = 15\text{ V}$, $V_D = -15\text{ V}$	0.12	
	Drain ON Leakage Current	$I_{\text{D(on)}}$		$V_S = -15\text{ V}$, $V_D = 15\text{ V}$	-0.12	
INPUT	Address Enable Input Current Input Voltage High	I_{AH}	$V_A = 2.4\text{ V}$	-10		μA
	Address Enable Input Current Input Voltage Low	I_{AL}	$V_A = 15\text{ V}$		10	
	Address Enable Input Current Input Voltage High	I_{AH}	All $V_A = 0$	$V_{\text{EN}} = 2.4$	-10	
	Address Enable Input Current Input Voltage Low	I_{AL}		$V_{\text{EN}} = 0$	-10	
SUPPLY	Positive Supply Current	I_+	$V_{\text{EN}} = 5\text{ V}$		2.4	mA
	Positive Supply Current	I_+	$V_{\text{EN}} = 0$		2.4	
	Negative Supply Current	I_-	$V_{\text{EN}} = 5\text{ V}$	-1.5		
	Negative Supply Current	I_-	$V_{\text{EN}} = 0$	-1.5		

NOTES:

1. The algebraic convention whereby the most negative value is a minimum, and the most positive value is a maximum, is used in this data sheet.

DG507A



PAD NO.	FUNCTION
1	V+ (Substrate)
2	Drain B
4	Source 8B
5	Source 7B
6	Source 6B
7	Source 5B
8	Source 4B
9	Source 3B
10	Source 2B
11	Source 1B
12	GND
15	Address 2
16	Address 1
17	Address 0
18	Enable
19	Source 1A
20	Source 2A
21	Source 3A
22	Source 4A
23	Source 5A
24	Source 6A
25	Source 7A
26	Source 8A
27	V-
28	Drain A

DC ELECTRICAL CHARACTERISTICS

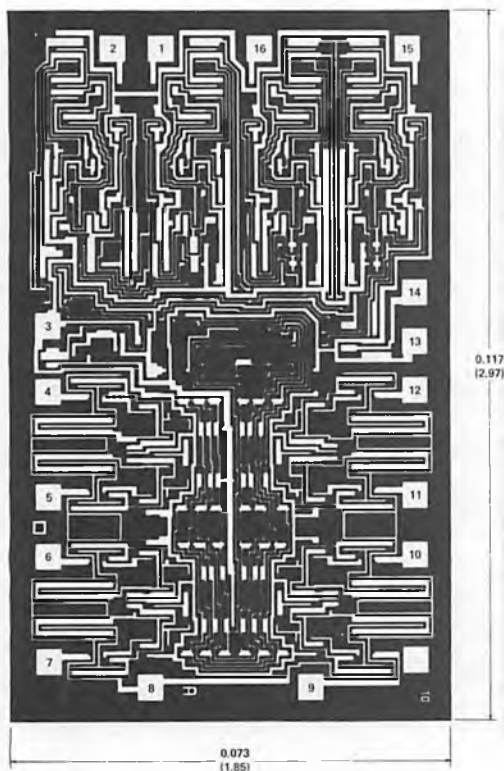
$T_A = 25^\circ\text{C}$

	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: $V_+ = 15\text{ V}$, $V_- = -15\text{ V}$, $\text{GND} = 0\text{ V}$, $V_{\text{REF}} = 2\text{ Open}$	LIMITS		UNIT
				MIN ¹	MAX	
SWITCH	Drain-Source ON Resistance	$r_{\text{DS(on)}}$	$V_D = \pm 10\text{ V}$, $I_S = -200\text{ }\mu\text{A}$, $V_{\text{AL}} = 76\text{ mV}$, $V_{\text{AH}} = 2.4\text{ V}$		450	Ω
	Source OFF Leakage Current	$I_{\text{S(off)}}$	$V_{\text{EN}} = 0$	$V_S = 10\text{ V}$, $V_D = -10\text{ V}$	0.12	μA
	Drain OFF Leakage Current	$I_{\text{D(off)}}$		$V_S = -10\text{ V}$, $V_D = 10\text{ V}$	-0.12	
	Drain ON Leakage Current	$I_{\text{D(on)}}$		$V_S = 10\text{ V}$, $V_D = -10\text{ V}$	0.12	
INPUT	Address Input Current	I_{AH}	$V_{\text{AL}} = 0.8\text{ V}$, $V_{\text{AH}} = 2.4\text{ V}$	$V_D = 10\text{ V}$		μA
	Input Voltage High			$V_D = -10\text{ V}$	-0.12	
	Address Input Current	I_{AL}	All $V_A = 0$, $V_{\text{EN}} = 2.4\text{ V}$		-10	
SUPPLY	Positive Supply Current	I_+	$V_A = 0$	$V_{\text{EN}} = 5\text{ V}$	2.4	mA
	Negative Supply Current	I_-		$V_{\text{EN}} = 0$	2.4	
	Enable Supply Current	I_{EN}		$V_{\text{EN}} = 5\text{ V}$	-1.5	μA
				$V_{\text{EN}} = 0$	-1.5	

NOTES:

1. The algebraic convention whereby the most negative value is a minimum, and the most positive value is a maximum, is used in this data sheet.

DG508A



PAD NO.	FUNCTION
1	Address 0
2	Enable
3	V-
4	Source 1
5	Source 2
6	Source 3
7	Source 4
8	Drain
9	Source 8
10	Source 7
11	Source 6
12	Source 5
13	V+ (Substrate)
14	Ground
15	Address 2
16	Address 1

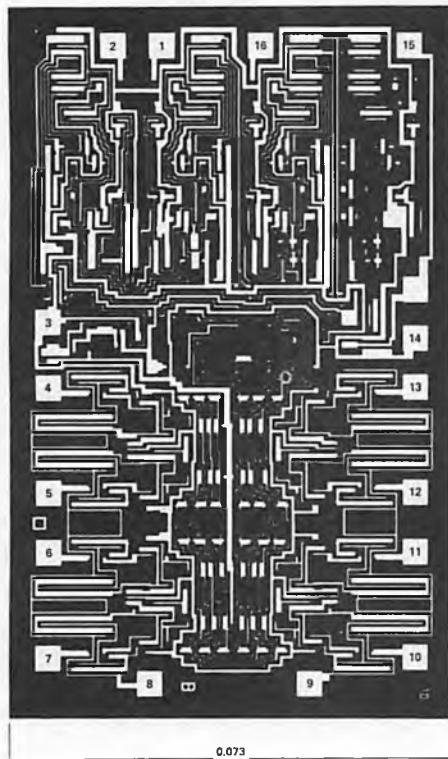
DC ELECTRICAL CHARACTERISTICS

$T_A = 25^\circ\text{C}$

PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: $V_+ = 15\text{ V}$, $V_- = -15\text{ V}$, $\text{GND} = 0\text{ V}$	LIMITS		UNIT
Drain-Source ON Resistance	$r_{DS(on)}$	$I_S = -200\text{ }\mu\text{A}$, $V_{AL} = 0.8\text{ V}$, $V_{AH} = 2.4\text{ V}$	$V_D = 10\text{ V}$ $V_D = -10\text{ V}$	450 450	Ω
Source OFF Leakage Current	$I_{S(off)}$	$V_{EN} = 0$	$V_S = 10\text{ V}$, $V_D = -10\text{ V}$ $V_S = -10\text{ V}$, $V_D = 10\text{ V}$	0.12 0.12	μA
Drain OFF Leakage Current	$I_{D(off)}$		$V_D = 10\text{ V}$, $V_S = -10\text{ V}$ $V_D = -10\text{ V}$, $V_S = 10\text{ V}$	0.12 -0.12	
Drain ON Leakage Current	$I_{D(on)}$		$V_{AL} = 0.8\text{ V}$, $V_{AH} = 2.4\text{ V}$ $V_S(\text{all}) = V_D = 10\text{ V}$ $V_S(\text{all}) = V_D = -10\text{ V}$	0.12 -0.12	
Address Input Current Input Voltage High	I_{AH}		$V_A = 2.4\text{ V}$ $V_A = 15\text{ V}$	-12 -12	
Address Input Current Input Voltage Low	I_{AL}	All $V_A = 0$	$V_{EN} = 2.4\text{ V}$ $V_{EN} = 0$	-12 -12	

NOTES:

1. The algebraic convention whereby the most negative value is a minimum, and the most positive value is a maximum, is used in this data sheet.



PAD NO.	FUNCTION
1	Address 0
2	Enable
3	V-
4	Source 1A
5	Source 2A
6	Source 3A
7	Source 4A
8	Drain A
9	Drain B
10	Source 4B
11	Source 3B
12	Source 2B
13	Source 1B
14	V+ (Substrate)
15	Ground
16	Address 1

DC ELECTRICAL CHARACTERISTICS

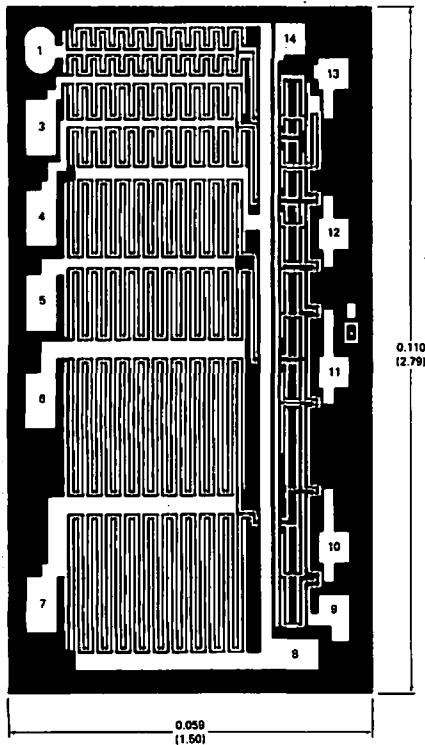
T_A = 25°C

	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: V ₊ = 15 V, V ₋ = -15 V, GND = 0 V	LIMITS		UNIT
				MIN ¹	MAX	
SWITCH	Drain-Source ON Resistance	r _{DS(on)}	V _{AL} = 0.8 V, V _{AH} = 2.4 V, I _S = -200 μA	V _D = 10 V V _D = -10 V	450 450	Ω
	Source OFF Leakage Current	I _{S(off)}	V _{EN} = 0	V _S = 10 V, V _D = -10 V V _S = -10 V, V _D = 10 V	0.12 -0.12	μA
	Drain OFF Leakage Current	I _{D(off)}		V _D = 10 V, V _S = -10 V V _D = -10 V, V _S = 10 V	0.12 -0.12	
	Drain ON Leakage Current	I _{D(on)}		V _{AL} = 0.8 V, V _{AH} = 2.4 V V _{S(all)} = V _D = 10 V V _{S(all)} = V _D = -10 V	0.12 -0.12	
INPUT	Address Input Current Input Voltage High	I _{AH}	All V _A = 0	V _A = 2.4 V V _A = 15 V	-10 -10	10 10
	Address Input Current Input Voltage Low	I _{AL}		V _{EN} = 2.4 V V _{EN} = 0	-10 -10	10 10
	Positive Supply Current	I ₊	V _{EN} = V _A = 0 or 2.4 V		2.4	mA
	Negative Supply Current	I ₋			-1.5	

NOTES:

1. The algebraic convention whereby the most negative value is a minimum, and the most positive value is a maximum, is used in this data sheet.

DG515



PAD NO.	FUNCTION
1	Source 4
3	Analog Ground 2
4	Source 3
5	Source 2
6	Analog Ground 1
7	Source 1
8	Sum JCT
9	V+ (Substrate)
10	B1
11	B2
12	B3
13	B4
14	V-

DC ELECTRICAL CHARACTERISTICS

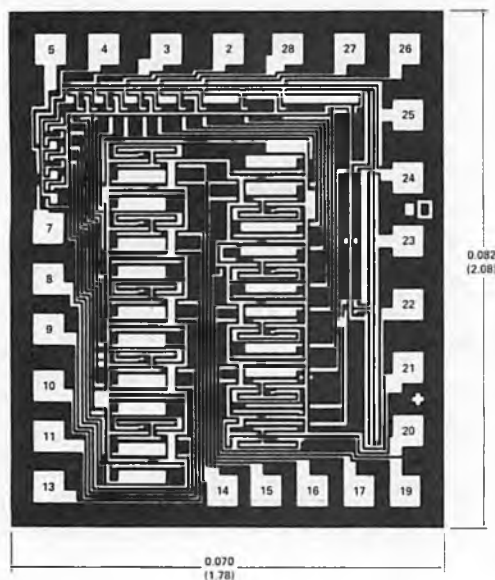
T_A = 25°C

PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: V ₊ = 8 V, V ₋ = 0 V	LIMITS		UNIT
			MIN ¹	MAX	
Drain-Source ON Resistance-Switch 1	r _{DS(on)}	I _S = 10 mA Either Switch Position		7.8	Ω
Drain-Source ON Resistance-Switch 2	r _{DS(on)}			15.6	
Drain-Source ON Resistance-Switch 3	r _{DS(on)}			31.2	
Drain-Source ON Resistance-Switch 4	r _{DS(on)}			62.5	
Summing Junction Drain OFF Leakage Current	I _{D(off)}	V _S = 100 mV, V _{SUMMING JUNCTION} = 0 V		0.12	μA
Analog Ground Drain OFF Leakage Current	I _{D(off)}	V _S = -100 mV, V _{ANALOG GROUND} = 0 V	-0.12		
Input Current Input Voltage Low	I _{INL}	V _{IN} = 0 V	-12		
Input Current Input Voltage High	I _{INH}	V _{IN} = 8 V		1.2	
Positive Supply Current	I ₊	V _{IN} = 8 V		5	
		V _{IN} = 0 V		5	
Negative Supply Current	I ₋	V _{IN} = 8 V		-5	
		V _{IN} = 0 V		-5	

NOTES:

1. The algebraic convention whereby the most negative value is a minimum, and the most positive value is a maximum, is used in this data sheet.

DG516



PAD NO.	FUNCTION
2	Source 6
3	Source 7
4	Source 8
5	Source 9
7	Source 10
8	V-
9	B10
10	B9
11	B8
13	B7
14	B6
15	B5
16	B4
17	B3
19	B2
20	B1
21	V+ (Substrate)
22	Sum JCT
23	S1
24	Analog Ground
25	S2
26	S3
27	S4
28	S5

DC ELECTRICAL CHARACTERISTICS

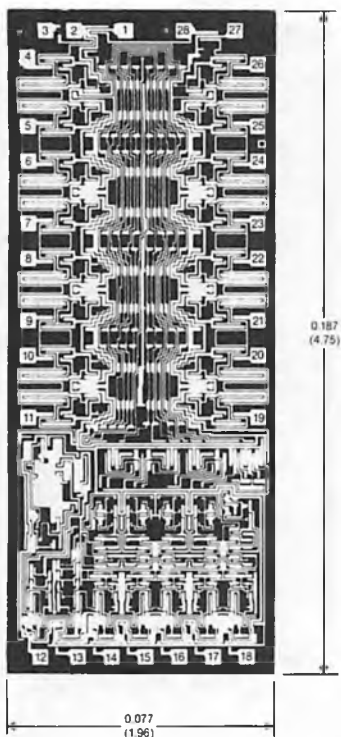
$T_A = 25^\circ\text{C}$

PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: $V_+ = 8\text{ V}, V_- = 0\text{ V}$		LIMITS		UNIT
				MIN ¹	MAX	
Drain-Source ON Resistance-Switch 1	$r_{DS(on)}$	$V_{in} = 0.27\text{ V}$, Either Switch Position	$I_S = 3.2\text{ mA}$		125	Ω
Drain-Source ON Resistance-Switch 2	$r_{DS(on)}$		$I_S = 1.6\text{ mA}$		250	
Drain-Source ON Resistance-Switch 3	$r_{DS(on)}$		$I_S = 0.8\text{ mA}$		500	
Drain-Source ON Resistance-Switch 4	$r_{DS(on)}$		$I_S = 0.4\text{ mA}$		1000	
Drain-Source ON Resistance-Switch 5	$r_{DS(on)}$		$I_S = 0.2\text{ mA}$		2000	
Drain-Source ON Resistance-Switch 6-10	$r_{DS(on)}$		$I_S = 0.1\text{ mA}$		4000	
Summing Junction Drain OFF Leakage Current	$I_{D(off)}$	$V_S = 100\text{ mV}$, $V_{SUMMING\ JUNCTION} = 0\text{ V}$			0.12	μA
Analog Ground Drain OFF Leakage Current	$I_{D(off)}$	$V_S = -100\text{ mV}$, $V_{ANALOG\ GROUND} = 0\text{ V}$		-0.12		
Input Current Input Voltage High	I_{INH}	$V_{in} = 8\text{ V}$			1.2	
Input Current Input Voltage Low	I_{INL}	$V_{in} = 0\text{ V}$		-12		
Positive Supply Current	I_+	$V_{in} = 8\text{ V}$			5	
		$V_{in} = 0\text{ V}$			5	
Negative Supply Current	I_-	$V_{in} = 8\text{ V}$		-5		
		$V_{in} = 0\text{ V}$		-5		

NOTES:

1. The algebraic convention whereby the most negative value is a minimum, and the most positive value is a maximum, is used in this data sheet.

DG526



PAD NO.	FUNCTION
1	V-
2	No Connection
3	RS
4	S16
5	S15
6	S14
7	S13
8	S12
9	S11
10	S10
11	S9
12	GND
13	WR
14	A3
15	A2
16	A1
17	A0
18	EN
19	S1
20	S2
21	S3
22	S4
23	S5
24	S6
25	S7
26	S8
27	V-
28	D

DC ELECTRICAL CHARACTERISTICS

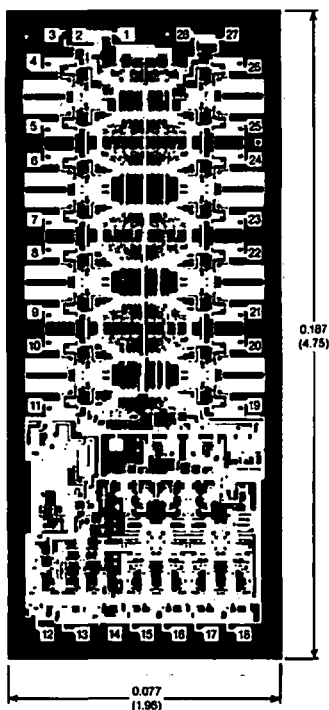
T_A = 25°C

	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: V+ = 15 V, V- = -15 V, GND = 0 V WR = 0 V, RS = 2.4 V	LIMITS		UNIT
				MIN ¹	MAX	
SWITCH	Drain-Source ON Resistance	r _{DS(on)}	V _{AL} = 0.8 V, V _{AH} = 2.4 V, I _S = -200 μA	V _D = 10 V V _D = -10 V	400 400	Ω
	Source OFF Leakage Current	I _{S(off)}	V _{EN} = 0	V _S = 10 V, V _D = -10 V V _S = -10 V, V _D = 10 V	100 -100	nA
	Drain OFF Leakage Current	I _{D(off)}		V _D = 10 V, V _S = -10 V V _D = -10 V, V _S = 10 V	100 -100	
	Drain ON Leakage Current	I _{D(on)}		V _{S(all)} = V _D = 10 V V _{S(all)} = V _D = -10 V	100 -100	
INPUT	Address Input Current	I _{AH}	V _A = 2.4 V	-10	10	μA
	Input Voltage High	I _{AL}	V _A = 15 V	-10	10	
	Address Input Current	I _{AL}	All V _A = 0 V, V _{EN} = 0 V, RS = 0 V	-10	10	mA
	Input Voltage Low	I _{AL}		-10	10	
	Positive Supply Current	I+		-2	3	
	Negative Supply Current	I-		-2		

NOTES:

1. The algebraic convention whereby the most negative value is a minimum, and the most positive value is a maximum, is used in this data sheet.

DG527



PAD NO.	FUNCTION
1	V+
2	D _b
3	RS
4	S _{8b}
5	S _{7b}
6	S _{6b}
7	S _{5b}
8	S _{4b}
9	S _{3b}
10	S _{2b}
11	S _{1b}
12	GND
13	WR
14	No Connection
15	A ₂
16	A ₁
17	A ₀
18	EN
19	S _{1a}
20	S _{2a}
21	S _{3a}
22	S _{4a}
23	S _{5a}
24	S _{6a}
25	S _{7a}
26	S _{8a}
27	V-
28	D _a

DC ELECTRICAL CHARACTERISTICS

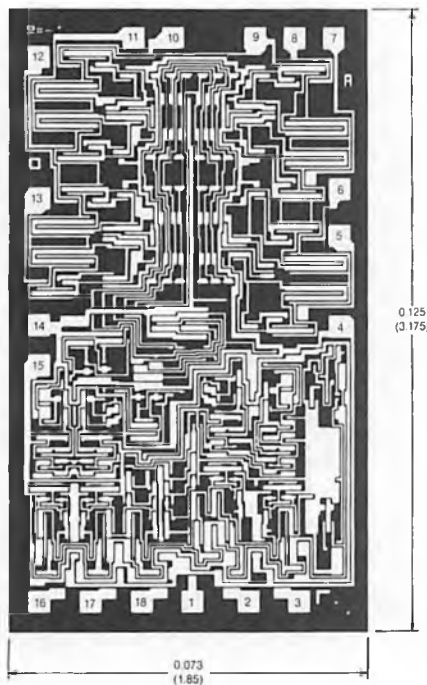
T_A = 25°C

	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: V ₊ = 15 V, V ₋ = -15 V, GND = 0 V WR = 0 V, RS = 2.4 V	LIMITS		UNIT
				MIN ¹	MAX	
SWITCH	Drain-Source ON Resistance	r _{DS(on)}	V _{AL} = 0.8 V, V _{AH} = 2.4 V, I _S = -200 μA	V _D = 10 V V _D = -10 V	400 400	Ω
	Source OFF Leakage Current	I _{S(off)}	V _{EN} = 0	V _S = 10 V, V _D = -10 V V _S = -10 V, V _D = 10 V	100 -100	nA
	Drain OFF Leakage Current	I _{D(off)}		V _D = 10 V, V _S = -10 V V _D = -10 V, V _S = 10 V	100 -100	
	Drain ON Leakage Current	I _{D(on)}	V _{AL} = 0 V, V _{AH} = 2.4 V	V _{S(all)} = V _D = 10 V V _{S(all)} = V _D = -10 V	100 -100	μA
	Address Input Current Input Voltage High	I _{AH}	V _A = 2.4 V	-10	10	
INPUT	Address Input Current Input Voltage Low	I _{AL}	V _A = 15 V	-10	10	
	Positive Supply Current	I ₊	All V _A = 0 V, V _{EN} = 0 V, RS = 0 V		3	mA
	Negative Supply Current	I ₋		-2		

NOTES:

1. The algebraic convention whereby the most negative value is a minimum, and the most positive value is a maximum, is used in this data sheet.

DG528



PAD NO.	FUNCTION
1	$\overline{WR}$
2	Address 0
3	Enable
4	V-
5	Source 1
6	Source 2
7	Source 3
8	Source 4
9	Drain
10	Source 8
11	Source 7
12	Source 6
13	Source 5
14	V+
15	Ground
16	Address 2
17	Address 1
18	$\overline{RS}$

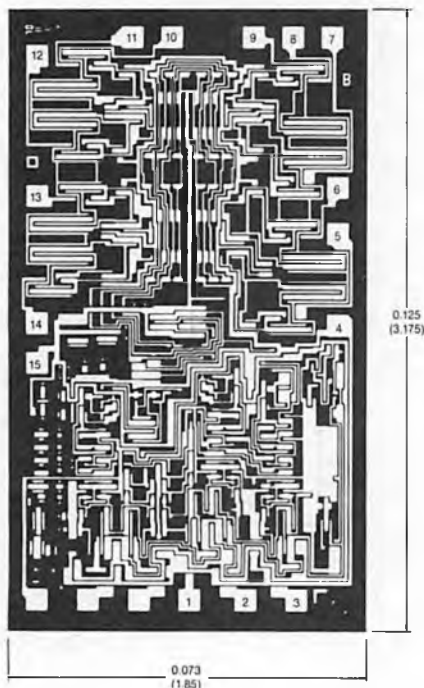
DC ELECTRICAL CHARACTERISTICS

$T_A = 25^\circ\text{C}$

	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: $V_T = 15\text{ V}$, $V_- = -15\text{ V}$, $GND = 0\text{ V}$ $\overline{WR} = 0\text{ V}$, $\overline{RS} = 2.4\text{ V}$	LIMITS		UNIT
				MIN ¹	MAX	
SWITCH	Drain-Source ON Resistance	$r_{DS(on)}$	$V_{AL} = 0.8\text{ V}$, $V_{AH} = 2.4\text{ V}$, $I_S = -200\text{ }\mu\text{A}$	$V_D = 10\text{ V}$ $V_D = -10\text{ V}$	450 450	Ω
	Source OFF Leakage Current	$I_{S(off)}$	$V_{EN} = 0$	$V_S = 10\text{ V}$, $V_D = -10\text{ V}$ $V_S = -10\text{ V}$, $V_D = 10\text{ V}$	0.12 -0.12	μA
	Drain OFF Leakage Current	$I_{D(off)}$		$V_D = 10\text{ V}$, $V_S = -10\text{ V}$ $V_D = -10\text{ V}$, $V_S = 10\text{ V}$	0.12 -0.12	
	Drain ON Leakage Current	$I_{D(on)}$		$V_{AL} = 0\text{ V}$, $V_{AH} = 2.4\text{ V}$ $V_{S(all)} = V_D = 10\text{ V}$ $V_{S(all)} = V_D = -10\text{ V}$	0.12 -0.12	
	Address Input Current Input Voltage High	I_{AH}		$V_A = 2.4\text{ V}$ $V_A = 15\text{ V}$	-12 12	mA
INPUT	Address Input Current Input Voltage Low	I_{AL}	$\text{ALL } V_A = 0\text{ V}$, $V_{EN} = 0\text{ V}$, $\overline{RS} = 0\text{ V}$		-12	
	Positive Supply Current	I^+	$\text{ALL } V_A = 0\text{ V}$, $V_{EN} = 0\text{ V}$, $\overline{RS} = 0\text{ V}$		2.25	
	Negative Supply Current	I^-	$\text{ALL } V_A = 0\text{ V}$, $V_{EN} = 0\text{ V}$, $\overline{RS} = 0\text{ V}$			

NOTES:

1. The algebraic convention whereby the most negative value is a minimum, and the most positive is a maximum, is used in this data sheet.



PAD NO.	FUNCTION
1	WR
2	A ₀
3	EN
4	V-
5	S _{1a}
6	S _{2a}
7	S _{3a}
8	S _{4a}
9	D _a
10	D _b
11	S _{4b}
12	S _{3b}
13	S _{2b}
14	S _{1b}
15	V+
16	GND
17	A ₁
18	$\overline{RS}$

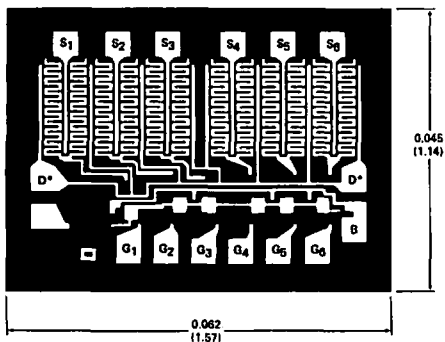
DC ELECTRICAL CHARACTERISTICS

T_A = 25°C

	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: V ₊ = 15 V, V ₋ = -15 V, GND = 0 V, WR = 0 V, $\overline{RS}$ = 2.4 V	LIMITS		UNIT
				MIN ¹	MAX	
SWITCH	Drain-Source ON Resistance	r _{DS(on)}	V _{AL} = 0.8 V, V _{AH} = 2.4 V, I _S = -200 μ A	V _D = 10 V V _D = -10 V	450 450	Ω
	Source OFF Leakage Current	I _{S(off)}	V _{EN} = 0 V	V _S = 10 V, V _D = -10 V	0.12	μ A
	Drain OFF Leakage Current	I _{D(off)}		V _S = -10 V, V _D = 10 V	-0.12	
	Drain ON Leakage Current	I _{D(on)}		V _D = 10 V, V _S = -10 V V _D = -10 V, V _S = 10 V	0.12 -0.12	
INPUT	Address Input Current	I _{AH}	V _{AL} = 0 V, V _{AH} = 2.4 V	V _{S(all)} = V _D = 10 V V _{S(all)} = V _D = -10 V	0.12 -0.12	μ A
	Input Voltage High		V _A = 2.4 V V _A = 15 V	-12 12		
	Address Input Current	I _{AL}	ALL V _A = 0 V, V _{EN} = 0 V, $\overline{RS}$ = 0 V	-12		mA
	Positive Supply Current	I ₊	All V _A = 0 V, V _{EN} = 0 V, $\overline{RS}$ = 0 V		2.25	
	Negative Supply Current	I ₋	All V _A = 0 V, V _{EN} = 0 V, $\overline{RS}$ = 0 V	-135		

NOTES:

1. The algebraic convention whereby the most negative value is a minimum, and the most positive value is a maximum, is used in this data sheet.



PAD DESIGNATION	FUNCTION
†G ₁	Gate 1
†G ₂	Gate 2
†G ₃	Gate 3
†G ₄	Gate 4
†G ₅	Gate 5
†G ₆	Gate 6
B	Body (Substrate V ₊)
D	Drain
S ₆	Source 6
S ₅	Source 5
S ₄	Source 4
S ₃	Source 3
S ₂	Source 2
S ₁	Source 1

†Any unused gates should be connected to the substrate V₊; unused sources can be left open.

* Both "D" pads are electrically common. Either can be used for drain contact.

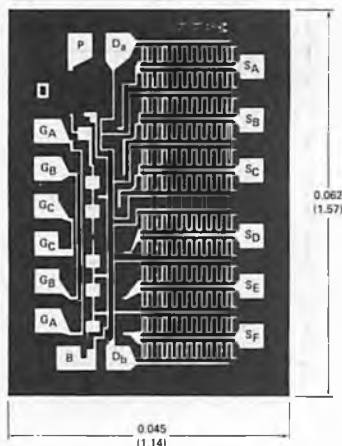
DC ELECTRICAL CHARACTERISTICS

T_A = 25°C

	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: V _{DB} = 0 V, V _{PB} = 0 V	LIMITS		UNIT
				MIN ¹	MAX	
SWITCH	Drain-Source ON Resistance	r _{DS(on)}	I _S = -1 mA V _{GD} = -30 V V _{DB} = -20 V, V _{GD} = -10 V		125 500	Ω
	Drain ON Leakage Current	I _{D(on)}	V _{DS} = -30 V, V _{GS} = 0 V, V _{SB} = 0 V		1.2	μA
	Gate ON Current	I _{G(on)}	V _{GB} = -30 V, V _{PB} = -30 V	-2.5		mA
	Gate-Source Threshold Voltage	V _{GS(th)}	V _{DG} = 0 V, V _{SG} = 0 V, I _D = -10 μA	-4	-1.5	V
	Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} = 0 V, V _{SB} = 0 V, I _D = -100 μA	-30		
	Source-Drain Breakdown Voltage	BV _{SDS}	V _{GD} = 0 V, I _S = -10 μA	-30		
	Gate-Source Maximum Voltage	BV _{GSS}	V _{GS} = 0 V, V _{SB} = 0 V, I _G = -10 μA	-35		

NOTES:

- The algebraic convention whereby the most negative value is a minimum, and the most positive value is a maximum, is used in this data sheet.



PAD DESIGNATION	FUNCTION
G _A	Gate 1
G _B	Gate 3
G _C	Gate 5
B	Body (Substrate V ₊)
D _b	Drain 2
S _F	Source 2
S _E	Source 4
S _D	Source 6
S _C	Source 5
S _B	Source 3
S _A	Source 1
D _a	Drain 1
P	Pull Up Gate Input

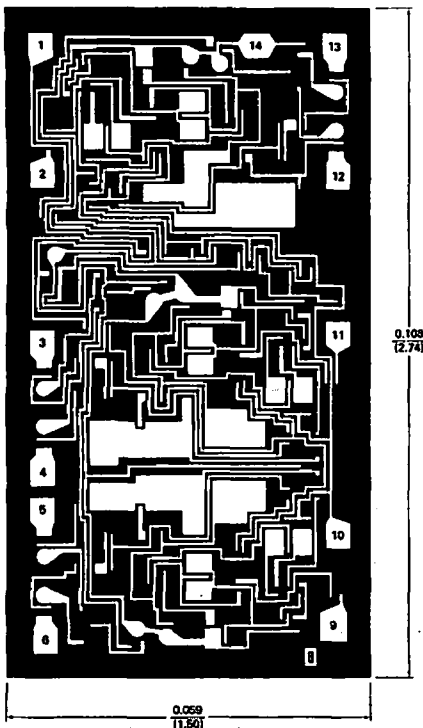
DC ELECTRICAL CHARACTERISTICS

T_A = 25°C

	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: V _{DB} = 0 V, V _{PB} = 0 V	LIMITS		UNIT
				MIN ¹	MAX	
SWITCH	Drain-Source ON Resistance	r _{DS(on)}	I _S = -1 mA V _{GD} = -30 V V _{DB} = -20 V, V _{GD} = -10 V		125 500	Ω
	Drain ON Leakage Current	I _{D(on)}	V _{DS} = -30 V, V _{GS} = 0 V, V _{SB} = 0 V		1.2	μA
	Gate ON Current	I _{G(on)}	V _{GB} = -30 V, V _{PB} = -30 V	-2.4	-0.4	mA
	Gate-Source Threshold Voltage	V _{GS(th)}	V _{DG} = 0 V, V _{SG} = 0 V, I _D = -10 μA	-4	-1.5	V
	Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} = 0 V, V _{SB} = 0 V, I _D = -100 μA	-30		
	Source-Drain Breakdown Voltage	BV _{SDS}	V _{GD} = 0 V, I _S = -10 μA	-30		

NOTES:

1. The algebraic convention whereby the most negative value is a minimum, and the most positive value is a maximum, is used in this data sheet.



PAD NO.	FUNCTION
1	SET
2	OUT 1
3	-IN2
4	+IN2
5	+IN3
6	-IN3
9	OUT3
10	-V _S *
11	OUT2
12	+IN1
13	-IN1
14	+V _S

* Substrate = -V_S

ELECTRICAL CHARACTERISTICS

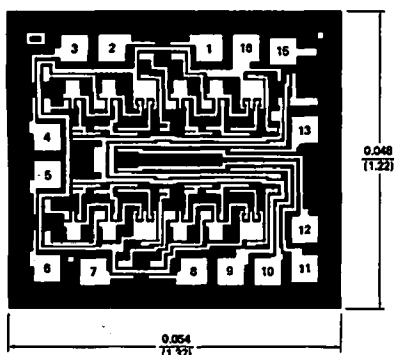
T_A = 25°C

	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: ¹ +V _S = 15 V, -V _S = -15 V, R _{SET} = 3 MΩ R _L = 50 kΩ	LIMITS		UNIT
				MIN ²	MAX	
INPUT	Input Offset Voltage	V _{OS}	R _S ≤ 50 kΩ		10	mV
	Input Offset Current	I _{OS}			70	nA
	Input Bias Current	I _{BIAS}		-250		
OUTPUT	Output Voltage Swing	V _{OUT}		-10	10	V
	DC Open Loop Voltage Gain	A _{VOL}		1.0		V/mV
	Common Mode Rejection Ratio	CMRR	V _{in} = ±12 V	70		dB
SUPPLY	Power Supply Rejection Ratio	PSRR		80		
	Source Current	I _S	Unity Gain, V _{in+} = 0 On all amps		400	μA

NOTES:

1. I_{SET} is adjustable. See AN73-6 for more detailed information.
2. The algebraic convention whereby the most negative value is a minimum, and the most positive value is a maximum, is used in this data sheet.

L161



PAD NO.	FUNCTION
1	+IN ₁
2	-IN ₁
3	+IN ₂
4	-IN ₂
5	-IN ₃
6	+IN ₃
7	-IN ₄
8	+IN ₄
9	-V [*]
10	OUT ₄
11	OUT ₃
12	OUT ₂
13	OUT ₁
15	I _{SET}
16	+V

* Substrate = -V

LOW POWER ELECTRICAL CHARACTERISTICS

T_A = 25°C

	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: V ⁺ = 3 V, V ⁻ = -3 V, I _{SET} = 10 μA R _L = 10 MΩ, C _L = 10 pF	LIMITS		UNIT
				MIN ¹	MAX	
INPUT	Input Offset Voltage	V _{OS}			6.0	mV
	Input Offset Current	I _{OS}			25	nA
	Input Bias Current, Total	I _{BT}			200	nA
DYN OUTPUT	DC Open Loop Voltage Gain	A _{VOL}		10		V/mV
	Low Output Voltage ²	V _{OL}	R _L = 20 kΩ		-2.6	V
	High Output Voltage ²	V _{OH}	R _L = 200 kΩ	2.5		
SUPPLY	Common Mode Rejection Ratio	CMRR	V _{in} = CMR = 1.3 to -3.0 V	75		dB
	Power Supply Rejection Ratio	PSRR		65		
	Source Current ³	I _S	All Inputs Grounded, R _L = ∞		300	

HIGH POWER ELECTRICAL CHARACTERISTICS

T_A = 25°C

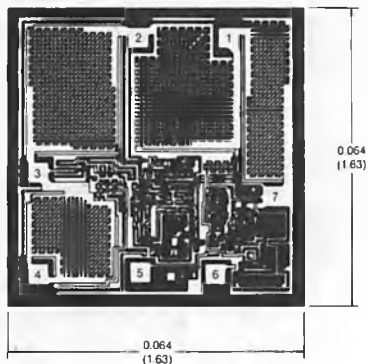
	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: V ⁺ = 15 V, V ⁻ = -15 V, I _{SET} = 10 μA R _L = 10 MΩ, C _L = 10 pF	LIMITS		UNIT
				MIN ¹	MAX	
INPUT	Input Offset Voltage	V _{OS}			6.0	mV
	Input Offset Current	I _{OS}			90	nA
	Input Bias Current, Total	I _{BT}			600	nA
DYN OUTPUT	DC Open Loop Voltage Gain	A _{VOL}		30		V/mV
	Low Output Voltage ²	V _{OL}	R _L = 20 kΩ		-14.6	V
	High Output Voltage ²	V _{OH}	R _L = 200 kΩ	14.5		
SUPPLY	Common Mode Rejection Ratio	CMRR	V _{in} = CMR = 5 to -15 V	75		dB
	Power Supply Rejection Ratio	PSRR		65		
	Source Current ³	I _S	All Inputs Grounded, R _L = ∞		3500	

NOTES:

- The algebraic convention whereby the most negative value is a minimum, and the most positive value is a maximum, is used in this data sheet.
- The output current drive of the L161 is non-symmetrical. This facilitates the wire-ORing of two comparator outputs. The output pull-down current capability is typically 75-150 times the pull-up current.
- Set current (I_{SET}) and supply current (I_S) can be determined by the following formulas:

$$I_{SET} = \frac{((+V) - (2V_{BE}) - (-V))}{R_{SET}}; I_{SUPPLY} = 21 \times I_{SET}$$

Si7660



PAD NO.	FUNCTION
1	CAP+
2	GND
3	CAP-
4	V _{OUT}
5	LV
6	OSC
7	V+

ELECTRICAL CHARACTERISTICS

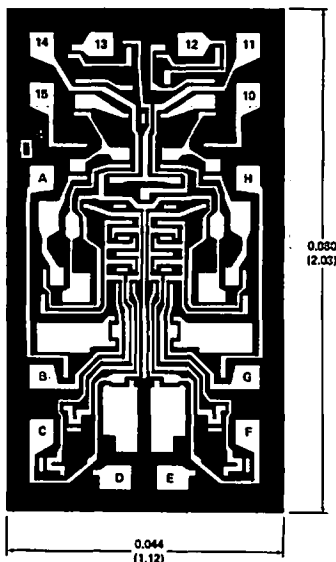
T_A = 25°C

	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED:	LIMITS		UNIT
				MIN ¹	MAX	
INPUT	Supply Voltage Range-Lo (DX Out of Circuit)	V _{+L}	R _L = 10 k Ω , LV = Ground	1.5	3.5	V
	Supply Voltage Range-Lo (DX In Circuit)			1.5	3.5	
	Supply Voltage Range-Hi ² (DX Out of Circuit)	V _{+H}	R _L = 10 k Ω , LV = No Connection	3	6.5	
	Supply Voltage Range-Hi ² (DX In Circuit)			3	10	
	Supply Current	I ₊	R _L = ∞ , LV = Open		500	μ A
OUTPUT	Output Source Resistance	R _{OUT}	LV = Open, I _O = 20 mA		100	Ω
	Power Conversion Efficiency	P _{E1}	R _L = 5 k Ω	95		%
	Voltage Conversion Efficiency	V _{OUT} E1	R _L = ∞	97		

NOTES:

- The algebraic convention whereby the most negative value is a minimum, and the most positive value is a maximum, is used in this data sheet.
- D_X is required for supply voltages greater than 6.5 V @ -55°C $\leq$ T_A $\leq$ 25°C

CMJA1000 — DRIVER CHIP



INTERCHIP PAD CONNECTIONS

A	From JFET 1, Source
B	To JFET 1, Gate
C	To JFET 3, Gate
D	From JFET 3, Source
E	From JFET 4, Source
F	To JFET 4, Gate
G	To JFET 2, Gate
H	From JFET 2, Source

PAD NO. FUNCTION

10	Input 2
11	V+
12	V _L
13	V _R
14	V- (Substrate)
15	(Input 1)

CMJA1000 is used for following devices:

DEVICE	JFET USED	NO. OF JFETs
DG183	NIP1000	4
DG184	NC1000	4
DG185	NC2000	4

DC ELECTRICAL CHARACTERISTICS

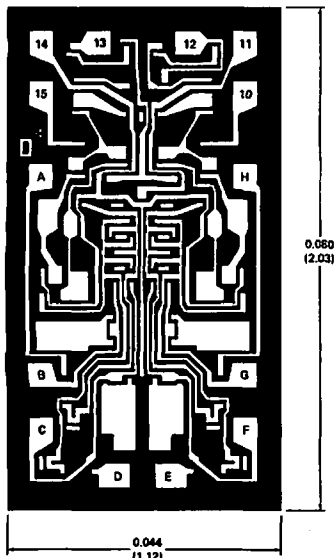
T_A = 25°C

	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: V ₊ = 15 V, V ₋ = -15 V, V _R = 0 V, V _L = 5V	LIMITS		UNIT
				MIN ¹	MAX	
INPUT	Input Current Input Voltage Low	I _{INL}	V _{in} = 0 V	-250		μA
	Input Current Input Voltage High	I _{INH}	V _{in} = 5 V		20	
SUPPLY	Logic Supply Current	I _L	V _{in} = 0 V V _{in} = 5 V		4.5 4.5	mA
	Reference Supply Current	I _R	V _{in} = 0 V V _{in} = 5 V	-2 -2		
	Negative Supply Current	I ₋	V _{in} = 0 V V _{in} = 5 V	-5.5 -4		
	Positive Supply Current	I ₊	V _{in} = 0 V V _{in} = 5 V		3 0.1	

NOTES:

- The algebraic convention whereby the most negative value is a minimum, and the most positive value is a maximum, is used in this data sheet.

CMJB1000 — DRIVER CHIP



INTERCHIP PAD CONNECTIONS	
With 2 JFETs:	
A	No Connection
B	No Connection
C	To JFET 2, Gate
D	From JFET 2, Source
E	From JFET 1, Source
F	To JFET 1, Gate
G	No Connection
H	No Connection
With 4 JFETs:	
A	From JFET 1, Source
B	To JFET 1, Gate
C	To JFET 3, Gate
D	From JFET 3, Source
E	From JFET 4, Source
F	To JFET 4, Gate
G	To JFET 2, Gate
H	From JFET 2, Source

PAD NO.	FUNCTION
10	Input 2
11	V+
12	V _L
13	V _R
14	V- (Substrate)
15	Input 1

CMJB1000 is used for following devices:

DEVICE	JFET USED	NO. OF JFETs
DG180	NIP1000	2
DG181	NC1000	2
DG182	NC2000	2
DG189	NIP1000	4
DG190	NC1000	4
DG191	NC2000	4

DC ELECTRICAL CHARACTERISTICS

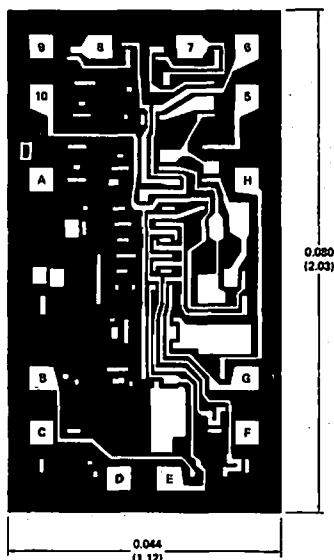
T_A = 25°C

	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: V ₊ = 15 V, V ₋ = -15 V, V _R = 0 V, V _L = 5 V	LIMITS		UNIT
				MIN ¹	MAX	
INPUT	Input Current Input Voltage Low	I _{INL}	V _{in} = 0 V	-250		μA
	Input Current Input Voltage High	I _{INH}	V _{in} = 5 V		20	
SWITCH	Logic Supply Current	I _L	V _{in} = 0 V		4.5	mA
			V _{in} = 5 V		4.5	
	Reference Supply Current	I _R	V _{in} = 0 V	-2		
			V _{in} = 5 V	-2		
	Negative Supply Current	I ₋	V _{in} = 0 V	-5		
			V _{in} = 5 V	-5		
	Positive Supply Current	I ₊	V _{in} = 0 V		1.5	
			V _{in} = 5 V		1.5	

NOTES:

1. The algebraic convention whereby the most negative value is a minimum, and the most positive value is a maximum, is used in this data sheet.

CMJC1000 — DRIVER CHIP



INTERCHIP PAD CONNECTIONS	
A	Not Connected
B	From JFET 2, Source
C	Not Connected
D	Not Connected
E	To JFET 2, Gate
F	Not Connected
G	To JFET 1, Gate
H	From JFET 1, Source

PAD NO.	FUNCTION
5	Input 1
6	V+
7	V _L
8	V _R
9	Not Connected
10	V- (Substrate)

CMJC1000 is used for following devices:

DEVICE	JFET USED	NO. OF JFETs
DG186	NIP1000	2
DG187	NC1000	2
DG188	NC2000	2

DC ELECTRICAL CHARACTERISTICS

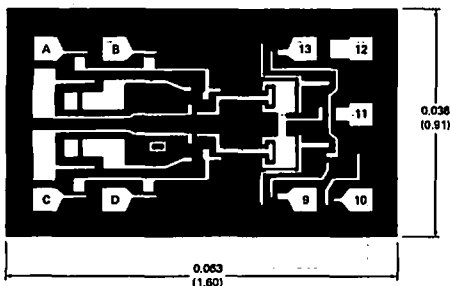
T_A = 25°C

	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: V ₊ = 15 V, V ₋ = -15 V, V _R = 0 V, V _L = 5 V	LIMITS		UNIT
				MIN ¹	MAX	
INPUT	Input Current Input Voltage Low	I _{INL}	V _{IN} = 0 V	-250		μA
	Input Current Input Voltage High	I _{INH}	V _{IN} = 5 V		10	
SUPPLY	Logic Supply Current	I _L	V _{IN} = 0 V		3.2	mA
			V _{IN} = 5 V		3.2	
	Reference Supply Current	I _R	V _{IN} = 0 V	-2		
			V _{IN} = 5 V	-2		
	Negative Supply Current	I ₋	V _{IN} = 0 V	-3		
			V _{IN} = 5 V	-3		
	Positive Supply Current	I ₊	V _{IN} = 0 V		0.8	
			V _{IN} = 5 V		0.8	

NOTES:

1. The algebraic convention whereby the most negative value is a minimum, and the most positive value is a maximum, is used in this data sheet.

LODC1000 — DRIVER CHIP



INTERCHIP CONNECTIONS	
With 2 JFETs:	
A	To Gate 2
B	No Connection
C	To Gate 1
D	No Connection
With 4 JFETs:	
A	To Gate 4
B	To Gate 2
C	To Gate 3
D	To Gate 1

PAD NO.	FUNCTION
9	Input 1
10	V_R
11	V_+
12	V_- (Substrate)
13	Input 2

LODC1000 is used for following devices:

DEVICE	JFET USED	NO. OF JFETs
DG126	NC2000	4
DG129	NC1000	4
DG133	NC1000	2
DG134	NC2000	2
DG140	NIP1000	4
DG141	NIP1000	2

DC ELECTRICAL CHARACTERISTICS^{1, 2}

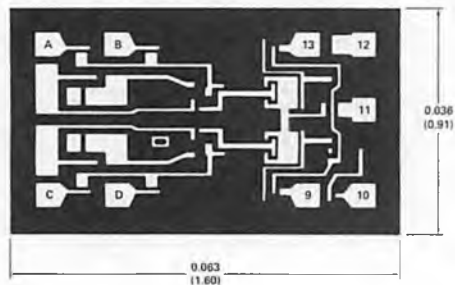
$T_A = 25^\circ\text{C}$

	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: $V_+ = 12\text{ V}$, $V_- = -18\text{ V}$, $V_R = 0\text{ V}$	LIMITS		UNIT
				MIN ³	MAX	
INPUT	Input Current Input Voltage Low	I_{INL}	$V_{in} = 0.8\text{ V}$		0.1	μA
	Input Current Input Voltage High	I_{INH}	$V_{in} = 2.5\text{ V}$		100	
SUPPLY	Positive Supply Current	I_+	$V_{in} = 2.5\text{ V}$, One Channel ON		3.3	mA
	Negative Supply Current	I_-		-2.0		
	Reference Supply Current	I_R		-1.5		
	Positive Supply Current	I_+	Both $V_{in} = 0\text{ V}$, All Channels OFF		25	μA
	Negative Supply Current	I_-		-25		
	Reference Supply Current	I_R		-25		

NOTES:

- V_{in} must be a step function with a minimum rise and fall rate of $1\text{ V}/\mu\text{S}$.
- The supply voltage condition of $+12\text{ V}/-18\text{ V}$ is standard test condition. Specs will also be met with $+15\text{ V}/-15\text{ V}$ supplies, but are not tested.
- The algebraic convention whereby the most negative value is a minimum, and the most positive value is a maximum, is used in this data sheet.

LODF1000 — DRIVER CHIP



INTERCHIP CONNECTIONS	
With 2 JFETs:	
A	To Gate 2
B	No Connection
C	To Gate 1
D	No Connection
With 4 JFETs:	
A	To Gate 4
B	To Gate 2
C	To Gate 3
D	To Gate 1

PAD NO.	FUNCTION
9	Input 1
10	V_R
11	V_+
12	V_- (Substrate)
13	Input 2

LODF1000 is used for following devices:

DEVICE	JFET USED	NO. OF JFETs
DG139	NC1000	4
DG142	NC2000	4
DG143	NC2000	2
DG144	NC1000	2
DG145	NIP1000	4
DG146	NIP1000	2

DC ELECTRICAL CHARACTERISTICS^{1, 2}

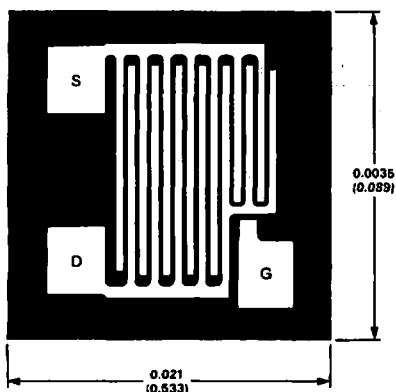
$T_A = 25^\circ\text{C}$

	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: $V_+ = 12\text{ V}$, $V_- = -18\text{ V}$, $V_R = 0\text{ V}$, $V_{in1} = 2.5\text{ V}$	LIMITS		UNIT
				MIN ³	MAX	
INPUT	Input Current	I_{INL1}	$V_{in1} = 2\text{ V}$, $V_{in2} = 2.5\text{ V}$		0.1	μA
	Input Voltage Low	I_{INL2}	$V_{in1} = 2.5\text{ V}$, $V_{in2} = 2\text{ V}$		0.1	
	Input Current	I_{INH1}	$V_{in1} = 3\text{ V}$, $V_{in2} = 2.5\text{ V}$		100	
	Input Voltage High	I_{INH2}	$V_{in1} = 2.5\text{ V}$, $V_{in2} = 3\text{ V}$		100	
SUPPLY	Positive Supply Current	I_+	$V_{in1} = 2\text{ V}$ or $V_{in1} = 3\text{ V}$, One Channel ON		4.5	mA
	Negative Supply Current	I_-		-2.2		
	Reference Supply Current	I_R		-2.4		
	Positive Supply Current	I_+	$V_{in1} = V_{in2} = 0.8\text{ V}$, All Channels OFF		25	μA
	Negative Supply Current	I_-		-25		
	Reference Supply Current	I_R		-25		

NOTES:

- V_{in} must be a step function with a minimum rise and fall rate of $1\text{ V}/\mu\text{S}$.
- The supply voltage condition of $+12\text{ V}/-18\text{ V}$ is standard test condition. Specs will also be met with $+15\text{ V}/-15\text{ V}$ supplies, but are not tested.
- The algebraic convention whereby the most negative value is a minimum, and the most positive value is a maximum, is used in this data sheet.

NC1000/NC2000 JFET Switches



INTERCHIP CONNECTIONS	FUNCTION
S	Source
D	Drain
G	Gate*

*Gate is also on backside of chip.

DC ELECTRICAL CHARACTERISTICS

$T_A = 25^\circ\text{C}$

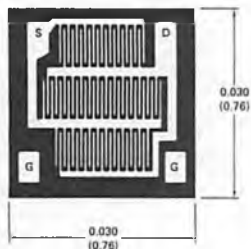
PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED:	LIMITS				UNIT
			NC1000		NC2000		
			MIN ¹	MAX	MIN ¹	MAX	
Gate-Drain Breakdown Voltage	BV _{GDS}	I _G = -1 μA	-35		-35		V
Drain Cut Off Current	I _{D(off)}	V _{DS} = 22 V, V _{GS} = -6.2 V, NC1000 V _{GS} = -3.9 V, NC2000		1.0		1.0	nA
Source Cut Off Current	I _{S(off)}			1.0		1.0	
Drain-Source ON Resistance	r _{DS(on)}	V _{GS} = 0 V, V _{DS} = 0.2 V		30		75	Ω

NOTES:

- The algebraic convention whereby the most negative value is a minimum, and the most positive value is a maximum, is used in this data sheet.

NIP1000 JFET Switch

BOTH GATE PADS ARE COMMON



INTERCHIP PAD CONNECTIONS	FUNCTION
S	Source
D	Drain
G	Gate*

* Gate is also on backside of chip

DC ELECTRICAL CHARACTERISTICS

$T_A = 25^\circ\text{C}$

PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED:	LIMITS		UNIT
			MIN ¹	MAX	
Gate-Drain Breakdown Voltage	BV_{GDS}	$I_G = -1 \mu\text{A}$, $V_{DS} = 0$	-33		V
Drain Cut Off Current	$I_{D(off)}$	$V_{GS} = -6.2 \text{ V}$, $V_{DS} = 22 \text{ V}$		10	nA
Source Cut Off Current	$I_{S(off)}$			10	
Drain-Source ON Resistance	$r_{DS(on)}$	$V_{GS} = 0 \text{ V}$, $V_{DS} = 0.2 \text{ V}$		10	Ω

NOTES:

1. The algebraic convention whereby the most negative value is a minimum, and the most positive a maximum, is used in this data sheet.

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PACKAGE DATA

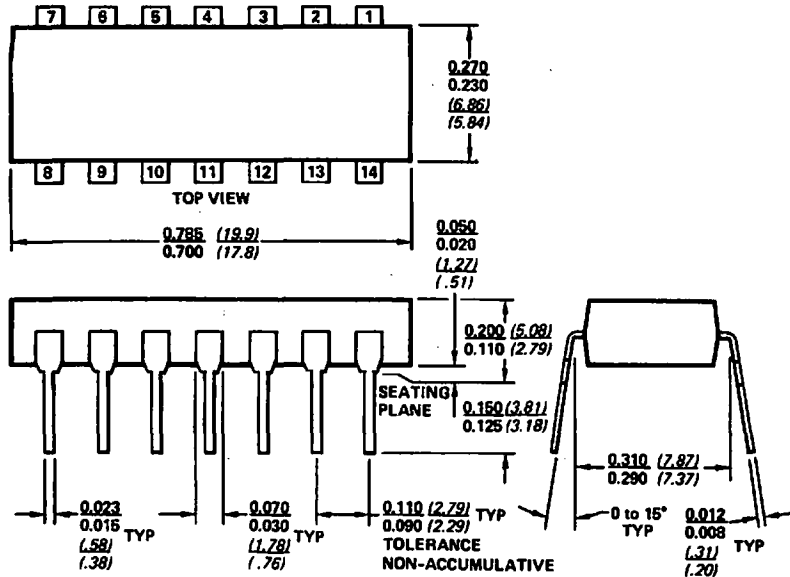
Package	Letter Code	Package Type	Page
2	A	10 Lead Metal Can (TO-100)	9-3
5	L	14 Lead Bottom-Braze Flatpack	9-3
7	J	14 Pin Plastic Dual-In-Line	9-4
8	J	16 Pin Plastic Dual-In-Line	9-4
9	K	14 Pin Ceramic Dual-In-Line	9-5
10	K	16 Pin Ceramic Dual-In-Line	9-5
11	P	14 Pin Side-Braze Dual-In-Line	9-6
12	P	16 Pin Side-Braze Dual-In-Line	9-6
13	R	28 Pin Side-Braze Dual-In-Line	9-7
14	J	28 Pin Plastic Dual-In-Line	9-7
16	L	14 Lead Bottom-Braze Flatpack	9-8
17	L	16 Lead Bottom-Braze Flatpack	9-8
19	J	18 Pin Plastic Dual-In-Line	9-9
20	P	18 Pin Side-Braze Dual-In-Line	9-9
22	J	40 Pin Plastic Dual-In-Line	9-10
23	K	18 Pin Ceramic Dual-In-Line	9-10
24	K	28 Pin Ceramic Dual-In-Line	9-11
25	J	8 Pin Plastic Dual-In-Line	9-11
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27	J	24 Pin Plastic Dual-In-Line	9-12
28	K	24 Pin Ceramic Dual-In-Line	9-13
29	Y	8 Pin Plastic SO	9-13
30	Y	14 Pin Plastic SO	9-14
31	Y	16 Pin Plastic SO	9-14



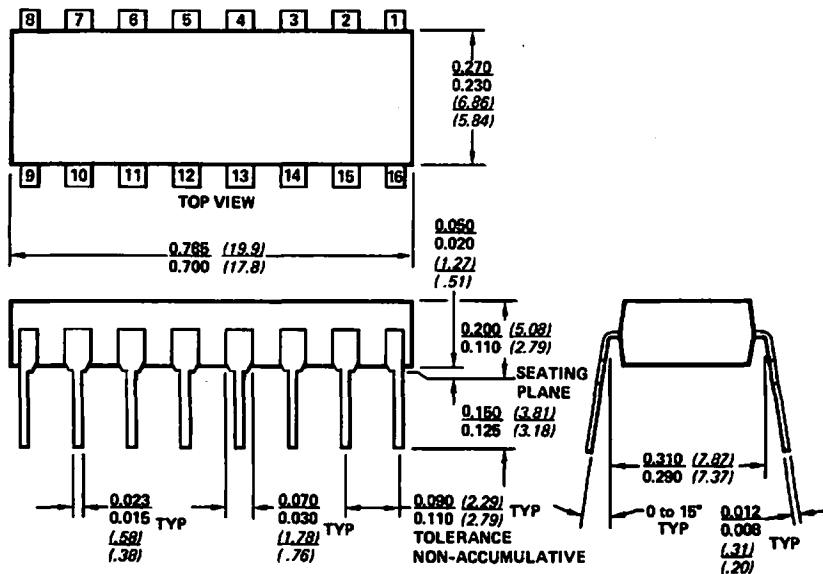
BOTTOM VIEW



ALL DIMENSIONS IN INCHES
(ALL DIMENSIONS IN MILLIMETERS)



PACKAGE 7
14 LEAD DUAL IN LINE PACKAGE (J)
(PLASTIC)

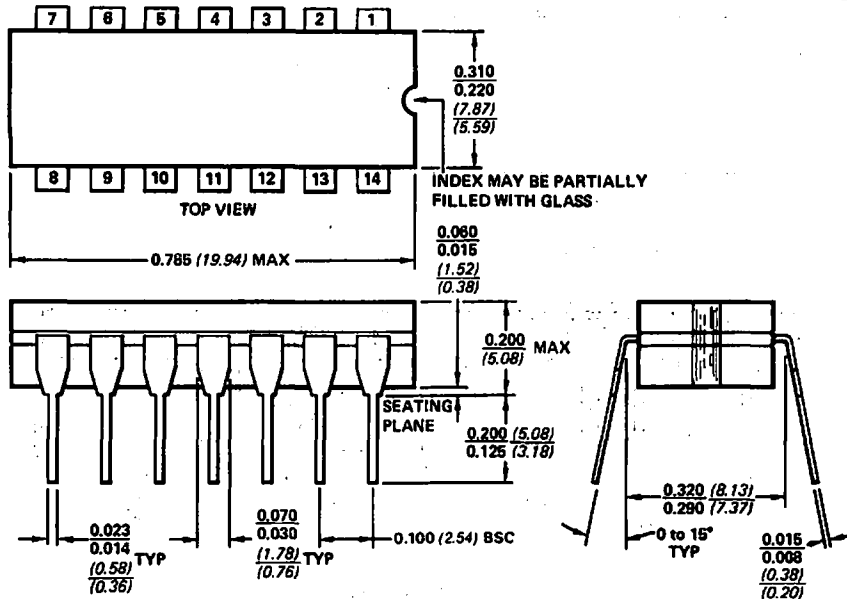


PACKAGE 8
16 LEAD DUAL IN LINE PACKAGE (J)
(PLASTIC)

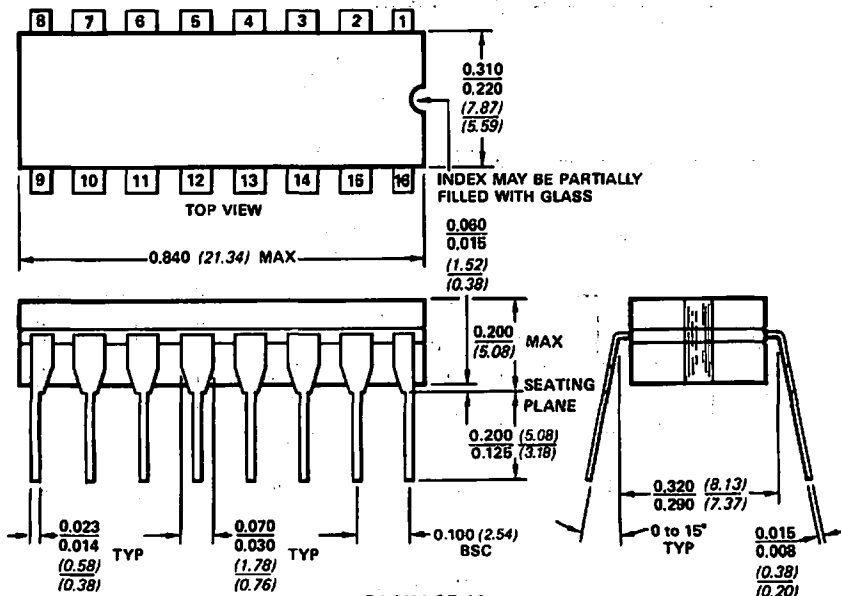
NOTES: PIN 1 INDEX IS ONE OR MORE OF THE FOLLOWING

- DOT (INK OR IMPRESSION) ON TOP OF PACKAGE
- NOTCH OR HOLE IN PIN 1 VISIBLE FROM TOP AND/OR SIDE
- NOTCH IN END OF PACKAGE VISIBLE FROM TOP AND/OR BOTTOM

ALL DIMENSIONS IN INCHES
(ALL DIMENSIONS IN MILLIMETERS)



PACKAGE 9
14 LEAD DUAL IN LINE PACKAGE (K)
(CERDIP)

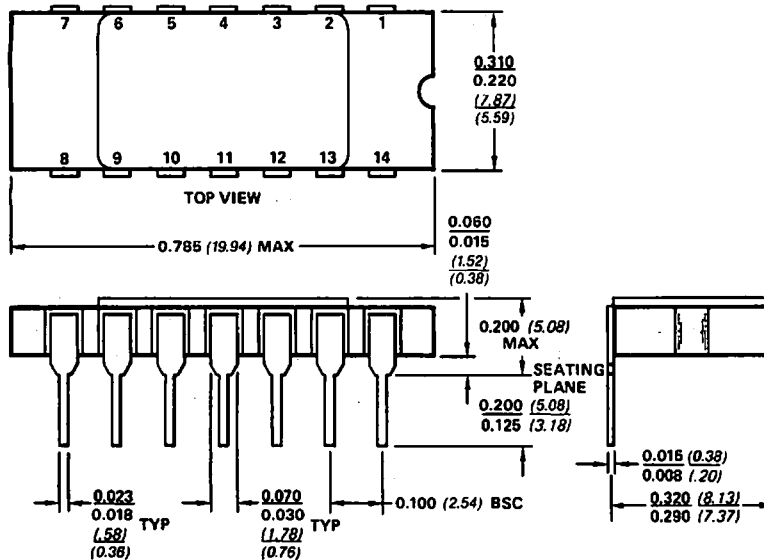


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16 LEAD DUAL IN LINE PACKAGE (K)
(CERDIP)

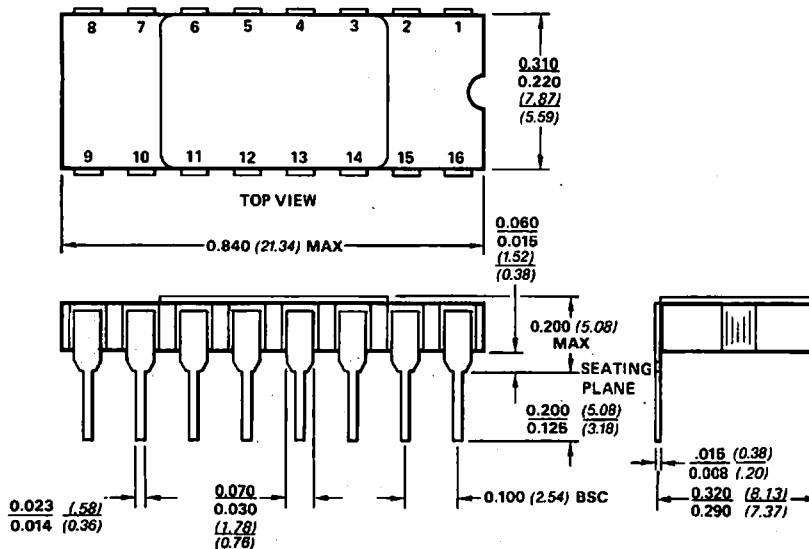
NOTES: PIN 1 INDEX IS ONE OR MORE OF THE FOLLOWING

- DOT (INK OR IMPRESSION) ON TOP OF PACKAGE
- NOTCH OR HOLE IN PIN 1 VISIBLE FROM TOP AND/OR SIDE
- NOTCH IN END OF PACKAGE VISIBLE FROM TOP AND/OR BOTTOM

ALL DIMENSIONS IN INCHES
(ALL DIMENSIONS IN MILLIMETERS)

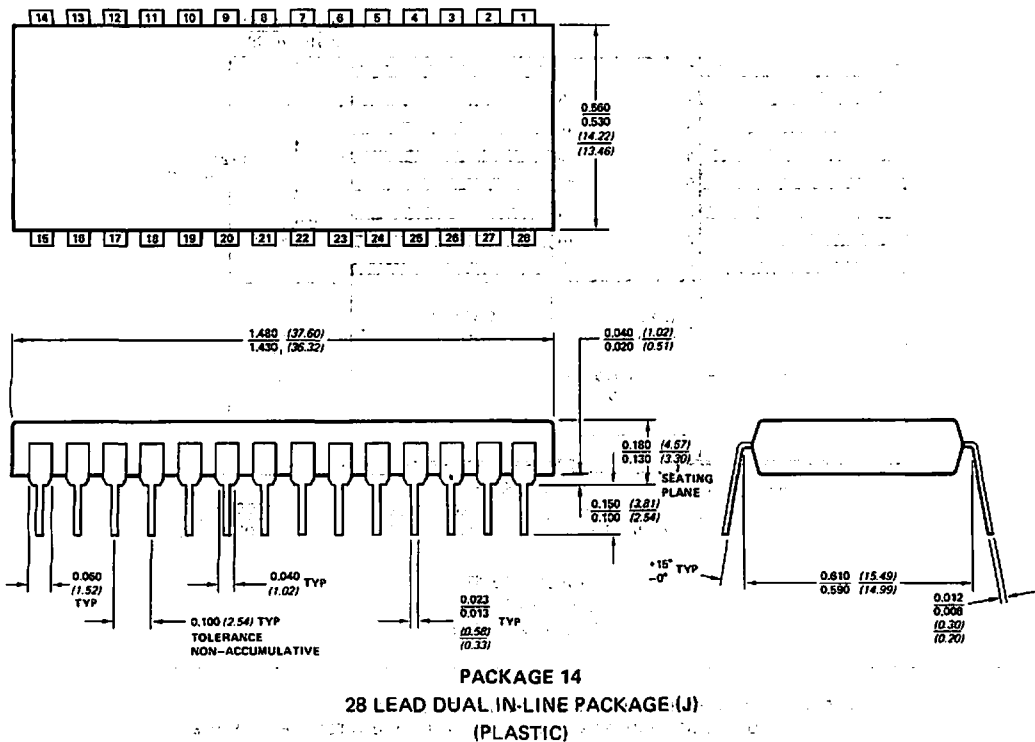
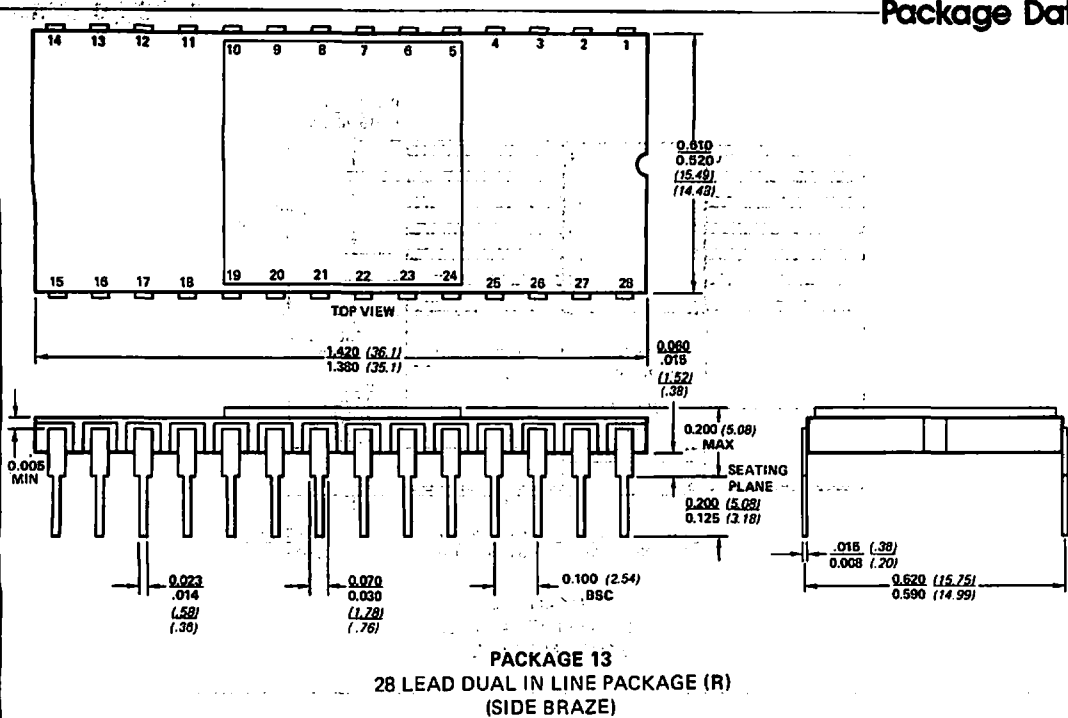


PACKAGE 11
14 LEAD DUAL IN LINE PACKAGE (P)
(SIDE BRAZE)



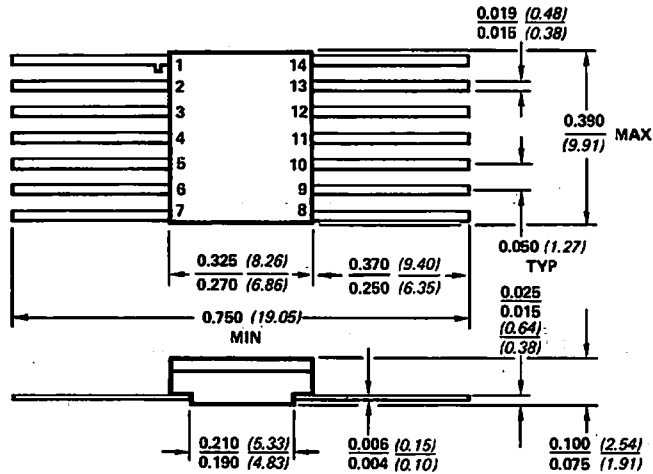
PACKAGE 12
16 LEAD DUAL IN LINE PACKAGE (P)
(SIDE BRAZE)

- NOTES: PIN 1 INDEX IS ONE OR MORE OF THE FOLLOWING
- DOT (INK OR IMPRESSION) ON TOP OF PACKAGE
 - NOTCH OR HOLE IN PIN 1 VISIBLE FROM TOP AND/OR SIDE
 - NOTCH IN END OF PACKAGE VISIBLE FROM TOP AND/OR BOTTOM
- ALL DIMENSIONS IN INCHES
(ALL DIMENSIONS IN MILLIMETERS)

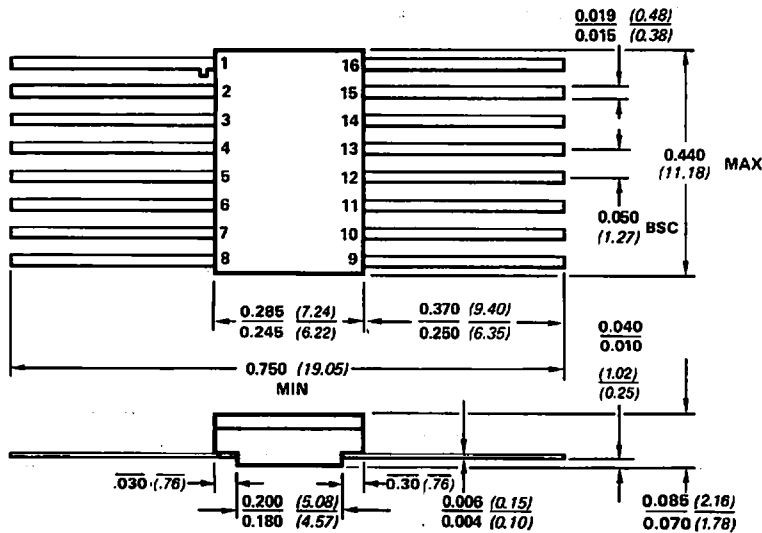


NOTES: PIN 1 INDEX IS ONE OR MORE OF THE FOLLOWING

- DOT (INK OR IMPRESSION) ON TOP AND/OR BOTTOM OF PACKAGE
- NOTCH OR HOLE IN PIN 1 VISIBLE FROM TOP AND/OR SIDE
- NOTCH IN END OF PACKAGE VISIBLE FROM TOP AND/OR BOTTOM



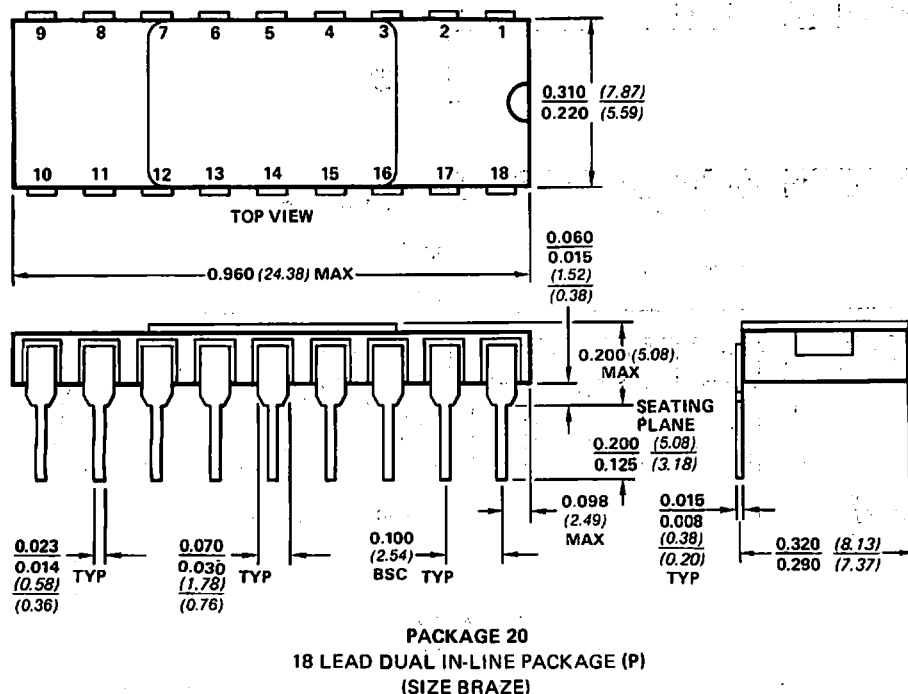
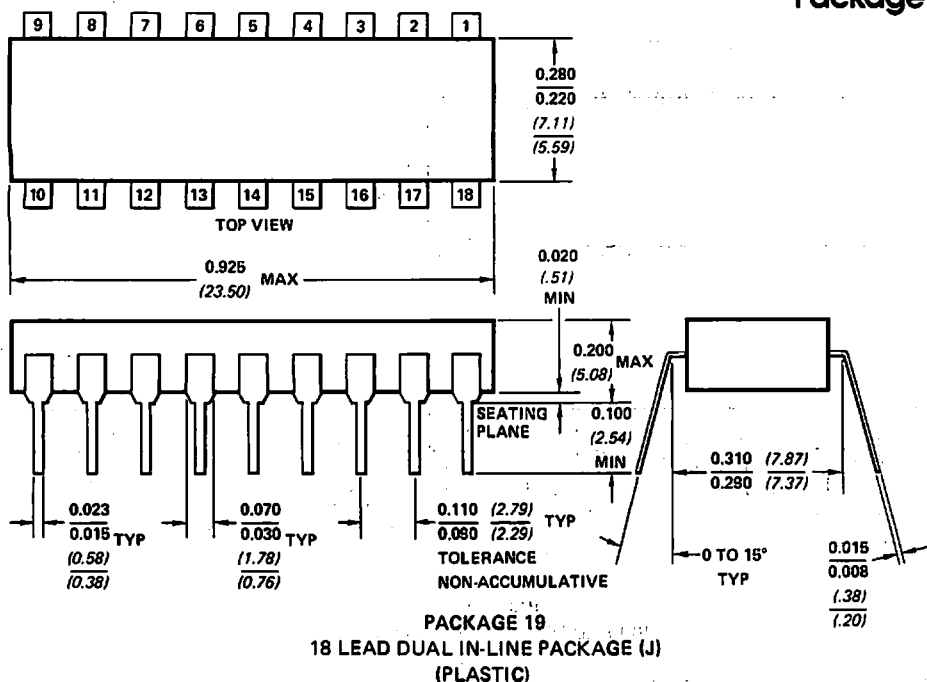
PACKAGE 16
14 LEAD FLATPACK (L)
(BOTTOM BRAZE)



PACKAGE 17
16 LEAD FLATPACK (L)
(BOTTOM BRAZE)

- NOTES:** PIN 1 INDEX IS ONE OR MORE OF THE FOLLOWING
- DOT (INK OR IMPRESSION) ON TOP AND/OR BOTTOM OF PACKAGE
 - NOTCH OR HOLE IN PIN 1 VISIBLE FROM TOP AND/OR SIDE
 - NOTCH IN END OF PACKAGE VISIBLE FROM TOP AND/OR BOTTOM

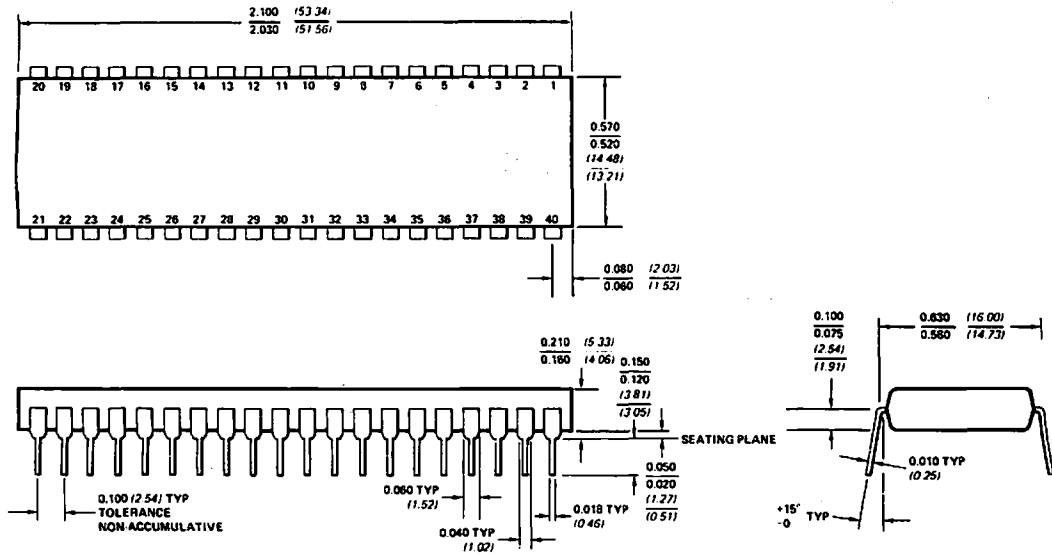
ALL DIMENSIONS IN INCHES
(ALL DIMENSIONS IN MILLIMETERS)



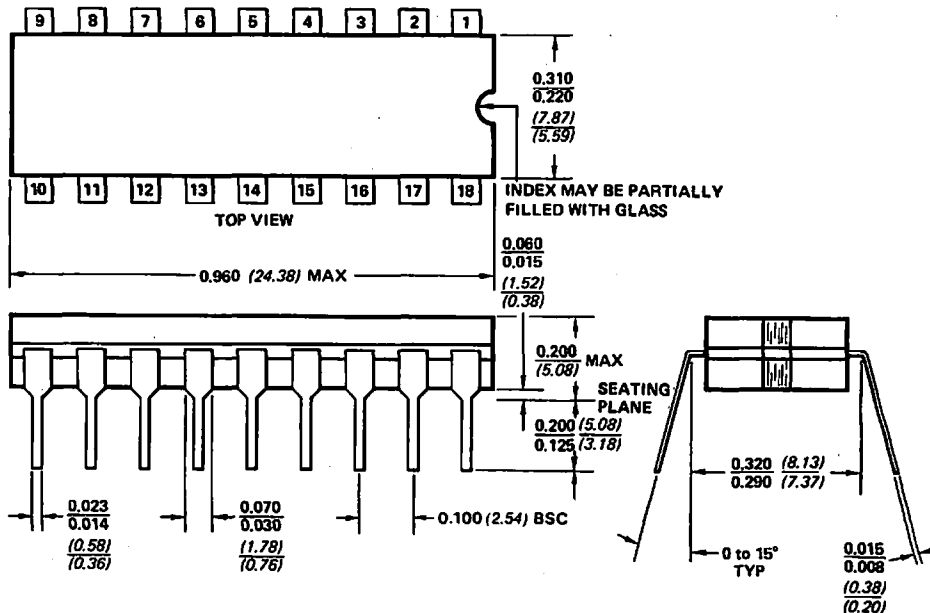
NOTES: PIN 1 INDEX IS ONE OR MORE OF THE FOLLOWING

- DOT (INK OR IMPRESSION) ON TOP AND/OR BOTTOM OF PACKAGE
- NOTCH OR HOLE IN PIN 1 VISIBLE FROM TOP AND/OR SIDE
- NOTCH IN END OF PACKAGE VISIBLE FROM TOP AND/OR BOTTOM

ALL DIMENSIONS IN INCHES
(ALL DIMENSIONS IN MILLIMETERS)



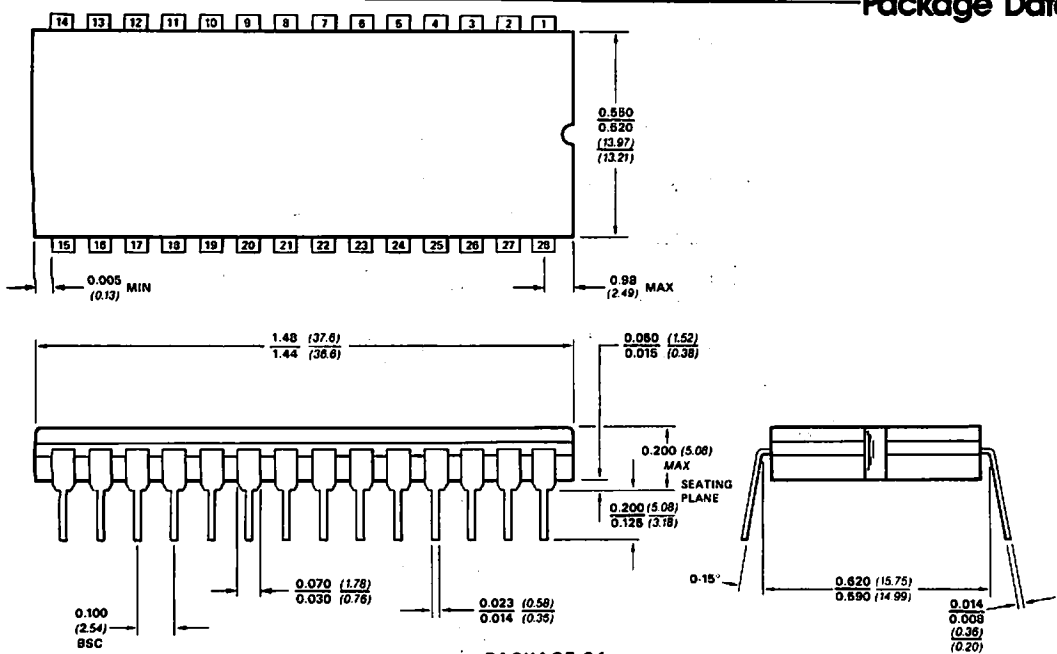
PACKAGE 22
40 LEAD DUAL IN-LINE PACKAGE (J)
(PLASTIC)



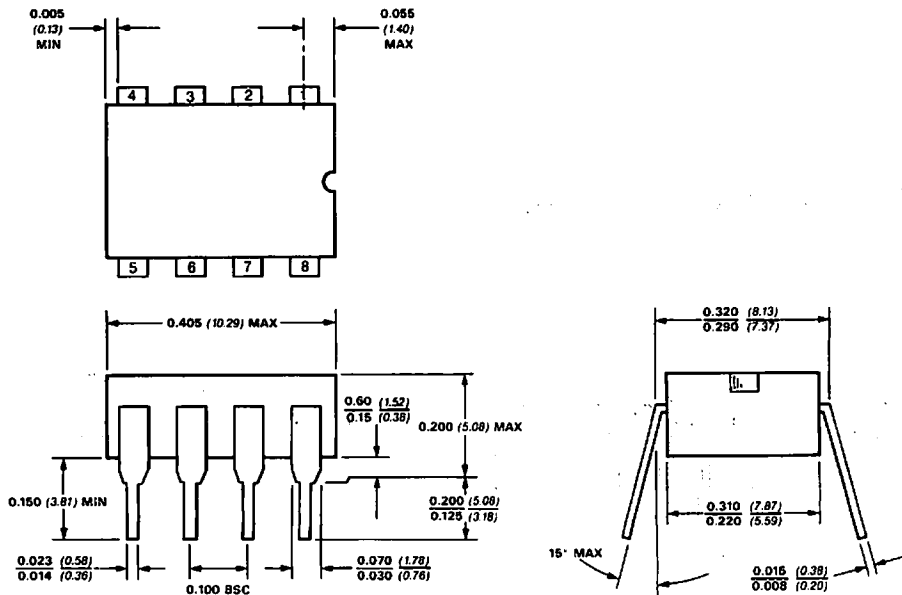
PACKAGE 23
18 LEAD DUAL IN-LINE PACKAGE (K)
(CERDIP)

- NOTES: PIN 1 INDEX IS ONE OR MORE OF THE FOLLOWING
- DOT (INK OR IMPRESSION) ON TOP AND/OR BOTTOM OF PACKAGE
 - NOTCH OR HOLE IN PIN 1 VISIBLE FROM TOP AND/OR SIDE
 - NOTCH IN END OF PACKAGE VISIBLE FROM TOP AND/OR BOTTOM

ALL DIMENSIONS IN INCHES
(ALL DIMENSIONS IN MILLIMETERS)



PACKAGE 24
28 LEAD DUAL IN-LINE PACKAGE (K)
(CERDIP)

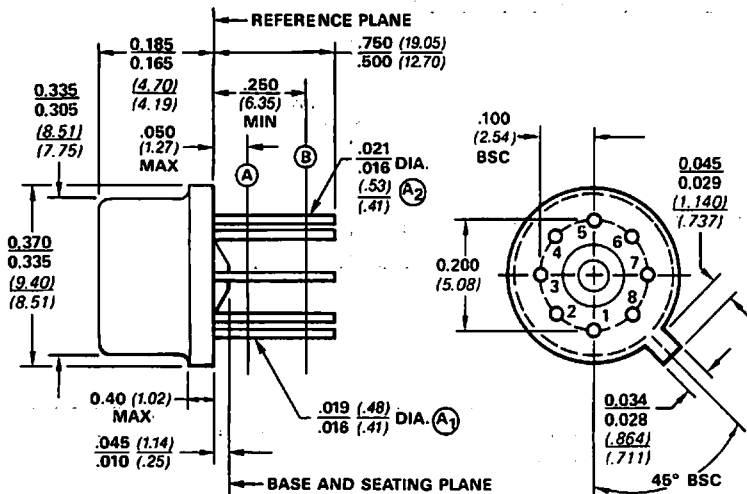


PACKAGE 25
8 LEAD DUAL IN-LINE PACKAGE (J)
(PLASTIC)

NOTES: PIN 1 INDEX IS ONE OR MORE OF THE FOLLOWING

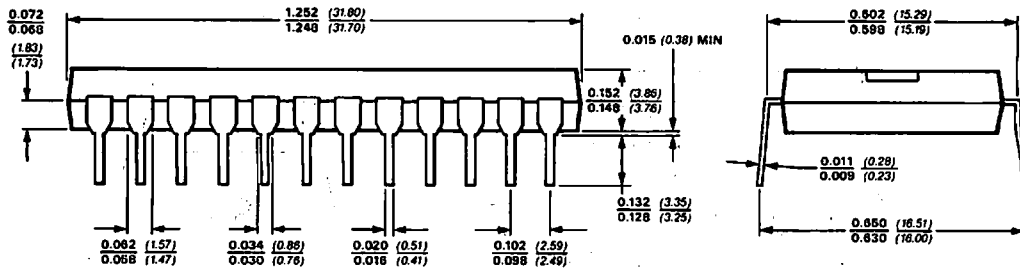
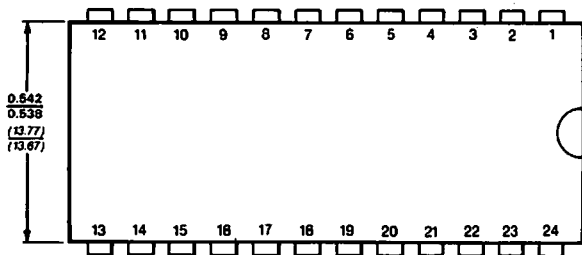
- DOT (INK OR IMPRESSION) ON TOP AND/OR BOTTOM OF PACKAGE
- NOTCH OR HOLE IN PIN 1 VISIBLE FROM TOP AND/OR SIDE
- NOTCH IN END OF PACKAGE VISIBLE FROM TOP AND/OR BOTTOM

ALL DIMENSIONS IN INCHES
(ALL DIMENSIONS IN MILLIMETERS)



NOTE: (ALL LEADS) A, APPLIES BETWEEN A & B A₂ APPLIES BETWEEN B AND .500 (12.70 m.m.) FROM THE REFERENCE PLANE.

PACKAGE 26
8 LEAD TO-99 METAL CAN (A)
(BOTTOM BRAZE)

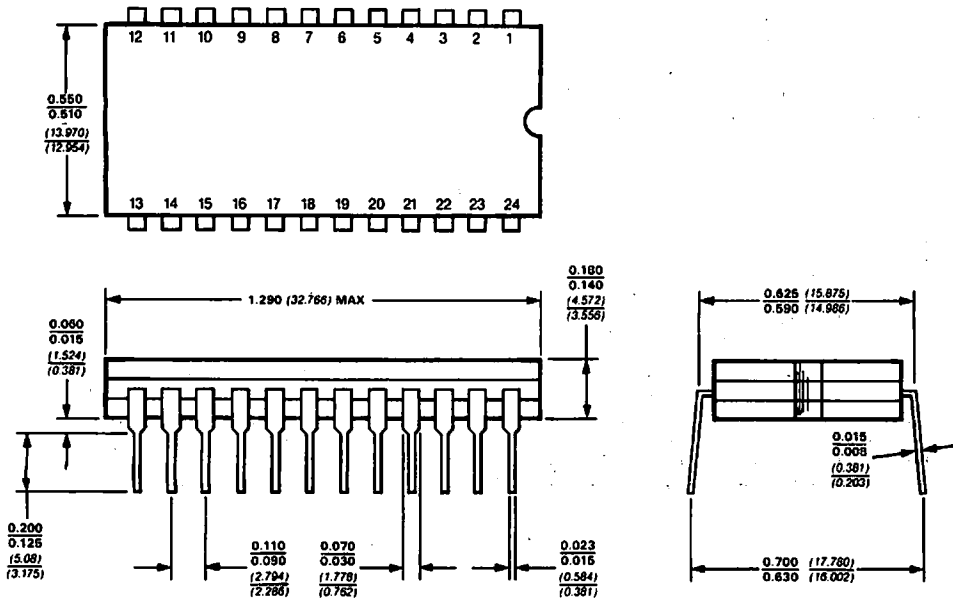


PACKAGE 27
24 LEAD DUAL-IN-LINE PACKAGE (J)
(PLASTIC)

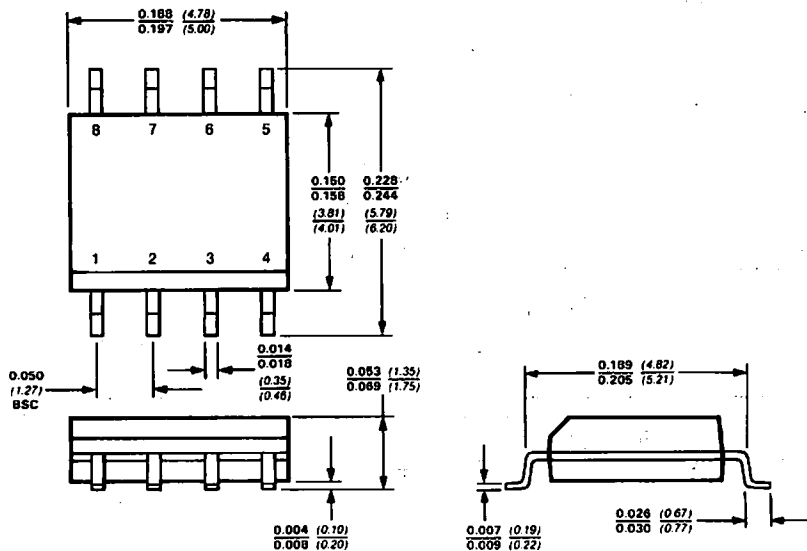
NOTES: PIN 1 INDEX IS ONE OR MORE OF THE FOLLOWING

- DOT (INK OR IMPRESSION) ON TOP AND/OR BOTTOM OF PACKAGE
- NOTCH OR HOLE IN PIN 1 VISIBLE FROM TOP AND/OR SIDE
- NOTCH IN END OF PACKAGE VISIBLE FROM TOP AND/OR BOTTOM

ALL DIMENSIONS IN INCHES
(ALL DIMENSIONS IN MILLIMETERS)



PACKAGE 28
24 LEAD DUAL-IN-LINE PACKAGE (K)
(CERDIP)

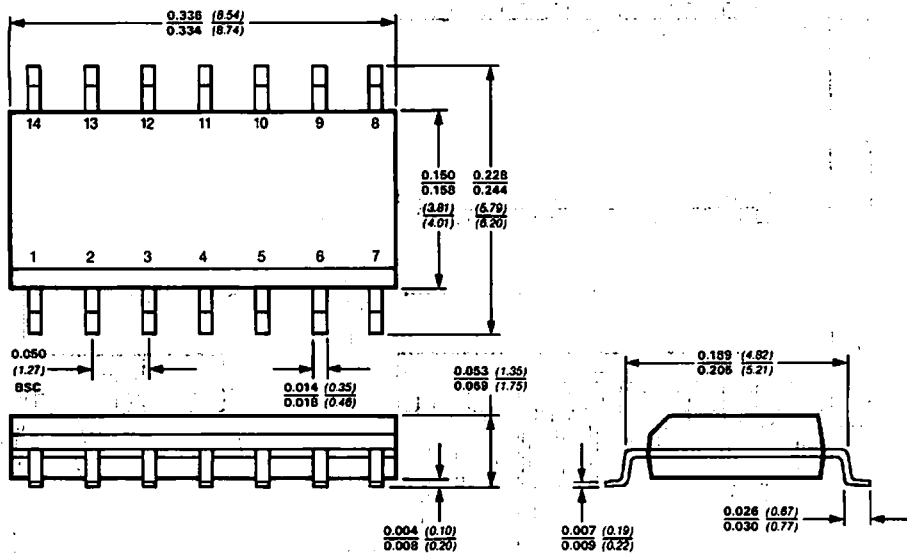


PACKAGE 29
8 LEAD SO (Y)
(PLASTIC)

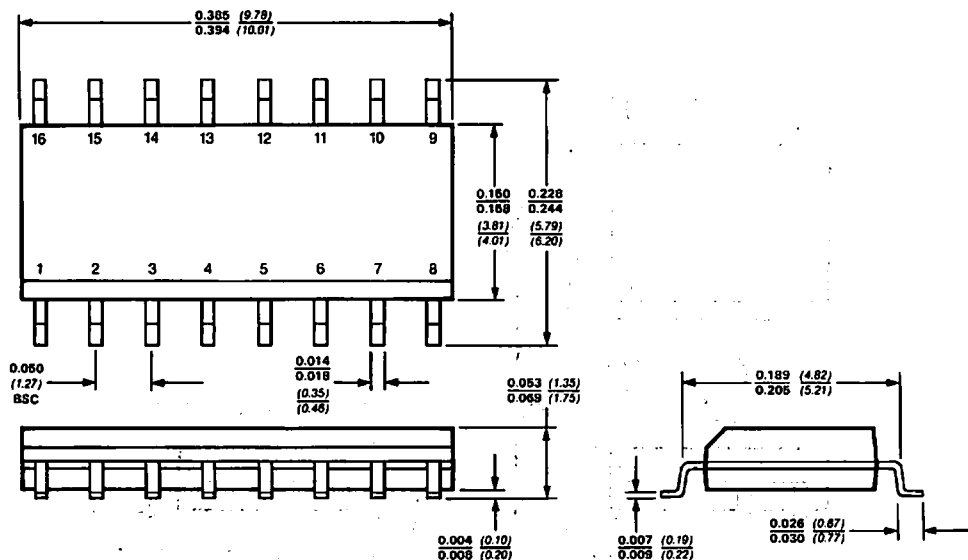
NOTES: PIN 1 INDEX IS ONE OR MORE OF THE FOLLOWING

- DOT (INK OR IMPRESSION) ON TOP AND/OR BOTTOM OF PACKAGE
- NOTCH OR HOLE IN PIN 1 VISIBLE FROM TOP AND/OR SIDE
- NOTCH IN END OF PACKAGE VISIBLE FROM TOP AND/OR BOTTOM

ALL DIMENSIONS IN INCHES
(ALL DIMENSIONS IN MILLIMETERS)



PACKAGE 30
14 LEAD SO (Y)
(PLASTIC)



PACKAGE 31
16 LEAD SO (Y)
(PLASTIC)

NOTES: PIN 1 INDEX IS ONE OR MORE OF THE FOLLOWING

- DOT (INK OR IMPRESSION) ON TOP AND/OR BOTTOM OF PACKAGE
- NOTCH OR HOLE IN PIN 1 VISIBLE FROM TOP AND/OR SIDE
- NOTCH IN END OF PACKAGE VISIBLE FROM TOP AND/OR BOTTOM

ALL DIMENSIONS IN INCHES
(ALL DIMENSIONS IN MILLIMETERS)

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FETS AS ANALOG SWITCHES

Revised December 1984

INTRODUCTION

The past has seen a pronounced growth of analog/digital systems which employ integrated circuits. One of the interface elements in such a system is the digitally-controlled analog switch. As more and more applications arise for the analog switch, especially in the areas of industrial processing and control, the question is often asked: "Which is the best switch for my application?"

The sheer variety of applications precludes any pat answer to this question; however, the user of analog switches can gain valuable insight on the subject through an understanding of the nature of solid-state switches. Areas which require exploration include:

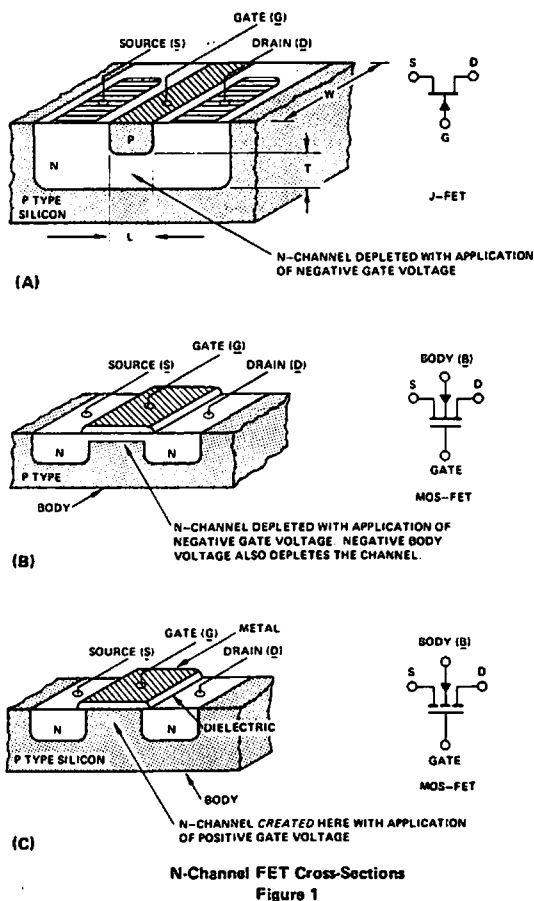
- (1) Basic factors affecting switch performance.
- (2) Details of switch-driver circuit design.
- (3) Total switching characteristics of driver circuits and switches.
- (4) Characterization of the analog switch at high frequencies.

The intent of this Application Note is to consider (1) above, in detail, with minor attention to the other areas.

Field-Effect Transistor Operation

The field-effect transistor (FET) is in effect a conductor whose cross-sectional area may be varied by the application of appropriate voltages. When the conducting area (the channel) is maximum, conductance is also maximum (minimum resistance). When the conducting area is minimum, conductance is minimum (maximum resistance). This phenomenon makes possible the use of FETs as analog switches. When conductance is maximum, the switch is in the ON state; when conductance is minimum, the switch is in the OFF state. In the ON state, an N-type channel contains N-type carriers; similarly, P-channel FETs contain P-type carriers.

Cross-sections for three types of N-channel FETs are shown in Figure 1.



P-channel FET cross-sections are quite similar, except that the channel contains P-type carriers and the voltage polarities are reversed. Depletion-mode devices are shown in Figures 1A and 1B; these FET types have high channel conductance (are ON) with zero gate-channel voltage, and are characterized as "normally-ON" switches. An enhancement-mode FET is shown in Figure 1C. This device requires that voltage be applied to the control gate to create a conducting channel — the ON state. Enhancement-mode FETs are said to be normally-OFF.

For enhancement-mode devices, channel conductance (g_{DS}) is a function of length (L), width (W), thickness (T), carrier mobility (μ), and mobile carrier concentration (N_c):

$$g_{DS} = K_1 \frac{WT}{L} \mu N_c$$

Effective channel thickness and carrier concentration are functions of the electric field in the channel. Voltage on the control gate changes the field, and hence the channel conductance, g_{DS} .

The gate voltage is applied with respect to the channel (source or drain). In most devices, the function of the source and drain can be interchanged, because of symmetrical FET geometry. By convention, however, voltage is specified between gate and source, V_{GS} . Figure 2 shows the variation of g_{DS} with V_{GS} for both N- and P-channel devices. In all cases, $g_{DS} = 1/r_{DS}$.

Note that the slopes ($\Delta g_{DS}/\Delta V_{GS}$) for all three types of N-channel FETs are constant and positive, while the slopes for the P-channel devices are constant and negative. N- and P-channel depletion-mode FETs are ON when $V_{GS} = 0$, while enhancement-mode devices of both types are OFF when $V_{GS} = 0$. Typically, the cut-off voltage, $V_{GS(off)}$, is designed to fall in the 1-to-10 volt range, while the gate-to-source threshold voltage, $V_{GS(th)}$ — that amount of voltage applied to the point where the device begins to conduct — falls in the 1-to-5 volt range. Figure 2 also demonstrates that g_{DS} is approximately a linear function of V_{GS} , with zero g_{DS} occurring at $V_{GS(off)}$ or $V_{GS(th)}$, as follows:

$$g_{DS} = K_2 |V_{GS} - V_{GS(off)}| \quad (\text{depletion})$$

$$g_{DS} = K_2 |V_{GS} - V_{GS(th)}| \quad (\text{enhancement})$$

For a given active area, a junction FET (JFET) will have a higher conductance slope than a MOS FET. Additionally, N-channel carriers have higher mobility than P-type carriers. Thus, all things being equal, N-type FETs have higher g_{DS} ($= 1/r_{DS}$) than P-type devices. If the active area of the device is increased to raise the g_{DS} level, three other FET parameters will also be increased: leakage, capacitance, and cost. The design tradeoffs of these latter parameters are discussed in this Application Note.

When a FET is used as an analog switch, the drain-to-source voltage, V_{DS} , may be either positive or negative. In the OFF state, a typical switch may have $V_{DS} = \pm 20$ V. In the ON state, current flows equally well from drain to source or from source to drain (the channel is a resistor). For most applications, the voltage across the switch will be small.

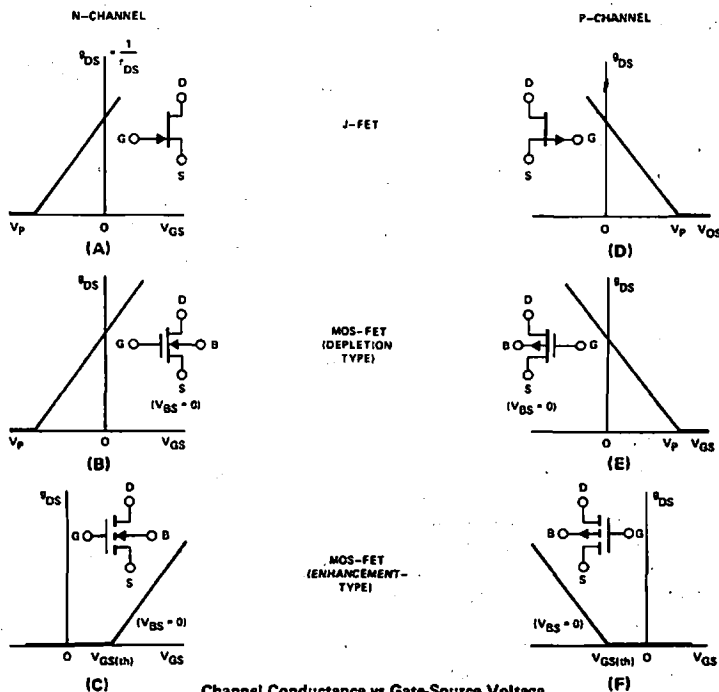
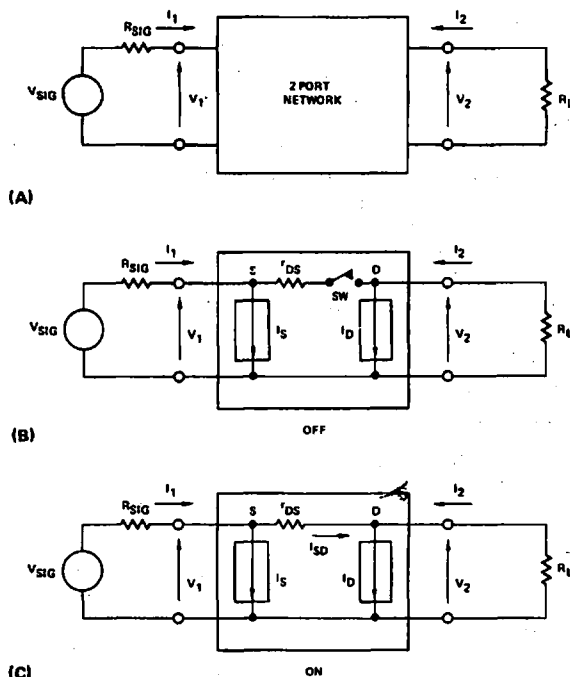


Figure 2



D-C Equivalent Circuits
Figure 3

DC Equivalent Circuits

The perfect switch would have infinite resistance (zero conductance) when open and zero resistance (infinite conductance) when closed. While the FET is not a perfect switch, there are many applications where this deviation from perfection is unimportant. This statement can be justified by an analysis of the implications of the circuits shown in Figure 3.

The general two-port network in Figure 3A couples the signal source, V_{SIG} , to a resistive load, R_L . The network can be characterized by its terminal voltages and currents, V_1 , V_2 , I_1 , and I_2 . Figure 3B shows the equivalent circuit of a FET switch in the OFF state. In this condition, the "source" and "drain" are not connected to one another; however, two leakage current sources, I_S and I_D , are present. The same device is shown in the ON state in Figure 3C. The following typical values are assumed for the circuit:

$$V_{SIG} = 10 \text{ V (full scale)}$$

$$I_S = I_D = 1 \text{ nA}$$

$$r_{DS} = 100 \Omega$$

$$R_L = 200 \text{ K } \Omega$$

$$R_{SIG} = 10 \Omega$$

In the following calculations, leakage current (deviation from the state of a perfect switch) is expressed in terms of error percentage.

OFF Condition Calculation

$$(1) \quad I_1 = I_S = 1 \text{ nA}$$

$$V_{SIG} - V_1 = I_1 \cdot R_{SIG} = (1 \text{ nA})(10 \Omega) = 10 \text{ nV}$$

$$\% \text{ Error in } V_1 = \frac{(10^{-8} \text{ V})(10^2)}{10 \text{ V}} = 1 \times 10^{-7} \%$$

$$(2) \quad I_2 = I_D = 1 \text{ nA}$$

$$V_2(\text{off}) = I_2 R_L = (1 \text{ nA})(200 \text{ K } \Omega) = -200 \mu\text{V}$$

$$\% \text{ Error in } V_2(\text{off})^* = \frac{(2 \times 10^{-4})(10^2)}{10} = 0.002 \%$$

ON Condition Calculation

$$I_1 = I_S + I_D - I_2$$

$$I_2 = \frac{V_2}{R_L} \cong \frac{V_{SIG}}{R_L + R_{SIG} + r_{DS}}$$

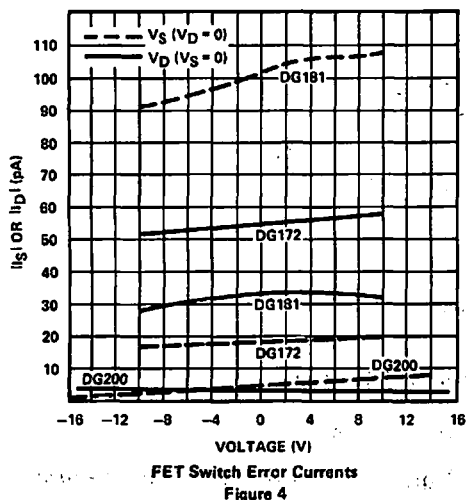
$$V_{SIG} - V_2 \cong (50 \mu\text{A})(110 \Omega) = 5.5 \text{ mV}$$

$$\% \text{ Error in } V_2^* = \frac{(5.5 \times 10^{-3})(10^2)}{10} = 5.5 \times 10^{-2} = 0.055 \%$$

*Referred to V_{SIG} (full scale)

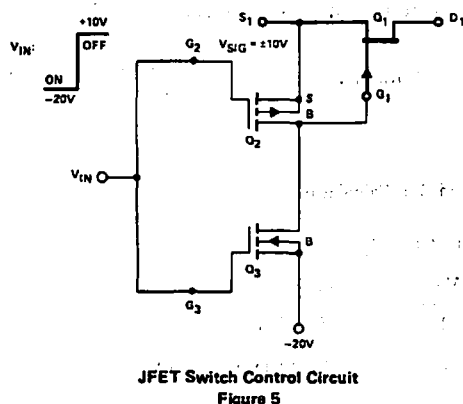
The foregoing calculations indicate that for all but the most critical applications the performance of the FET equivalent circuits in Figure 3 is a good approximation of the perfect switch. In particular, the OFF condition leakage currents contribute only a negligible portion of total error.

The actual error currents of three different types of FET switches are shown in Figure 4. The measured error is much lower than the 1 nA (1000 pA) obtained from the sample calculations. These data are taken from a MOS FET, an N-channel JFET, and a complementary MOS (CMOS) combination including a P-channel device and an N-channel device diffused onto the same substrate. The behavior of these FETs as elements of analog switching integrated circuits will be dealt with in detail elsewhere in this Application Note.



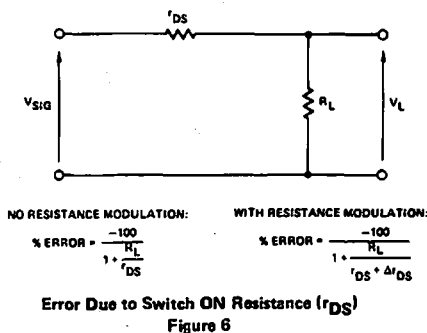
The JFET as a Switch

A suitable driving circuit must be considered when assessing the performance of the JFET as a switch. Such a circuit is shown in Figure 5.



Note that Q_1 is an N-channel JFET, Q_2 is an enhancement-mode P-channel MOS FET, and Q_3 is an enhancement-mode N-channel MOS FET. From Figure 2, V_{IN} of -20 V will

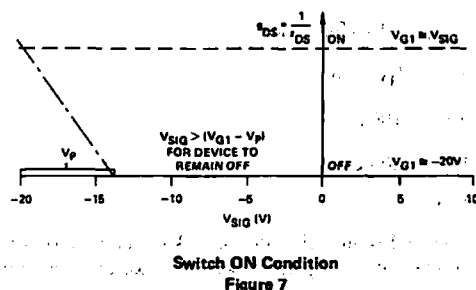
turn Q_2 ON and Q_3 OFF, so that S_1 and G_1 are connected ($V_{GS} = 0$ V) and Q_1 is ON. If V_{GS} is allowed to vary, g_{DS} ($= 1/r_{DS}$) will also vary. This variation in resistance appears as a source of error when the switch is ON, and the error is defined as resistance modulation. In Figure 6, the error percentage in the case of resistance modulation is greater than that which occurs when $\Delta r_{DS} = 0$.



The suggested driving circuit of Figure 5 eliminates Δr_{DS} at low frequencies. The typical positive supply voltage is +10 V and the typical negative supply voltage is -20 V. In order for V_{GS} to change, current must flow through Q_2 , which is ON. There are only two possible current paths through Q_2 : (1), through Q_3 , which is OFF and subject only to variations in leakage current, or (2), into the gate of Q_1 , which is also subject to leakage current. Since both paths through Q_2 provide only negligible changes in V_{GS} , their effect in the circuit may be ignored. As the switching frequency is increased, capacitive reactance will provide lower impedance paths, so that some degree of Δr_{DS} is possible. Thus two conditions contribute to $\Delta r_{DS} = 0$ in the circuit. First, $V_{SIG} \approx V_{G1}$, due to the low impedance between these points. Second, the output impedance of Q_3 (driver output) is very large when compared to the R_{ON} of Q_2 .

When V_{IN} is +10 volts, Q_2 is OFF and Q_3 is ON; G_1 is at -20 volts and Q_1 is OFF. In Figure 7, note that Q_1 will remain OFF only so long as $V_{SIG} > (V_{G1} - V_{GS(off)})$. $V_{GS(off)}$ is a negative voltage for an N-channel FET; thus the negative analog signal is limited by the $V_{GS(off)}$ of Q_1 and the negative supply ($V_{G1} \approx -20$ V).

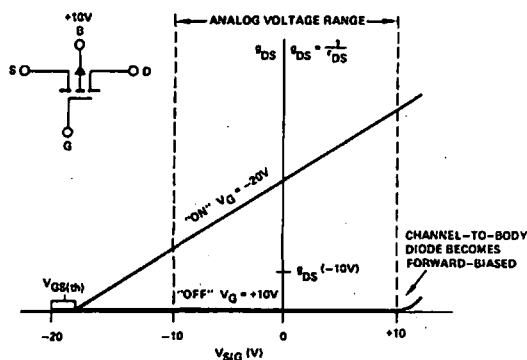
The ON condition is also shown in Figure 7. g_{DS} is constant because with $V_{G1} \approx V_{SIG}$ imposed by the switch control circuit, $V_{GS} \approx 0$.



The MOS FET as a Switch

The P-channel enhancement-mode MOS FET is currently used in more applications than its N-channel counterpart. The consideration of MOS FET switch performance will thus center on P-channel devices.

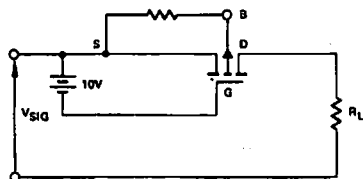
The ON and OFF conditions of the MOS FET are analyzed in Figure 8. When the device is in the ON stage, note that the FET begins to turn ON when V_{SIG} (V_S or V_D) becomes $V_{GS(th)}$ volts more positive than $V_G (= -20 \text{ V})$.



PMOS Channel Conductance (r_{DS}) vs Signal Voltage

Figure 8

Figure 8 also indicates that at any given point along the g_{DS} vs V_{SIG} curve, a unique value of g_{DS} will be obtained. Assume that a battery is inserted between the source and the gate, with the source clamped to the body as shown in Figure 9.



"Floating" Battery and Clamped Source

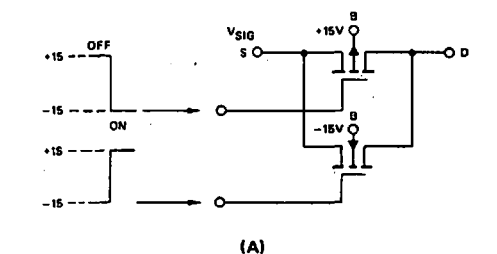
Figure 9

A constant voltage between source and gate will produce a constant value of g_{DS} vs V_{SIG} , provided that the body-to-source voltage is also constant. In a MOS FET, variation of the body-to-source voltage will also cause a modulation of g_{DS} . To further complicate the picture, several MOS FETs will have a common body when they are integrated on a single chip. Finally, the construction of a "floating battery" circuit is difficult. Thus MOS FET switch designers currently cope with the problem of Δr_{DS} by specifying r_{DS} for a given switch at several points over the entire analog voltage range.

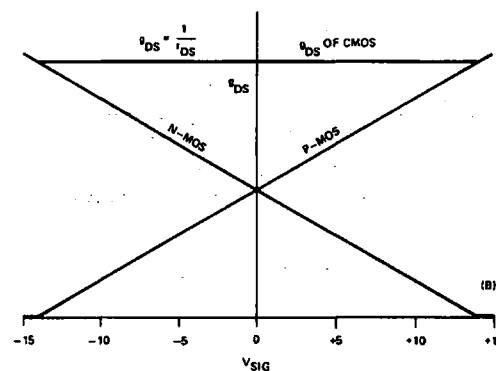
Referring to the switch in the OFF condition ($V_G = +10 \text{ V}$), it is apparent that no problem will exist until the source-to-body or drain-body diode becomes forward-biased.

The CMOS Switch

As noted previously, the typical PMOS switch circuit will exhibit a variation in ON conductance as the analog voltage is varied. This undesirable characteristic can be overcome by paralleling P- and N-channel FETs, as shown in Figure 10A. For the ON state, the N-channel gate is forced positive and the P-channel gate is forced negative. Figure 10B shows the combined conductance of the two FET switches. The integrated combination of N-channel and P-channel devices on a common substrate is referred to as complementary MOS (CMOS).



(A)



	P-MOS	N-MOS	
V_G	-15V	+15V	ON
V_G	+15V	-15V	OFF

(B)

PARALLEL P-MOS AND N-MOS (CMOS)

OFF CONDITION:
 V_G (N-TYPE) = -15V,
 V_G (P-TYPE) = +15V.

$$g_{DS} = \frac{1}{r_{DS}}$$



(C)

Characteristics of CMOS Devices

Figure 10

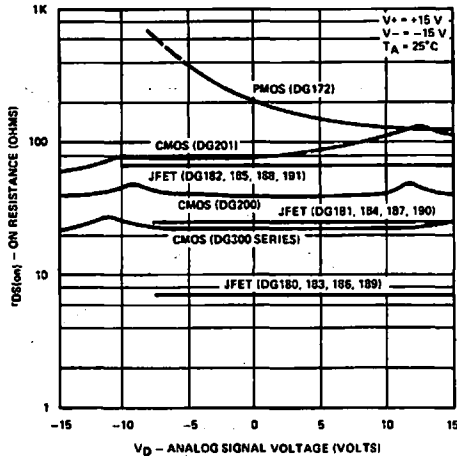
The OFF condition for the CMOS device will be maintained so long as the channel-to-body diodes do not become forward-biased, as shown in Figure 10C.

The major advantages the CMOS construction technique makes to analog switching are:

- Lower r_{DS} variation with analog signal characteristics, similar to the performance of a junction FET.
- Analog signal range extends to + and - supply voltages. For instance, using the same ± 15 V supplies typical of operational amplifiers, the signal-handling capability of the system is limited by the op amp, not by the switch.

Summary of FET Switch Performance and Tradeoffs

Figure 11 compares the performance of three switch types with respect to $r_{DS(on)}$ vs V_{SIG} . If one examines the r_{DS} characteristics of the integrated switching circuits DG172 and DG181, there may be a tendency to dismiss the DG172 on the basis of its apparent inferior performance.

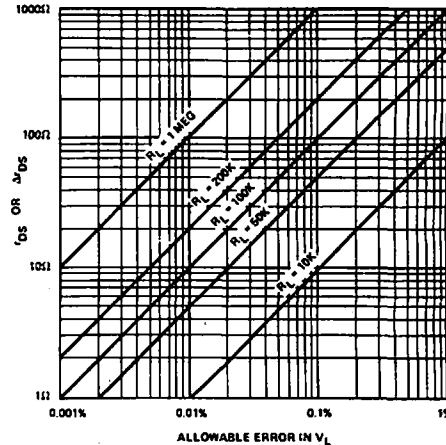


Performance of Three FET Switches
Figure 11

In reality, the comparison between the monolithic DG172 and the hybrid DG181 is not clear-cut. Initial circuit design considerations must determine what degree of error can be tolerated by the application in terms of Δr_{DS} and r_{DS} . Once this error factor has been determined, the designer should contact a switch manufacturer for applications assistance in selecting the best switch for his purpose, in terms of both r_{DS} and cost. From this viewpoint, the single-chip DG172 will perform creditably in applications where Δr_{DS} and r_{DS} error are not critical, and the device costs considerably less than the DG181.

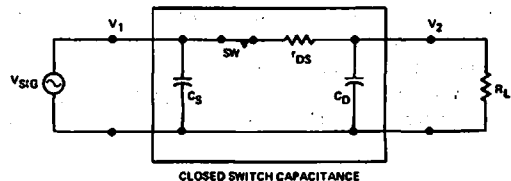
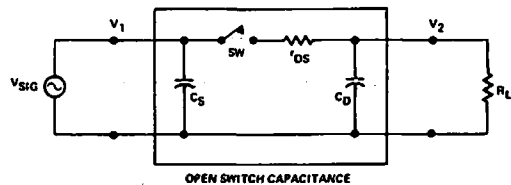
To amplify the preceding point, consider the definition of the tolerable level of Δr_{DS} and r_{DS} .

The curves in Figure 12 define the maximum r_{DS} (or Δr_{DS}) which can exist for a given allowable error percentage with a fixed value of R_L . Recall that in the circuit in Figure 3, a resistive load of 200K Ω was assumed. If it is also assumed that an error level of 0.1% is tolerable, then $r_{DS} = 200 \Omega$ is the maximum allowable switch resistance. On the other hand, if settling time is not critical, then an R_L of 1 megohm, yielding $r_{DS} = 1K \Omega$ is permissible.



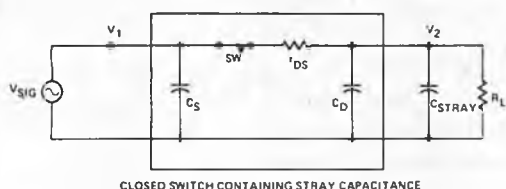
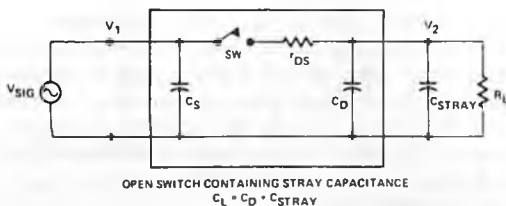
Tolerable Level of Δr_{DS} and r_{DS}
Figure 12

In situations where settling time is indeed a design consideration, the circuits in Figure 13 will provide an overview of the exact nature of settling time for $V_2 (=V_1)$ at turn-OFF and turn-ON. For a turn-ON signal, C_L charges through r_{DS} . During turn-OFF, C_L discharges through R_L . For a system error level of 0.1%, $R_L = 1000 r_{DS}$; therefore, the maximum settling time for V_2 occurs during turn-OFF.



Switch Settling Time Equivalent Circuits
Figure 13

(Cont'd)



Switch Settling Time Equivalent Circuits
Figure 13

Consider a switch with $C_S = C_D = 3 \text{ pF}$, for an application requiring 0.1% accuracy with $5 \mu\text{sec}$ settling time. A typical stray capacitance (C_{IN} for an op amp) may be 6 to 7 pF. Therefore, $C_L = 3 \text{ pF} + 7 \text{ pF} = 10 \text{ pF}$. Resistance loads, R_L , of $100 \text{ K}\Omega$, $50 \text{ K}\Omega$, and $25 \text{ K}\Omega$ are considered for the switch. The time required for an RC system to settle to within 0.1% of its final value is 6.9 time constants (6.9 RC). Table I shows the R_L and r_{DS} values necessary to satisfy a number of settling time specifications. From Table I, it is apparent that so long as $R_L \leq 72 \text{ K}\Omega$, the desired settling time of $5 \mu\text{sec}$ will be achieved.

TABLE I

R_L (Ω)	r_{DS} (Ω)	C_L (pF)	$t_{ON} (V_2)^{**}$ (0.1% settling time) (nsec)	$t_{OFF} (V_2)^{**}$ (0.1% settling time) (μsec)
25K	25	10	1.72	1.72
50K	50	10	3.45	3.45
*72K	72	10	5.00	5.00
100K	100	10	6.90	6.90

*Maximum R_L for $t_{set} = 5 \mu\text{sec}$

**Does not include delay times

If cost is a design constraint, it is wise to make a close analysis of actual system switch requirements. Too often, designers buy unnecessary performance capability. In Table I, the switch with $r_{DS} = 25 \Omega$ costs nearly twice as much as does the switch with $r_{DS} = 50 \Omega$, yet either switch will meet the $5 \mu\text{sec}$ settling time specification.

Switch Capacitance

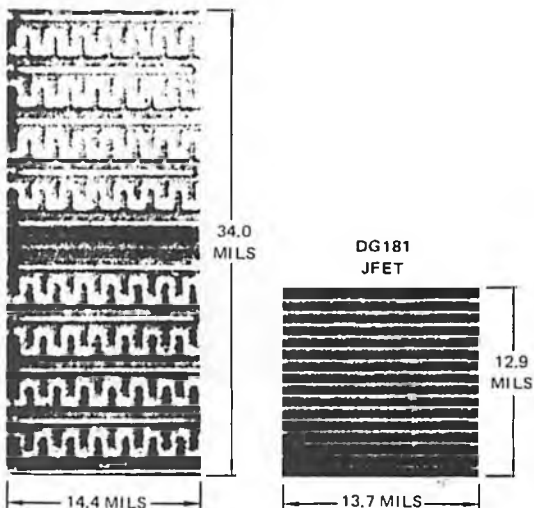
In general, the lower the switch capacitance the better the switching time and high-frequency isolation performance. The subjects of switching time and high-frequency isolation are covered in other Application Notes in this series.

The simplified representation of switch capacitance shown in Figure 13 can be used to provide a very good estimate of what problems (if any) will be caused by switch capacitance in a given application.

In general, capacitance is proportional to the active area in a FET chip, prior to bonding onto a header. Additional stray capacitances are introduced when the leads are brought out through the device package. Thus, as lower r_{DS} (higher g_{DS}) is required, the active area is generally increased to obtain that parameter. The increase in area leads to an increase in capacitance.

The foregoing statements are true so long as one is dealing with a given device type. However, in transition from a JFET to a PMOS device, a significant difference will be observed in the active areas required for a given r_{DS} . Figure 14 compares the area of a JFET (from the hybrid DG181 circuit) and the monolithic PMOS circuit of all 4 switches of a DG172. Note that the r_{DS} for the JFET is approximately one-third that of the total PMOS device, while the active PMOS area is almost three times greater than that of the JFET. Yet the ratio of PMOS-to-JFET capacitance is almost 2:1. For the single DG172 switch the comparison to the JFET is a larger $r_{DS(on)}$ for the smaller area.

DG172 (ALL 4 SWITCHES)
MOS-FET (PMOS)



$r_{DS} = 42 \Omega$
AREA = 489.6 MIL^2
 $C_D = 10 \text{ pF}$

$r_{DS} = 15 \Omega$
AREA = 176.7 MIL^2
 $C_D = 6 \text{ pF}$

Active Area Comparison of PMOS and JFET Switches
Figure 14

Switch Comparison

A comparison between the characteristics of the three types of JFET switches is made in Table II.

This Application Note has surveyed the characteristics of FET switches and their associated drivers. In considering the FET as an analog switch, discussion has largely centered on the devices themselves, including specific load problems and

applicable driver circuits. Total switch performance is a function of the switch *and* the switch driver. Typically, high-performance switch drivers require numerous switching transistors. When discrete devices are considered, the total parts count will be high and the cost will be prohibitive. From the standpoint of cost, improved performance, and smaller size, the integrated circuit FET switch and driver is often the superior choice.

TABLE II

Switch Type	Analog Signal Range	r_{DS}	Δr_{DS}	Leakage, I_D or I_S
PMOS	$(V_- - V_{GS(th)}) < V_{SIG}^*$	High	High	Low
JFET	$(V_- - V_{GS(off)}) < V_{SIG}^*$	Low	Low	Low
CMOS	$V_- \leq V_{SIG} \leq V_+$	Medium	Medium	Low

*Both $V_{GS(th)}$ (for PMOS) and $V_{GS(off)}$ (for N-channel JFET) are *negative* voltages.

V_+ is defined as positive supply voltage.

V_- is defined as negative supply voltage.

INTRODUCTION TO QUANTIZED FEEDBACK

INTRODUCTION

Siliconix' "Quantized Feedback" (or charge balancing as it is sometimes called) approach towards A/D conversion is an integrating technique, implemented through the use of an analog processor and digital controller. Intrinsic features of this approach are Auto-Polarity, Auto-Zero and ratio-metric operation. As we shall see, this technique offers superior linearity, normal mode rejection and stability over that of other integrating techniques while at the same time requiring no critical components except a stable voltage reference.

Let's begin our discussion by considering the following op-amp adder:

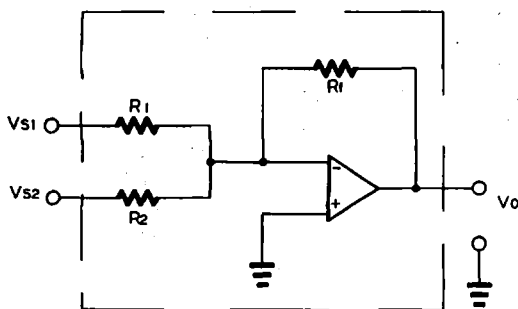


Figure 1.

$$\text{where } V_0 = -\left(\frac{R_f V_{S1}}{R_1} + \frac{R_f V_{S2}}{R_2}\right)$$

Recalling basic op-amp operation, it is easy to see that the output voltage V_0 is equal to the algebraic sum of V_{S1} and V_{S2} appropriately scaled. By taking this simple adder circuit and a few

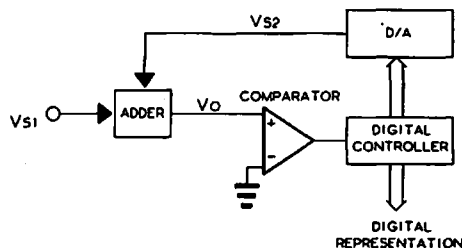


Figure 2.

Rudimentary A/D Converter

$$\frac{V_{S1}}{R_1} \approx -\frac{V_{S2}}{R_2} \therefore V_0 \approx 0$$

V_{S1} must be stable during conversion $\therefore$ requires S/H in front end.

additional components it is possible to construct a rudimentary A/D converter as shown in Figure 2.

If V_{S1} is the unknown voltage that we would like to measure and V_{S2} an input voltage that we control, then by examining the state of V_0 and feeding back a V_{S2} sufficient to cancel out V_{S1} , (i.e. keep V_0 as close to zero as possible) we can digitally keep track of V_{S1} as diagrammed in Figure 2.

This is the technique used by successive approximation and counting type converters. Although conceptually simple and apparently easily implemented, this technique is entirely dependent upon the linearity and stability of the feedback D/A. In addition, the complexity of a very high precision D/A (greater than 8 bits input) which would be necessary to construct a high-precision A/D could prove prohibitive both in cost and circuit complexity. A more accurate and less complex approach as we shall see, would be to feed back just 2 voltage levels (say $+V_{ref1}$, $-V_{ref2}$) instead of the multitude of voltages possible with a D/A. However in using this approach we become interested in the time average of the feedback voltage as compared to the voltage under measurement, since we are now restricted to 2 voltage levels which should bracket the input voltage to be measured.

This being the case we now want to change our simple op-amp adder (of Fig. 1) into an integrator (Fig. 3) to perform the necessary averaging function.

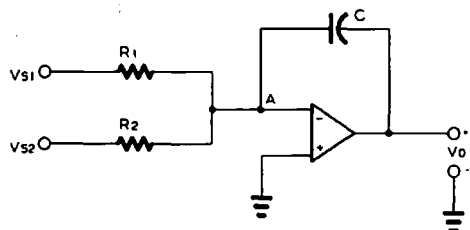


Figure 3.
Op-Amp Integrator

$$\text{where } V_0 = -1/C \int \left(\frac{V_{S1}}{R_1} + \frac{V_{S2}}{R_2} \right) dt$$

Once again V_{S1} is the unknown voltage we would like to measure and V_{S2} one of two voltage levels returning from our feedback network. We examine V_0 and feed back a voltage (V_{S2}) such that the time average of V_{S2} is sufficient to cancel out the analog unknown, V_{S1} . However since the input node (point A in Figure 3) to our analog adder is really a virtual ground, what we are really trying to balance out are the 2 currents flowing into the node (i.e. $\frac{V_{S1}}{R_1}$ and $\frac{V_{S2}}{R_2}$). This is easily seen in the integrator circuit (Fig. 3) where the quantity that

we are interested in integrating ($\frac{V_{S1}}{R_1} + \frac{V_{S2}}{R_2}$) is in reality a current. But recalling that the integral of a current is charge, $Q = \int idt$, what we are really trying to balance in order to keep V_0 as close to zero as possible is the charge on the capacitor C as supplied by V_{S1} and V_{S2} . But since in our averaging process the feedback V_{S2} can only assume one of 2 voltage levels for an integer number of *time units*, we can only add or take away capacitor charge in quantum lumps ($-1/C \frac{V_{ref1}}{R_2} dt$ or $+1/C \frac{V_{ref2}}{R_2} dt$), thus giving us our technique name *quantized feedback*. A block diagram of such an A/D converter is shown in Figure 4.

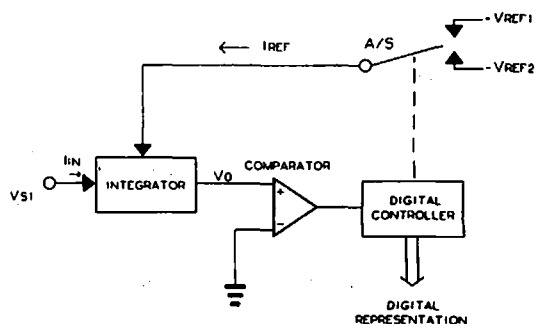


Figure 4.
Quantized Feedback A/D Converter

Figure 4 is the quantized feedback technique in its most basic form. As previously mentioned, by feeding back only 2 voltage levels we can significantly improve our linearity and accuracy in high precision measurements while reducing our feedback circuit complexity to a switch and stable voltage reference. Although our digital control logic is now somewhat more complex as compared to a counting technique, we are able to effect significant gains in precision with only modest increases in digital control circuit complexity. And since in this technique both the unknown and reference voltages are simultaneously integrated with the objective of keeping the integrator output as close to zero as possible, large voltage swings at the integrator output as typically seen in Dual Slope converters are avoided, thus easing integrator requirements. This dynamic feedback measurement process also ensures equally spaced count transition windows under varying conversion rates; even

around zero. Although timing is now critical to proper high resolution operation, our task is easily met through dedicated digital-control logic. Another feature inherent in this technique is that since we are trying to balance charges which are proportional to the input voltages, scale changes are easily accomplished through simple ratiometric resistor (R_1 and R_2) changes (i.e. Fullscale $\propto R_1/R_2$).

The basic principles underlying the quantized feedback technique should now be apparent, as well as the fundamental relationship between the voltage-under-measurement (V_{IN} , formerly V_{SI}) and our 2 feedback voltage levels V_{ref1} and V_{ref2} . That is, the current supplied by V_{IN} must be of opposite polarity and lie within the range bounded by the reference currents, $I_{ref2} \leq I_{in} \leq I_{ref1}$, (see Fig. 4) in order for V_{IN} to be measured. So in order to measure a $\pm V_{IN}$ using our simple system, we would have to supply both a $\pm$ reference voltage. We are also limited in our simple system to

measuring single ended inputs (i.e. no common mode voltage). Siliconix however, has overcome these problems through an enhancement of the basic technique in which only 1 polarity V_{ref} is necessary for auto-polarity operation and where a zeroing measurement is automatically performed. Briefly, the way it is done is through the use of negative feedback to impress a system offset voltage when zeroing.

Let's now look at Figure 5 which is a diagram of the analog processor architecture as found in the Siliconix LD111A, LD120 and LD122 (the input buffer is user-supplied). Note that outside of a few additions, this circuit closely resembles our basic Quantized Feedback Converter (Figure 4). We still have the integrator summing node, pin 9 fed by a voltage reference source, unknown input voltage source, and (new here) an Auto-Zero (whose use will soon be explained) voltage source. The control logic near the Auto-Zero buffer is used by the digital controller to implement the

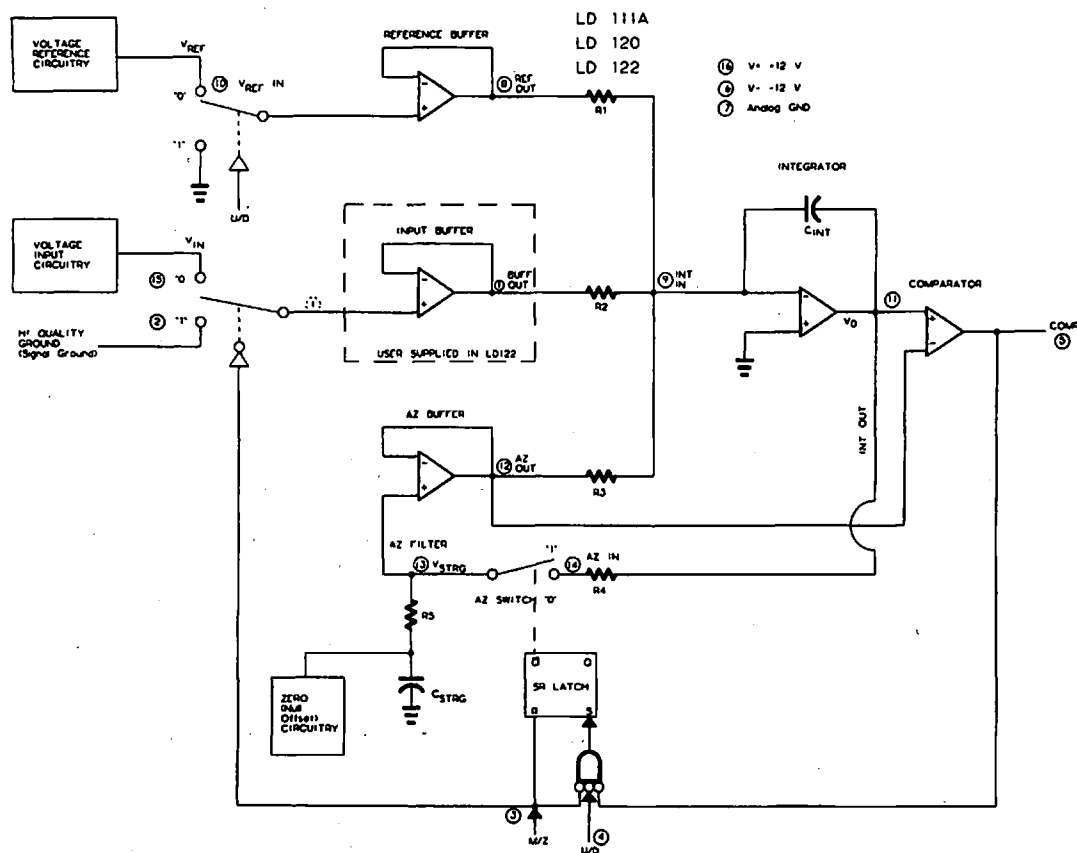


Figure 5. Siliconix Analog Processor

measurement algorithm. All of the inputs are now unity buffered so that loading effects on inputs are effectively eliminated. As before the output of the integrator is fed to a comparator whose output COMP 5 is monitored by the digital control logic. A feedback control signal UP/DOWN, U/D 4, from the digital controller determines which of 2 reference voltage levels (V_{ref} or GND) are to be fed back. The addition of the Measure/Zero M/Z 3 control line permits the division of our sampling process into 2 parts, a zeroing and a measuring interval.

The aforementioned system offset impression is accomplished in an auto-zeroing interval which is of sufficient duration to ensure equilibrium conditions. In the auto-zeroing interval the M/Z line is set low, connecting the input buffer to the input signal ground (or negative input if doing differential measurements). With the combination of the other 2 control lines U/D and COMP, the SR latch is set, forcing the switch between pins ⑬ and ⑭ closed. The digital control logic toggles the U/D line at a 50% duty cycle rate, thereby feeding a d-c pulse train (of amplitude V_{ref}) to the reference buffer. Ignoring all other contributions to the sum node, the reference buffer will contribute a current equal to V_{ref}/R_1 to the node half of the time with the average current being

$\frac{V_{ref}}{2R_1}$. The output of the integrator feeds the

comparator, but the comparator output is ignored in the zeroing interval so that this route can be disregarded for now. By virtue of the closed Auto-Zero switch however, the integrator output is also fed back to the A/Z buffer which in turn supplies current to the integrator summing node thereby forming a closed negative feedback loop. Along the way though, the integrator output V_0 charges up a capacitor C_{STRG} which, as we shall see, is instrumental to proper operation. Resistor R_4 is used to guard against oscillations by assuring that the negative feedback gain is less than unity. R_5 is used to provide low pass filtering action in conjunction with C_{STRG} . Now since our buffers have such high input impedances, let's assume that the voltage on C_{STRG} is the same as that on pin ⑬, the input to the A/Z buffer or V_{STRG} . Because of the filtering action provided by $R_5 - C_{STRG}$, V_{STRG} will be the average of the integrator output. Therefore, a current V_{STRG}/R_3 , opposite in polarity to that supplied by the reference buffer will be fed to the summing node. With a little imagination we can envision that

the DC or time average of all the current flowing into the integrator sum node will eventually cancel each other out and in equilibrium the net current will equal zero. There will however, be an integrator output voltage V_0 the average of which will be V_{STRG} and both will be opposite in polarity to the V_{ref} voltage. Thus far all mention of the input buffer and error/offset currents have been avoided, but it can easily be seen that any current supplied through the input buffer from the negative differential input (Hi-Quality Ground ②) as well as any error currents will simply either aid or oppose the A/Z buffer in its attempts to balance out current from the reference source. Consequently in equilibrium, the V_{STRG} will be shifted slightly from what it would have been had none of these other current sources been present. Of course we assume that these additional sources do not change appreciably with time when we later move into the measurement interval. The key point to remember here is that the reference buffer is constantly supplying an average current of $1/2 \left(\frac{V_{ref}}{R_1} \right)$ to the integrator sum node and in auto-zero

equilibrium the sum of all other sources of current (A/Z, INPUT, ERROR) are equal and opposite to

$1/2 \left(\frac{V_{ref}}{R_1} \right)$. This auto-zero equilibrium current

balance $\left(\frac{V_{ref}}{2R_1} \right)_{avg} - \frac{V_{STRG}}{R_3}$ (supplied by A/Z,

INPUT, etc.) = 0 is our desired offset impression and its use in the measurement process will now be described.

One of the things that we have succeeded in doing in the auto-zeroing process is to determine the average integrator output voltage level (V_{STRG} or A/Z output buffer voltage) when our system is zeroed. By tracing back the negative input of the comparator, we can see that this is the voltage that our integrator output is compared against when we actually do our measurements. When we leave the auto-zeroing interval to do a measurement, the M/Z line goes high, reconnecting the input buffer to the + end of the voltage under measurement and opening the switch between ⑬ and ⑭. We can now appreciate the importance of C_{STRG} , for in addition to averaging out the integrator output, it holds for us the value of V_{STRG} necessary for proper comparator operation and charge balancing. During the measurement interval V_{IN} begins to supply current to the sum node and the comparator output is closely monitored by the

digital controller. In response to the state of COMP, the controller feeds back either V_{ref} or GND to the reference buffer by toggling the U/D line. Measurement now is exactly as described in our simple A/D converter circuit (Figs. 3 & 4). However since all of our equilibrium conditions in auto-zero were calculated with an average $\frac{V_{ref}}{2}$

being fed into the reference buffer, feeding back a constant V_{ref} will result in a net current over and above that in equilibrium of $+V_{ref}/2R_1$ being sent to the sum node. Likewise feeding back a constant GND will cause a net current of $-V_{ref}/2R_1$ (from A/Z, etc.) to flow into the sum node. So whatever polarity V_{IN} may be, we will be able to balance it out with appropriate resistor scaling. An interesting

aside here is that in all of our discussions the absolute polarity of V_{ref} (i.e. + or - with respect to GND) was never specified and any polarity could have been used with equal, but differing polarity results. However due to the nature of the switch Siliconix uses with the V_{ref} buffer (PMOS) only positive references will work.

THE "QUANTIZED FEEDBACK" ALGORITHM

The measurement algorithm used by all of our digital processor chips (LD110, 121A) is basically the same. There are some minor variations due to slightly different analog control structures and the different precision that each processor offers. For an example,

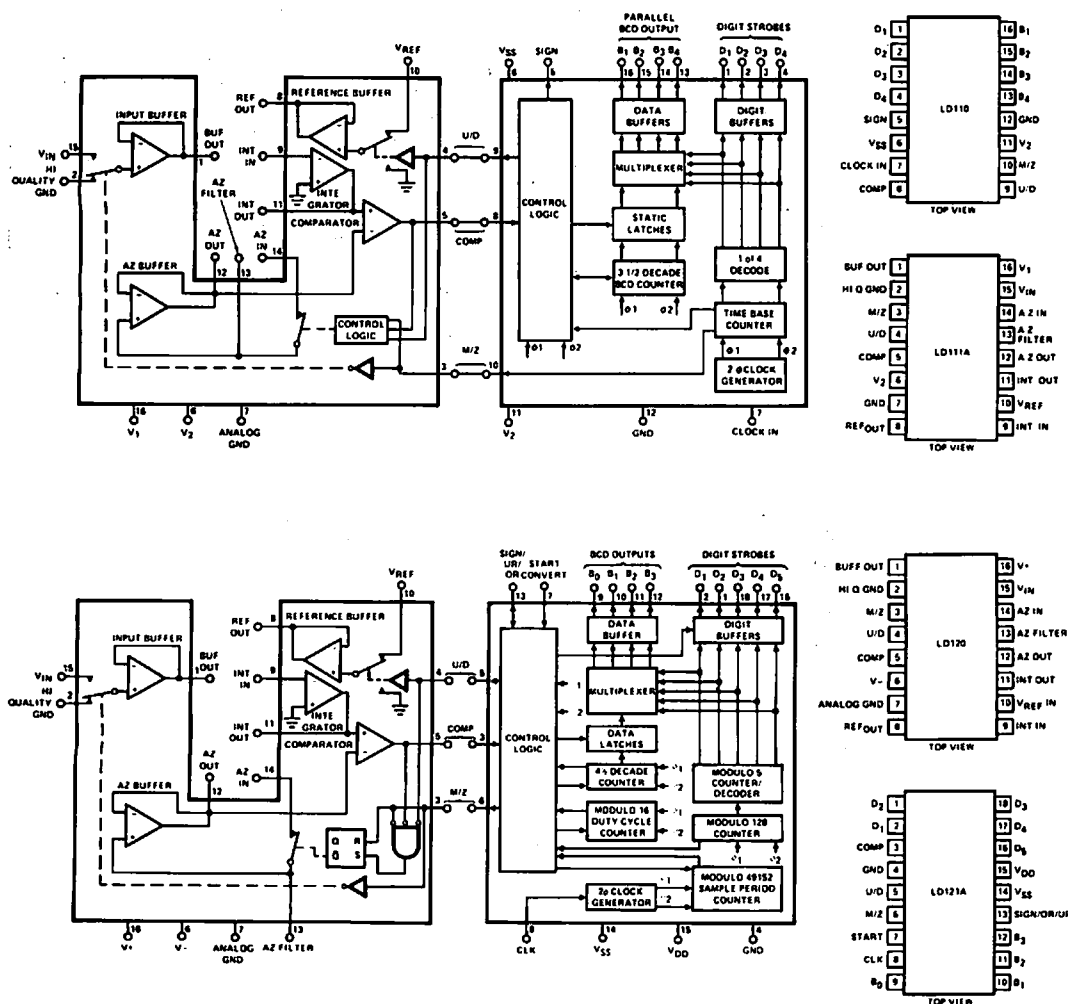


Figure 6

the LD110 (114), $3\frac{1}{2}$ digits and the LD121A, 4½ digits. All chips, though for greater stability and accuracy derive their timing from a stable clock signal generated either internally or externally. Inside the chip the clock is further divided by 2, or split into

a 2-phase signal as the case may be. However, for our discussion, the timing signal as used by all of the internal circuitry will be the clock. Figure 6 shows the internal organization, pinout and typical analog processor interfacing for each of the digital controllers.

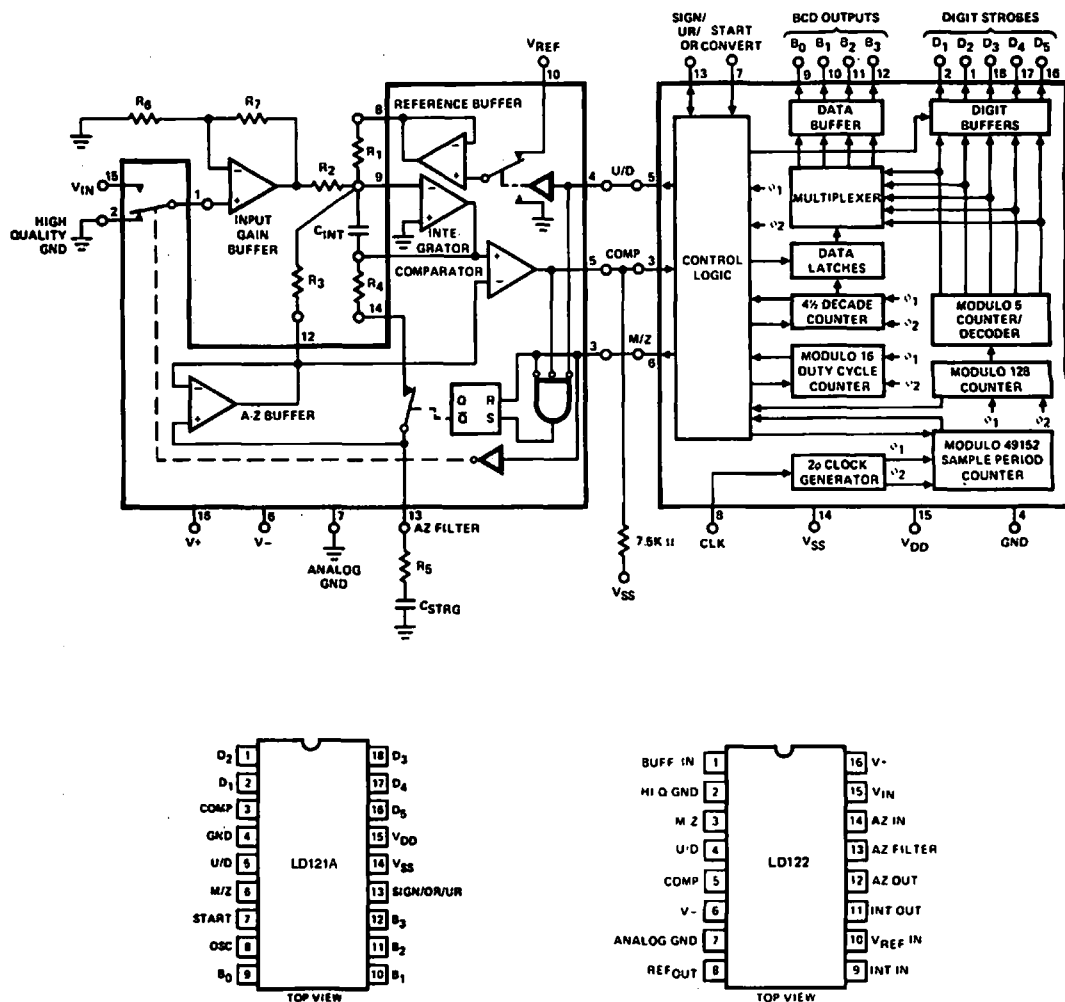


Figure 6
Continued

Every sampling interval is composed of an integral number of clock periods (LD110 = 6144, LD121A = 49,152). The sampling interval can be further subdivided into 2 operational periods, the Auto-Zero (A/Z) and Measure intervals. The A/Z interval, as we know, gives us a means of nulling offset voltages and establishing a second tracking reference voltage necessary for bipolar conversion. The interval is signified by the Measure-Zero control line (M/Z) going low and consists of the following number of clocks: LD110 = 2048, LD121A = 16,384. In the Measurement interval (when M/Z = 1), the actual charge balancing process is implemented and consists of the following number of clocks: LD110 = 4096, LD121A = 32,768. As you may have noticed, A/Z makes up 1/3 and Measure Interval 2/3's of the sampling interval. The reason why such a significant fraction of time is devoted

to A/D to insure that equilibrium zero conditions are attained. The M/Z line is the principal signal to the analog circuitry to tell it which interval it is in so that the appropriate switches can be closed. The Up-Down (U/D) line, on the other hand, is responsible for controlling the reference voltage fed back in the A/Z and Measure Intervals. As we may recall, during the A/Z interval a 50% duty cycle pulse train of V_{REF} amplitude is fed back in the analog system. This is accomplished by toggling the U/D line once every 4 clocks in the LD110 and once every 8 clocks in the LD121A.

Figure 7 shows typical waveforms in the auto-zero interval for the LD110. The LD121A has essentially the same timing except that twice as many clocks are required for U/D toggling.

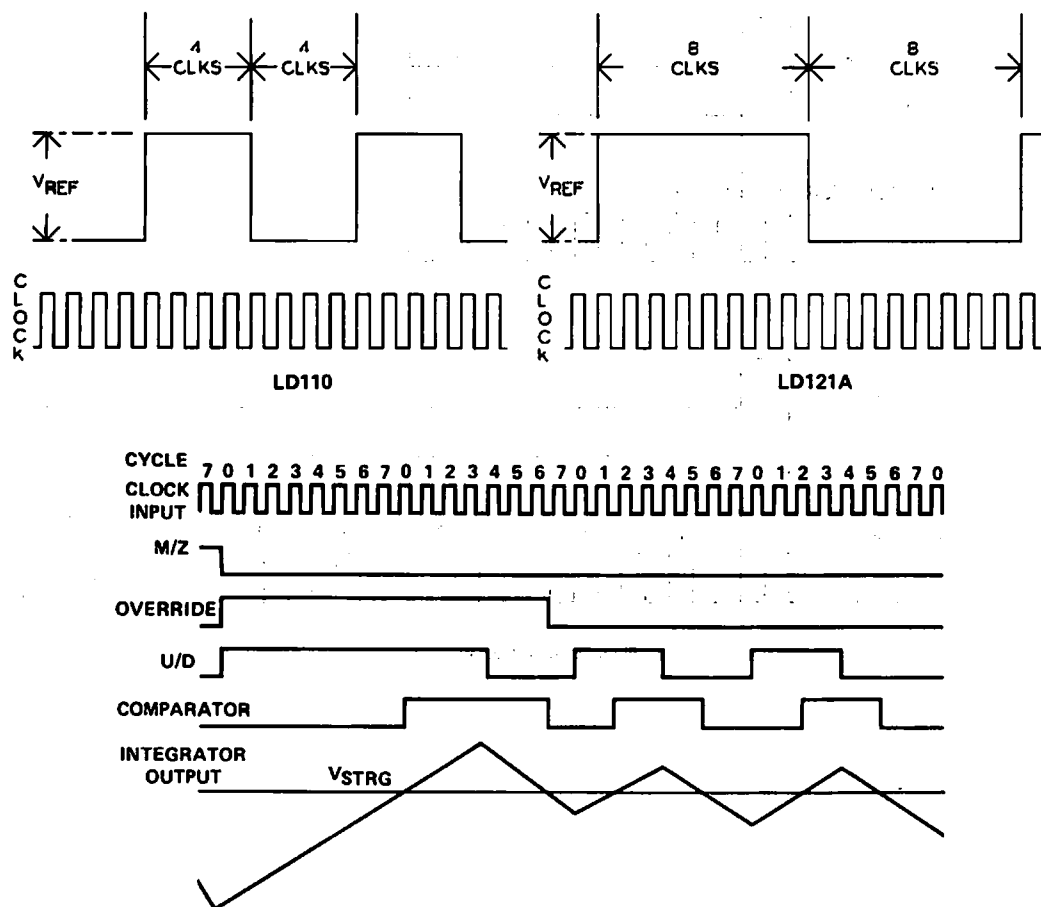


Figure 7
Auto-Zero Timing

In the measure interval, where we attempt to balance integrator charge, U/D is set in response to the state of the COMP input, so that the appropriate reference voltage will be fed back in the analog system. A counter automatically increments or decrements once every clock cycle, depending on the state of the U/D line, so that an accurate record can be kept of the net number of charge packets fed back. Ordinarily one would think that once every clock cycle the U/D would be set accordingly. However, since this technique is as dependent on timing as it is on feedback voltage level, we really have to be mindful of U/D

transitions since they bring with them error in the form of rise and fall time. One way around this problem is to insure that in every measure interval there is always the same number of U/D transitions, irrespective of the unknown, V_{IN} . This can be done by dividing the measure interval into an integral number of duty cycle periods in which the U/D line can assume 1 of 2 duty cycle waveforms. In the LD121A the duty cycle period consists of 16 clocks while it's 8 in the LD110. The 2 duty cycle waveforms possible in each 16 or 8 clock period is:

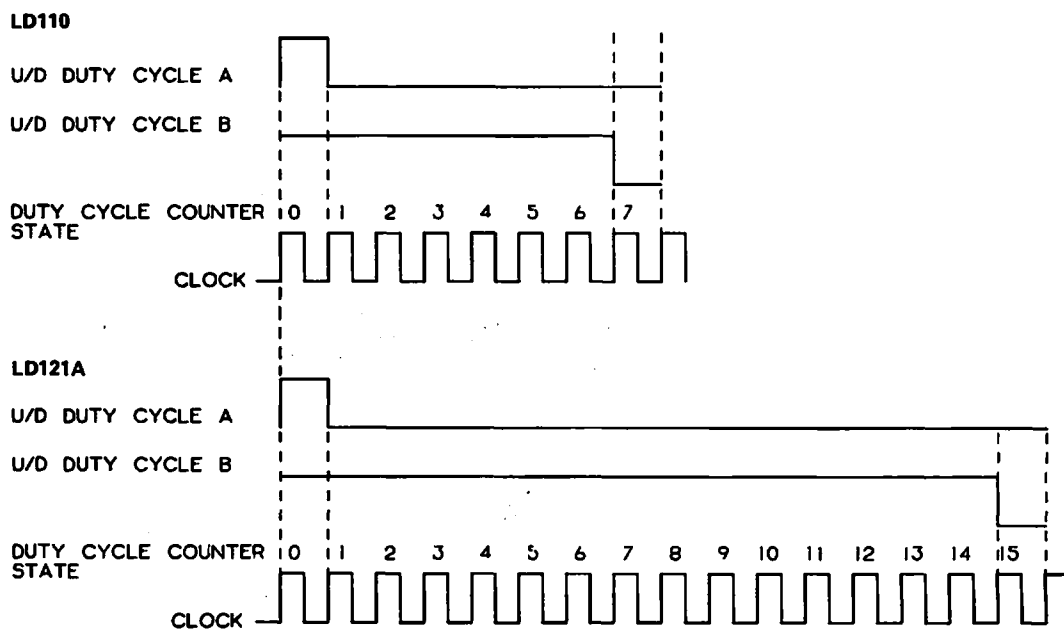


Figure 8 Duty Cycle Waveforms

So instead of depositing a maximum possible (± 16 or ± 8) charge packets every duty cycle period, we have to be content with a net maximum of ± 14 or ± 6 . Consequently the maximum counts possible are: LD110 = 3072, LD121A = 28,672. However, since these maximum counts are larger than the advertised precision of the A/D's, overrange capability is possible and built into some of the converters.

Since we can only feedback rather large lumps of charge (± 14 , ± 6 counts), when the measure interval comes to an end, there will, undoubtedly, be some residual charge left over to be resolved to the nearest count. This is done in a brief override period at the start of the A/Z interval where normal A/Z operation is temporarily inhibited while we fine tune (i.e. abandon duty cycles and feedback charge packets one at a time). The override period starts at the end of the measure interval when M/Z $\rightarrow$ low and the input buffer is switched to input 'gnd' so that no more charge is accumulated. The U/D line is set high and held until the comparator goes high and the next state 8 of the duty cycle counter comes around at which time U/D is set low. When the comparator next goes low again, the override period is ended (M/Z = 0, COMP = 0, U/D = 0, Auto-Zero switch closes initiating normal Auto-Zero action). The counter which until now has been faithfully keeping track of the charge packets fed back, is inhibited and its count used to update the data outputting latches on the next clock pulse. Figure 9 shows typical Measure, Override, and Auto-Zero waveforms in an LD120/LD121A system.

Now that the measurement algorithm has been described, a few words about the relationship

between the count and unknown input voltage are in order. What the count represents is the net number of reference charge units ($\pm \frac{V_{REF}}{2R_1} \frac{1}{f_{CLK}}$) which were needed to cancel out the charge as supplied by the unknown input

$$\left(\frac{V_{IN}}{R_2} \cdot \frac{\# \text{ clocks in measure interval}}{f_{CLK}} \right).$$

Neglecting signs, this equality is:

$$\text{COUNT} \cdot \frac{V_{REF}}{2R_1} \cdot \frac{1}{f_{CLK}} =$$

$$\frac{V_{IN}}{R_2} \cdot \frac{\# \text{ clocks in measure interval}}{f_{CLK}}$$

rearranging, this becomes:

$$\text{COUNT} = \frac{V_{IN}}{V_{REF}} \cdot \frac{R_1}{R_2} \cdot 2$$

(# clocks in measure interval).

For an LD121A with 32,768 clocks in the measure interval, this equality becomes:

$$\text{COUNT} = \frac{V_{IN}}{V_{REF}} \cdot \frac{R_1}{R_2} \cdot 65,536$$

By manipulating the resistor ratios and V_{REF} we could theoretically scale the A/D to any input voltage range desired. Practical circuit limitations, though, prevent us from getting carried away.

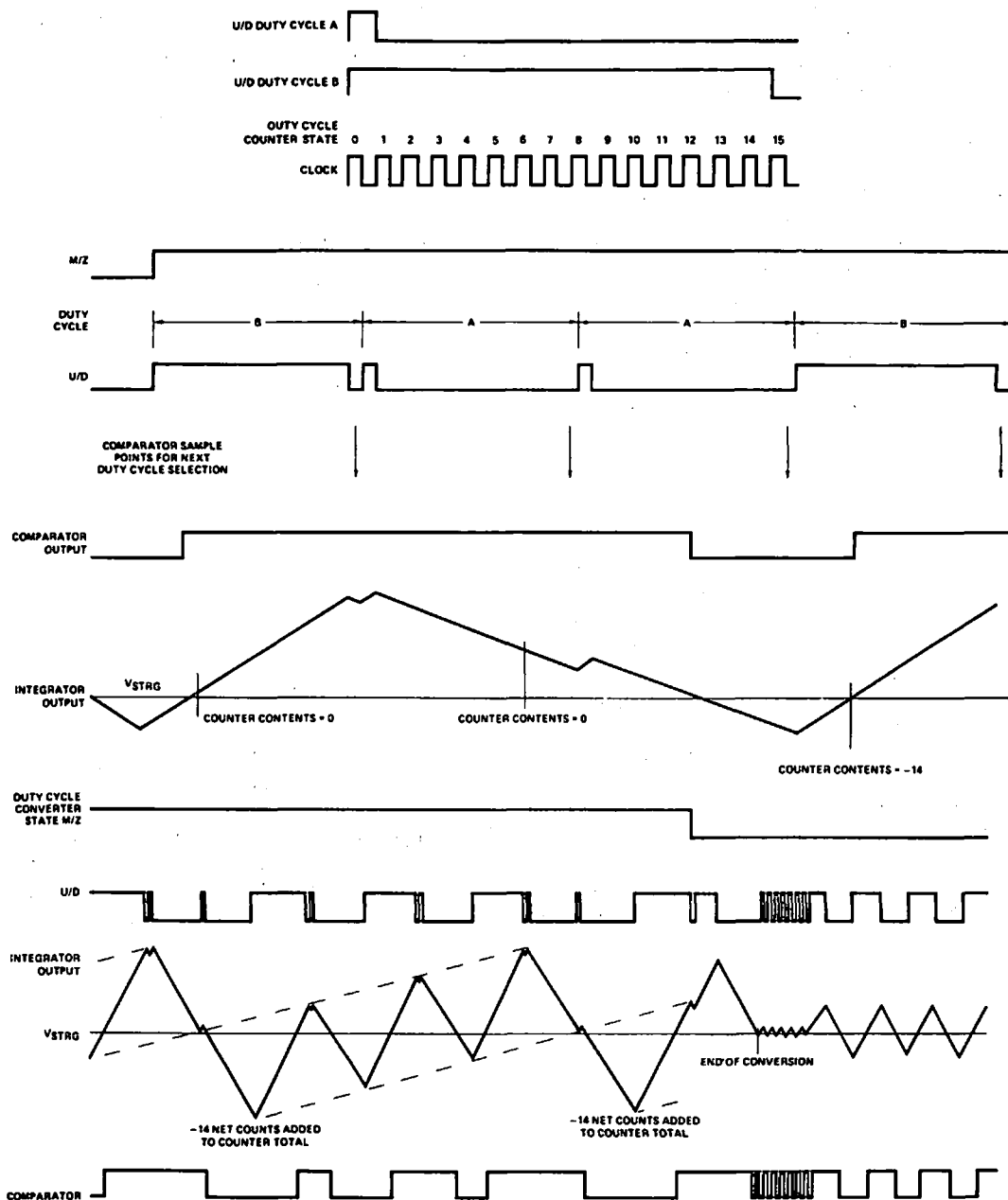


Figure 9. Up/Down and Integrator Waveforms

THE D469: AN OPTIMIZED CMOS QUAD DRIVER FOR MOSPOWER FET SWITCHES

Mark Alexander and Jim Harnden
November 1983

INTRODUCTION

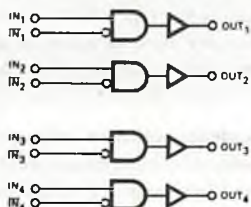
Many applications of power MOSFETs call for the devices to be used as on-off switches. While they can be directly driven by TTL or CMOS logic if moderate switching times are acceptable, to take full advantage of their high speed switching capabilities, a more robust driver is required. This driver should be able to provide at least 10 to 12 volts of gate drive at peak current of several hundred milliamps.

Until now, the only devices capable of driving MOSPOWER FETs in high speed switching applications were discrete bipolar devices or IC's such as National's DS0026 MOS clock driver. While the DS0026 can drive a 1000pF load with typically 20nS rise and fall times, it does suffer from some serious drawbacks that restrict its use. Being a bipolar device, it draws a fair amount of current quiescently (30mA) and also requires a large logical "1" input current (10mA). Because the DS0026 is configured internally as a dual inverting driver, two additional TTL inverters are required to make the part usable when non-inverting drive is required.

The DS0026 is unsuitable for use in many applications, particularly where the control logic is low-power CMOS. Its configuration as an inverting-only driver is also an inconvenience to the designer. Clearly a device that retains the high speed drive capabilities of the DS0026 but has none of its disadvantages is desirable.

Enter the D469 IC, which was designed as an optimized driver for MOSPOWER FET switches from the start. Internally it contains four independent drive channels, and each one can be configured as either a logically inverting or non-inverting driver (see Figure 1). Since it is a CMOS device, the D469 is compatible with low-power CMOS logic and microprocessors and draws very little current quiescently (2.5mA). Each of the D469's outputs can drive a 500pF load with typically 20nS rise and fall times and can be connected in parallel to drive larger capacitive loads if desired.

LOGIC DIAGRAM



PIN CONFIGURATION

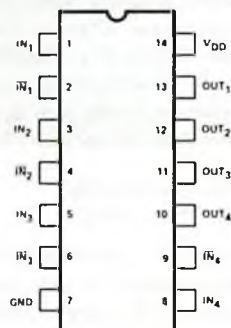
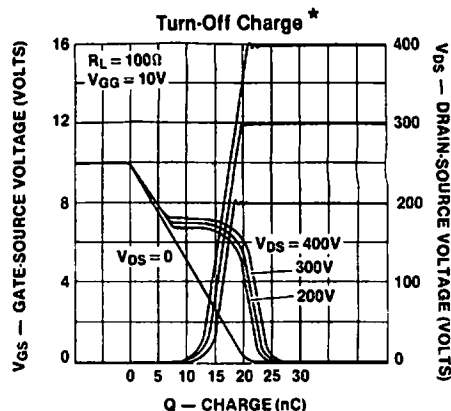
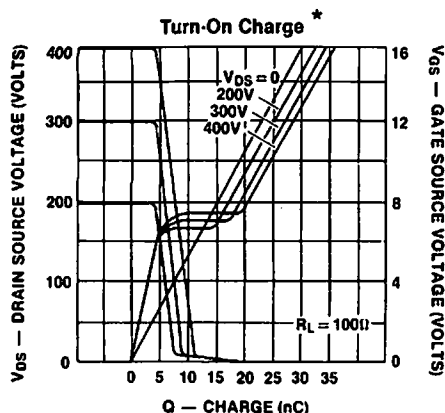


FIGURE 1

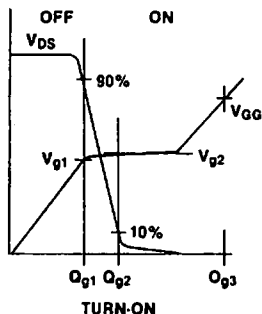
The block diagram of the D469 reveals that each channel can be configured as either an Inverting or non-inverting driver.



Switching Time Equations

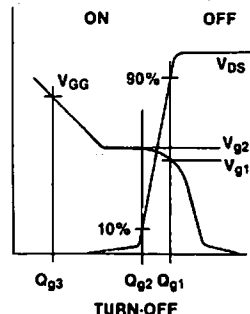
$$t_{d(on)} = \frac{Q_{g1}}{V_{g1}} R_{gen} \ln \left(\frac{V_{GG}}{V_{GG} - V_{g1}} \right)$$

$$t_r = \frac{Q_{g2} - Q_{g1}}{V_{g2} - V_{g1}} R_{gen} \ln \left(\frac{V_{GG} - V_{g1}}{V_{GG} - V_{g2}} \right)$$



$$t_{d(off)} = \frac{Q_{g3} - Q_{g2}}{V_{GG} - V_{g2}} R_{gen} \ln \left(\frac{V_{GG}}{V_{g2}} \right)$$

$$t_f = \frac{Q_{g2} - Q_{g1}}{V_{g2} - V_{g1}} R_{gen} \ln \left(\frac{V_{g2}}{V_{g1}} \right)$$



* VNDA
GEOMETRY

FIGURE 2

The charge transfer characteristics of a high-voltage power MOSFET show the occurrence of maximum input-capacitance ($C = dQ/dV$) at a gate-to-source voltage of approximately 7V.

This applications note introduces the charge transfer characteristics of a power MOSFET and shows that the D469 is very well suited to gate drive applications. A brief discussion of additional driver power dissipation due to gate current then follows. To prove that the D469 is a better choice than the DS0026 as a MOSFET gate driver, a comparative analysis between the two devices in switching time tests is performed. Finally, some applications of the D469 in DC motor drive circuitry are described.

THE D469 AND MOSFET CHARGE TRANSFER CHARACTERISTICS

Each of the four output drivers in the D469 has an output resistance of approximately 8 ohms and is capable of sinking or sourcing a peak current of 500mA. The output voltage swing at peak output current is then limited to 4 volts above and below the ground and V_{DD} rails respectively.

At a cursory glance, the limited output voltage swing at peak current might seem to be a disadvantage. However, if one examines the charge-transfer characteristics of some of the higher current power MOSFETs, it becomes apparent that the maximum input capacitance occurs at gate-to-source voltages in the region of 7V. These charge transfer characteristics are now included in all Siliconix data sheets. Figure 2 shows pertinent data for the VNDA type geometry.

The D469 is ideally suited to driving MOSPOWER FETs because its peak source and sink current capability occurs in the output voltage ranges of 0 to 8 volts and 12 to 4 volts respectively, with a 12 volt power supply. When used to drive common-source connected N or P channel MOSFETs, maximum drive current is available at the point of maximum input capacitance.

The currents that flow in a D469's output stage during charge/discharge cycles of the effective gate capacitance

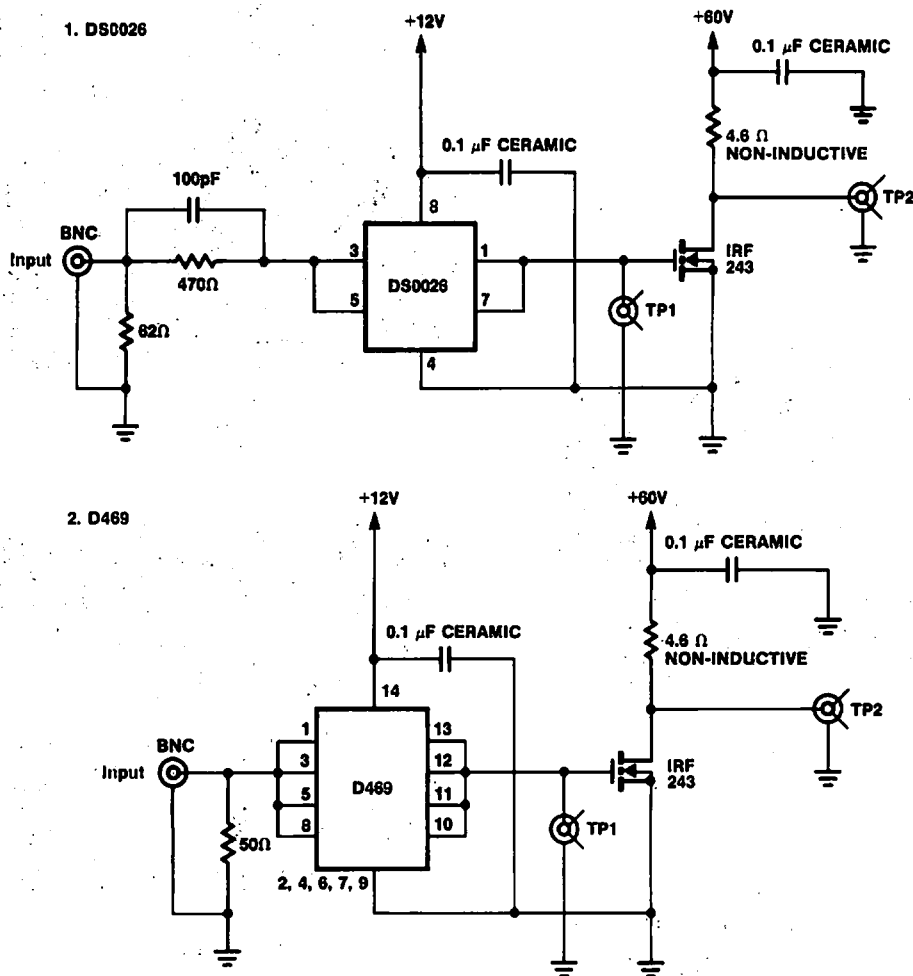


FIGURE 3

The schematic of the fixture used to perform the D469 versus DS0026 switching time tests.

cause additional power to be dissipated by the driver. Equation (6) of reference 2 shows that this power is proportional to the gate-drive voltage as well as the switching frequency. For switching frequencies below 100 KHz, the additional power dissipated by the driver is so low it can be neglected. However, when the switching frequency is above 500KHz and the gate-drive voltage is appreciable, the additional driver power dissipation cannot be neglected. It should be calculated and added to the DC power dissipation of the driver. This value can then be used to determine if the operating junction temperature of the driver is within the maximum data sheet limits.

A COMPARATIVE ANALYSIS THE D469 vs. THE DS0026 IN SWITCHING TIME TESTS

D469 and DS0026 IC's were incorporated into a test fixture, driving identical power MOSFETs with identical loads. Figure 3 shows the schematic diagram of this fixture. The power MOSFETs used were Siliconix IRF243s with typical gate-to-source capacitance of 1600pF and drain-to-gate capacitance of 300pF. The load resistance for both MOSFETs was approximately 4.6 ohms (non-inductive), and the power-supply voltage was 60V. Both the DS0026 and D469 were powered from a separate 12 volt power supply and driven by a TTL level pulse train. The pulse train had a pulse width of 150nS and a repetition rate of 1KHz.

10

Since the DS0026 contains two independent drivers and the D469 four, a fair test would be to compare the two devices as dual drivers. Thus, two D469 outputs were paralleled and compared to a single DS0026 output in drive capability. Figures 4 and 5 indicate that on a "per chip" basis the D469 was essentially the equal of the DS0026. To be precise, the D469 waveform's rise and fall times were 36nS and 44nS respectively while the DS0026's were 26nS and 42nS. It appears that the DS0026 was somewhat faster (by 10nS) on the rising edge of its waveform than the D469 was, but both had very similar fall times.

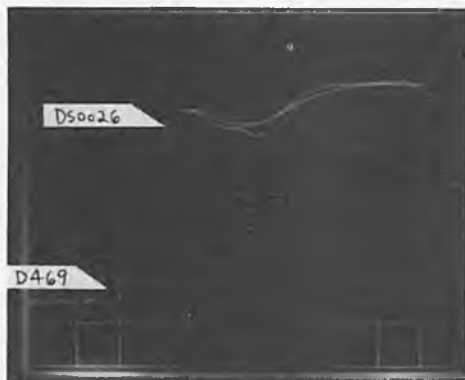


FIGURE 4

The rise time of 2 paralleled D469 outputs versus 1 DS0026 output is shown in this photograph. (VERT: 2.4V/Div, HORIZ: 20 nS/Div)



FIGURE 5

The fall time of 2 paralleled D469 outputs versus 1 DS0026 output is shown in this photograph. (VERT: 2.4V/Div, HORIZ: 20 nS/Div)

Some further tests were conducted to see how the D469 with two or more outputs connected in parallel compared to the DS0026 with both of its outputs connected in parallel.

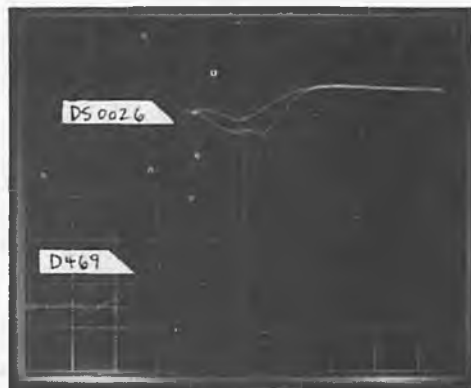


FIGURE 6

The rise time of 4 paralleled D469 outputs versus 2 DS0026 output is shown in this photograph. (VERT: 2.4V/Div, HORIZ: 20 nS/Div)

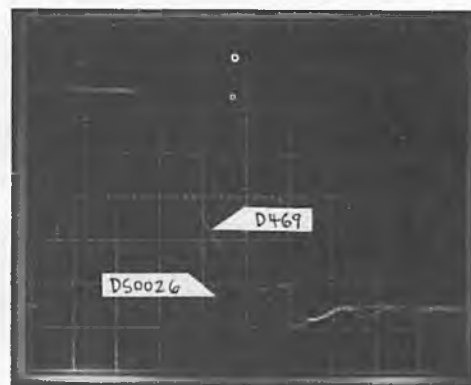


FIGURE 7

The fall time of 4 paralleled D469 outputs versus 2 DS0026 output is shown in this photograph. (VERT: 2.4V/Div, HORIZ: 20 nS/Div)

Figures 6 and 7 show the rise and fall times of the D469 with four outputs in parallel versus the DS0026 with two outputs in parallel. Here it can be seen that the DS0026 with rise and fall times of 22nS and 30nS respectively was still the faster of the two - but not by much. The D469 came in a very close second with rise and fall times of 32nS and 42nS respectively. Interestingly enough, the rise and fall times of the D469 with four outputs connected in parallel were virtually the same as those with two outputs in parallel. The rise and fall times for the DS0026, on the other hand, showed some improvement.

The main difference observed between the D469 and the DS0026 was the propagation delay-time each device exhibited. For the D469 this parameter was approximately 50nS while that of the DS0026 was in the range of 5 to 10nS. Figure 8 clearly shows this difference. It should be

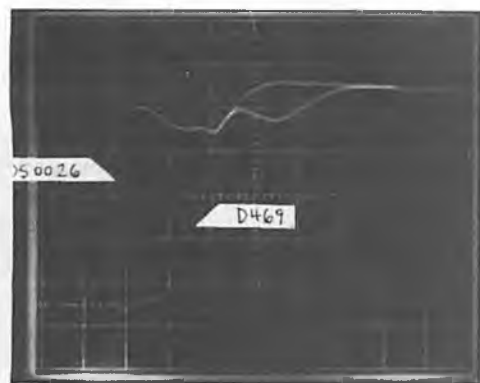


FIGURE 8

The 50 nS difference in propagation delay between the DS0026 and the D469 is clearly seen photograph. (VERT: 2.4V/Div, HORIZ: 20 nS/Div)

noted that Figure 8 is the only one in which the difference in propagation delay is shown. Figures 4 to 7 do not show this because it is easier to compare switching waveforms when the oscilloscope traces are overlaid with one another.

SUMMARY

In summarizing the results of this comparative analysis, we can say that the D469 is really a DS0026 in a "CMOS disguise". Although the DS0026 was faster than the D469 in both cases, its speed advantage was no more than about 10nS in any of the rise and fall time tests. As a 2-channel driver the D469 is the obvious choice especially when one considers its power consumption compared to the DS0026. In the test fixture shown in Figure 2, the DS0026 drew an average supply current of 30mA and thus consumed about 360 mW of power while the D469 drew slightly more than 2 mA and consumed about 25mW of power. Needless to say, the DS0026 ran quite hot to the touch while the D469 was cold. The 50nS propagation delay of the DS469 should not pose any problem if all the MOSFETs in a particular circuit are driven by D469s.

APPLICATIONS OF THE D469 QUAD DRIVER

The D469 quad driver is well suited to applications such as DC motor control. Motors ranging in size from fractional up to several horsepower can be directly driven with power MOSFET devices, if they are provided with suitable gate drive. The D469 fulfills the gate-drive requirements and provides the interface between the MOSFETs and low-power CMOS or TTL control logic.

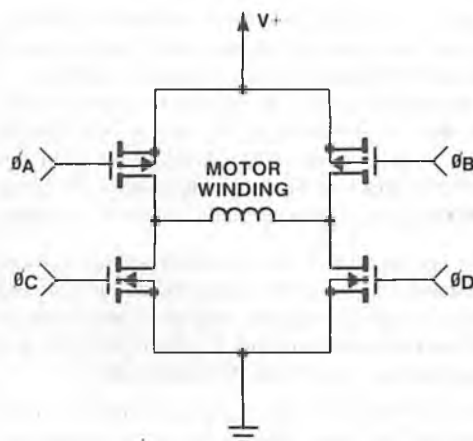


FIGURE 9

A bipolar H-bridge motor drive circuit using N and P-channel MOSFETs.

Figure 9 shows a typical "H-bridge" motor drive circuit in which the winding current flow is bidirectional. N-channel MOSFETs are invariably used in the lower legs of the bridge since they can be directly driven by the D469. In the upper legs of the bridge, both N and P-channel devices can be used. In each case, driving the upper MOSFETs presents a problem that is common to a number of applications other than motor drives. The problem is that the upper MOSFET switches which control the positive power supply to the load cannot have their gate-drive voltage referenced to ground.

When the P-channel MOSFETs are used as the upper switches, their source terminals are connected to the positive power rail. The gates of these MOSFETs are then driven 10 to 12 volts below the positive rail to turn them on. Because the gate drive is always referenced to the positive rail, the gates of the N and P channel MOSFETs in each half of the bridge can be driven directly by the D469 if the power supply voltage is 14V or less. Operation at higher supply voltages, however, requires that the P-channel devices be isolated in some fashion from the D469 which is ground referenced.

The isolation problem crops up again if N-channel MOSFETs are used as the upper switches in the bridge. Since their source terminals are connected to the load, one can see that the gate waveforms must swing to at least 10 or 12 volts above the positive rail if they are to turn on completely. Also, when either of the lower N-channel MOSFETs is conducting, the respective upper N-channel device must be off or cross-conduction will occur. To prevent this, the gate-to-source voltage of the upper

MOSFET must be zero when the respective lower MOSFET is on and vice versa. This means that the gate-voltage of the upper N-channel devices must swing from the $R_{DS(on)}$ voltage drop of the lower MOSFETs all the way to 10 or 12 volts above the positive rail. Even with a 12 volt power supply, the gate voltage swing is almost 24 volts, and thus the D469 cannot be used to directly drive the upper MOSFETs. Again, some form of driver isolation is required.

There are many methods of providing isolation between the D469 and the gates of the upper MOSFETs when using elevated supply voltages. As may be expected, certain methods will work better with N-channel MOSFETs, and others will work better with P-channel devices.

Three methods of providing gate-drive isolation will be considered. Two of them provide DC isolation between the D469 and the gates of upper MOSFETs while the third provides isolation between a floating D469 and the control-logic inputs.

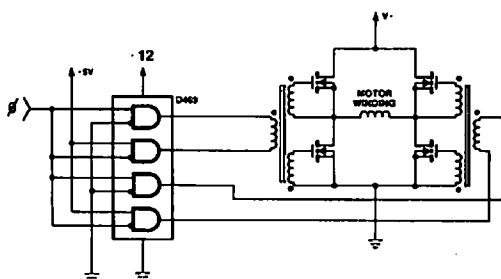


FIGURE 10

An all N-Channel H-bridge drive using transformer isolation.

a. Transformer Isolated Gate Drive

Figure 10 shows an all N-channel H-bridge motor drive using transformer isolation between the D469 and the gates of both the upper and lower MOSFETs. Each transformer is driven by an AC waveform generated by two D469 driver channels

In many cases the transformer will prove to be one of the most compact, least expensive and simplest methods of isolation to implement. It also works well with either N or P-channel MOSFETs in the upper half of the bridge.

However, there is a drawback with this method. The interwinding capacitance of the isolation transformers allow noise spikes appearing at the MOSFET gates to be coupled back to the D469 and cause possible damage. Care must be taken to ensure that any transients coupled back to the driver are of sufficiently low magnitude such that no damage is done. They can be minimized by the inclusion of a Faraday shield between the primary and secondary windings of the isolation transformer.

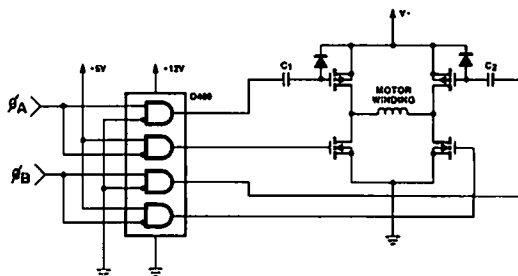


FIGURE 11

An H-bridge drive using capacitive isolation for the P-channel MOSFETs.

b. Capacitor Isolated Gate Drive

A capacitor isolated N and P-channel H-bridge motor drive is shown in Figure 11. In this circuit, only the P-channel MOSFETs are isolated from the D469; the N-channel devices are driven directly. The diodes are included to clamp positive gate-to-source transitions on the P-channel MOSFETs to +0.7V.

This method of isolation is even more compact and less expensive than that using transformers. Although a coupling capacitor several times the effective input capacitance of the P-channel MOSFETs is required, it is still small and inexpensive. This method does have the drawback of coupling noise spikes appearing at the MOSFET gates back to the outputs of the D469. Also capacitor isolation does not work well with N-channel MOSFETs in the upper half of the bridge. This is because the sources of the upper N-channel MOSFETs are not connected to an AC ground (such as the positive supply rail). Thus, there is no fixed reference for the AC coupled signal on the MOSFET side of the capacitor.

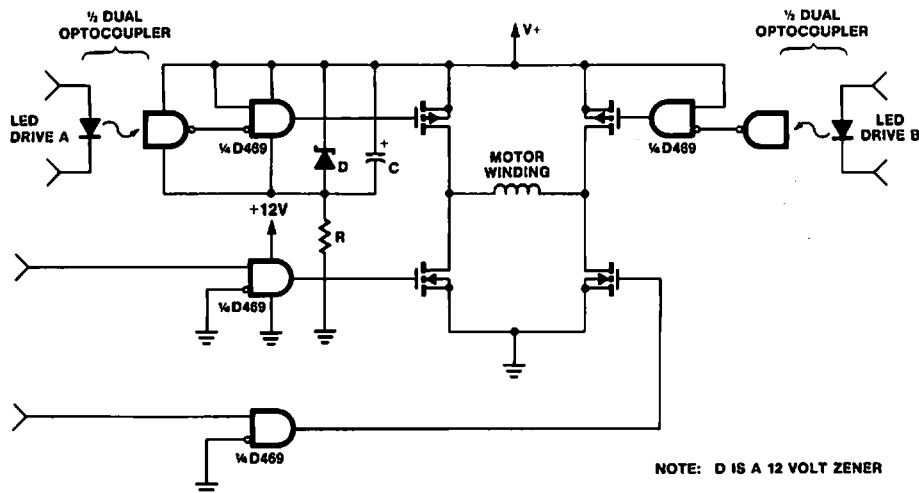


FIGURE 12

A different method of isolation: floating a D469 driver and optically coupling the logic drive for the P-channel MOSFETs.

c. Floating D469 With Opto-Isolated Logic Inputs

Figure 12 shows a different method of providing isolation, namely referencing a D469 driver to the positive power rail and using an opto-coupler to provide the DC isolation between it and the low-voltage control logic. A +12V power supply, referenced to the positive rail, is generated for the D469's ground pin with a zener-diode, capacitor and resistor. The D469 thus provides gate-drive waveforms to the P-channel MOSFETs that swing from the positive rail to 12 volts below it. If the reservoir capacitor C is made large enough, it will be able to supply enough charge to the D469 for transfer to the gates of the MOSFETs. This ensures that the upper MOSFETs will have fast switching times.

Although this circuit is more complex than the previous ones, DC operation of the motor coils is provided if so required. Since the upper D469 floats with respect to the positive power rail, any noise transients on this rail will not affect the operation of the driver or be coupled back to the logic inputs. This method has the disadvantage of being difficult to implement with an all N-channel bridge. The large voltage swing required at the gates of the upper N-channel devices precludes the use of the circuit in this case.

In summarizing this look at motor drive circuits using the D469 as a gate driver, one can see that if the correct methods of isolation are used then the D469 certainly simplifies the task of interfacing logic circuitry to a DC motor.

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1. Ed Oxner, Siliconix, Inc., "Correlating the Charge Transfer Characteristics of Power MOSFETs with Switching Speed". *Proceedings of Powercon 9*, H-4 pages 1 to 5, 1982.
2. Rudy Severns, INTERNATIONAL RECTIFIER, Inc., "Simplified HEXFET Power Dissipation and Junction Temperature Calculation Speeds Heatsink Design". *IR HEXFET Catalog*, 1980. Page A-80 to A-86.
3. Siliconix, Inc., *D469 Data Sheet*, May 1983.
4. NATIONAL SEMICONDUCTOR CORP. *DS0026 Interface Data Book 1980*, Pages 6-10 to 6-16.

SWITCHING HIGH-FREQUENCY SIGNALS WITH FET INTEGRATED CIRCUITS

Revised December 1984

INTRODUCTION

A number of available integrated circuits employing FET switches with their associated drivers can be used to switch high-frequency signals with greater convenience than other types of RF switches, such as PIN diodes or electromechanical devices. Wideband RF signals, to 100 MHz, can be switched with excellent OFF isolation and small ON insertion loss. FET analog switches also permit direct interface with 5 V computer logic, including TTL and CMOS. No external interface elements are required. FET analog switches have high reliability, long life, low power dissipation, and are quite small. Attractive DC properties of these devices include very low leakage, zero offset voltage, and large signal voltage ranges.

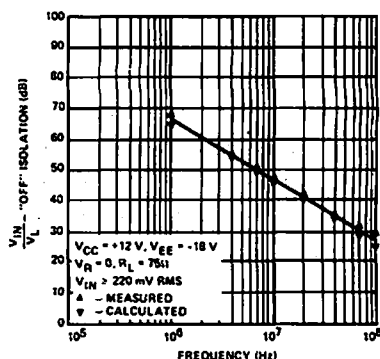
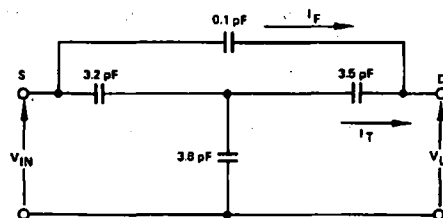
Effective RF switching concerns the control of RF signals, and not high-speed switch actuation. The point of major interest is switch RF performance in the static OFF and ON states. A number of standard FET analog switches can qualify as good RF switches; four specific types will be used as examples, since each type represents a different IC structure. Typical devices include the DG133, an N-channel junction FET switch with bipolar driver; DG172, a P-channel MOS FET switch with PMOS/bipolar driver; DG181, an N-channel junction FET switch with PMOS/bipolar driver; and the DG200A, a monolithic CMOS switch with CMOS driver. However, the DG180-190 series and the DG200-201A take advantage of newer technologies and therefore have the best performance/cost tradeoff available.

Elements of OFF Isolation

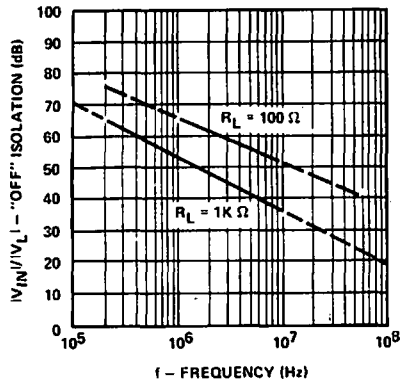
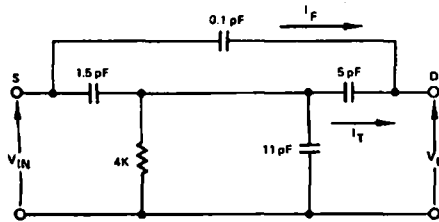
Most RF applications involving high-frequency switching are frequency-limited due to reduction in OFF isolation, rather than to degradation in ON performance. Generally, the quality of OFF isolation depends on three factors: selection of the appropriate analog switch, the magnitude of load resistance, and the amount of external stray (wiring) capacitance present in the circuit. Usually two of these elements can be controlled by the circuit designer, i.e., switch selection and stray capacitance.

Probably the most important factor affecting OFF isolation is selection of the appropriate analog switch. As a rule, information available to the designer in the form of product specifications does not provide OFF isolation data in sufficient depth to make switch selection easy. There are three major actions which may be taken to overcome this lack of data. They include measurement of actual isolation performance (see footnote, page 2); analysis of equivalent circuits to predict isolation (see Appendix); and simplification of the analysis to produce a useable set of design aids.

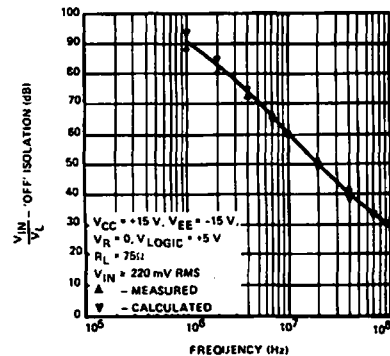
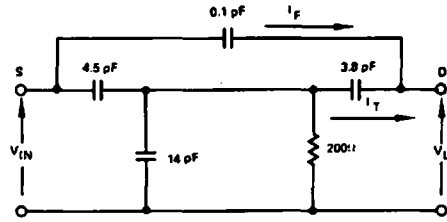
Measured data, calculated data, and equivalent circuits are presented in Figures 1 through 4.



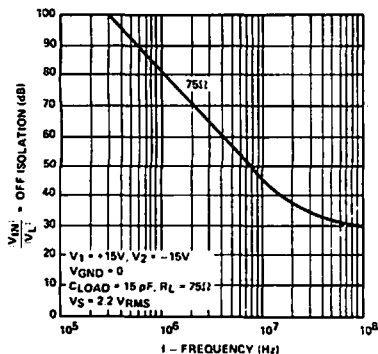
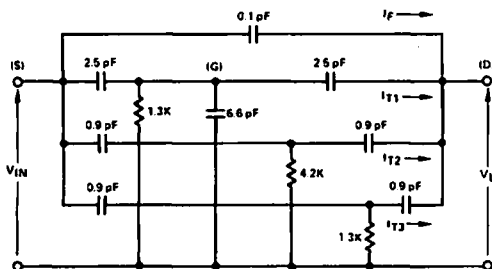
DG133 Equivalent Circuit and OFF Isolation Data
Figure 1



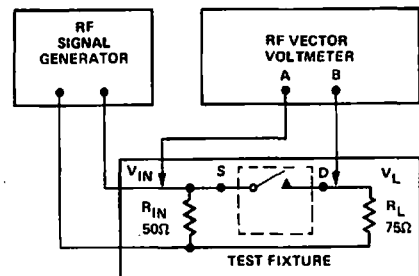
DG172 Equivalent Circuit and OFF Isolation Data
Figure 2



DG181 Equivalent Circuit and OFF Isolation Data
Figure 3



DG200A Equivalent Circuit and OFF Isolation Data
Figure 4



Isolation Test Circuit
Figure A

*Data was taken for each switch in a special test fixture (Figure A). In the test fixtures, inputs were shielded from outputs, and RF decoupling was provided on all DC connections. Great care was taken in the mechanical layout of fixtures, to minimize stray capacitance. The characteristic impedance of video transmission lines, 75 Ω, was issued as the value of load resistance. Voltage measurements were made with an RF vector voltmeter, H/P Model 8405A.

Plots of switch OFF isolation vs frequency performance are quite similar. OFF isolation reduces with increasing frequency at rates from 20 dB to 40 dB per decade. A small capacitance in series with R_L has a similar response, except that the OFF isolation reduces at a fixed rate of 20 dB per decade. If the equivalent circuit models of Figures 1 through 4 are replaced with a single capacitance, $|C_{Eq}|$, (which varies uniquely with frequency for each switch structure) the rather formidable equivalent circuits can be ignored. (See Appendix for discussion of $|C_{Eq}|$).

An additional capacitance path from input to output is through C_{STRAY} .

To show the magnitude of a potential source of capacitance, two parallel conducting strips were etched on a piece of 2-oz. copper-clad terminal board. The strips were 50 mils wide, with 100 mils center-to-center separation (which is essentially the same spacing as adjacent leads in a TO-116 dual in-line package). Measured strip-to-strip capacitance was 0.9 pF per inch. It is obvious that stray capacitance is the direct result of circuit layout. Because of the dramatic influence of stray capacitance in OFF isolation, great care must be taken in the layout of PC boards in a circuit (see Appendix for example).

In Figure 5, a graphic design aid (derived from the simple $|C_{Eq}|$ model) is presented to simplify the analysis of OFF isolation in a variety of analog switches and resistive loads. Since C_{Eq} is dependent somewhat on R_L , this design aid is only approximate for $R_L > 150 \Omega$.

In Figure 5, only those RF signals of a sinusoidal nature are considered. Certain other signals, such as video, may be more conveniently viewed as having a pulse characteristic. Thus Figure 5 is modified as Figure 6 to yield a design aid useful in making analyses of pulse isolation.

Crosstalk

Crosstalk is also of concern to the RF circuit designer. Crosstalk is basically channel-to-channel isolation, and may be analyzed with the tools presented in Figure 5 and 6. It occurs in either of two circuit configurations.

The first instance (Figure 7A) comes about when several switches are arranged in a circuit to feed a common load (or when one signal source is used to feed multiple loads). The total effect of crosstalk from Switch 1 to Switch 2 is found by summing I_L' (due to isolation parameter of Switch 1) with I_C (the capacitive coupling between Switch 1 and Switch 2). If C_{STRAY} is small, then the crosstalk effect will be negligible. C_{STRAY} must be minimized with the same care indicated for C_{STRAY} .

The second configuration (Figure 7B) includes loads which are independent of one another. In this case, the major coupling from Switch 1 to the output of Switch 2 is through C_{STRAY} . In general, the crosstalk generated by the circuit in Figure 7B should be less than that which occurs in Figure 7A.

Actual RF Switching Application

How well does a high-performance RF switch work in an actual application? Figure 8 is a block diagram of a switching circuit which controls a video monitor. The video signal is switched ON and OFF by a DG190, a 2-channel SPDT member of the DG181 family. Then a 75 Ω attenuator was cycled between 0 dB and 40 dB. Results of the experiment are shown in Figures 9 through 13, with attenuation occurring at 0 dB, 20 dB, and 40 dB.

For an even more critical switch application, consider switching a monitor between two cameras in a high-resolution closed-circuit TV system. Each camera has a signal bandwidth of 32 MHz, and a signal-to-noise ratio of 30 dB. OFF isolation must be at least 36 dB to prevent more than 1 dB degradation of the system signal-to-noise ratio. The resistive load, R_L , is 75 Ω .

The technique for selection of the proper switch for such an application, using the graphic design aid presented in Figure 5, is as follows:

- (1) From Figure 5A, required $R_L \times C_I$ is approximately 80 Ω - pF.
- (2) Dividing by R_L , $C_{I(max)}$ is determined to be 1.06 pF.
- (3) Planned C_{STRAY} , using careful board layout, is ≤ 0.2 pF. Thus $|C_{Eq}| \leq 1.06 \text{ pF} - 0.2 \text{ pF} = 0.86 \text{ pF}$.
- (4) Transfer this value of $|C_{Eq}|$ to Figure 5B. It is apparent that the only available switch which will satisfy the maximum capacitance criteria is a DG181, with $|C_{Eq}| = 0.59 \text{ pF}$.
- (5) Having selected the DG181 as the proper switch, one now works backward on the design aid to predict an OFF isolation of 38 dB.

The example illustrated requires the best FET switch (DG181) and fairly small C_{STRAY} . If the same degree of OFF isolation is required with a larger R_L , or a higher operating frequency, multiple switches must be used.

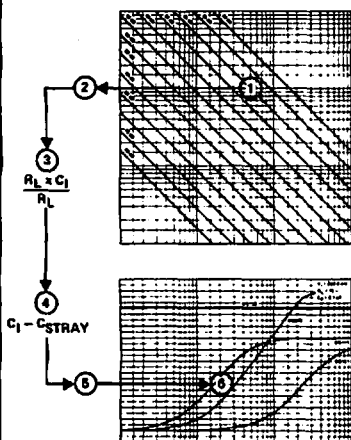
Several multiple switch configurations may be used to achieve an impressive increase in OFF isolation under otherwise difficult conditions. The simplest multiple switch configuration is the shunted load, shown in Figure 14.

The load resistance, R_L , is shunted by a second switch, S_2 , which operates out of phase with the primary switch, S_1 . This has the effect of reducing R_L to r_{DS2} . Switch ON characteristics are not affected. This configuration should be used only when the load can be shunted without introducing unwanted side effects.

Probably the most effective multiple switch configuration is the tee, which is shown in Figure 15. In the tee, S_2 operates out of phase with S_1 and S_3 , and provides two stages of isolation. The input to S_3 is the isolation leakage of S_1 working into an $R_L = r_{DS2}$. This multiple switch arrangement can bring about a considerable degree of OFF isolation, but only at the expense of doubling switch ON resistance, which increases the ON insertion loss.

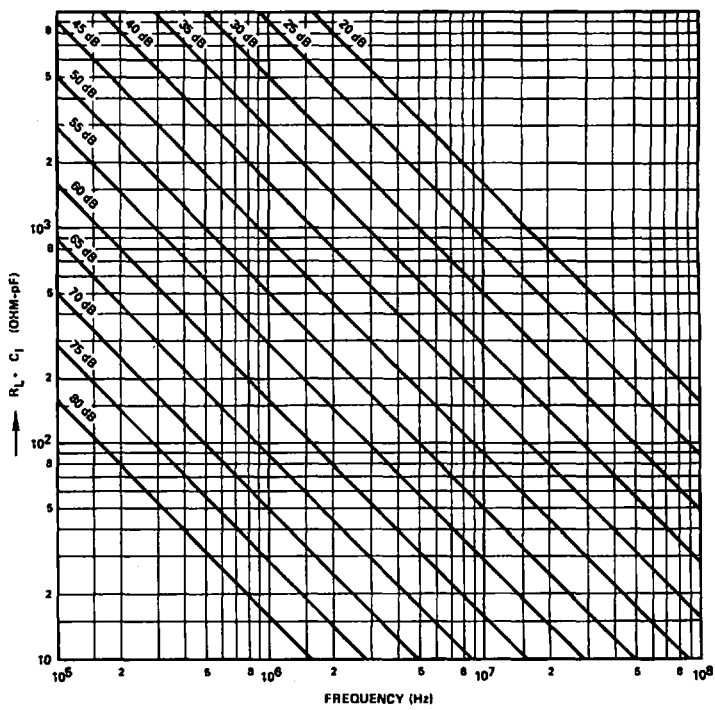
HOW TO USE:

- (1) Find required OFF isolation⁽¹⁾ at required frequency on Figure 5A
- (2) Find $R_L \times C_I$ on vertical axis of 5A
- (3) Divide $R_L \times C_I$ by R_L to obtain C_I
- (4) Subtract C_{STRAY} from C_I to obtain $|C_{Eq}|$
- (5) Find $|C_{Eq}|$ on vertical axis of Figure 5B
- (6) Locate intersection of $|C_{Eq}|$ with required frequency on 5B
- (7) Select switch below or to the right of intersection of $|C_{Eq}|$ and f on 5B. If no switch is shown, multiple switches must be used.

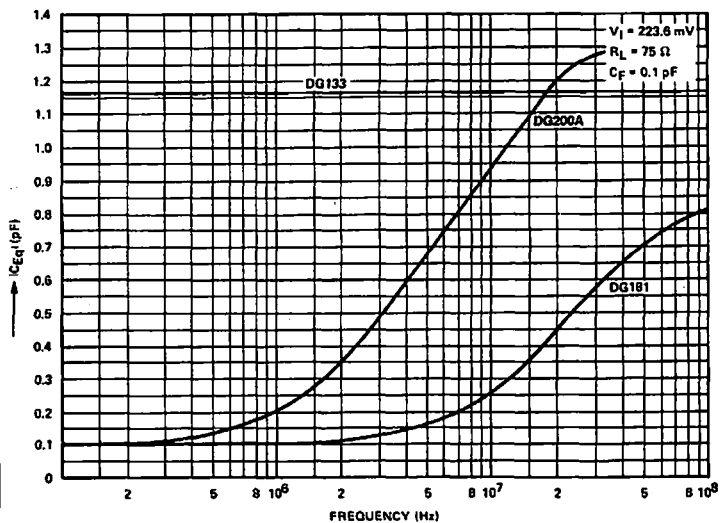


NOTES:

1. $OFF\ ISO = 20 \log \frac{V_{IN}}{V_L}$
 2. V_{IN} is voltage at switch input terminals
- DG172 did not transfer to this curve.



(A)

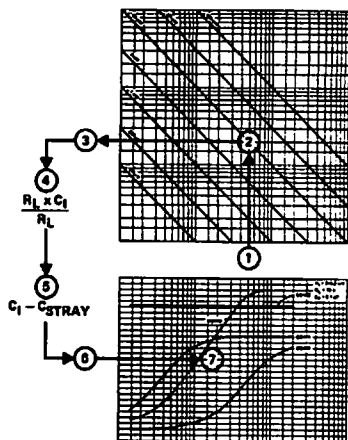


(B)

Isolation Design Aid (Sinusoidal Signals)
Figure 5

HOW TO USE:

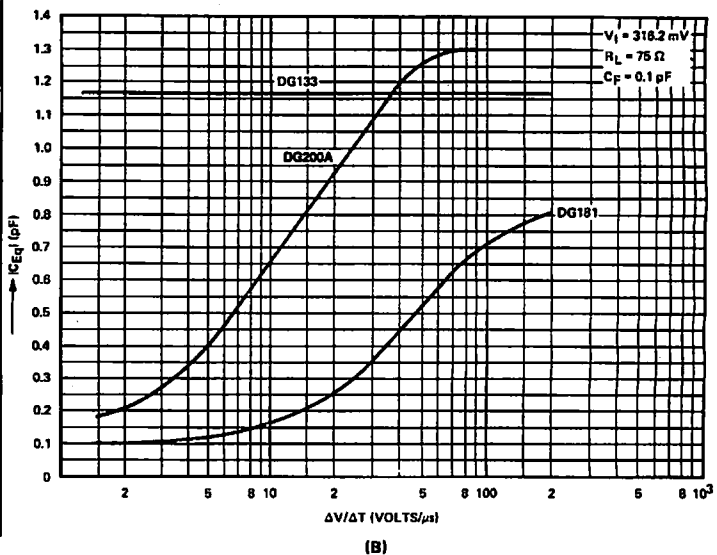
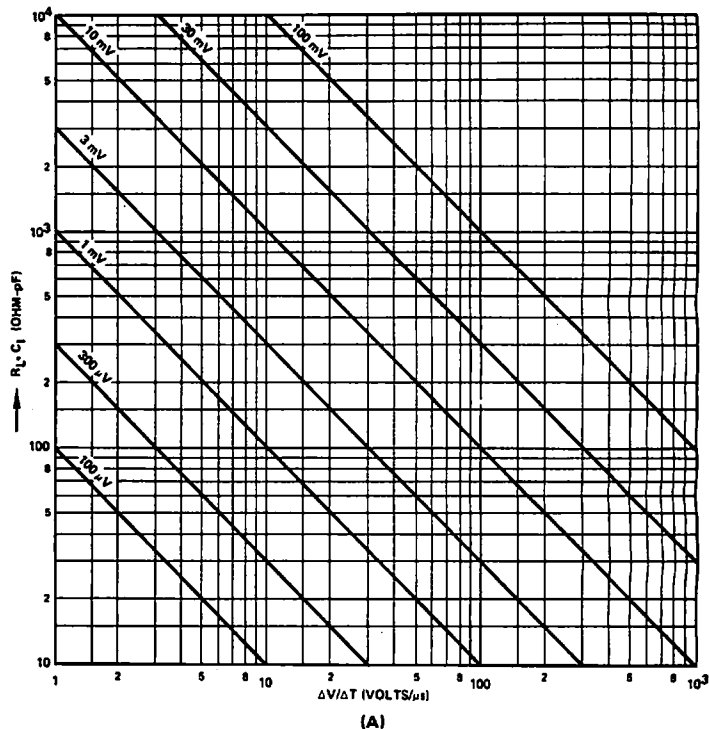
- (1) Determine $\frac{\Delta V^{(1)}}{\Delta T}$ of input pulse
- (2) Find required maximum peak pulse output at $\frac{\Delta V}{\Delta T}$ on Figure 6A.
- (3) Find $R_L \times C_1$ on vertical axis of 6A.
- (4) Divide $R_L \times C_1$ by R_L to obtain C_1
- (5) Subtract C_{STRAY} from C_1 to obtain $|C_{Eq}|$
- (6) Find $|C_{Eq}|$ on vertical axis of Figure 6B
- (7) Locate intersection of $|C_{Eq}|$ and $\frac{\Delta V}{\Delta T}$ on 6B
- (8) Select switch below or to right of intersection on 6B. If no switch is shown, multiple switches must be used



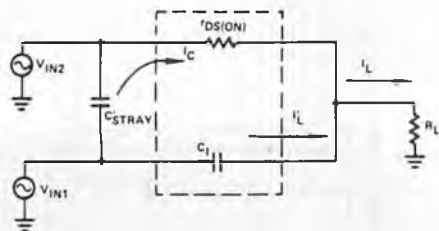
NOTE:

$$1. \frac{\Delta V}{\Delta T} = \frac{V_{PEAK}}{\Delta T}$$

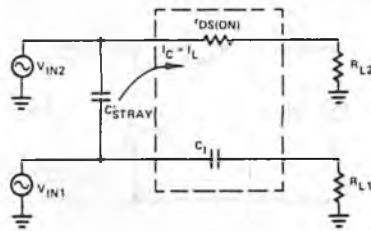
DG172 did not transfer to this curve.



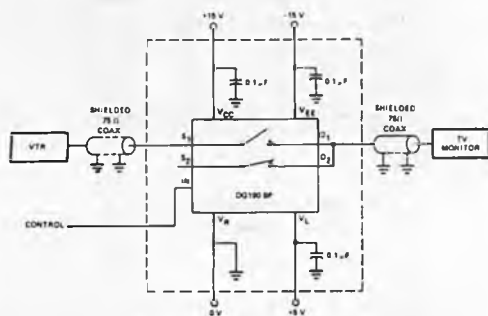
Isolation Design Aid (Pulse Signals)
Figure 6



Crosstalk with a Common Load
Figure 7A



Crosstalk with Independent Loads
Figure 7B



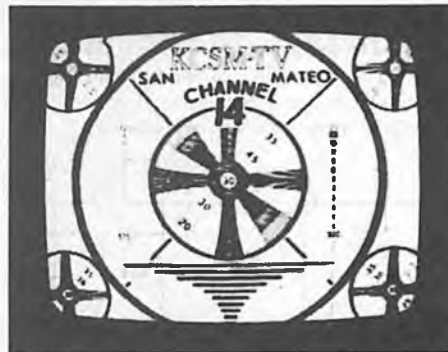
Video Switch Block Diagram
Figure 8



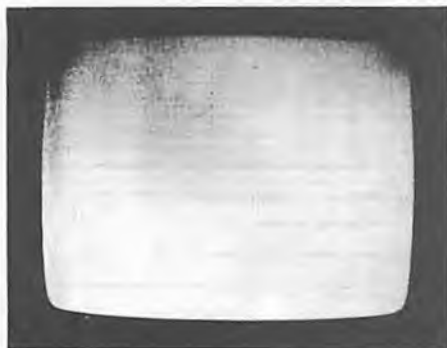
Switch ON
Figure 9



Switch OFF
Figure 10



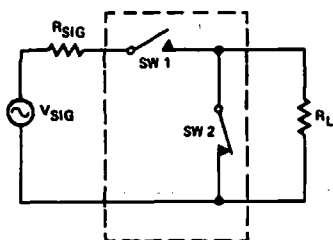
Attenuation = 0 dB
Figure 11



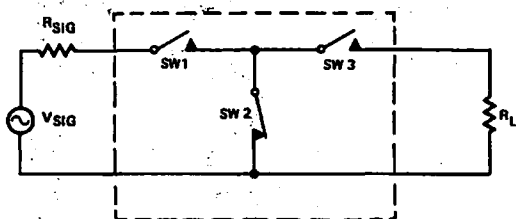
Attenuation = 40 dB
Figure 12



Attenuation = 20 dB
Figure 13

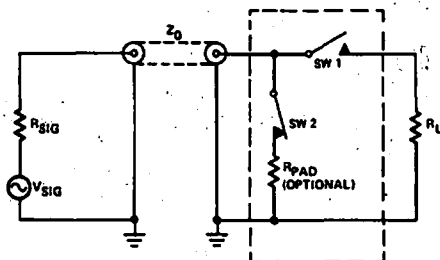


Shunted Load for Isolation Improvement
Figure 14



TEE for Isolation Improvement
Figure 15

A third multiple switch arrangement may be used to improve OFF isolation if the input signal is presented to the switch via a transmission line. The input impedance of an OFF switch is essentially infinite. The result of this condition is a reflection coefficient of 1, which means that the switch input voltage is twice as large as the voltage at the signal source. This switch configuration is shown in Figure 16, where the additional switch, S_2 , operates out of phase with the primary switch, S_1 , to terminate the transmission line.



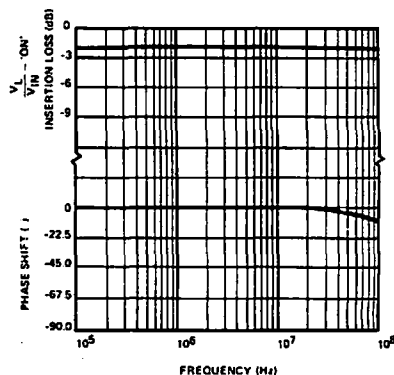
Transmission Line Isolation Improvement
Figure 16

A padding resistor, R_{PAD} , can be used to assist in matching the characteristic transmission line impedance Z_0 . The value of R_{PAD} can be determined from the term $Z_0 \cong r_{DS2} + R_{PAD}$. Note that the reflection coefficient is now nearly zero, and thus the switch input voltage is approximately equal to V_{SIG} .

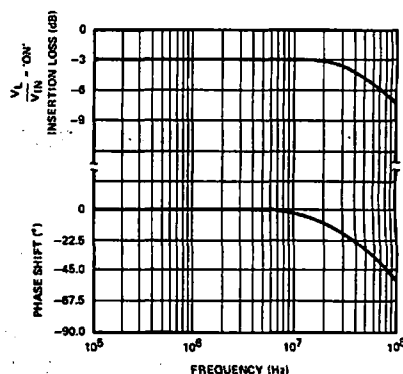
"ON" Switch Characteristics

Behavior of the switch in the ON condition is simple. ON performance is essentially independent of frequency for any load capacitance likely to be used. The ON resistance, $r_{DS(on)}$, causes an insertion loss which is basically constant; phase shift is negligible.

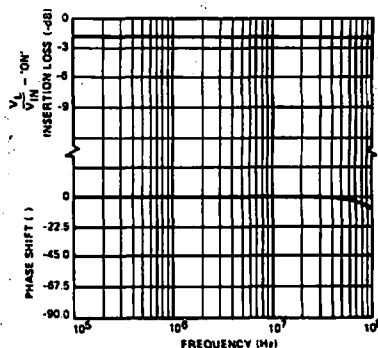
With the test fixture described in Figure A, measured ON performance was observed as shown in Figures 17 through 20.



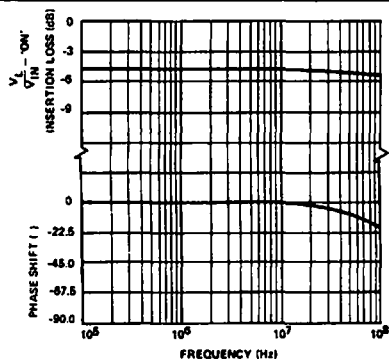
DG133 ON Performance
Figure 17



DG200A ON Performance
Figure 18



DG181 ON Performance
Figure 19



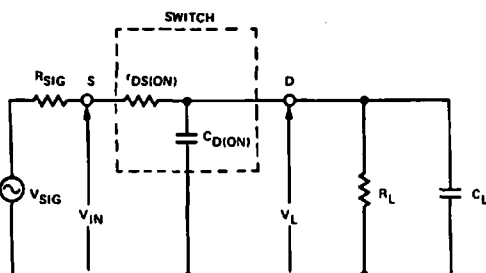
DG200A ON Performance
Figure 20

The ON state equivalent circuit for any of the four switches discussed in this Application Note is a series resistance, shunt capacitance ($r_{DS(on)}$, $C_{D(on)}$) model, as shown in Figure 21. The range of element values for each is given in Table I.

Table I

Value of Equivalent Circuit Elements

Switch Type	$r_{DS(on)}$ (Ω)	$C_{D(on)}$ (pF)
DG133	15-25	4-6
DG172	100-150	25-35
DG181	15-25	10-14
DG200A	45-60	18-24



ON Equivalent Circuit
Figure 21

The transfer function for the ON switch is

$$\frac{V_L}{V_{IN}} = \frac{\frac{R_L}{R_L + r_{DS(on)}}}{1 + jf \left\{ 2\pi \left[\frac{R_L \cdot r_{DS(on)}}{R_L + r_{DS(on)}} \right] \left[C_{D(on)} + C_L \right] \right\}} \quad (1)$$

Insertion loss is computed from the numerator as

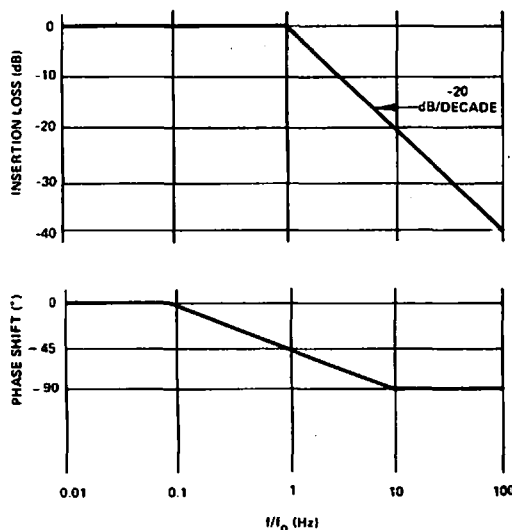
$$\text{ON insertion loss, dB} = 20 \log_{10} \frac{R_L}{R_L + r_{DS(on)}} \quad (2)$$

Table II lists the insertion loss, OFF isolation, and ON/OFF ratio for each switch, over a range of load resistance.

Table II
Switch Performance Summary

Switch	$r_{DS(on)}$ (Ω)	R_L (Ω)	Insertion Loss (dB)	OFF Isolation (dB) $f = 10 \text{ MHz}$ $C_{STRAY} = 0.1 \text{ pF}$	ON/OFF (dB)
DG133	25	100	2.0	42.7	40.7
		75	2.5	45.2	42.7
		50	3.6	48.7	45.1
DG172	150	100	8.0	51	43
		75	9.5	54	44.5
		50	12	57	45
DG181	25	100	2.0	55.9	53.9
		75	2.5	58.4	55.9
		50	3.6	61.9	58.3
DG200A	60	100	4.1	43.8	39.7
		75	5.1	46.3	41.2
		50	6.8	49.8	43.0

The frequency response of the ON transfer function has the normalized form shown in Figure 22.



$$f_0 = \frac{1}{2\pi \left[\frac{R_L \cdot r_{DS(ON)}}{R_L + r_{DS(ON)}} \right] (C_{D(ON)} + C_L)}$$

ON Frequency Response
Figure 22

Computing the minimum break frequency, f_o , for each switch discussed reveals that the DG172 has the lowest f_o , 133 MHz. Table III lists $f_{o(\min)}$ for each switch.

Larger R_L will decrease f_o only slightly, while larger C_L will decrease f_o considerably. However, 10 pF is a fairly liberal load capacitance.

Table III
Minimum Break Frequency

Switch Type	$f_o(\min)$ (MHz)	$r_{DS(on)}$ (Ω)	Values Used		C_L (pF)
			$C_{D(on)}$ (pF)	R_L (Ω)	
DG133	530	25	6	75	10
DG172	71	150	35	75	10
DG181	354	25	14	75	10
DG200A	140	60	24	75	10

CONCLUSIONS

Comparison of the OFF and ON performance of the four switches discussed shows that a tradeoff exists involving the load resistance, R_L . If R_L is decreased, isolation improves, but there is an attendant increase in insertion loss. The best compromise (greatest ON/OFF ratio) is with small R_L (see last column of Table II). Insertion loss of 2 to 5 dB indicates that the FET switches are probably not suitable for applications which require minimum signal loss as a primary design criteria.

FET analog switches — especially those in the DG181/DG191 family — have excellent RF switching capability. Any of the switches considered will satisfy the great majority of video requirements. FET integrated circuit analog switches offer simplicity and convenience in circuit design.

APPENDIX — Analysis of OFF Isolation

Switch Performance Ranking

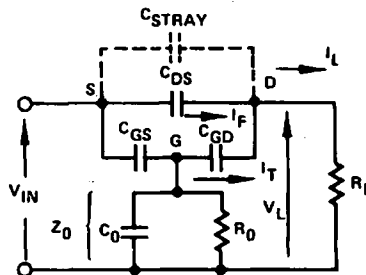
OFF isolation data taken at 10 MHz establishes the following order of performance for the four switches discussed in this presentation:

DG181 (JFET)
DG172 (PMOS)
DG200A (CMOS)
DG133 (JFET)

It is somewhat surprising that the best performer and the poorest performer are both junction FET analog switches; however, analysis of their equivalent circuits will provide an explanation for the performance differences. A general equivalent circuit for a JFET switch is shown in Figure 23.

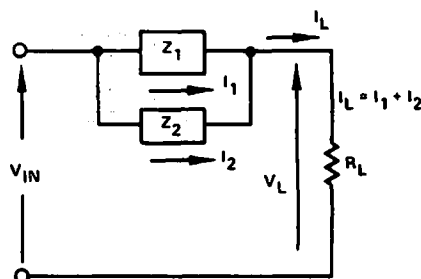
In Figure 23, two separate paths exist between source (S) and drain (D). They are (1), the path through C_{DS} and C_{STRAY} , and (2) the path which passes through the gate circuit on its way to the drain. For full understanding of the

circuit it must be assumed that I_F (current through C_{DS}) and I_T (the current flowing out of the tee network) are independent of one another.



JFET Equivalent Circuit
Figure 23

While in fact this assumption is not entirely valid, in those cases where OFF isolation is greater than or equal to 20 dB ($V_{IN} = 10 V_L$) it yields excellent agreement with measured results. Before considering the transfer functions of I_F and I_T , it will be helpful to analyze the errors caused by the assumption that I_F and I_T may be derived independently. Figure 24 may be used to analyze the magnitude of error as $V_{IN}/V_L = 10$ (20 dB) is reached.



Error Analysis Equivalent Circuit
Figure 24

The exact solutions to I_1 and I_2 are given by

$$I_1 = \frac{V_{IN}}{Z_1} \cdot \frac{1}{1 + \frac{R_L}{Z_1} + \frac{R_L}{Z_2}} \quad (1)$$

and

$$I_2 = \frac{V_{IN}}{Z_2} \cdot \frac{1}{1 + \frac{R_L}{Z_1} + \frac{R_L}{Z_2}} \quad (2)$$

The approximate solutions for I_1 and I_2 are given by

$$I_1 \approx \frac{V_{IN}}{Z_1} \cdot \frac{1}{1 + \frac{R_L}{Z_1}} \quad (3)$$

and

$$I_2 \cong \frac{V_{IN}}{Z_2} \cdot \frac{1}{1 + \frac{R_L}{Z_2}} \quad (4)$$

The approximation is valid when both Z_1 and $Z_2 \gg R_L$. For a given value of I_L/V_{IN} the error is maximum when $I_1 = I_2$. From Equations (1) and (2) one can conclude that the condition $I_1 = I_2$ implies that $Z_1 = Z_2$. Thus the exact solution for I_L becomes

$$I_L = 2I_1 = \frac{V_{IN}}{Z_1} \cdot \frac{2}{1 + \frac{2R_L}{Z_1}} \quad (5)$$

and solving for V_L/V_{IN} (since $V_L = I_L R_L$),

$$\frac{V_L}{V_{IN}} = \frac{R_L}{Z_1} \cdot \frac{2}{1 + \frac{2R_L}{Z_1}} \quad (6)$$

when $V_{IN}/V_L = 10$ (in equation 6), then $R_L/Z_1 = 1/18$.

Referring to Equations (3) and (4),

$$I_L \cong \frac{V_{IN}}{Z_1} \cdot \frac{2}{1 + \frac{R_L}{Z_1}} \quad (7)$$

and

$$\frac{V_L}{V_{IN}} \cong \frac{R_L}{Z_1} \cdot \frac{2}{1 + \frac{R_L}{Z_1}} \quad (8)$$

Thus, when $R_L/Z_1 = 1/18$, Equation (8) yields $V_L/V_{IN} = 1/9.5$ ($V_{IN}/V_L = 9.5$). In other words, when V_{IN}/V_L is equal to 10, the approximate solution yields only 5% error.

Since the circuit in Figure 23 is used to describe isolations greater than 20 dB ($V_{IN}/V_L = 10$), the results thus obtained are valid quantitatively while retaining physical insight. The transfer functions for I_F and I_T are given in Equations (9) and (10):

$$I_F = \frac{j\omega C_{DS} R_L}{1 + j\omega C_{DS} R} \quad (9)$$

and

$$I_T = \frac{j\omega C_{GS} V_{IN}}{1 + \frac{R_L}{R_O} + \frac{C_{GS} + C_O}{C_{GD}} + j \left[\frac{R_L}{R_O} \left(\omega R_O (C_{GS} + C_O) - \frac{1}{\omega R_L C_{GD}} \right) \right]} \quad (10)$$

R_O and C_O are the output resistance and capacitance of the FET driver circuit. An inspection of Equation (10) will show that as $R_O \rightarrow 0$, $I_T \rightarrow 0$. This is desirable since an ideal switch allows zero current to flow when the switch is open (off). It is thus possible to reduce R_O and make I_T an arbitrarily small value; however, I_F remains to be dealt with. Actually, I_F is the sum of the currents through C_{DS} (device capacitance) and C_{STRAY} (additional wiring capacitance, etc.); moreover, I_F may be the dominant current at certain frequencies. Table IV shows that I_F is dominant at 1 MHz and I_T is dominant at 100 MHz.

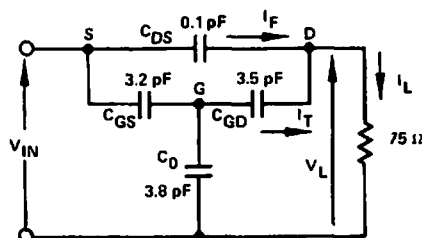
Table IV
Variations in Current with Frequency for DG181

f (MHz)	I_F	I_T	I_L	$ V_{IN}/V_L $ (dB)	$ C_{Eq} $ (pF)
1.0	141 $\angle 90^\circ$ nA	30.3 $\angle 178^\circ$ nA	145 $\angle 102^\circ$ nA	+86	0.103
4.0	563 $\angle 90^\circ$ nA	481 $\angle 173^\circ$ nA	784 $\angle 128^\circ$ nA	+72	0.139
10.0	1.41 $\angle 90^\circ$ μ A	2.91 $\angle 163^\circ$ μ A	3.58 $\angle 141^\circ$ μ A	+58	0.254
40.0	5.63 $\angle 90^\circ$ μ A	31.9 $\angle 128^\circ$ μ A	36.5 $\angle 123^\circ$ μ A	+38	0.648
100.0	14.1 $\angle 90^\circ$ μ A	99.6 $\angle 101^\circ$ μ A	113 $\angle 100^\circ$ μ A	+28	0.803

$V_L = 224$ mW $R_L = 75 \Omega$ $C_{DS} = 0.1$ pF $C_{STRAY} = 0$

NOTE: The equivalent circuit shown in Figure 26 was used to calculate the results shown in Table IV.

The separate expressions derived for I_F and I_T make it relatively simple to evaluate the effect of varying certain parameters to minimize I_L (maximize isolation).



$f = 10$ MHz; $V_1 = 224$ mV

$I_F = 1.41 \angle 90^\circ \mu$ A

$I_T = 13.3 \angle 90^\circ \mu$ A

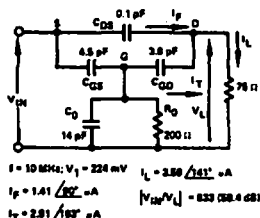
$I_L = 14.7 \angle 90^\circ \mu$ A

$|V_{IN}/V_L| = 204$ (46.2 dB)

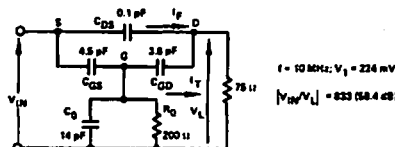
DG133 OFF Isolation
Figure 25

The isolation characteristics shown in Figures 25 and 26 dramatically illustrate the effect that variations of Z_O can have on OFF isolation. Note that C_{DS} , C_{GS} , and C_{GD} are approximately equal for both the DG133 and the DG181; however, Z_O of the DG181 is significantly lower than that of the DG133. The result is an improvement of 12 dB in OFF isolation at 10 MHz.

Figure 27 shows the effect of varying R_O between 200 Ω (the output resistance of the DG181 driver) and 0 Ω . Note that the DG181 is only 8 dB lower in OFF isolation than is



DG181 OFF Isolation
Figure 26



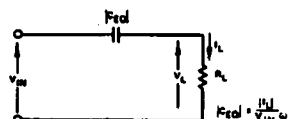
R_O	I_F	I_T	I_L	$ V_{IN}/V_L $ (dB)
0	$1.41 \angle 82^\circ \mu\text{A}$	0	$1.41 \angle 82^\circ \mu\text{A}$	66.3
200	$1.41 \angle 82^\circ \mu\text{A}$	$2.81 \angle 83^\circ \mu\text{A}$	$3.58 \angle 81^\circ \mu\text{A}$	58.4

Comparison of Ideal Driver Case ($I_T = 0$) with Actual
Performance of DG181 Analog Switch
Figure 27

the case with an ideal switch. This represents an excellent tradeoff, since $R_O = 0 \Omega$ would increase the power required by the analog switch.

Isolation Parameter

From a design viewpoint, analysis of the circuit shown in Figure 23 does not permit an easy comparison of different types of analog switches. In addition, the designer must be aware that the switch OFF isolation will degrade because of stray capacitance *outside* the body of the switch. Thus it becomes necessary to define an isolation parameter, as shown in Figure 28.



Isolation Parameter
Figure 28

Isolation Parameter
Figure 28

The magnitude sign is used in Figure 28 because the OFF isolation parameter has the dimensions of capacitance; however, the phase shift through the circuit is not necessarily 90° (see I_L vs frequency in Table IV). The phase shift through

the network is unimportant for this discussion, because consideration centers on the feedthrough signal being *less than* some allowable magnitude. Equation (11) defines the *total* isolation parameter, C_1 , as

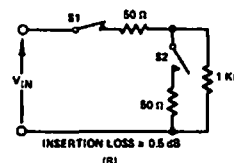
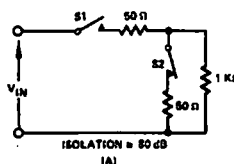
$$C_1 = C_{\text{STRAY}} + |C_{\text{Eq}}| \quad (11)$$

where C_{STRAY} = total stray capacitance *external* to the analog switch itself. To obtain an order of magnitude for this stray capacitance, a test PC board yielded a measured 0.9 pF per inch for the TO-116 package. To fully appreciate this problem, consider the OFF isolation at 10 MHz for the DG181, with only 0.5 in of adjacent line external to the switch. $C_{\text{STRAY}} = 0.45 \text{ pF}$ and $|C_{\text{Eq}}| = 0.25 \text{ pF}$; thus $C_1 = 0.7 \text{ pF}$, for an OFF isolation of 50 dB (a loss of 8 dB of isolation).

Extending the Range of the Design Aids

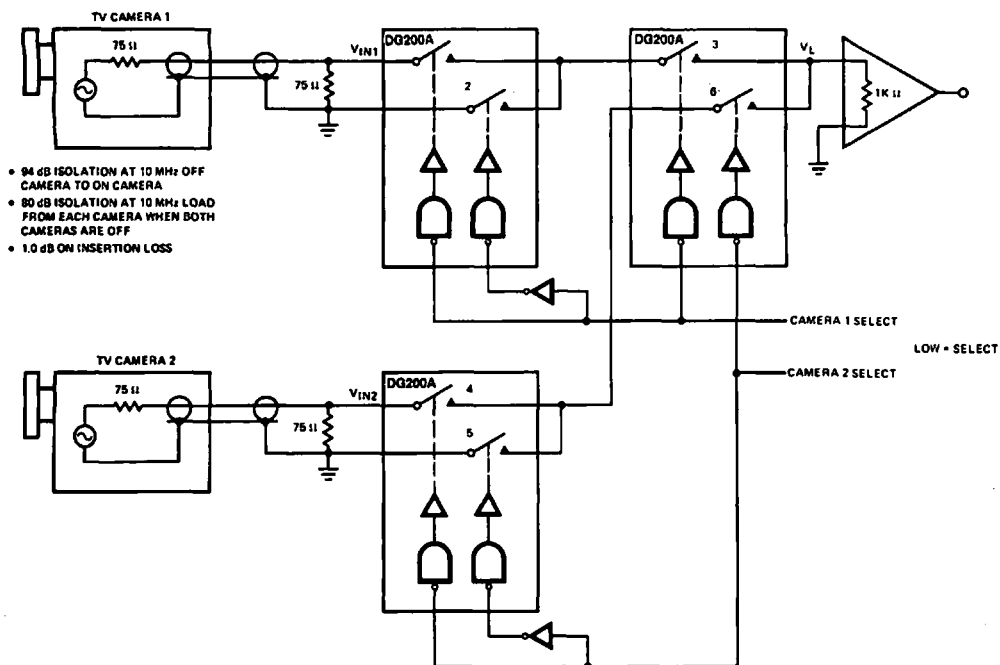
The body of this application note explains the general use of the design aids for high-frequency isolation (sinusoidal) and pulse feedthrough isolation (see Figures 5 and 6). However, there are cases where the identification of the proper analog switch for a circuit lies beyond the range of the design aid. For example, the design aid may be extended to solve for $C_1 \approx |C_{\text{Eq}}|$ where $f = 2 \text{ MHz}$, $R_L = 1 \text{ K} \Omega$, and desired isolation is 80 dB. The 80 dB isolation curve does not have an $R_L C_1$ product on the graph at 2 MHz. However, $R_L C_1$ for 60 dB at 2 MHz is $80 \Omega - \text{pF}$. Since $R_L C_1 (80 \text{ dB}) = 0.1 R_L C_1 (60 \text{ dB})$, then $R_L C_1 (80 \text{ dB}) = 8 \Omega - \text{pF}$. $R_L = 1 \text{ K} \Omega$ and $C_1 = 8 \Omega - \text{pF} \div 1 \text{ K} \Omega = 0.008 \text{ pF}$. No single switch will satisfy the isolation requirement. But if one uses a multiple switch configuration, as in the series shunt circuit shown in Figure 29, it is possible to obtain the required isolation, since $R_L \approx 50 \Omega$ and $C_1 = 0.16 \text{ pF}$. Thus two DG181 analog switches will do the job, since $C_1 \approx 0.12 \text{ pF}$ at 2 MHz.

The same type of extension can be applied to the pulse feedthrough design aid shown in Figure 6.

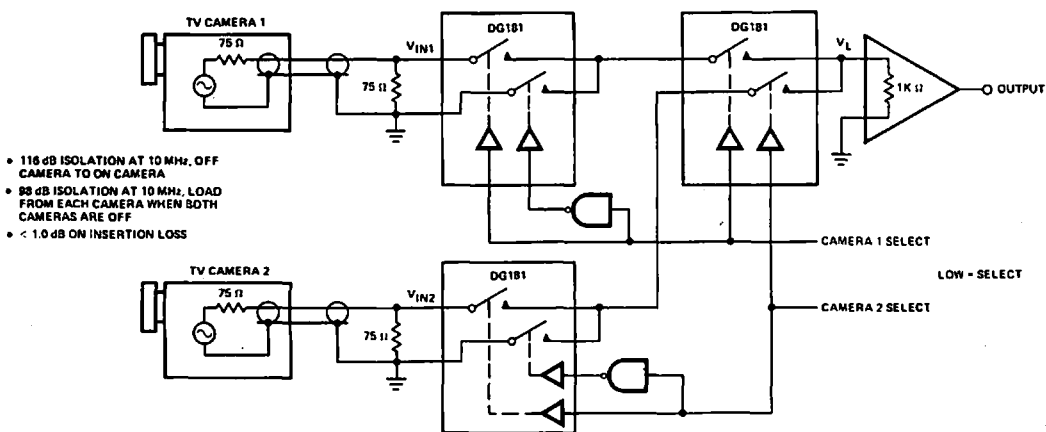


Series Shunt Circuit
Figure 29

Additional Application Circuits:



Video Switch with Very High OFF Isolation
(f = DC to 10 MHz)
Figure 30



Video Switch with Very High OFF Isolation
(f = DC to 10 MHz)
Figure 31

DRIVER CIRCUITS FOR THE JFET ANALOG SWITCH

August, 1973

INTRODUCTION

Both junction field-effect transistors (JFETs) and metal-oxide-silicon (MOS) FETs may be used as analog switches, but the JFET offers the advantages of lower ON resistance ($r_{DS(on)}$), and a constant ON resistance vs signal level characteristic.⁽¹⁾ However, these attributes of the JFET switch can only be realized through design of a suitable driver circuit for the transistor. Design of proper driving circuits presents a number of subtle problems, and overall performance of the analog switch is primarily limited by the characteristics of the driver. This Application Note deals with the design considerations encountered in drivers for FET switches.

Before exploring the problems of driver circuit design, it will be well to define the tasks that an analog switch may be expected to perform. Analog signal processing may be divided into two broad categories:

- (1) Handling DC and low-frequency AC signals, and
- (2) Handling high-frequency AC signals.

If one is to multiplex a large number of DC or low-frequency AC signals onto a common bus, the major concern will be centered around rapid switching (typically 1 μ sec or so). On the other hand, if high-frequency AC signals are to be processed, good ON/OFF ratios are a prime consideration, and switching speed is relatively unimportant (typically tens to hundreds of microseconds). In other words, a single switch will not usually be called upon to perform both high-speed switching and high-frequency signal processing. Of course, if both tasks can be performed by a given type of analog switch, then a user can realize economy by procuring large quantities.

Primary speed limitations on complete analog switch circuits are imposed by the switch driver circuits themselves. An example of this limiting effect is shown in Table I, where a 2N4392 (discrete JFET) is compared with several analog switching integrated circuits.

Table I
Effect of Driver Circuit on Switch Speed

Device	t_{on} (ns)	t_{off} (ns)	$r_{DS(on)}$ (Ω)
2N4392 ⁽¹⁾	20	55	60
1H5007 ^(2, 3)	500	1,000	80
AH0126 ^(2, 3)	800	1,600	80
DG126 ^(2, 3)	600	1,600	80
DG182 ^(2, 3)	250	130	75

(1) The 2N4392 is a discrete JFET, driven from a 500 ps pulse generator with 50 Ω source impedance.
 (2) These analog switches contain, in addition to an IC driver circuit, chips for 2N4392 JFETs.
 (3) These analog switches have TTL-compatible control inputs. The discrete 2N4392 does not.

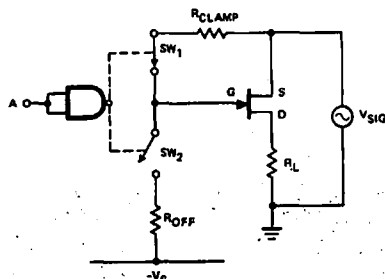
Table I makes two major points. First, the discrete JFET, by itself, has a considerably faster switching time than that of the analog switch containing the FET chip plus a driver. Second, the DG182 is a much faster analog switch integrated circuit than are the other three similar devices. The evolution of the DG182 switch/driver will be observed as the design details of four analog switch circuits are explored in depth.

The four basic driver circuits considered in this presentation will show the evolution of junction FET drivers from the fairly simple forms of several years ago to the complex integrated circuit drivers of today. The four circuit types include (1) resistor-coupled, (2) diode charge transfer, (3) transistor charge transfer, and (4) switched-resistor. They will be covered in terms of circuit operational theory, performance comparison, and the economics of make-or-buy decisions.

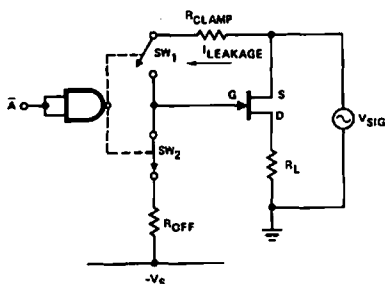
The junction FET is ON when $V_{GS} = 0$ volts, and this state may be achieved by placing a resistance between the gate and the source. So long as the current through this resistance

is zero, the gate-to-source voltage will also be zero (care must be taken that the gate-to-source diode is not forward-biased during the analog signal excursion). The functional diagram for an ideal JFET driver is shown in Figure 1. Figure 1A considers the ON case, and helps establish desirable characteristics for the driver under ON conditions. Since both gate and source will follow the analog signal, the impedance from gate to ground must be very large, to prevent current from flowing through R_{CLAMP} . In Figure 1B, the switch is in the OFF state, and the gate is clamped to the negative supply (V_2) through R_{OFF} . SW_1 should be open, since leakage will be small under these conditions. When processing high-frequency signals, R_{OFF} should have a small value.⁽²⁾

One additional point: the logic input levels are typically zero to 5 volts, while the switch driver output will range from the negative to the positive supply voltages. The positive supply voltage must at least equal the peak analog signal (typically +10 volts), and may even be higher.



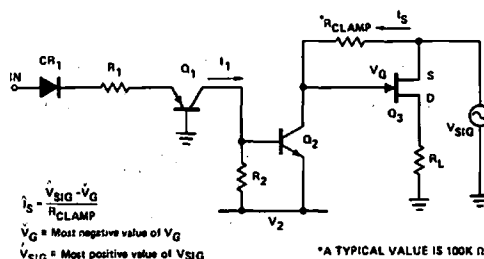
ON Condition for JFET
Figure 1A



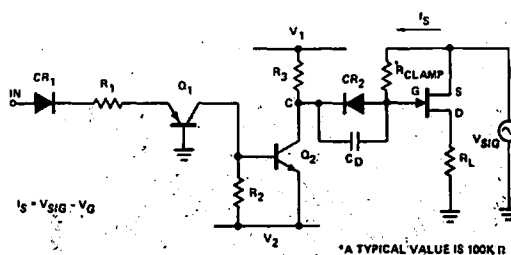
OFF Condition for JFET
Figure 1B

RESISTOR-COUPLED AND DIODE CHARGE TRANSFER DRIVERS

The simplest driver circuit is the resistor-coupled arrangement shown in Figure 2. Recall that in the circuit in Figure 1, SW_1 is permanently closed. In addition, Q_2 (in Figure 2), assumes the role of SW_2 in the ideal circuit (Figure 1). Q_2 (ON) presents a low impedance to AC ground and Q_2 (OFF) presents a high impedance to AC ground. The operation of the diode charge transfer circuit in Figure 3 is similar, in that SW_1 is permanently closed and SW_2 (Q_2 and CR_2) is the only JFET control.



Resistor-Coupled Driver
Figure 2



Diode Charge Transfer Driver
Figure 3

In Figure 2, assume that V_{IN} is 5 volts. Q_1 is ON, and I_1 turns Q_2 ON, which pulls its collector to V_2 (typically -15 volts). Since the gate of Q_3 is tied to the collector of Q_2 , then V_G is also at V_2 . In this condition, Q_3 is OFF and will remain OFF so long as the most negative value of V_{SIG} ($= V_{SIG}$) is greater than $(V_G - V_{GS(off)})$. If $V_{GS(off)}$ is assumed to be -3.5 V, then

$$V_{SIG} = -15 \text{ V} - (-3.5 \text{ V}) = -11.5 \text{ V}$$

If the rated V_{SIG} is 10 V, then I_S will flow when V_G is at -15 V (Q_3 is OFF). This value of I_S depends on R_{CLAMP} and introduces a conflict between switching time and leakage current (I_S). The data in Table II emphasizes the magnitude of this conflict. The following voltages were used to establish performance of the resistor-coupled driver circuit:

- (1) $V_{SIG} = 10 \text{ V}$
- (2) $V_G = -15 \text{ V}$ ($E_q = V_{SIG} - V_G = 25 \text{ V}$)
- (3) $V_0 = 500 \text{ mV}$ (Insures that devices with $|V_{GS(off)}| = 1 \text{ V}$ will turn ON).

Table II
Performance of Resistor-Coupled Circuit

R_{CLAMP} (Ω)	t_{on} (μs)	I_S (μA)
1 M	82.1	25
100 K	8.21	250
10 K	0.821	2,500

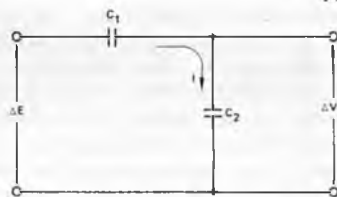
$Q_2 = 2N4400, C_{OB} \cong 5 \text{ pF}$
 $Q_3 = 2N4393, C_{iss} \cong 16 \text{ pF}$
 $C = C_{OB} + C_{iss} = 21 \text{ pF}$

Note 1: $R_{CLAMP} C \ln E_q/V_0$, where E_q is the initial voltage ($t = 0$) on C and V_0 is the instantaneous voltage at time t.

Note 2: $E_q/V_0 = 25 \text{ V}/0.5 \text{ V} = 50$ in the above t_{on} calculations.

Operation of the diode charge transfer driver circuit (Figure 3) is similar to that of the resistor-coupled circuit. Assume that Q_2 is ON ($V_C \cong -14.3 \text{ V}$). Thus $V_{SIG} \sim V_G = 24.3 \text{ V}$, and E_q/V_0 remains essentially the same as in the resistor-coupled circuit. Additionally, C_{OB} of 6 pF is replaced by the capacitance of CR_2 (about 2 pF), and total circuit capacitance thus reduces from 21 pF to 17 pF, with a corresponding reduction in turn-ON time.

At first glance, this reduced turn-ON time appears to offer very little improvement over the resistor-coupled circuit. However, the capacitance labeled C_D in the circuit in Figure 3 contributes to a significant difference in turn-ON time; Figures 4A and 4B demonstrate this difference.



$$\begin{aligned}
 (1) \Delta E &= \Delta V_1 + \Delta V_2 & (6) \Delta V_2 &= \frac{\Delta E}{1 + C_2/C_1} \\
 (2) Q_1 &= C_1 \Delta V_1 & \text{If } C_1 \gg C_2 \text{ then } \Delta V &\cong \Delta E \\
 (3) Q_2 &= C_2 \Delta V_2 & (4) Q_1 = Q_2 &= C_1 \Delta V_1 = C_2 \Delta V_2 \\
 (5) \Delta E &= \frac{C_2}{C_1} \Delta V_2 + \Delta V_2 & \text{Circuit equivalences: } C_1 &= C_D \\
 & & & C_2 = C_{iss}
 \end{aligned}$$

Analysis of Charge Distribution Between
Two Capacitor in Series
Figure 5

Analysis of the equivalent circuit shown in Figure 5 shows why the variation of 0 to 160 pF in C_D causes the reduction in turn-ON time.

In Figure 5, the voltage across $C_2 (= C_{iss})$ is affected as $C_1 (= C_D)$ is varied. Note that ΔE and ΔV_2 change at the same rate, since the total series circuit is capacitive. (Figure 4B also illustrates this condition).



$R_{CLAMP} = 100K, C_D = 0, V_{SIG} = +10 \text{ V DC}$

TOP: V_{IN}
MIDDLE: V_D 4(A)
BOTTOM: V_C

SCALES:

Horizontal = 1 $\mu s/\text{div}$
Vertical = 5 V/div*



$R_{CLAMP} = 100K, C_D = 160 \text{ pF}, V_{SIG} = +10 \text{ V DC}$

TOP: V_{IN}
MIDDLE: V_D 4(B)
BOTTOM: V_C

SCALES:

Horizontal = 1 $\mu s/\text{div}$
Vertical = 5 V/div*

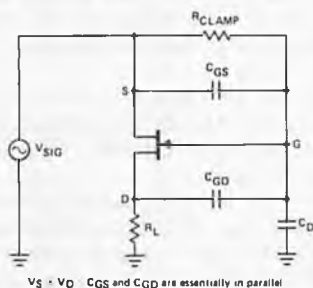
*Refers to V_D only, as V_{IN} and V_C are shown for timing information only; note t_r of $V_C \cong 200 \text{ ns}$ in each instance

Effect of C_D on Turn-ON Time
Figure 4

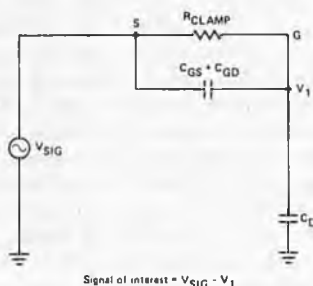
The diode charge transfer driver circuit (Figure 3) produces an analog switch which can be turned ON in less than 1 μ s and which has an I_S of 243 μ A. The resistor-coupled driver circuit in Figure 2 has an I_S value of 250 μ A but requires 8 μ s to turn ON. What happens if one tries to pass high-frequency signals through the ON switch of the diode charge transfer driver? Figure 6 shows the progression of an actual circuit (6A) to an intermediate equivalent circuit (6B) to a final circuit (6C), which solved for V_{GS} :

$$V_{GS} = \frac{j \omega R_{CLAMP} C_D V_{SIG}}{1 + j \omega R_{CLAMP} (C_D + C_{iss})} \quad (1)$$

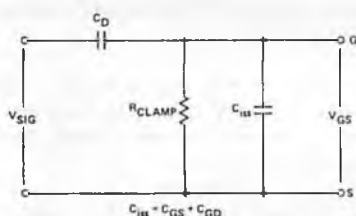
Equation (1) defines the peak voltage which will develop across R_{CLAMP} as the frequency is varied. The frequency at which a particular junction FET will pinch itself off is a function of the $V_{GS(off)}$ of that device, as well as V_{SIG} .



6(A)



6(B)

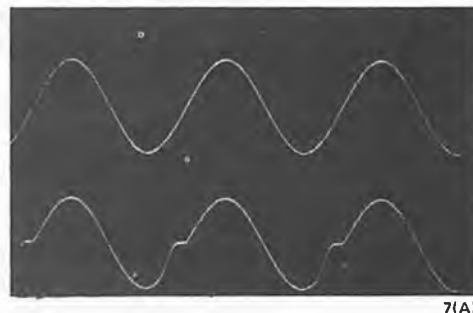


6(C)

Equivalent Circuit for ΔV_{GS} Analysis
at "High" Frequencies
Figure 6

Figure 7A shows the cut-off phenomenon occurring at 1.4 kHz, (a low frequency).

Measured $V_{GS(off)}$ of the device, in Figure 7A, is -1.6 V ($I_D = 1 \mu$ A). The calculated value of V_{GS} is 1.39 V. In Figure 7B, the switch is passing 500 kHz, no matter whether R_{CLAMP} is 100K Ω or 1M Ω . Thus if one wants to pass signals of relatively high frequency, and switching speeds of tens of microseconds can be endured, then the circuit condition with $C_D \rightarrow 0$, should be used. On the other hand, if the data to be passed is at a frequency below 1 kHz, and fast switching speed is mandatory, then the $C_D = 160$ pF condition will suffice. The important point is: the diode charge transfer driver will not handle both problems with the same C_D condition.

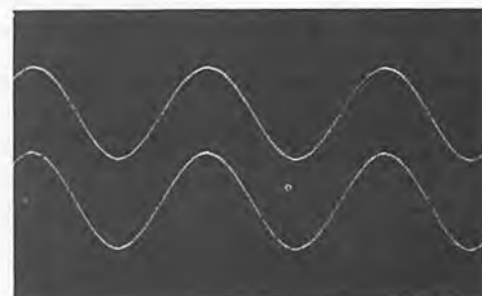


7(A)

$R_{CLAMP} = 100K \Omega$, $C_D = 160$ pF, $C_{iss} = 16$ pF.
 $V_{SIG} = 20$ V P-P, $R_L = 2.2K \Omega$

SCALES:

TOP: Input
BOTTOM: Output
Horizontal = 200 μ s/div
Vertical = 10 V/div
f = 1.4 kHz



7(B)

$R_{CLAMP} = 100K \Omega$ to 1M Ω , $C_D = 0$ pF, $C_{iss} = 16$ pF
 $V_{SIG} = 20$ V P-P, $R_L = 2.2K$

SCALES:

TOP: Input
BOTTOM: Output
Horizontal = 500 ns/div
Vertical = 10 V/div
f = 500 kHz

NOTE:

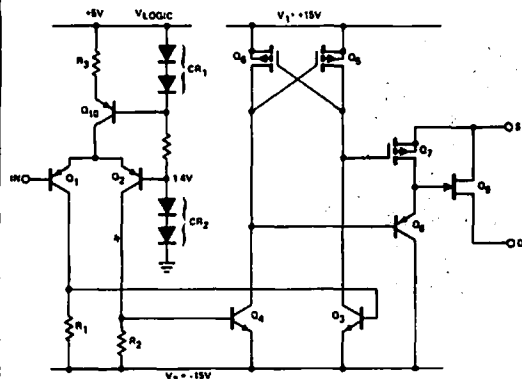
Self-pinchoff occurs when $\frac{\delta}{\delta t} (V_{SIG})$
is max, not when V_{SIG} is max.

AC Performance of Diode Charge Transfer
Driver Circuit
Figure 7

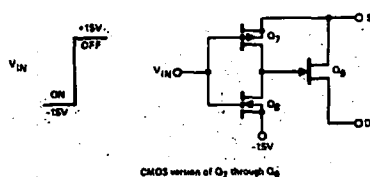
with $I_F \cong 1 \text{ nA}$ (i.e. $R_{\text{CLAMP}} \cong 26 \text{ M}\Omega$). Similarly, R_{OFF} is the equivalent resistance of two forward-biased junctions (Figure 9A), with I_F also $\cong 1 \text{ nA}$ (i.e., $R_{\text{OFF}} = 52 \text{ M}\Omega$).

THE SWITCHED-RESISTOR DRIVER

When compared to the ideal JFET driver circuit shown in Figure 1, both the diode charge transfer and transistor charge transfer circuits have several shortcomings. However, a circuit which approaches the performance of the ideal JFET driver is shown in Figure 10, and is known as a switched-resistor driver.



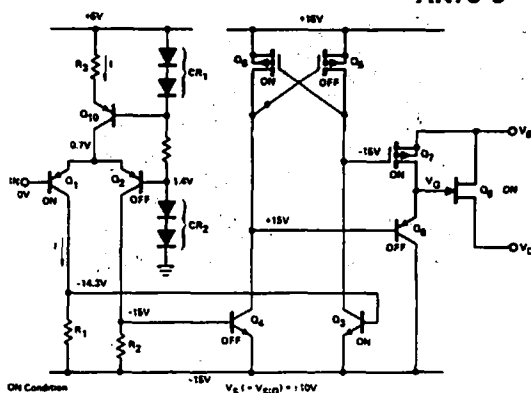
Switched-Resistor Driver Circuit
Figure 10A



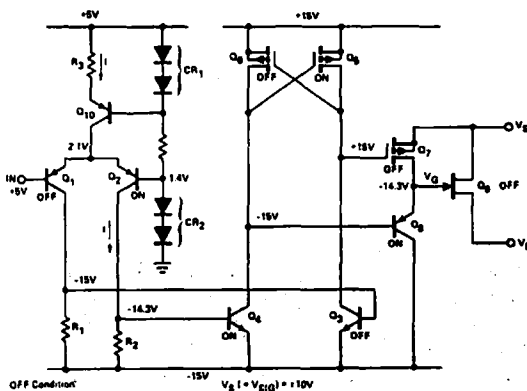
CMOS Version of Q_7 through Q_9
Figure 10B

An overview of the performance characteristics of this circuit shows that when Q_9 is ON, Q_7 is ON, clamping the gate to the source, and Q_8 is OFF. Thus the gate of Q_9 sees a high impedance to ground when it is ON. Assuming that Q_9 and Q_7 are OFF and Q_8 is ON, the gate of Q_9 sees a low impedance to ground (R_{OFF}) when the device is OFF. This circuit has low leakage currents in both the ON and OFF state, because the V_{GS} clamp is itself a switch, and not a fixed resistor.

Figure 11A shows details pertinent to the switched-resistor circuit when JFET Q_9 is ON, Q_1 is ON, and provides a base current for Q_3 , which is also ON. The collector of Q_3 is at -15 V , and turns Q_7 (SW₁ in the ideal JFET switch driver) ON. Q_7 thus turns Q_9 ON, since $V_{\text{GS}} = 0 \text{ V}$. In addition, since Q_3 is ON, Q_6 is turned ON; on the other hand, Q_2 is OFF, and Q_4 is thus turned OFF, clamping the collector of Q_4 to $+15 \text{ V}$ through Q_6 . Since the gate of Q_5 is at $+15 \text{ V}$, it is also OFF. Under the conditions shown in Figure 11A, Q_8 is OFF, since its emitter-base diode is reverse-biased (SW₂ in Figure 1 is open).



Switched Resistor Circuit Conditions When
Analog Switch is ON
Figure 11A



Switched Resistor Circuit Conditions When Analog
Switch is OFF
Figure 11B

Figure 11B is derived from Figure 11A by reversing the roles of the transistors — the ON transistors become the OFF transistors, and vice versa. Note that Q_8 in the ON state presents a low impedance to ground (R_{OFF} in Figure 1). The switched-resistor driver design is also conservative of power; both Figures 11A and 11B have open circuits between the $+15 \text{ V}$ and -15 V supplies.

PERFORMANCE COMPARISONS OF DRIVER CIRCUITS

Figures 12 through 15 and Table III summarize performance characteristics of three of the four types of JFET driver circuits which have been discussed in this presentation — diode charge transfer, transistor charge transfer, and switched-resistor drivers. Figures 12, 13 and 14 compare switching speeds, and the switched-resistor circuit is obviously the top performer.



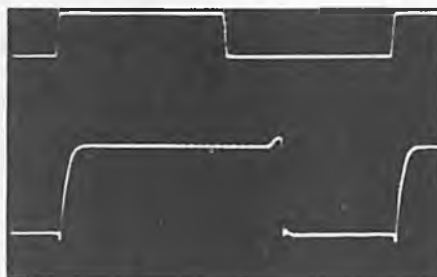
Vertical = 5 V/div
 $V_{SIG} = +10\text{ V}$

A



Vertical = 1 V/div
 $V_{SIG} = 0\text{ V}$

B



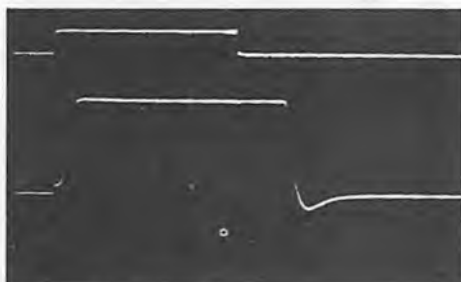
GROUND

Vertical = 5 V/div
 $V_{SIG} = -10\text{ V}$

C

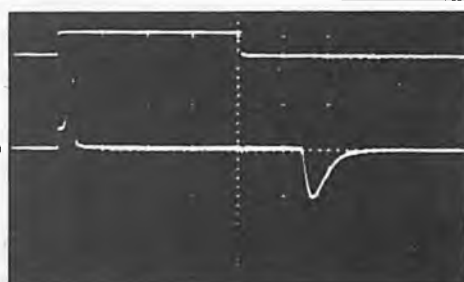
- Horizontal = 500 ns/div for all waveforms
- Top waveform is logic input for timing purposes only. When logic input is low, switch is ON.
- Same circuit as Figure 4B

Diode Charge Transfer Driver Circuit
 Switching Performance
 Figure 12



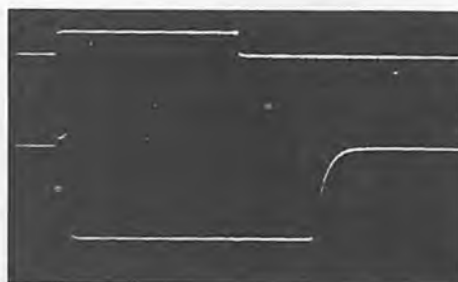
Vertical = 5 V/div
 $V_{SIG} = 10\text{ V DC}$

A



Vertical = 2 V/div
 $V_{SIG} = 0\text{ V}$

B



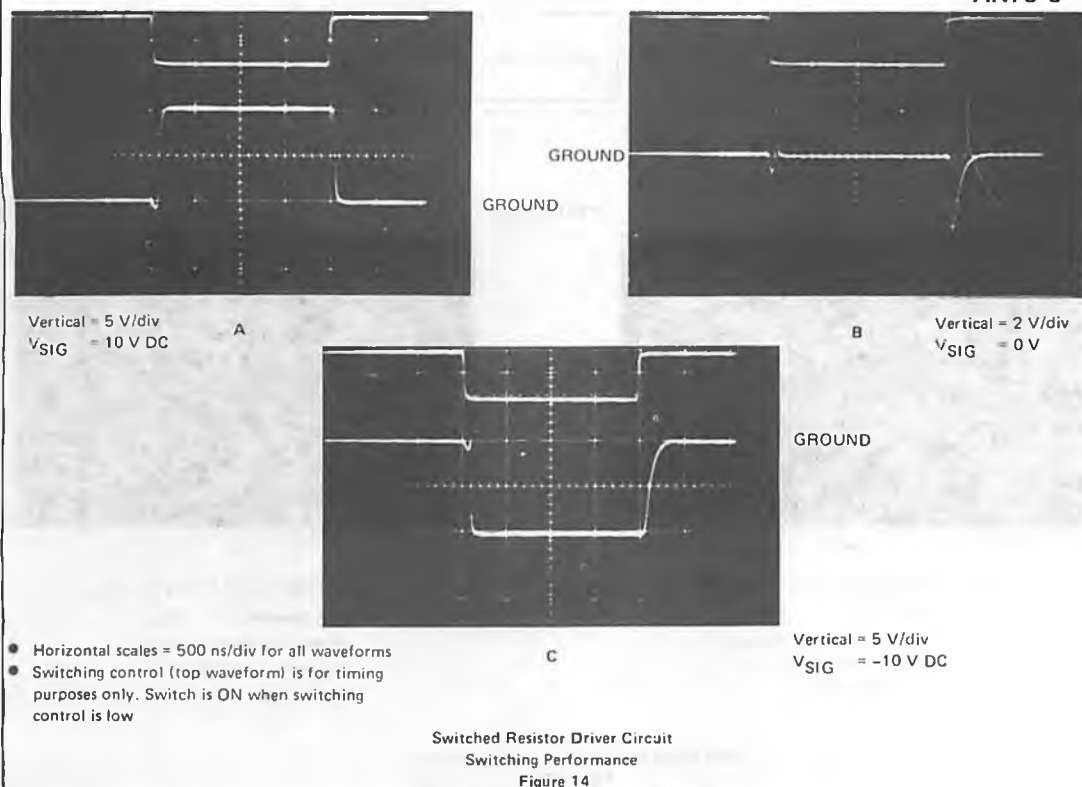
GROUND

Vertical = 5 V/div
 $V_{SIG} = 10\text{ V DC}$

C

- Horizontal = 500 ns/div for all waveforms
- Top waveform is logic input for timing purposes only. When logic input is high, switch is ON

Transistor Charge Transfer Driver
 Circuit Switching Performance
 Figure 13



The switched-resistor driver design is the same as that used in the Siliconix series DG181-DG191 analog switches. In addition to the obviously superior switching speed of this circuit, the DG181-DG191 family can handle high-frequency signals (to 100 MHz) with excellent OFF isolation. Details of high-frequency performance of this group of devices are presented in the Siliconix Application Note "Switching High-Frequency Signals With FET Integrated Circuits."

To compare the large signal handling capability of the three types of JFET driver circuits, data was taken at 500 kHz and 20 volts peak-to-peak analog signal range. Performance of the transistor charge transfer and switched resistor driver circuits is compared to Figure 15.

Data on performance of the diode charge transfer driver was presented in Figure 7B. Note that large signal high-frequency capability must be sacrificed if the diode charge transfer circuit is to perform at switching speeds comparable to the transistor charge transfer and switched-resistor circuits.

Table III summarizes the results presented in Figures 7B, 12, 13, 14 and 15. Leakage currents and average dissipation of the three analog switch circuits is compared.

Table III
Comparison of Leakage Current, Switching Time, High-Frequency Signal Handling and Power Dissipation

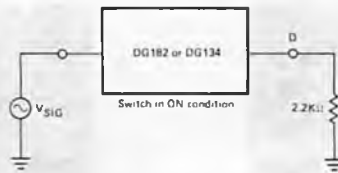
Characteristic	Diode Charge Transfer	Transistor Charge Transfer	Switched-Resistor
$I_{S(off)}$ (μA)	243 ⁽¹⁾	0.001	0.001
t_{on} (ns)	800	200	150 ⁽²⁾
t_{off} (ns)	200	1,200	100 ⁽²⁾
f (cut-off) (kHz) ⁽³⁾	1.4 ⁽¹⁾	>500	>500
P_d (channel) (mW) ⁽⁴⁾	166	17	60

NOTE 1: $R_{CLAMP} = 100\text{K } \Omega$, $C_D = 160 \text{ pF}$

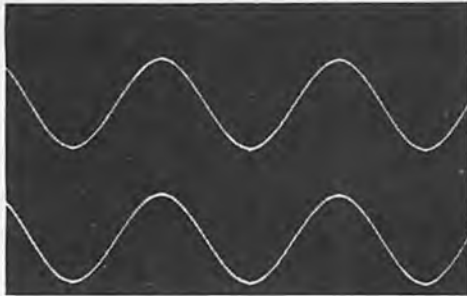
NOTE 2: $V_{SIG} = +10 \text{ V DC}$, $R_L = 10\text{K } \Omega$

NOTE 3: $V_{SIG} = 20 \text{ V P-P}$, $R_L = 2.2\text{K } \Omega$

NOTE 4: Switch is ON 50% of time



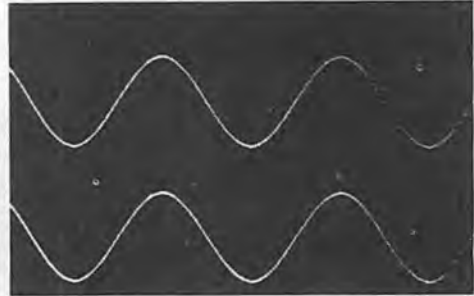
TEST CIRCUIT



A

TRANSISTOR CHARGE TRANSFER DRIVER

Top Waveform: V_{SIG}
 Bottom Waveform: V_{DRAIN}
 Voltage = 10 V/div
 Time = 500 ns/div



B

SWITCHED-RESISTOR DRIVER

Top Waveform: V_{SIG}
 Bottom Waveform: V_{DRAIN}
 Voltage = 10 V/div
 Time = 500 ns/div

Large Signal Performance at High Frequency
 Figure 15

MAKE OR BUY?

When the driver circuits which have been analyzed are compared, it is apparent that there is a close correlation between improved performance and increased circuit complexity. For instance, if discrete components were used in the switched-resistor circuit, the increased complexity of the circuit would make costs prohibitive. Fortunately, the switched-resistor driver circuit is available as a monolithic integrated circuit and costs are considerably lower than the same circuit constructed with discrete components. Thus the diode charge transfer driver (a discrete component circuit) is apparently inexpensive because of its simplicity. Is it really true? In reality, the real comparison is made when evaluating *total* costs to produce both the diode charge transfer circuit and the switched-resistor circuit. Table IV compares actual costs with parts costs.

Note that testing cost is calculated as 120% of the manufacturing cost. The rationale for this figure is the labor differential between production and technician help, *plus* additional time spent locating and replacing faulty components. For example, less time (less money) is spent replacing a faulty integrated circuit than is required to locate and replace a bad component in a discrete circuit. Additionally, the versatility of the analog switch integrated circuit permits its use in many applications, tending to increase the quantity purchased and thus reducing the cost.

Table IV
 Comparison of Circuit Manufacturing and Parts Costs

Cost Item	Diode Charge Transfer Circuit	Switched-Resistor Circuit
Parts	\$0.89	\$2.81 ⁽¹⁾
Assembly ⁽²⁾	2.23	0.69
Pre-Test Total	\$3.12 ⁽³⁾	\$3.50
Testing	2.68	0.83
Total Production	\$5.80 ⁽⁴⁾	\$4.33

Note 1: Pre-channel cost in large quantities.

Note 2: Includes labor costs and pro-rated costs of PC board "real estate."

Note 3: Pre-test cost of the diode charge transfer circuit is 89% of that of a high-performance IC.

Note 4: Total production cost for the diode charge transfer circuit is 134% of that of a high performance IC.

Note 5: Above manufacturing cost data obtained from a local OEM electronics firm (non-military).

Designing a circuit such as the switched-resistor driver is a relatively complicated affair. In the early days of semiconductor technology, when discrete components were widely prevalent, the cost for such a circuit would have been difficult to justify. But today's advanced integrated circuit technology removes this cost obstacle. In short, the user of IC analog switches can procure high performance at low cost, and be relieved of the concerns associated with the manufacture of the circuit with discrete components.

REFERENCES

- (1) "FETs as Analog Switches," Siliconix inc., Application Note, Sept. 1972.
- (2) "Switching High-Frequency Signals with FET Integrated Circuits," Siliconix inc., Application Note, March, 1973.

DESIGNING WITH MONOLITHIC FET SWITCHES

INTRODUCTION

Field-effect transistor switches have become increasingly common components of analog multiplex systems, sample-and-hold circuits, and even digital switching circuits. The major advantages of field-effect transistors (FETs) include an ON-to-OFF current ratio of 10^9 , a relatively simple equivalent ON circuit (resistive and bilateral), inherent high-speed switching capability and, if properly used, a high degree of control-signal isolation.

MOSFETs are Simple

Among solid-state switches, the MOSFET switch is the simplest to use. The switch itself is easy to construct, and the ON/OFF drive circuitry is quite basic (Figure 1). As the PMOS gate is forced negative with respect to the source, the resultant field attracts holes or p-type carriers, forming a conductive p-channel (resistive path) between source and drain. The point where conduction begins is called the threshold voltage V_{TH} . As gate-to-source voltage V_{GS} is forced more and more negative, the conductive channel widens and the drain-to-source resistance r_{DS} decreases. V_{TH} is commonly -3 V to -4 V. However, for a useful ON resistance of 200 ohms, it is necessary to force V_{GS} to -10 V.

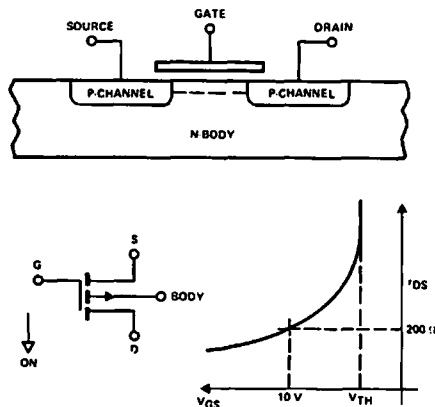


Figure 1. Cross sectional representation, schematic and threshold characteristics for a p-channel enhancement mode MOSFET.

Reprinted From ELECTRONIC PRODUCTS Magazine, January 1973.

Three basic types of PMOS driver-gates are shown in Figure 2: a basic FET and driver, a PMOS driver-gate employing both FETs and bipolar devices, and an all-PMOS unit. The

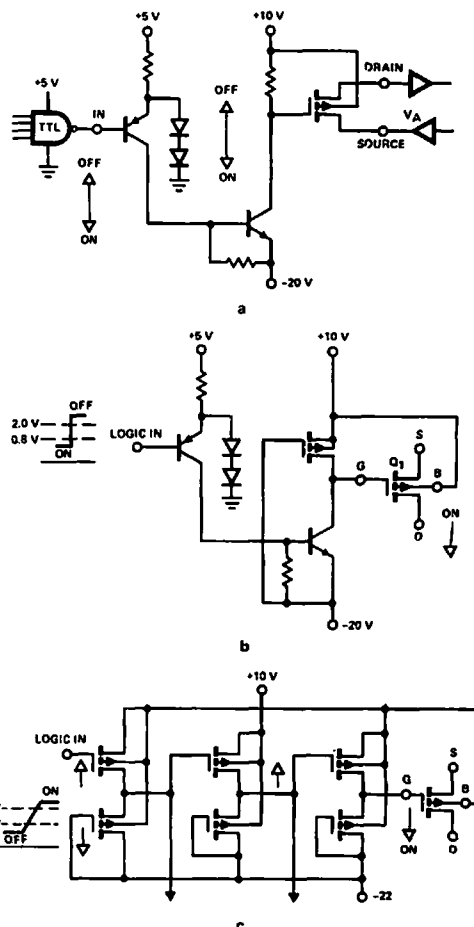


Figure 2. Three types of PMOS driver gates: a basic FET and driver (a), FETs combined with bipolars (b), and an all-PMOS unit (c).

gate is direct-driven by a level-shifting circuit that also serves as an amplifier, since it converts TTL logic signals (0.8 V to 2.0 V) into the -20 V to -10 V gate signals required to turn the FET ON or OFF. This range of drive-gate amplitude permits switching an analog signal of $\pm 10\text{ V}$. In these circuits, when the driver is ON, the PMOS gates are at -20 V .

Examining the main drawbacks of PMOS driver-gates, a portion of Figure 1 is modified to show the effect of analog voltage, V_A , on the gate (Figure 3). The chief disadvantage of the PMOS gate is the 3:1 ratio in $r_{DS(on)}$ for analog voltages varying between -10 V and 10 V . A second disadvantage lies in the requirement for 10 V and -20 V supplies (Figure 2), which is often a problem in analog systems built around the typical $\pm 15\text{ V}$ op amp power supply.

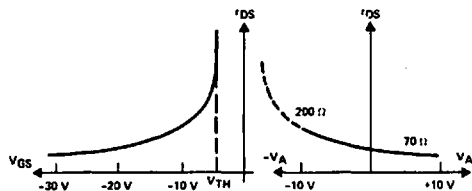


Figure 3. Threshold characteristic (Figure 1) modified to show the effect of analog voltage V_A on the gate.

An ideal means of avoiding variation of r_{DS} with analog signal voltages is to use a CMOS gate. The CMOS switch uses two enhancement-mode MOSFETs in parallel (one PMOS and one NMOS) between each source and drain terminal (Figure 4). The NMOS FET is similar to a PMOS FET, save for changed polarities. To turn the NMOS FET ON, V_{GS} is made more positive than $V_{GS(TH)}$, which is now 3 V to 4 V .

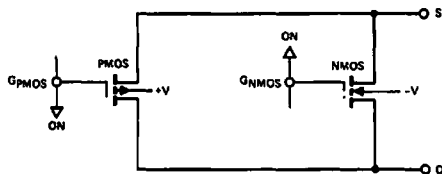


Figure 4. CMOS switch formed from PMOS and NMOS FETs connected in parallel.

The basic CMOS switch is derived by connecting the PMOS and NMOS FETs in parallel. The switch is turned ON by driving the PMOS gate negative, and the NMOS gate positive simultaneously (Figure 5a). Using "desirable" $\pm 15\text{ V}$ supply voltages, assume that the analog signal voltage is $V_A = 0$. $V_{GS(P)}$ is -15 V and $V_{GS(N)}$ is 15 V . Both FETs are ON, and r_{DS} of the complementary switch is the parallel combination of $r_{DS(P)}$ and $r_{DS(N)}$ (around 70 ohms for larger switches).

In Figure 5b, for $V_A = 15\text{ V}$, $V_{GS(P)}$ is -30 V , but $V_{GS(N)} = 0$. The NMOS FET is OFF, but since the PMOS FET has twice the necessary V_{GS} , that FET is "twice as ON." R_{DS} is again about 70 ohms .

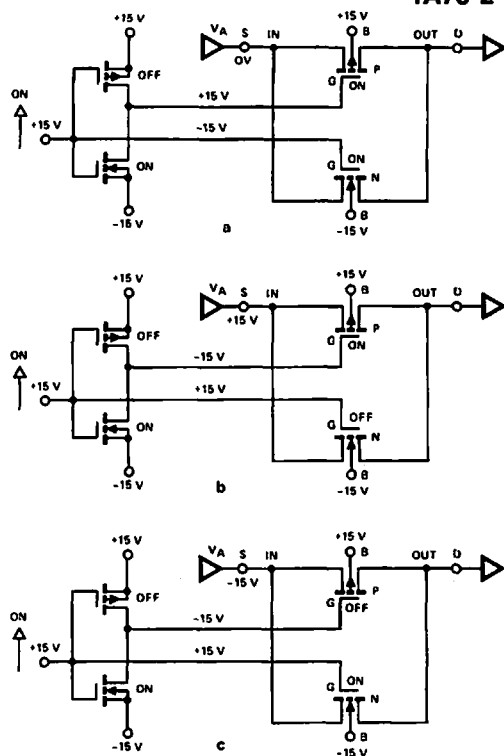


Figure 5. Resistance through the PMOS and NMOS parallel combination remains about 70 ohms for three different ON conditions.

In Figure 5c, for $V_A = -15\text{ V}$, $V_{GS(N)}$ is 0 while $V_{GS(P)}$ is 30 V . The PMOS FET is OFF while the NMOS FET has an r_{DS} of approximately 70 ohms . It is important that the relative sizes of the NMOS and PMOS FETs be balanced so that r_{DS} will be the same whether $V_A = 15\text{ V}$ or -15 V . If the PMOS and NMOS FET sizes are properly matched, then one FET will compensate for the other during varying analog voltage signals, and a nearly constant $r_{DS(on)}$ ($\pm 10\%$) will be achieved for an analog signal range equal to the supply voltages.

Like the PMOS switch, the analog signal in a CMOS switch cannot exceed the positive supply voltage. Neither can the analog signal exceed the level of the negative supply voltage (Figure 6).

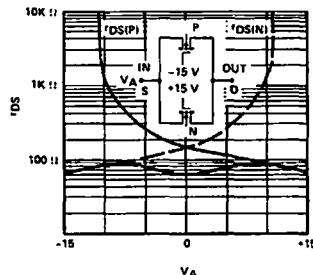


Figure 6. The CMOS switch's analog signal (V_A) range is equal to $\pm$ supply voltage.

Another advantage of the CMOS switch (shared with CMOS logic) is that driver stages, including all decode gates, have quiescent power requirements of nearly zero.

A number of CMOS switches are available today, ranging from simple dual spst devices to 16- and dual 8-channel multiplexers in a single package. CMOS construction puts both n-channel and p-channel devices on a common substrate.

The JFET Approach

CMOS technology is responsible for several new driver-gate switch combinations. One very important technique produces junction FET switching circuits. The cross-section of an idealized JFET is shown in Figure 11.

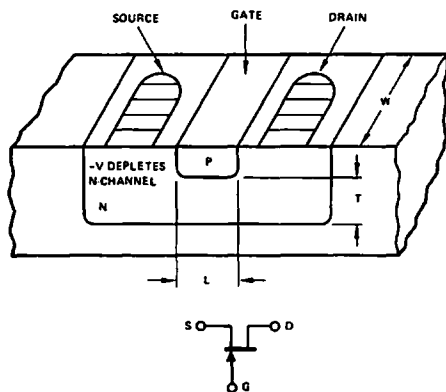


Figure 7. Cross sectional representation and schematic for a JFET.

Junction FETs are depletion-mode devices. When $V_{GS} = 0$, the FET is ON. The gate of a JFET surrounds the channel and is not separated by an insulating oxide layer, as is the case in MOSFETs. As a result, changes in channel current per change in gate-source voltage are higher in JFETs than in MOSFETs. Directly related to this characteristic is the ability of the JFETs to produce a lower r_{DS} than can be developed in a MOSFET with the same area and the same ON capacitance.

On the other hand, the JFET is harder to drive than the MOSFET. The drive problem arises in the gate to channel p-n junction. In the MOSFET, the gate may either be positive or negative relative to the source and drain (within breakdown limits), and current will not flow in the gate circuit. This MOSFET characteristic permits direct connection of the gate to a level-shifting driver circuit. Conversely, if the gate of an n-channel JFET becomes positive with respect to the source, not only does the device turn ON, but undesirable error current will flow between the gate and the source.

In a JFET driver circuit, the objective in turning the FET ON then becomes driving the gate so that $V_{GS} = 0$. The direct-coupled drive circuit shown in Figure 8 satisfies this JFET operating objective. If the npn transistor is OFF, then

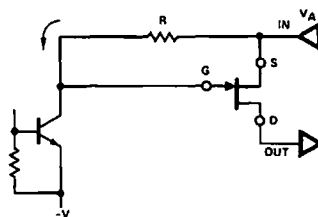


Figure 8. Direct-coupled JFET switch clamps the gate to the source through resistor r if the npn driver transistor is OFF.

a resistor clamps the gate to the source. A trade-off arising from this condition is that collector leakage in the driver transistor may draw current from the analog signal path.

A more serious problem common to direct-coupled circuits occurs when the switch is turned OFF. An n-channel JFET is turned OFF by application of a negative gate voltage, so that V_{GS} is more negative than the FET cut-off voltage. In such a circuit, the FET is turned OFF by turning ON the npn driver transistor. The negative supply must be more negative than the most negative analog voltage. When the driver is OFF in the circuit, a current flows from V_A to $-V$, limited only by R (Figure 8). An unreasonably long turn-ON time will result if R is too large.

A JFET driver circuit commonly used with low-cost systems that employ discrete components is shown in Figure 9. The diode permits the driver to pull the JFET negative and turn it OFF. When the driver cathode becomes positive, the diode is reverse-biased and the diode capacitor inserts sufficient charge into the FET gate to bring V_{GS} slightly above zero. The FET is thus turned ON and, if $C_{GS} + C_{GD}$ is more than C_d , the gate will stay ON, pulled along with the analog voltage being supplied to the source. This diode-coupled JFET switch produces a problem when handling a-c signals. A negative signal on the source forward-biases the gate-source junction, pulling the gate negative. When the source voltage rises, the diode capacitance C_d prevents the gate from fully following the source. Increased r_{DS} and even device cut-off may occur on the positive signal peak.

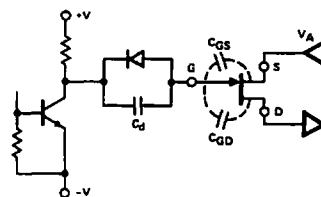


Figure 9. Diode capacitance in this low cost diode-coupled JFET switch prevents the gate from exactly following the source.

A charge-transfer driver for a JFET switch is shown in Figure 10. The circuit functions like the diode-coupled driver in Figure 9. A controlled amount of charge is inserted into the FET gate until C charges up to +V, then the transistor turns OFF. Compared to the diode-coupled driver circuit, the charge-transfer driver circuit's advantage is that its output capacitance is much lower than the 10 to 20 pF required for the diode-coupled arrangement. This charge-transfer type of driver gate is offered as an integrated circuit by several major manufacturers.

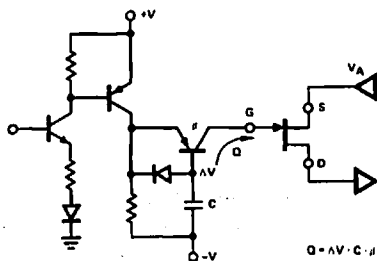


Figure 10. Charge-transfer driver has much less capacitance than the diode-coupled arrangement of Figure 9.

Earlier, it was pointed out that the best way to turn ON a JFET driver circuit is to clamp the gate to the source. An attractive way to accomplish this is suggested in Figure 11. When point A is pulled negative, the PMOS FET is turned ON, with the JFET tied to its source through a resistance of several hundred ohms. V_{GS} remains at zero, and the JFET will remain ON even at high frequencies.

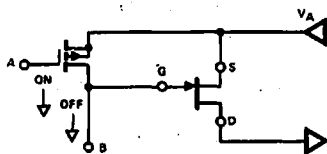


Figure 11. Using a PMOS driver for a JFET switch allows the JFET to remain ON even at high frequencies.

In Figure 12, an NMOS FET has been added to the circuit of Figure 11 to provide an excellent JFET driver. A negative input will turn the PMOS FET and the JFET ON. A positive input will turn the NMOS FET ON, the PMOS FET OFF, and since the JFET gate is also pulled to the negative state, that device also will turn OFF.

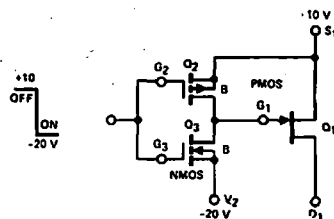


Figure 12. A negative (-20 V) input turns ON the PMOS FET and JFET. A positive (10 V) input turns ON the NMOS FET, but turns OFF the PMOS FET and the PFET (G_1 clamped to -20 V).

The circuit shown in Figure 13 also uses a PMOS FET to drive a JFET. The gate pull-down (turn-off) element is a pnp transistor. The entire drive circuit can be constructed on one monolithic chip.

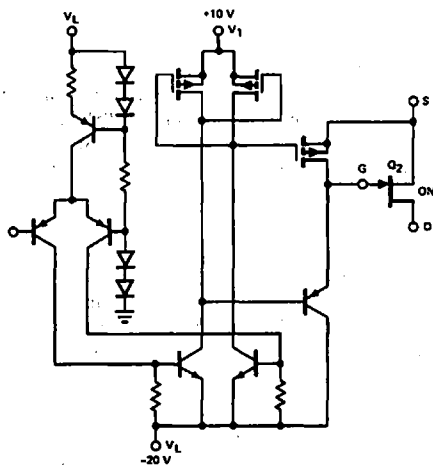


Figure 13. Monolithic JFET switch with both a push-pull driver and a level shifter.

ANALOG SWITCHES IN SAMPLE AND HOLD CIRCUITS

Gary Dixon

Revised October 1984

INTRODUCTION

In many cases the designers of sample-and-hold circuitry have relied upon "cut-and-try" methods to achieve good circuit performance. This Application Note provides analytic design information regarding sample-and-hold circuitry and practical design examples.

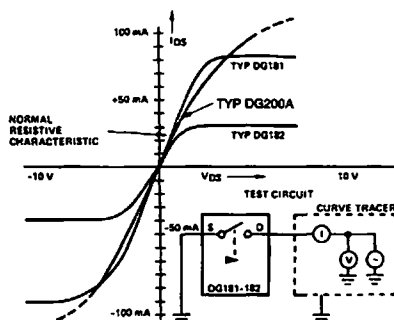
FET analog switches will meet the basic performance requirements for sample-and-hold circuitry. The criteria for choosing a given FET analog switch may seem rather simple since many of the D-C data sheet parameters are similar from one switch or from one technology (JFET, PMOS, or CMOS) to another. However, the dynamic features of a switch are the primary characteristics that must be examined. This task is not easy since any measurement assumes a given set of conditions and circuitry. This Application Note will consider two major characteristics of FET analog switches. The first area is that of the large current-handling characteristics of various switches, which can have a pronounced effect on circuit settling times. The second subject involves the offset characteristics of sample-and-hold circuits which may affect the basic accuracy of system design.

For high-speed sample-and-hold circuits, the large current handling capabilities of the switch can play an important role

in determining settling time. As a rule, the data sheet specifications for switch ON resistance are made at low current levels, such as those found in analog signal coupling circuits. When an analog switch is required to charge a capacitor, the switch may be required to handle large instantaneous currents and voltages. The switch dynamic characteristics will vary depending upon the type of switch and the drive circuitry used.

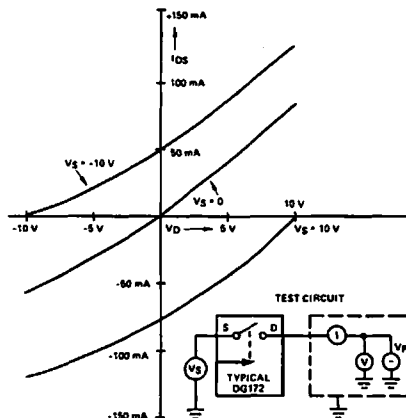
Of the many JFET switches, the DG181-191 series is recommended for its low ON resistances and its easily-determined high current characteristics. Figure 1 illustrates that the DG181, a 30 Ω device, typically enters I_{DSS} limiting at 80 mA. Further investigation indicates the DG182, a 75 Ω device, typically encounters current limiting at 30 mA. If we compare the DG181 with a CMOS device, the DG200A, we will find the DG200A has a somewhat more resistive characteristic.

Figure 2 shows the resistance characteristics of a PMOS switch, the DG172. The average ON resistance for settling purposes may be assumed to be between the minimum resistance at the most positive signal excursion and the maximum ON resistance at the most negative excursion.



Current Characteristics of a JFET Analog Switch, The DG181, and a CMOS Switch, the DG200A

Figure 1

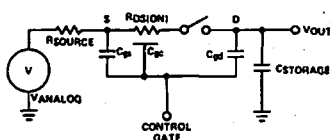


Characteristics of a PMOS Analog Switch

Figure 2

Figure 2 is based on a negative supply voltage to the DG172 of -20 V. If the supply were -15 V, the currents through the switch would decrease, which is a disadvantage of PMOS. The DG181 current is independent of supply voltage, while the DG200A is designed to work with ± 15 V supplies.

Let us now turn to the second subject to be covered, that of switch charge transfer. In the past, this subject has been called switching transients, "glitches", and various other names. Switching transients affect the intrinsic accuracy of any sample-and-hold design. During the sample interval, the capacitor charges to the sample voltage. Then during the transition from sample to hold, an offset voltage is introduced into the charged capacitor. The major phenomena is that of a capacitive voltage divider formed by the capacitive coupling between the control gate with its associated switch terminals and the storage capacitor, as shown in Figure 3.



Equivalent Switch Circuit
Figure 3

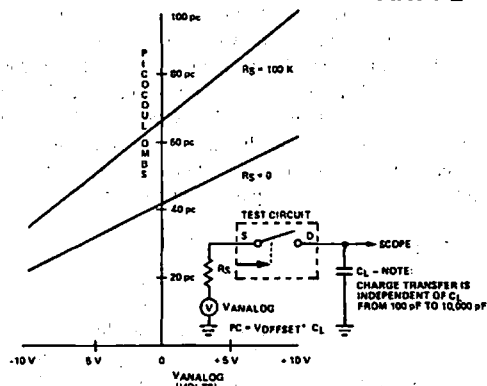
Charge transfer characteristics will vary to quite an extent, depending upon various switch and circuit configurations. To provide a method of comparison for various switches, the preferred terminology is charge transfer presented in pico coulombs.

Charge transfer (Pico Coulombs) = Voltage offset $\times$ Hold capacitance (Pico Farads).

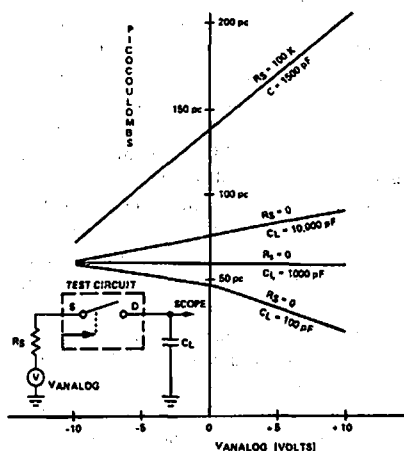
The DG181 series of JFET switches provides very good transient coupling characteristics. One of the reasons for this performance is the decrease in gate voltage swing, because the FET Gate is initially clamped at the analog voltage. The JFET construction also provides an optimization of low coupling capacitance along with low ON resistance. If we now compare a PMOS switch with the JFET characteristic we are able to see a major difference.

As may be seen from the two curves of Figures 4 and 5, the charge transfer characteristics for the DG181 and DG172 are similar at $C_L = 100$ pF and $R_S = 0$. It should be noted, however, that the DG172 has a typical ON resistance of 200Ω — an increase in ON resistance of 6 times more than that of the DG181. For values of capacitance greater than 100 pF in the charge transfer characteristics of the DG172 are seen to be inferior to those of the DG181. The major factor which causes the storage capacitance to be value-dependent is the large distributed gate-to-channel capacitance, plus the related circuit time constants.

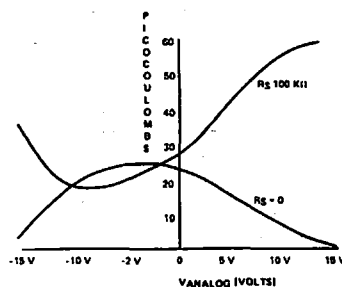
CMOS devices provide an improvement over the JFET and PMOS devices since two gates with complementary control signals are involved. The two resulting "glitches" tend to cancel each other. The transient is therefore greatly reduced but is not eliminated due to design compromises. This is shown in Figure 6.



Typical Charge Transfer Characteristic
of the DG181 JFET Switch
Figure 4



Typical Charge Transfer Characteristics
of the DG172 PMOS Switch
Figure 5



CMOS Charge Transfer Characteristics
Figure 6

When the various tradeoffs are considered, the DG181-191 family of JFET switches provides the best overall performance for critical sample-and-hold designs. This is due in large part to their fast (150 nsec) switching speeds, which allows a fast aperture time. The CMOS DG200A series comes in a close second, but they have somewhat slower switching times (1000 nsec). PMOS switches cost the least, and are useful in general purpose applications.

Inverting DG181 Sample-and-Hold Circuit

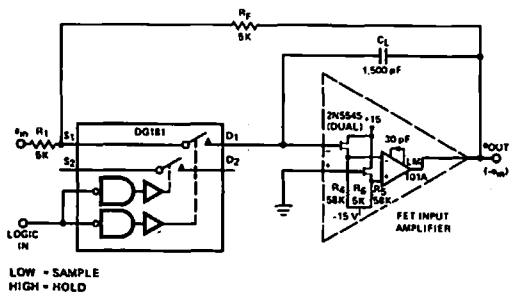
The inverting sample-and-hold circuit has several inherent advantages over the other design approaches. The switch operates at a constant voltage each time, thus reducing the aperture time jitter considerably. The input configuration reduces surge currents that are usually supplied by the signal source. A slight disadvantage of this circuit is the requirement that the two feedback resistors be matched to obtain reasonable accuracy. The feedback resistance value must be carefully chosen so that the amplifier output does not enter a current-limiting mode. General purpose amplifiers with a 20 mA limit will operate with a 5K Ω feedback network. The linear time response of the circuit is determined by the time constant $(R_f + 2 R_{SW}) C_L$. In this example $r_{SW} < R_f$; therefore, the settling time is determined by the feedback resistance. This circuit is current-limited by the amplifier and the feedback resistance, so the large current characteristics of the switch are of little importance. The circuit is also limited by the slew rate of the amplifier. If a 1500 pF storage capacitor is used, the amplifier slew rate should be greater than 2.7 V/ μ S. If, as shown in Figure 7, an LM101A op amp is used (with a slew rate of 0.5 V/ μ S), an additional 25 μ S will be required during slew rate limiting. For the circuit shown, an acquisition time of 98 μ S was measured for a swing of 20 volts settling into a 1 mV error band. If we now turn the task of determining the sample-to-hold offset, we must first examine the charge transfer characteristics of the switch. Since the source resistance is 5K Ω ; which is much greater than the 30 Ω $R_{DS(on)}$, we must examine the characteristics near the high impedance curves ($R_s = 100K \Omega$) on the charge transfer chart of Figure 4. The DG181 pro-

vides an offset voltage of 43 mV. The DG200 may be used in this circuit with a voltage jump of 18 mV. If a DG172 switch is used a 91 mV jump should be expected.

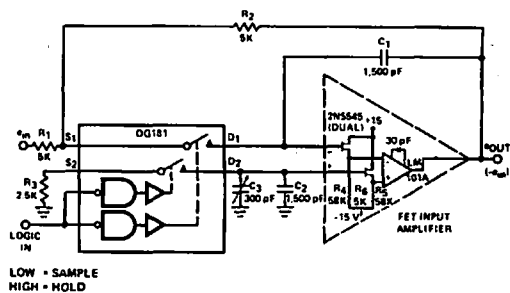
Improved DG181 Inverting Sample-and-Hold Circuit

If these foregoing charge transfer errors are too large for practical use, several methods of reducing the charge transfer are possible. The first method involves increasing the capacitor size which improves the droop rate, but also requires a direct trade-off of accuracy vs speed. A second method involves reducing the size of the switching FET, which also decreases charge transfer but increases the ON resistance. This method also requires that a trade-off be made due to the relationship of speed versus accuracy. A third and more practical method is to compensate for the charge transfer. Many circuits have been proposed in the past which vary from simple capacitors in logic circuitry to rather complex systems. The inverting sample-and-hold circuit is rather easy to compensate since it operates at a single voltage level. The basic concept involves an equal but opposite charge transfer and may be implemented by coupling to a level changer which provides transitions in the opposite direction of the FET gate voltage. A rather unique circuit using this principle uses the two switches normally found in analog switch packages.

The compensation circuit shown in Figure 8 employs three additional components (R_3 , C_2 and C_3) to provide total offset errors which are adjustable to much less than 1 mV. One feature that the DG181 device offers is a 20% larger charge transfer from the D2 terminal. This actually makes compensation much easier since only one side of the network must be adjusted. With other switches (such as the DG200A) parameter variations may require that hold capacitors of two different sizes be used to provide adjustability. An added feature of this circuit configuration of Figure 8 is a net reduction in the system droop due to a balancing effect of the leakage currents.



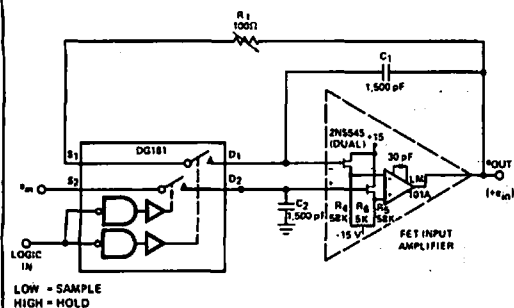
Inverting Sample & Hold Circuit
Figure 7



Improved Inverting Sample & Hold Circuit
Figure 8

High Performance DG181 Non-Inverting Sample-and-Hold Circuit

For those designers who require much faster settling times, the high-performance sample-and-hold circuit shown in Figure 9 should be used.



High Performance Non-Inverting Sample-and-Hold Circuit
Figure 9

As mentioned previously the DG181 JFET switch provides the best combination of settling speed and inherent charge transfer accuracy.

A typical DG181 analog switch is capable of charging a 1500 pF capacitor in 500 ns to within a 1 mV error band for a 20 volt swing. This statement assumes that the signal source is able to supply the capacitor charging current of 80 mA (zero source impedance).

The offset is adjusted to zero offset for zero analog signal by changing R_1 , which also provides a normalization for both source impedance and the differential charge transfer

characteristic between switches. The offset varies with analog voltage from +1.4 mV at 5 V to -1.5 mV at -5 V. This reduction provides an order-of-magnitude improvement over an uncompensated circuit. In general, for the faster sample-and-hold circuits which use the non-inverting technique, the charge transfer may be adjusted to zero at one voltage only. The compensated inverting sample-and-hold approach will provide much better offset characteristics, but at a sacrifice in overall speed. The non-inverting sample-and-hold circuit, however, has the disadvantages of CMRR gain errors and the source may be loaded with large sampling-surge currents.

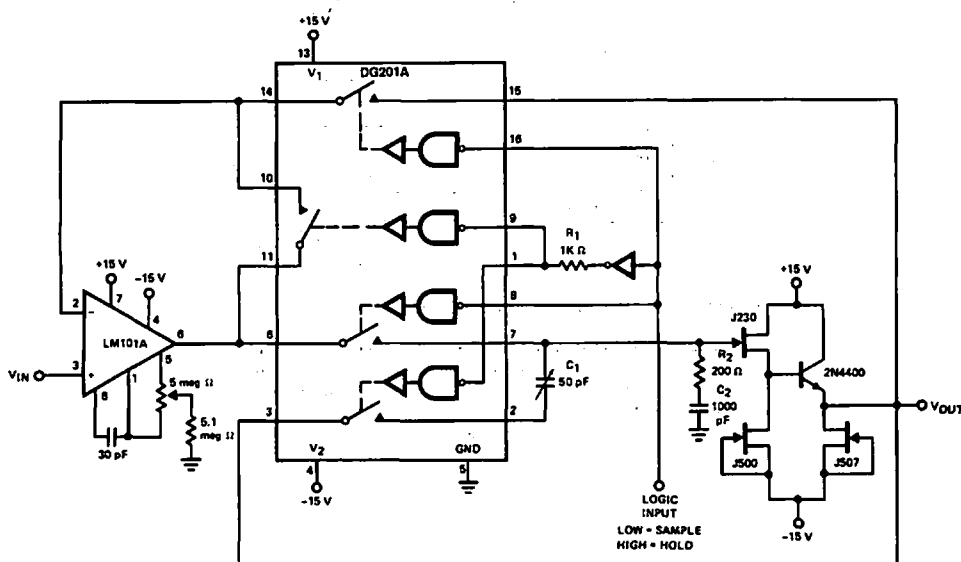
High-Quality DG201A Sample-and-Hold

Figure 10 shows a high-quality sample-and-hold using DG201A. (1) The DG201A has a higher ON resistance than the DG200A (175 Ω vs 70 Ω) but this does not affect the overall speed. The LM101A provides gain and buffers the input from storage capacitor C_2 . R_2 adds a zero in the open loop response to compensate for the pole caused by the switch resistance and C_2 , improving the closed loop stability. R_1 provides a slight delay in the digital drive to pins 1 and 9.

C_1 provides cancellation of coupled charge, keeping the sample-to-hold offset below 5 mV over the analog signal range of -10 to +10 V. Aperture time is typically 1 μ sec, the switching time of the DG201A. Acquisition time is 25 μ sec, but this can be improved by using a faster slewing op amp. Droop rate is typically less than 5 mV/sec at 25°C.

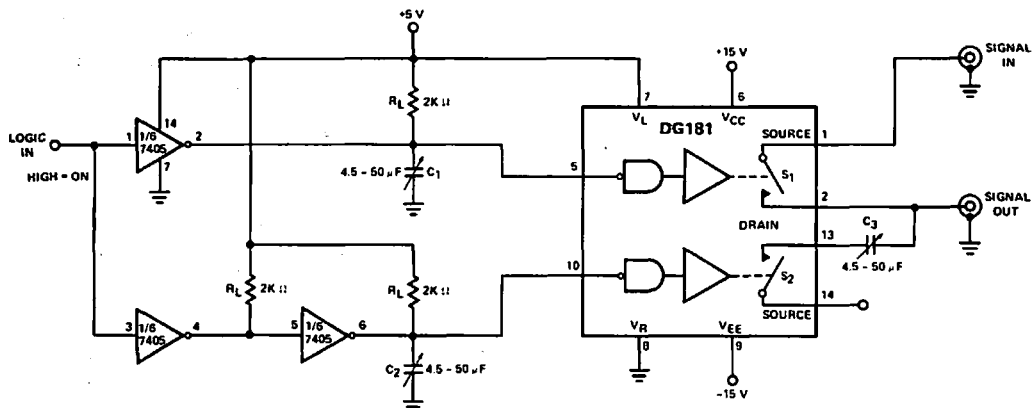
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- (1) Lee Shaeffer, "CMOS Analog Switches - A Powerful Design Tool," Siliconix Application Note AN75-1, July 1975.



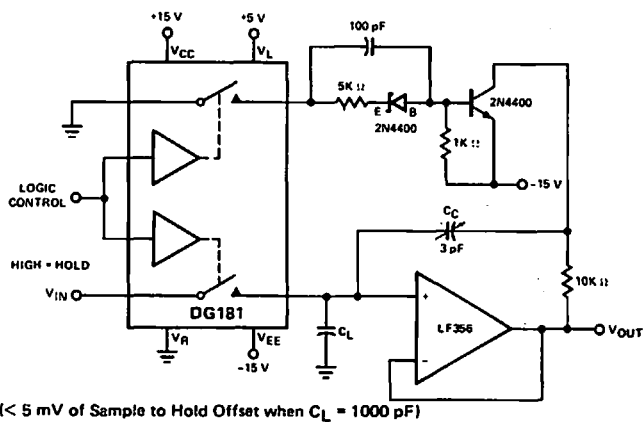
DG201 Sample-and-Hold
Figure 10

Additional Application Circuits:



Switching Transients Attenuated by Synchronization of Turn-On and Turn-Off of One Switch with Those of Another. (Refer to "Electronics," Oct. 3, 1974, pg. 108, "Attenuating Transients in Analog FET Switches.")

Figure 11



(< 5 mV of Sample to Hold Offset when $C_L = 1000 \text{ pF}$)

Charge Compensated Sample and Hold, < $\pm 5 \text{ pC}$ Charge Transfer (< 5 mV Sample to Hold Offset when $C_L = 1000 \text{ pF}$). (Refer to "Electronic Design," April 27, 1972, "Cut Transients in FET Analog Switches.")

Figure 12

CMOS ANALOG SWITCHES – A POWERFUL DESIGN TOOL

Revised December 1984

INTRODUCTION

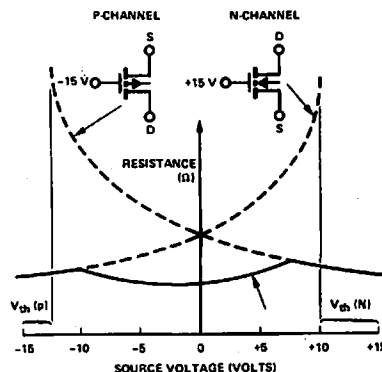
Siliconix CMOS analog switches combine large voltage handling capability, low power dissipation, low leakage, and direct TTL/CMOS interface capability for maximum design flexibility. In addition, a family of multiplexers are available which provide binary decoding on the chip for system simplicity. This application note describes the Siliconix CMOS switch family and offers circuits which illustrate their capabilities.

Properties of CMOS

CMOS (Complementary Metal-Oxide-Semiconductor) combines P-channel and N-channel enhancement-mode FETs in a common substrate. P-channel enhancement-mode FETs have a negative threshold voltage (the gate must be several volts more negative than the source or drain in order for current to flow between the source and the drain), while N-channel FETs have a positive threshold (Figure 1). When a P-channel FET is used as a switch (standard PMOS devices), the gate is held at the negative supply when in the ON condition, and the FET conducts for most voltages applied to the source. However, when the source voltage approaches the negative supply, the resistance approaches infinity. The result is a dead-band equal to the threshold voltage of the FET.

This problem is overcome by connecting an N-channel FET in parallel with the P-channel device. The N-channel gate is tied to the positive supply, and the FET is turned on hardest when the source is most negative. The resistance curve of the P-channel and N-channel FETs in parallel is shown in Figure 1.

The resistance curve is nearly flat for $V - \leq V_S \leq V^+$ (only CMOS is capable of this) but some resistance variation is normal. 20% peaking is typical for ± 15 volt power supplies, with greater peaking at lower supply voltages. If the P- and N-channel FETs have different thresholds the peaks will not be symmetrical. As the switch heats up the resistance increases 0.5%/°C.

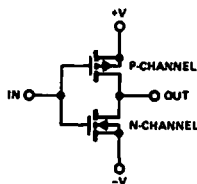


Resistance vs Source Voltage of
P-channel and N-channel FETs
Figure 1

Because the gates of the P- and N-channel FETs are internally switched to opposite supply voltages, one would expect that leakage currents and switching glitches would cancel when $V_S = 0$. This would indeed be true if the FETs were identical except for polarity. However, because the conductance of the N-doped silicon is 2.5 times greater than that of equally doped P-type silicon, it is a practical impossibility to make the leakage currents and capacitances equal for FETs of equal resistance (the P-channel is physically 2.5 times larger than the N-channel). The cancellation therefore takes place at some intermediate voltage. Because the measured leakage is the P-channel leakage minus the N-channel leakage, small variations in the absolute value of either can make a large change in the difference. Since small amounts of impurities can greatly influence the leakage, both the magnitude and polarity of the leakage measured at the source or drain will vary greatly from unit to unit, and will depend on the analog voltage and the temperature. Even though the leakage is unpredictable, it is still less than a comparable PMOS or bipolar switch.

10

In addition to a large analog voltage capability, a second advantage of CMOS is low power dissipation. Figure 2 shows a digital inverter with virtually no static power dissipation. When the input is pulled high, the N-channel turns ON and the P-channel OFF. Thus the output is tied to the negative supply through $r_{DS(on)}$ of the N-channel FET, while the P-channel device draws no current. If the input is changed to a negative voltage the state of the FET is reversed, pulling the output high. When a CMOS device is turned ON, the load is turned OFF; this overcomes a major disadvantage of PMOS structures, where the load is ON at all times and considerable power is drawn when the FET is ON.



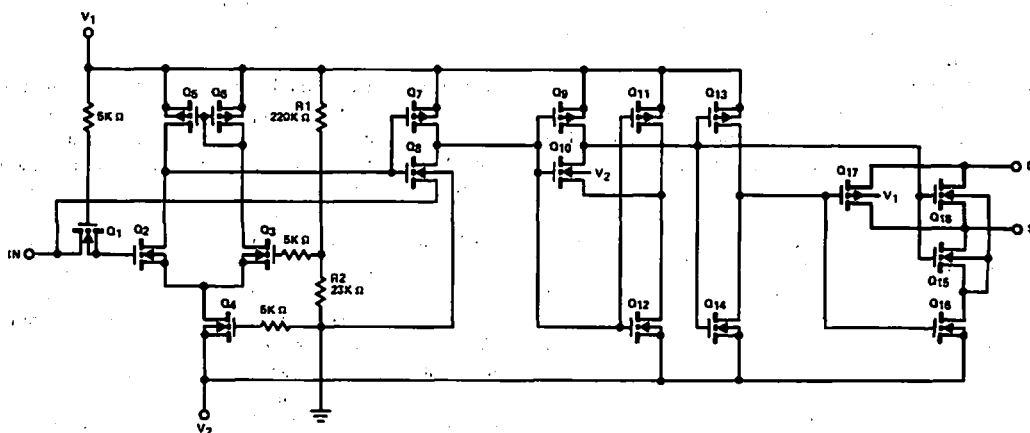
A CMOS Inverter
Figure 2

Figure 3 shows the schematic of the DG200A and DG201A, typical Siliconix CMOS switches. Q_2 , Q_3 and Q_4 form a differential amplifier with active loads Q_5 and Q_6 . Q_1 provides input protection for the gate of Q_2 , while the gate of Q_3 is connected to the logic threshold voltage established by the $R_1 - R_2$ voltage divider. The differential input stage allows a low and repeatable switching threshold voltage (1.4 V) independent of the threshold voltages of the FETs. The source of Q_8 is connected to the input to "bootstrap" the $Q_7 - Q_8$ inverter, making the switching threshold sharper. $Q_9 - Q_{10}$ and $Q_{13} - Q_{14}$ are also inverters, while $Q_{11} - Q_{12}$ level-shift the logic from 15 to 30 V p-p. Q_{15} and Q_{16}

switch the body of Q_{18} to either the negative supply (in the OFF state) or the source (when the switch is ON). The result of a positive clamp of the body to the source is a low ON threshold voltage which is not modulated by the analog voltage. In the OFF condition the isolation and breakdown voltage are high and the leakage is low when the body is firmly clamped to the negative supply. Because the clamping FET causes the switching glitches to be greater at the source than at the drain, it is good practice to connect the source to the actual signal source, or to the lower impedance point in the circuit.

An adjustable switching threshold is available on most Siliconix CMOS analog switches. As shown in Figure 3, V_{REF} is connected to the junction of two resistors which act as a voltage divider, dividing the +15 V supply down to +1.4 V. This voltage is connected to the differential input amplifier and establishes the switching threshold at 1.4 V. Normally V_{REF} is left open. If operation at reduced supply voltage is desired, however, the switching threshold will be lowered, resulting in less noise immunity. By connecting a resistive divider to V_{REF} , the threshold may be raised back up to 1.4 V. Operation is possible down to ± 8 V on the supplies.

All of the multiplexers (DG506A, DG507A, DG508A and DG509A) contain decode circuitry enabling a binary logic input to select one of 4, 8, or 16 channels. Each multiplexer also contains an ENABLE-INHIBIT control, which shuts the device off when in the INHIBIT mode. This allows the common connection (drains) of several multiplexers to be paralleled, and the units can then be enabled one at a time. This is useful when more than 16 channels are involved. Also, when the device is inhibited, its power dissipation is typically less than one-fourth the normal dissipation, for low total system power dissipation.



Schematic of a Typical CMOS Switch Channel
(DG200A and DG201A)

Figure 3

Latch-Proof Operation

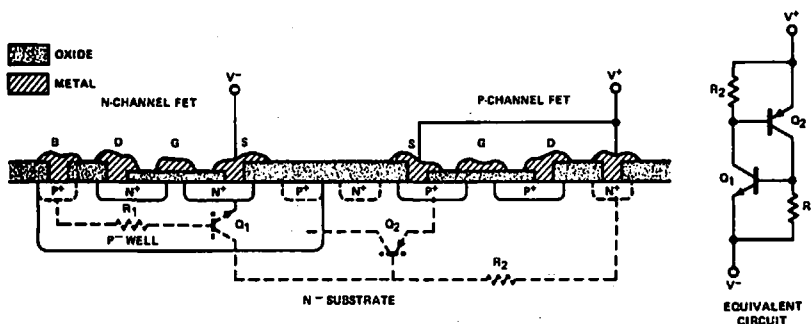
Latchup had been a thorny problem in first-generation CMOS switches. A cross section of two CMOS FETs (Figure 4) shows both a PNP and an NPN structure, which is connected as an SCR (PNPN). Under abnormal conditions, one or more of the PN junctions becomes forward biased, activating the bipolar transistor. This in turn activates the SCR, which appears as a short between the substrate (positive supply) and ground or V^- . Since the product of the NPN and PNP Betas is often greater than 1000, this short would persist until power was removed or until the device burned up. When 200 Ω resistors were placed in series in the power supply leads, device destruction was prevented; however, only removal of the power supply would return the circuit to normal operation.

By using a "buried layer" configuration, (patent pending, Figure 5) Siliconix has reduced the product of the NPN and

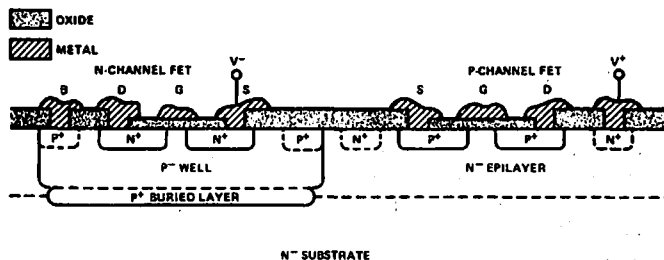
PNP betas to less than one, making latch-up impossible under any circumstances. The switches retain their desirable features such as low leakage, high OFF isolation, and high breakdown voltage. In addition, the latch-proof switches now have a much higher current capability (20 mA continuous, up to 100 mA peak on the DG200A).

General Switching Applications

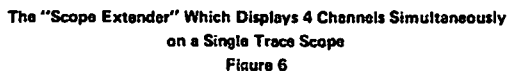
One of the significant advantages of the CMOS structure is in its ability to handle large analog voltages, since only CMOS can allow signal swings to the power supplies. A logical application is switching the outputs of operational amplifiers. The entire system can be run on ± 15 V, and the full output of the op-amps (typically ± 14 V) can be used. In most cases it is advantageous to switch at the relatively low-impedance output of an op-amp rather than at the summing junction, to minimize the effects of switch capacitance and leakage.



A Cross Section of Two CMOS FETs Showing the Parasitic Transistors, and Equivalent Circuit
Figure 4



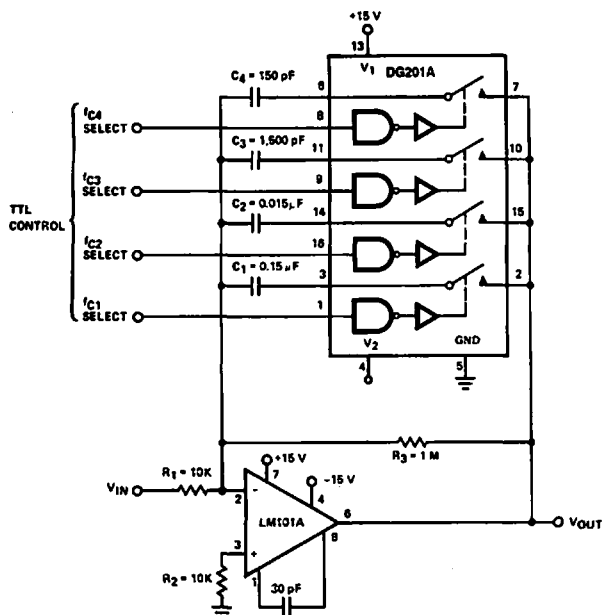
A Cross Section of the Siliconix "Buried Layer"
Figure 5



a maximum attenuation of 40 dB (80 dB relative to the low frequency gain).

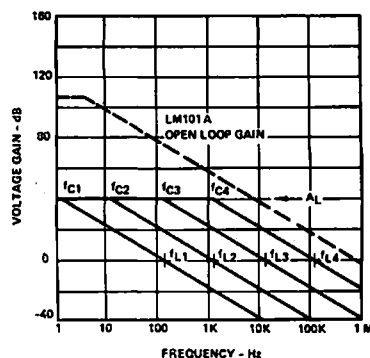
The amplifier shown in Figure 8 has digitally-programmable gain and inputs. The DG200A "looks" into the high input impedance of the op-amp, so the effects of $r_{DS(on)}$ are negligible. The DG201A is also connected in series with r_{IN} and is not included in the feedback dividers, thus

contributing negligible error to the overall gain. Because the DG200A and DG201A can handle ± 15 V, the unity gain follower connection ($\times 1$) is capable of the full op-amp output range (± 12 V).



Active Low Pass Filter with Digitally Selected Break Frequency

Figure 7



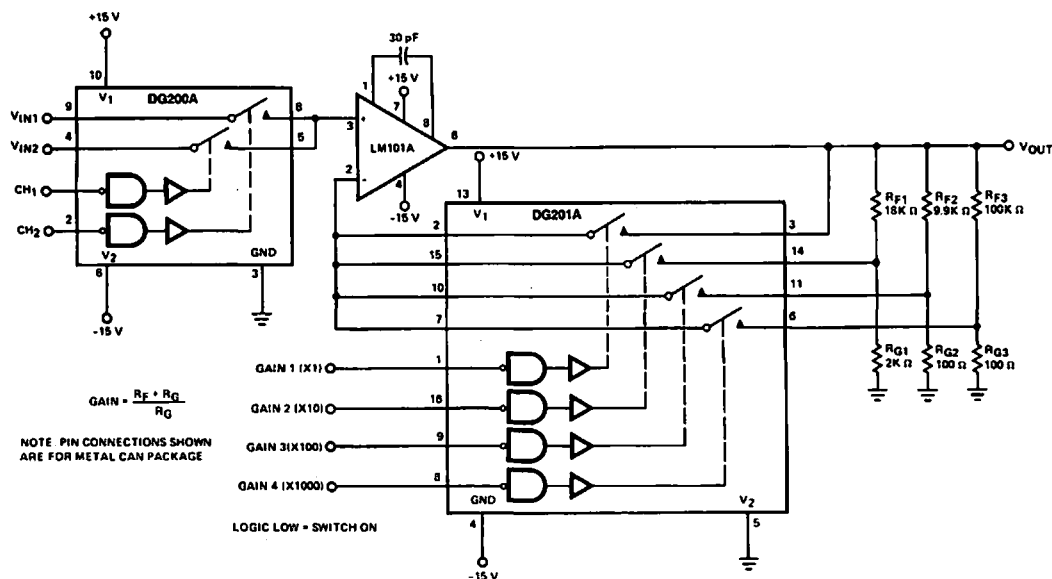
A_L (VOLTAGE GAIN BELOW BREAK FREQUENCY)

$$= \frac{R_3}{R_1} = 100 \text{ (40 dB)}$$

$$f_C \text{ (BREAK FREQUENCY)} = \frac{1}{2\pi R_3 C_X}$$

$$f_L \text{ (UNITY GAIN FREQUENCY)} = \frac{1}{2\pi R_1 C_X}$$

$$\text{MAX ATTENUATION} = \frac{f_{OS(0dB)}}{10K} \approx -40 \text{ dB}$$



A Precision Amplifier with Digitally Programmable Inputs and Gains

Figure 8

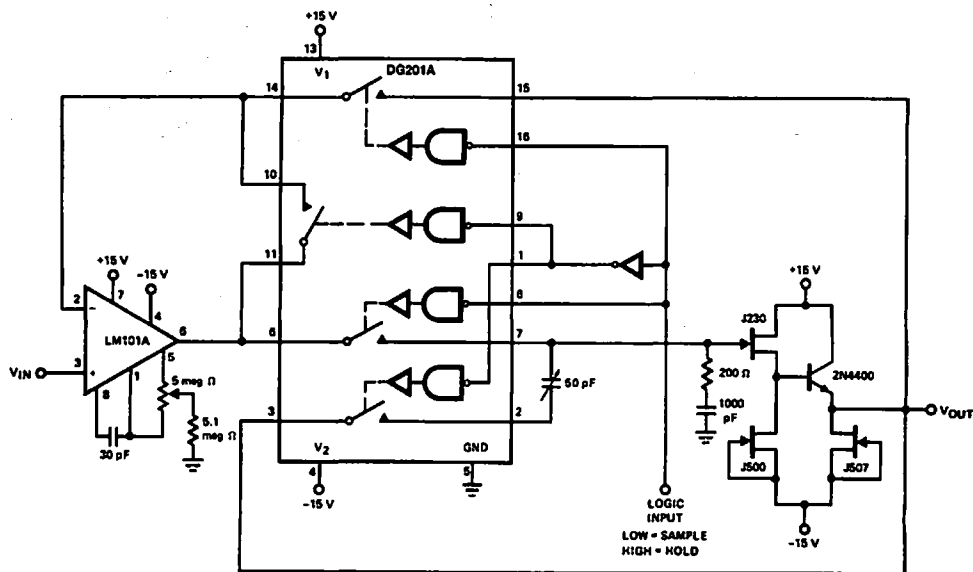
A single DG201A contains all the switches necessary for the sample-and-hold circuit shown in Figure 9. Switch 4 provides cancellation of coupled charge (glitches), keeping the sample-to-hold offset below 5 mV over the analog voltage range (-10 to +10 V). Aperture time is typically 1 μ sec. Acquisition time is 25 μ sec, but this can be improved by using a faster slewing op-amp. Droop rate is typically less than 5 mV/sec at 25°C.

The low $r_{DS(on)}$ and high peak current capability of the DG200A makes it ideal for discharging an integrator ca-

pacitor (Figure 10). A HIGH logic input pulse disconnects the integrator from the analog input and discharges the capacitor. When the logic input is returned to low the integrator is triggered, having the transfer characteristic,

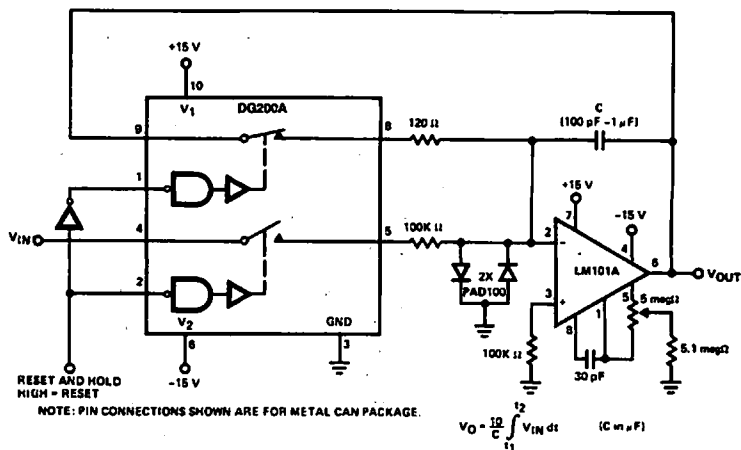
$$V_{OUT} = -\frac{1}{10^5 C} \int_{t_1}^{t_2} V_i dt \quad (4)$$

D_1 and D_2 prevent the capacitor from charging to over 15 V.



DG201A Sample and Hold

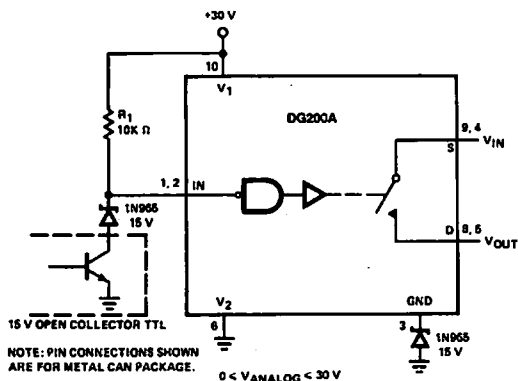
Figure 9



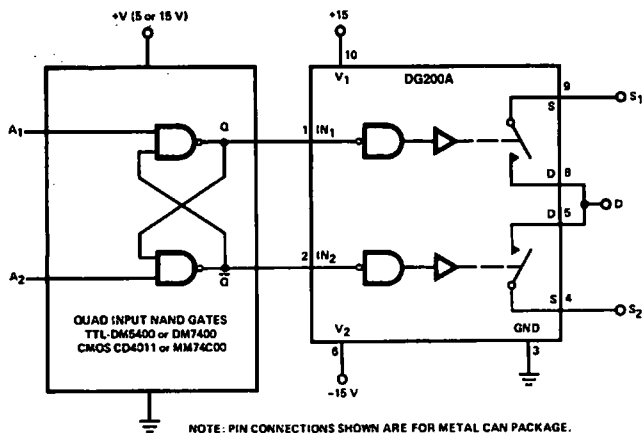
A Resettable Integrator

Figure 10

It is possible to operate a CMOS switch from a single supply by shifting the ground and logic inputs to an intermediate voltage, as shown in Figure 11. This allows an analog voltage range of 0 to +30 volts.



Operation from a Unipolar Supply
Figure 11



TRUTH TABLE

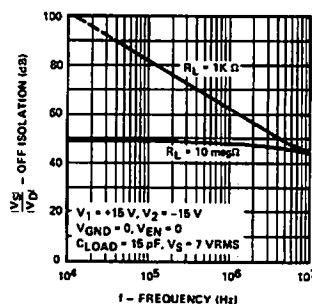
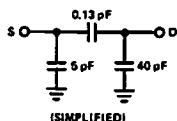
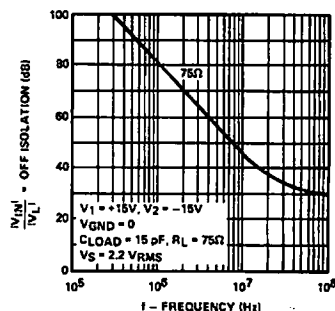
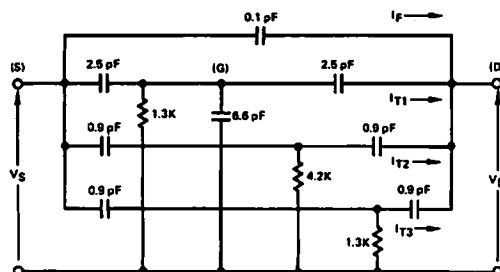
COMMAND		STATE OF SWITCHES AFTER COMMAND	
A_2	A_1	S_2	S_1
0	0 (normal)	same	same
0	1	OFF	ON
1	0	ON	OFF
1	1	INDETERMINATE	

A Latching SPDT
Figure 13

A latching SPDT switch is shown in Figure 13. This is recommended when the switch is activated by a peak or limit detector, or with mechanical switches (to eliminate contact bounce). The inputs are normally low, and the switches are held in predetermined states. When either A_1 or A_2 receive a HIGH pulse, the switches assume the states given in the truth table. Simultaneously holding A_1 and A_2 HIGH will cause both switches to be OFF; the last input to go low upon release of the commands will determine the eventual states of the switches.

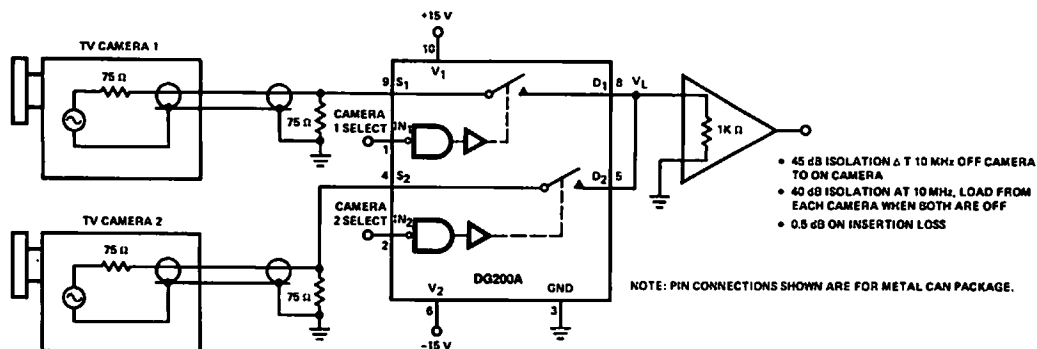
When switching high frequency signals (> 100 kHz), some knowledge of the OFF characteristics are helpful. Figure 14 shows the equivalent OFF circuit of a DG200A and the accompanying graph gives the isolation under the conditions specified. 40 dB isolation at 6 MHz is good for general purpose video switching. A DG200A can achieve this easily,

using the circuit shown in Figure 15 (assuming careful P.C. board layout). When greater isolation is needed, the circuit shown in Figure 16 is recommended. The "T" configuration provides over 40 dB more OFF isolation with only a slight increase in ON insertion loss.



Equivalent "OFF" Circuits and OFF Isolations
of the DG200A and DG506A

Figure 14



General Purpose Video Switch
(f = DC to 10 MHz)

Figure 15

Figure 14 also shows the high frequency characteristics of the DG506A and a simplified OFF equivalent circuit. The DG506A has OFF isolation which is constant when working into a capacitive load, allowing the designer to model the OFF DG506A as a capacitor of nominal value 1.13 pF. Not all sources have equal OFF isolation, however. S_g has the greatest isolation, while S_g is worse due to its proximity to the drain. Grounding the metal lid on the package (it normally floats) increases the isolation an average of 3 dB.

An in-depth study of switching high-frequency signals is presented in Siliconix applications note AN73-3, "Switching High Frequency Signals with FET Integrated Circuits."

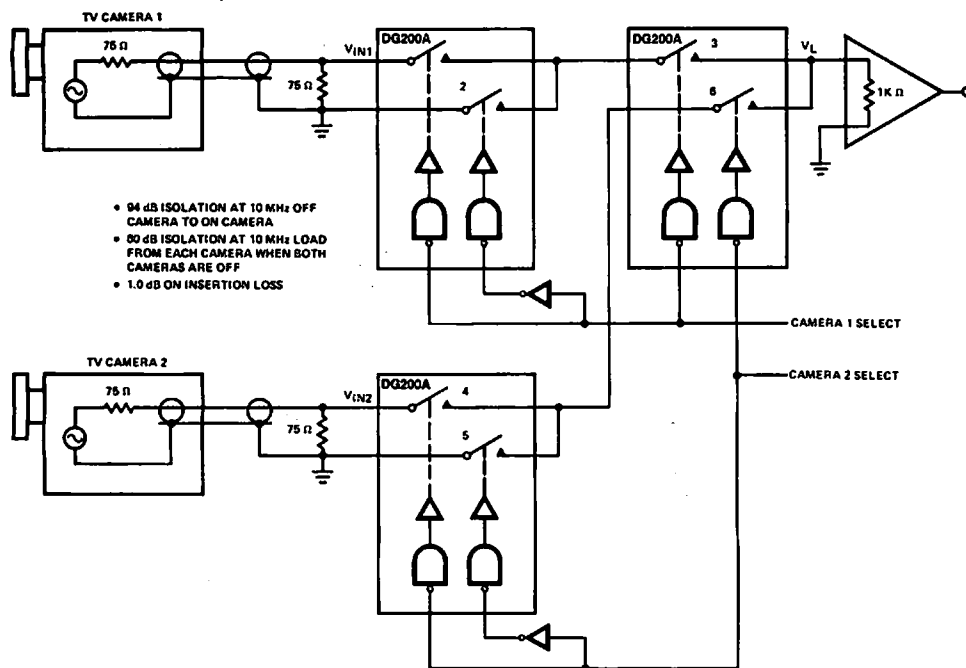
Multiplexing

Multiplexing allows a number of signals to be processed simultaneously through a single cable, amplifier, and data conversion system. Numerous industrial and commercial uses include factories and warehouses where conditions at remote parts of a building can be monitored and sent to a central control point over a single cable. Airplanes take great advantage of multiplex systems, both receiving and transmitting information from central points with a minimum of wire.

Many hotels and motels pipe up to 16 channels of music to each room. The music desired is selected by the guest in the room. When digitizing information, the economies are readily apparent between using a \$50 multiplex system and a single A to D converter, as compared to employing a separate expensive A to D converter for each of several channels.

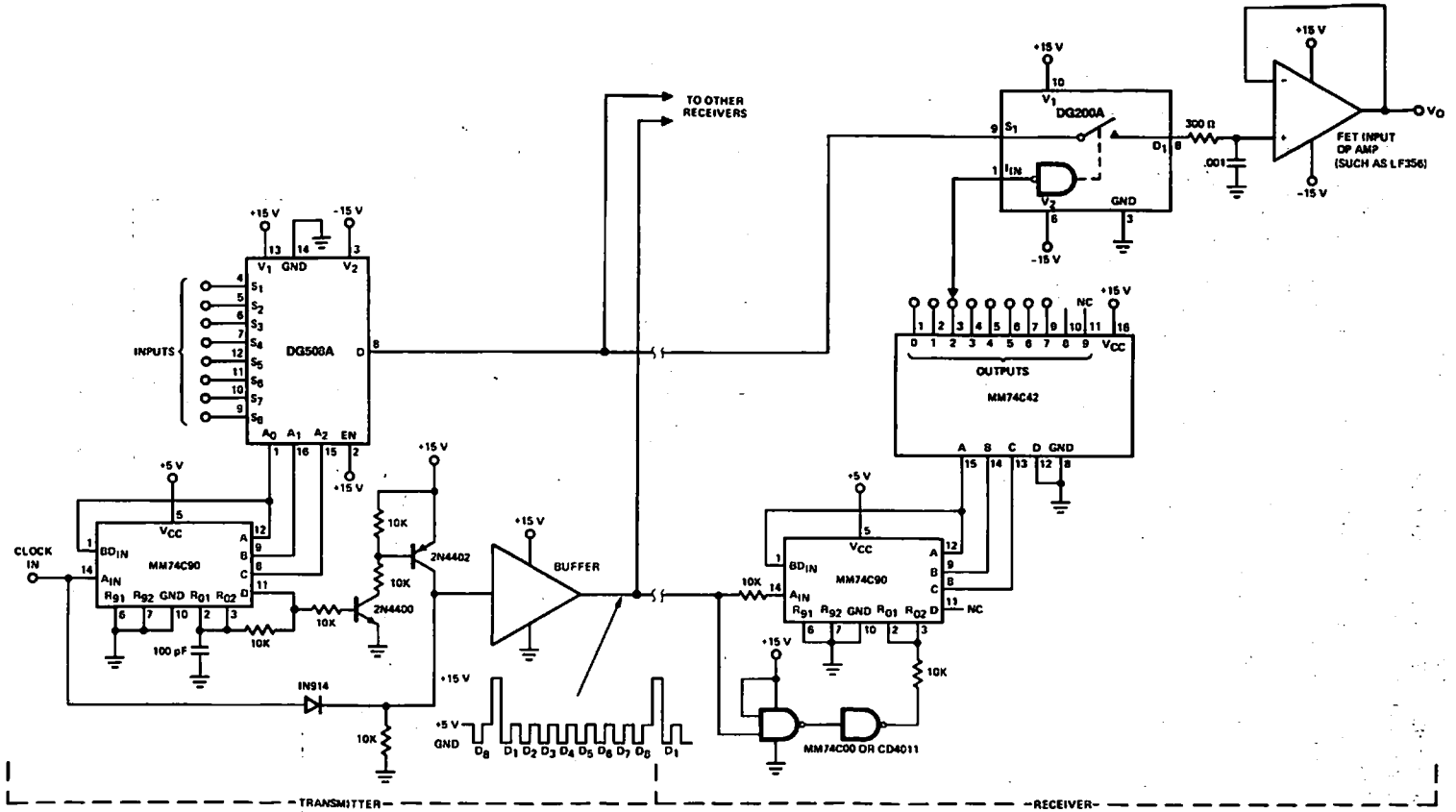
Figure 17 shows a typical multiplex system intended to carry one of 8 inputs into a remote location. A 5 V pulse train is sent down a separate channel to perform timing and synchronizing functions. A 15 V reset pulse is superimposed on the 5 V clock, which is detected by the MM74C00 in the receiver. Using this system, many remote points can be monitored, one at a time, at any of several locations.

A number of signals may be sent between two points simultaneously by making a slight modification in the receiver circuit (Figure 18). A second DG508A is used as a demultiplexer, allowing all 8 channels to be monitored continuously.



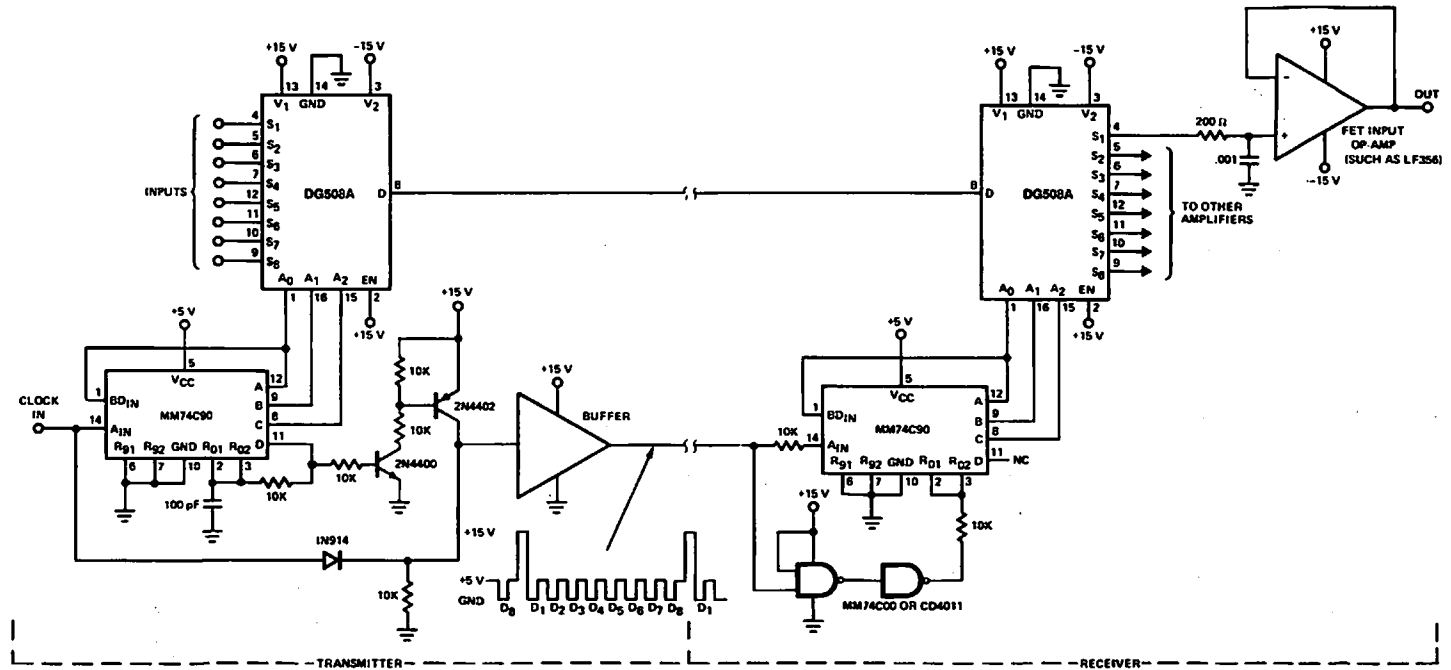
Video Switch with Very High OFF Isolation

Figure 16



A One of 8-channel Transmission System

Figure 17



An 8-channel Mux/Demux System
Figure 18

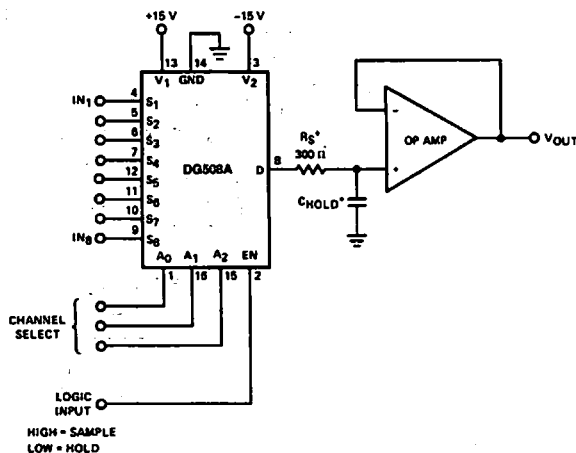
Often information is multiplexed into a conversion system which has a relatively slow processing time, necessitating a sample-and-hold after the multiplexer. Using the DG508A as a sample-and hold switch combines both functions, as shown in the "one of eight sample-and-hold" circuit (Figure 19).

Overvoltage

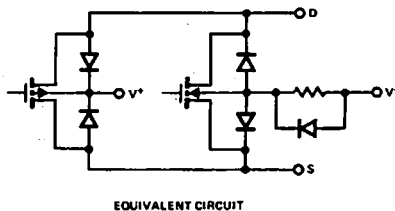
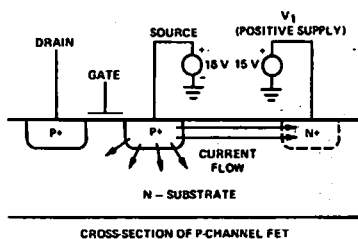
In certain applications the analog signal may exceed ± 15 V, or be present when the power supplies are off. This is a

condition known as overvoltage, and it can present problems unless certain precautions are taken.

When the analog voltage exceeds the supply voltage, the source-body junction will forward bias, as shown in Figure 20. Current will flow from the signal source into the supply. If the current source capability of the signal source and the current sink capability of the power supply are each greater than 20 mA, a resistor should be connected in series with source to limit the current.



A One of 8-channel Sample and Hold
Figure 19



Current Paths During an Over-voltage Condition
Figure 20

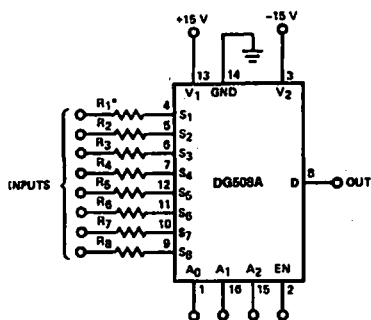
If the analog signal is present when the supplies are off, diodes in series with the supplies will allow the supply pins to float and prevent excessive current from flowing. A DG508A with full overvoltage protection is shown in Figures 21a and 21b.

2-Level Multiplexing

When a large number of channels are multiplexed, the outputs of two or more multiplexers can be connected together and each multiplexer sequentially enabled. In the INHIBIT mode the multiplexer draws less power and its output and inputs act as open circuits. Theoretically, an infinite number of channels can be accommodated in this way; in practice the accumulated output capacitance and leakage of many paralleled multiplexers limits the speed and accuracy of the system. A much better method is the two level multiplex system, shown in Figure 22. The two-level system has a bank of high speed switches at the output which sequentially switch between the 4 DG506A's. Each DG506A is able to switch during the time the other 3 are being interrogated, and they contribute leakage and capacitance at the output only when they are switched on by the DG181 (¼ of the time). This circuit has several important advantages over a multi-unit single-level system, such as:

1. The switching speed of the system is dependent on the DG181, which is a high-speed 2-channel SPST ($t_{ON} \approx 150$ nsec). The slower switching time of the DG506A (≈ 1 μ sec) is not important because this switching transition can take place while the other DG506A's are being interrogated. In this way a very fast multiplex system can be made with a large number of low-cost, moderate-speed multi-channel multiplexers and several high speed SPST switches.
2. The output capacitance of the 2-level system is much lower than that of the single level. It consists of a single DG506A (40 pF) and several DG181's (6 pF OFF, 15 pF ON) which is much less than several DG506A's in parallel. If 64 channels are multiplexed, for instance, C_{OUT} of the 2-level system would be 72 pF, vs 160 pF for the single-level system.
3. The output leakage current is reduced by a similar amount. (From ± 40 nA to ± 10 nA in a 64-channel system).

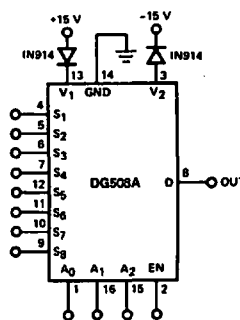
The two level multiplex system is very useful in communications links, high speed interfacing with comparators, or wherever a large number of channels must be multiplexed at high speeds.¹



* R_1 THROUGH $R_8 = \frac{\text{EXPECTED OVERVOLTAGE} - 15 \text{ V}}{20 \text{ mA}}$
EXAMPLE: $R = 250\Omega$ WHEN $V_S(\text{MAX}) = 20 \text{ V}$

(A)

A DG508A protected against analog signals which exceed 15V.

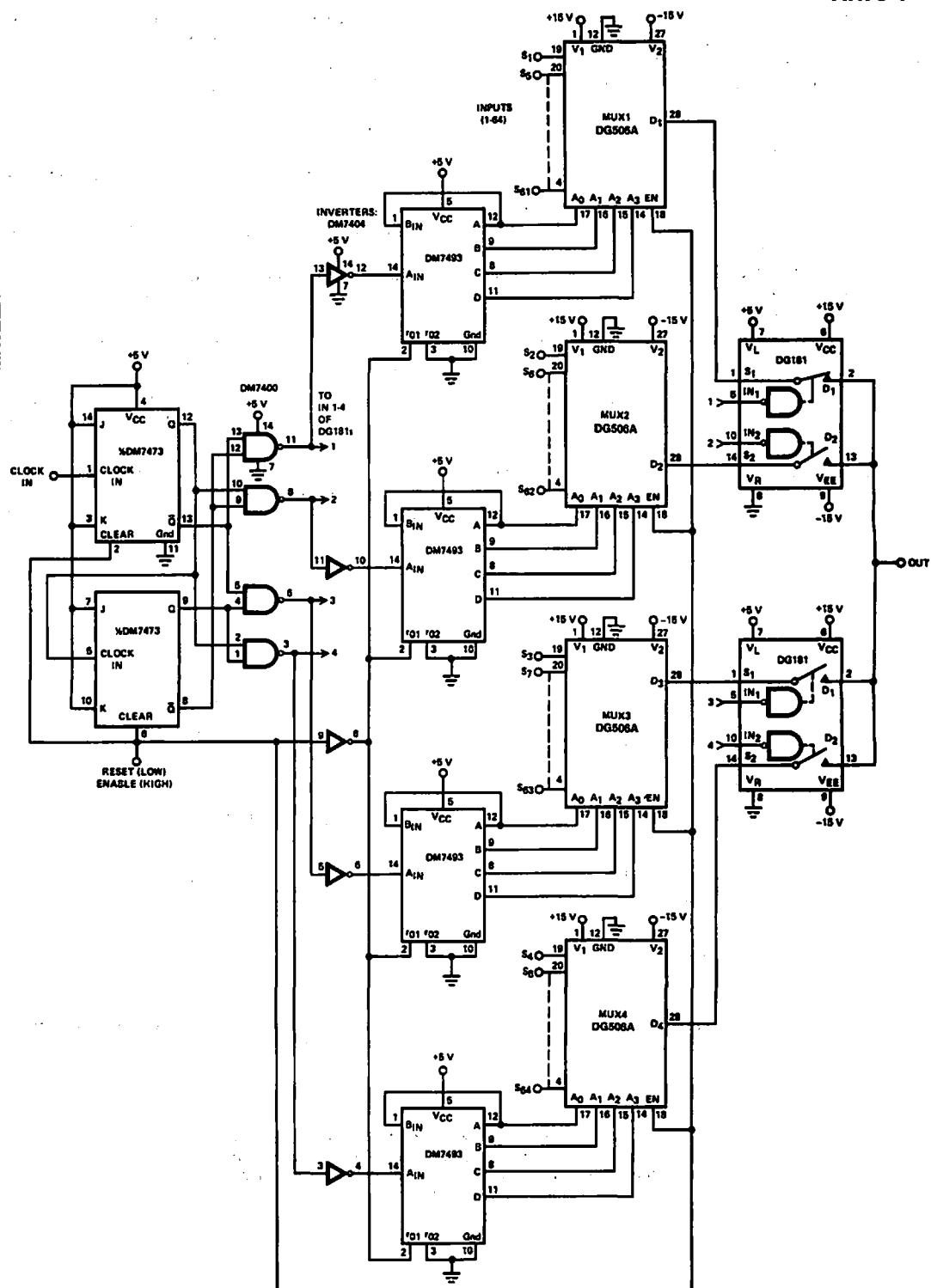


(B)

A DG508A protected against analog voltages being present when the power supplies are off.

Over-voltage Protection (shown for DG508A) is Normally Used Only When the Analog Voltage Exceeds the Power Supply Voltages, and the Signal Source is Capable of Generating Greater Than 20 mA

Figure 21



64-Channel 2-Level Multiplex System

Figure 22

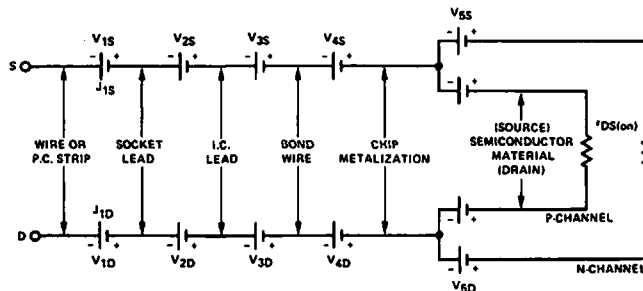
Low Level Multiplexing

When multiplexing low level signals, extra care must be used because the signal may be masked by A.C. noise pickup and D.C. voltages generated by thermocouple effects at the connections of dissimilar metals. Much greater accuracy is obtained if the signal is handled differentially, so that A.C. noise and D.C. thermocouple effects appear as common-mode signals which can eventually be rejected. For this reason a line of differential multiplexers is available which allows improved thermal tracking and differential cancellation of leakage and switching glitches.

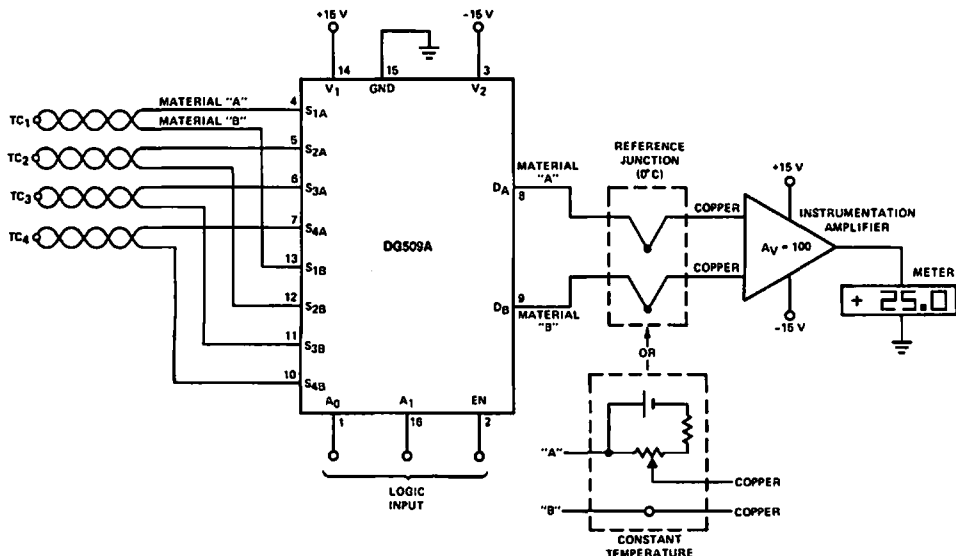
Figure 23 shows a thermocouple representation of a typical multiplexer mounted in a socket. If connection J_{1S} is at the same temperature as connection J_{1D} , then $V_{1S} = V_{1D}$. If all "S" junctions are at the same temperature as the corresponding "D" junctions, the total voltage across the multiplexer is zero. Conversely, if a temperature imbalance exists

between side "S" and side "D" then the voltages will not exactly cancel and a net error voltage will appear. For this reason the multiplexer and associated connections should be mounted in a thermally-stable environment, away from hot components and with as few drafts around the chip as possible. When a DG509A is mounted in a thermally-stable environment, the typical error developed across the switch is about $\pm 3 \mu V$ over the operating temperature range of the device. In free air, with random room drafts, it can be as high as 7 to 10 μV . When heated with a thermal probe at 85°C (resulting in uneven temperatures across the device) the absolute voltage across a switch is about 100 μV with a 30 μV differential error. I.C. multiplexers are therefore ideal in low level applications if care is exercised to insure an even temperature.

Figure 24 shows a DG509A thermocouple multiplexer. To decouple the sensors from the meter amplifier, either a



Thermocouple Representation of a Typical Multiplexer Switch
Figure 23



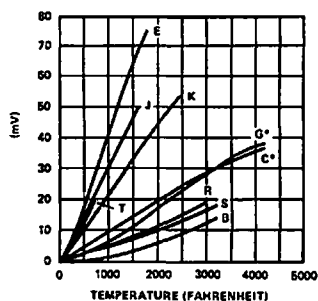
A Thermocouple Multiplex System
Figure 24

reference junction at 0°C or a bucking voltage set at room temperature may be used. The latter method is simpler, but is sensitive to changes in ambient temperature. Table I shows the output of several common types of thermocouples vs temperature.²

REFERENCES

- (1) J.O.M. Jenkins, "IC Multiplexer Increases Analog Switching Speeds," Siliconix Application Note AN73-2, February 1973.
- (2) The Omega Temperature Measurement Handbook (1975), Omega Engineering, Inc., Stamford, Conn.

Table I
Output Voltage vs Temperature of
Several Common Thermocouples

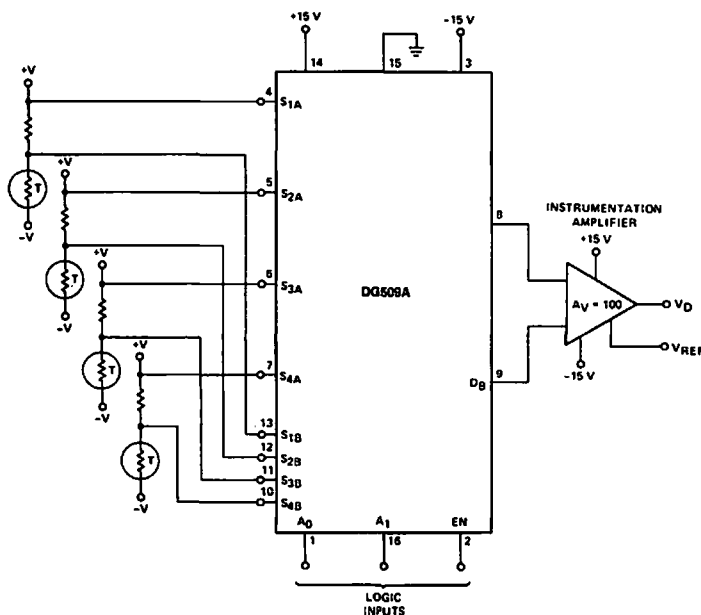


ANSI SYMBOL

T	Copper vs Constantan
E	Chromel vs Constantan
J	Iron vs Constantan
K	Chromel vs Alumel
G*	Tungsten vs Tungsten 26% Rhenium
C*	Tungsten 5% Rhenium vs Tungsten 26% Rhenium
R	Platinum vs Platinum 13% Rhodium
S	Platinum vs Platinum 10% Rhodium
B	Platinum 6% Rhodium vs Platinum 30% Rhodium

*Not ANSI Symbol

Used with permission of Omega Engineering, Inc., Stamford, Conn., 06907



Thermistor Differential Multiplexing
Figure 25

DG300A Series Analog Switch Applications

Thomas J. Mroz

Revised December 1984

INTRODUCTION

To round out its analog switch line, Siliconix has introduced the DG300A to DG307A analog switch family. The DG300A to DG307A switches were designed to approach the industry standard DG180 family of JFET switches in performance while keeping the economy and low power of CMOS circuitry, and offer fast switching (typically < 150 ns) and low ON resistance (< 50 Ω). Four switch functions, (dual SPST, SPDT, dual DPST, dual SPDT) are offered with TTL or CMOS compatible logic input options. The low ON resistance, fast switching speed and low power of these switches makes the DG300A family an excellent choice for sample and hold, Digital-to-Analog Converters, and multiplexing elements as well as other applications requiring low offsets, fast charging of capacitors and fast switching of analog signals. The SPDT functions offer break-before-make action which aids in simplification of system design.

DG300A Family Switch Structure

Figure 1 shows a partial schematic of a DG300A switch.

Device Q_1 along with the zener diode provide the input protection. This is accomplished by Q_1 being turned off

whenever the input voltage exceeds the positive supply (V_1) and by the zener breakdown whenever the input goes more negative than $V_1 - V_{ZENER}$. Q_2 and Q_3 form the first input buffer and are designed to set the proper input threshold. The DG300A to DG303A thresholds are typically between 1.5 and 2.5 volts and are designed to interface with TTL gates employing pullups to +5 V. These switches can also be driven from CMOS gates using 5 to 15 volt supplies. If 15 volt CMOS drive is available, faster switching can be accomplished by using the CMOS input DG304A to DG307A switches.

DG304A to DG307A switch inputs have thresholds typically between 4 volts and 6 volts with ± 15 V supplies and are designed to interface with inputs switching between ground and the +15 V supply. Q_4 through Q_{15} form additional buffers and create the necessary driving voltages for the switch devices, Q_{16} through Q_{19} . Q_{17} and Q_{18} are referred to as being body snatchers, not because of midnight escapades, but because they connect the body of Q_{19} to either its source or the negative supply. This reduces the ON resistance and the OFF leakage of this device.

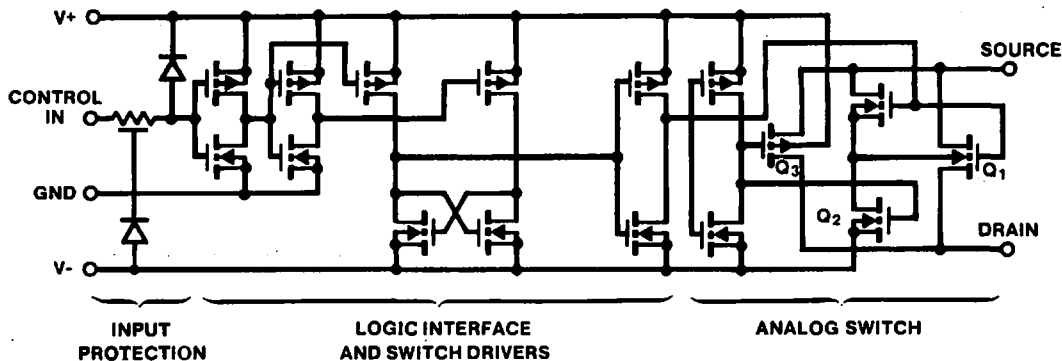
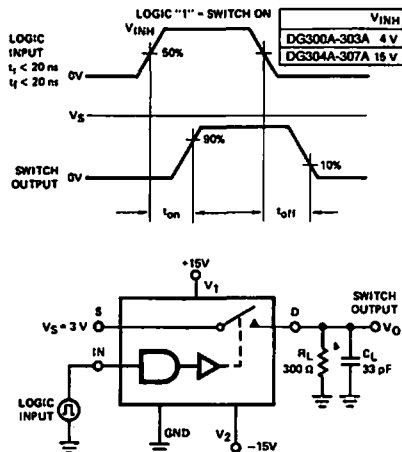


FIGURE 1

PERFORMANCE CHARACTERISTICS

Switching Time

In measuring switching time it is important to remember that the turn-off time as seen at the load is highly dependent on the load time constant. The switching time test circuit is shown in Figure 2 below.

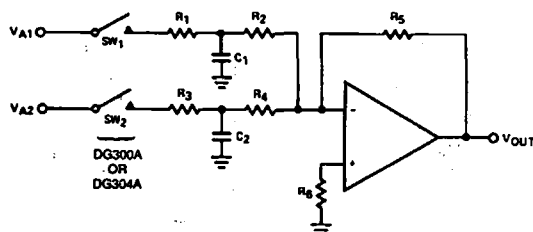


Switching Time Test Circuit
Figure 2

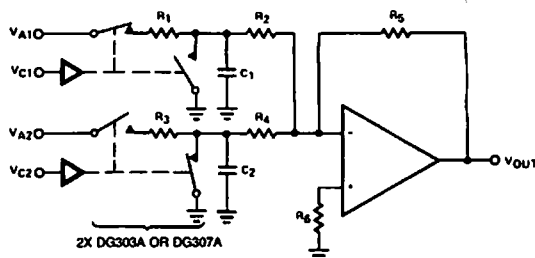
Turn-on time in the circuit shown in Figure 2 is governed primarily by the logic delay path and the $r_{DS(ON)}$ of the switch. The $r_{DS(ON)}$, C_{LOAD} time constant is normally shorter than the $R_L C_L$ time constant. The two time constants are:

$$\frac{r_{DS(ON)} \times R_L}{r_{DS(ON)} + R_L} \times C_L \text{ for } t_{ON} \text{ and } R_L \times C_L \text{ for } t_{OFF}$$

These two time constants determine rise and fall times of the analog switch. When the switch is driving a high impedance, high capacitance load such as that shown in Figure 3, which is the input of a summing amplifier having some noise filtering, it may be necessary to add a second switch (Figure 4) for rapid discharge of the filter capacitor thus preventing offsets from occurring at the summing amplifier output.



Summing Amplifier
Figure 3

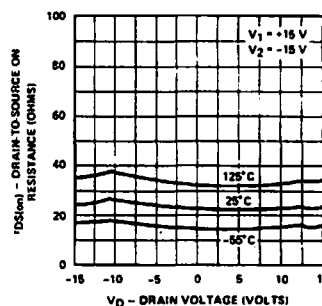


Improved Summing Amplifier
Figure 4

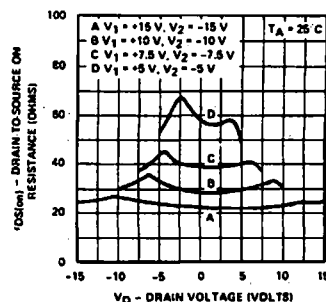
Channel ON Resistance

Another important specification of an analog switch is the channel ON resistance, $r_{DS(ON)}$. The $r_{DS(ON)}$ of the DG300A family of switches is typically below 40 ohms over the operating temperature range.

The two figures below show variations of $r_{DS(ON)}$ with respect to temperature (Figure 5) and supply voltage applied to the switches (Figure 6).



$r_{DS(on)}$ vs V_D and Temperature
Figure 5



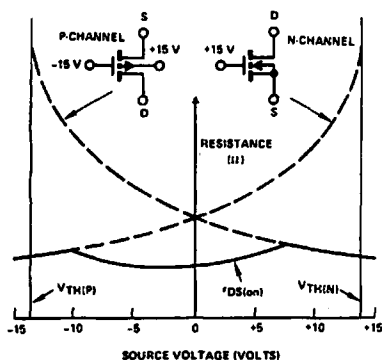
$r_{DS(on)}$ vs V_D and Power Supply Voltage
Figure 6

As shown by Figure 5, $r_{DS(ON)}$ increases as temperature increases. This is a typical FET characteristic due to the decreasing conductivity of silicon as temperature increases.

This decrease in conductivity is due to the shortening of the mean free path seen by the majority carriers of the device. The change of switch resistance with respect to temperature is approximately $0.1 \Omega/^{\circ}\text{C}$.

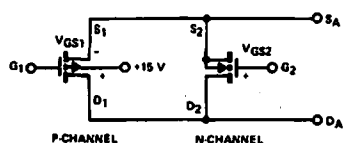
Figure 6 also shows $R_{DS(on)}$ variations with respect to analog signal voltage as a function of supply voltages. Supply variations are important because the maximum gate drive available for the switch output devices is determined by the supply voltages. Thus the change in $r_{DS(ON)}$ is proportional to the change in supply voltage.

The variation of $r_{DS(ON)}$ with respect to the analog voltage is due to the variation in the gate-source voltage of the "ON" switches as shown in Figure 7.



Resistance vs Source Voltage of P-Channel and N-Channel FETs
Figure 7

In Figure 8, the complementary output pair (for illustrative purposes) is shown in a very basic schematic. When the switch is ON, G_1 is tied to the negative supply and G_2 is tied to the positive supply. $V_{D1} = V_{S1} = V_{D2} = V_{S2}$. In order to understand the variation of $r_{DS(ON)}$ with respect to analog voltage, the complementary pair will be broken apart and the $r_{DS(ON)}$ of each device with respect to analog voltage examined.



Complementary Output Devices (Simplified)
Figure 8

As Figure 7 indicates, the N-channel device with its gate tied to +15 V, begins to turn ON as its source voltage drops a threshold voltage below +15 volts. Thus as the analog voltage decreases from +15 volts to -15 volts, V_{GS} increases from 0 volts to 30 volts increasing the channel conductivity. The P-channel device has its gate tied to -15 volts, thus as the analog signal increases from -15 volts to +15 volts, its V_{GS} goes from 0 volts to -30 volts. This results in a decreasing

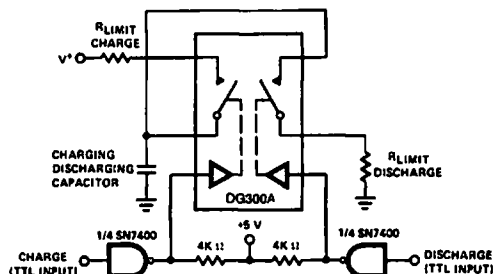
channel resistance. The switch resistance is the parallel combination of these two devices and the bottom curve in Figure 7 results.

APPLICATIONS

The DG300A series of analog switches having fast switching and low $r_{DS(ON)}$ lend themselves to applications such as sample and hold and high speed multiplexing. Low $r_{DS(ON)}$ also means small offsets when switching integrators or amplifiers. Nearly constant ON resistance also means lower distortion when switching into lower impedance loads.

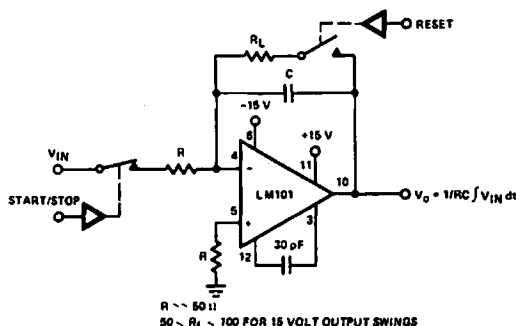
Charging and Discharging Capacitors

When charging or discharging capacitors, it is important not to exceed maximum ratings of the switch. Current through the switch must be limited to 30 mA continuous or a 100 mA pulse for 1 millisecond or less having a 10% duty cycle. Exceeding maximum ratings could mean poorer reliability than could otherwise be expected. One method of preventing excessive current is by using current limiting resistors in series with the switch as shown in Figure 9. If voltage differentials between the switch input and the capacitor are small, these resistors may not be necessary because the switch resistance itself would be sufficient to limit current.



Using Current Limiting Resistors in Capacitive Charge/Discharge Circuits
Figure 9

In the integrator of Figure 10, R_L controls the discharge rate of the capacitor. During reset to zero volts, the reset switch is closed and the start/stop switch is open. Opening the start/stop switch with the reset open will hold the output of the integrator at its present value.



Integrator With Analog Reset and Start/Stop Capability
Figure 10

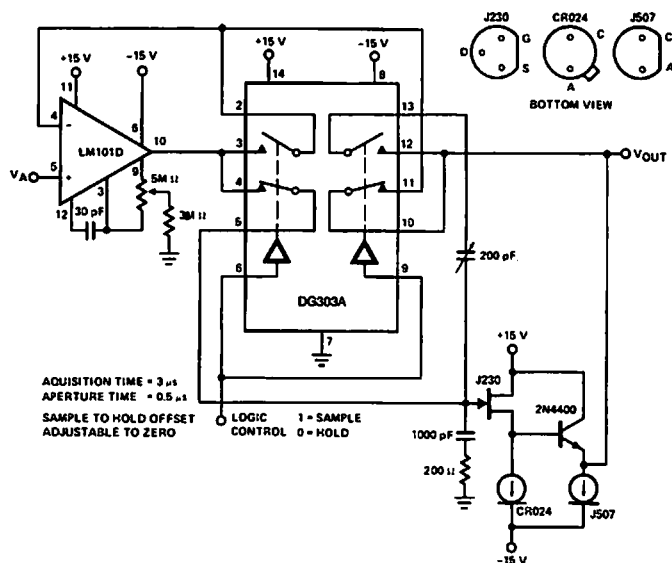
Charge Cancellation

Figure 11 shows a sample and hold circuit using the DG303A dual SPDT switch. Any analog switch when opened will inject charge into the source and drain nodes due to gate to source and gate to drain capacitance. This charge when injected into a sample and hold capacitor will create offset errors in the sample and hold output during hold. This error can be eliminated using another switch to inject charge into a small storage capacitor (200 pF) during the same period which is then subtracted off during the hold period.

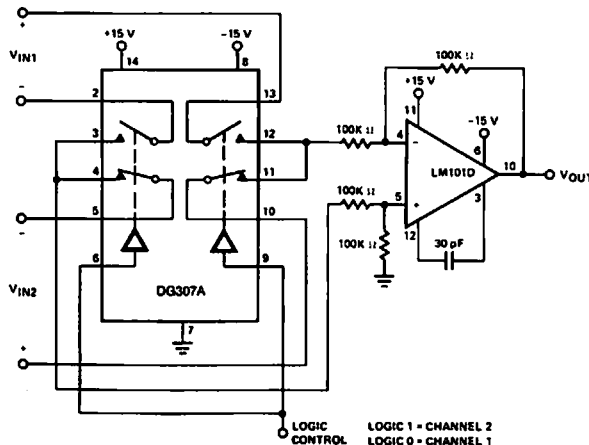
Fast switching times and low $r_{DS(ON)}$ of the DG303A allow fast data acquisition with acquisition times of $3 \mu s$ possible.

Fast Data Multiplexing

Having high switching speed, the DG300A series switches are ideal for fast multiplexing of data. Figures 12, 13, and 14 are applications of various DG300A switches employing their high speed in switching data.



Sample and Hold
Figure 11



Basic Switched Differential Amp
Figure 12

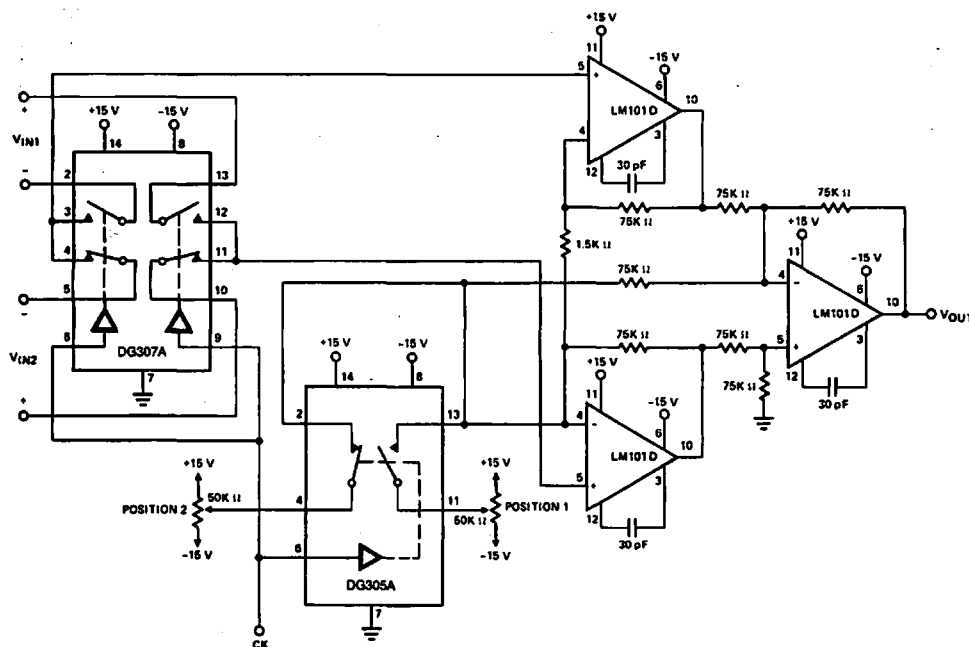
The high switching speed of the DG304A is taken advantage of in the 64-channel two level multiplex system of Figure 14. This circuit employs 4 each DG506A 16-channel multiplexers as the first MUX level and uses the high speed DG304A's in the second level to switch between DG506A outputs. CMOS digital logic forms the address logic for the multiplexers as well as the DG304's.

As one multiplexer is being sampled at the output, the other multiplexers are being switched to the next address line. This allows the overall system transition time to be shortened from $1.5 \mu\text{sec}$ to $0.25 \mu\text{sec}$. The two level system also lowers output node capacitance and output leakage (refer to Reference 5 for details).

Battery or Low Power Applications

The DG300A series of switches are inherently Low Power and are ideal candidates for applications using battery supplies. Figure 15 shows the variation of device power dissipation versus the switching frequency of the switch. It can be seen that in low frequency switching the power dissipation is negligible. One application for which this switch is ideal is in autoranging circuits for battery operated Digital Volt Meters.

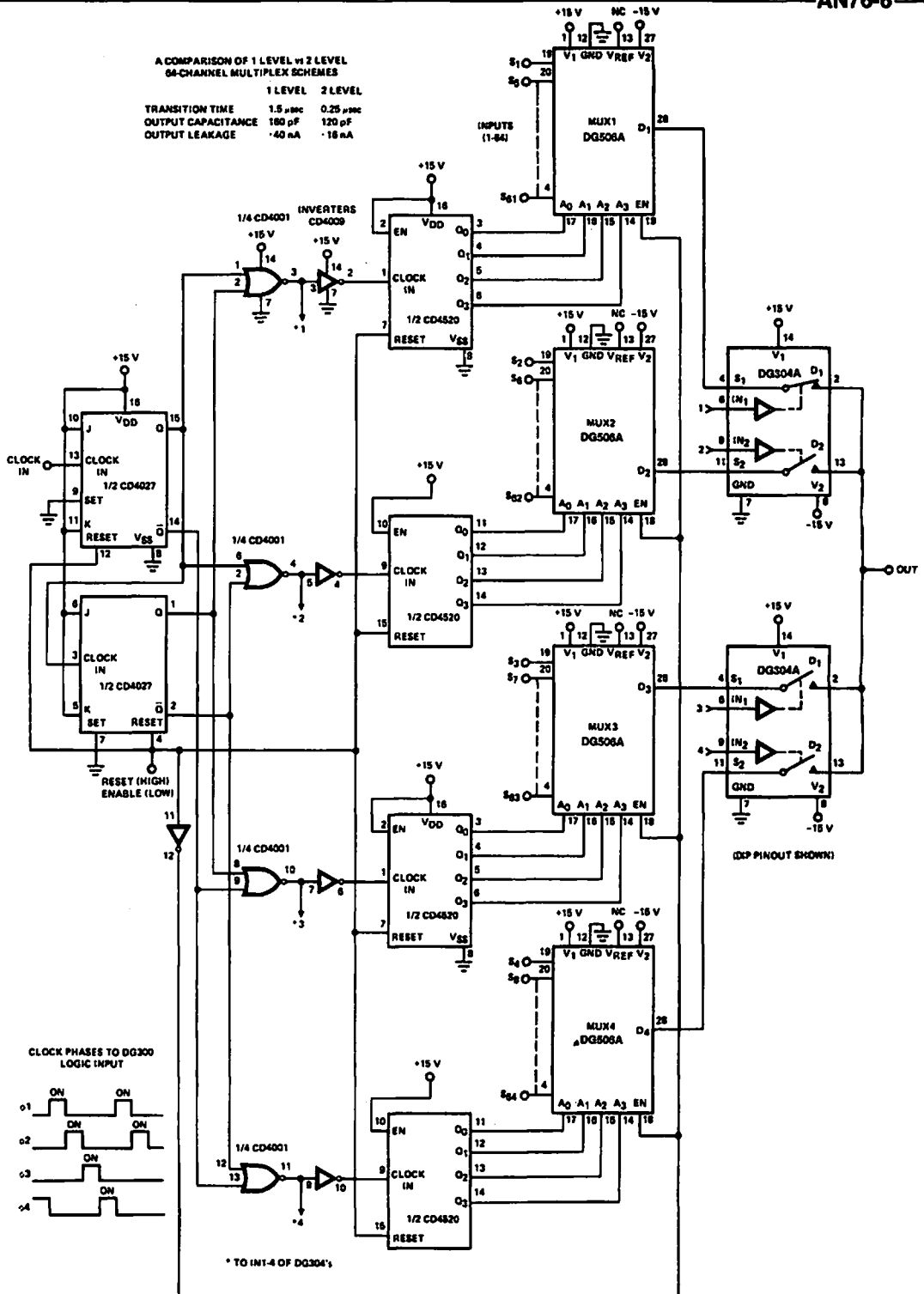
Figure 16 is the schematic of a binary addressed amplifier in which the gain increases by decades as the binary input decreases from 1,1 to 0,0. Its minimum gain, as shown in the table, is 1 and its maximum gain is 1000. Since the switch is static in this type of amplifier the power dissipation of the switch will be less than a tenth of a milliwatt.



2-Channel to 1-Channel Chopping Differential Amplifier
With Position Adjustment
Figure 13

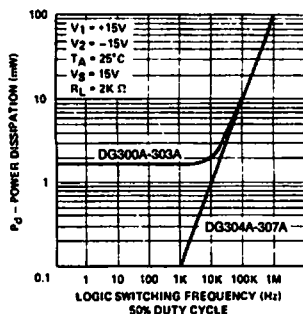
A COMPARISON OF 1 LEVEL vs 2 LEVEL
64-CHANNEL MULTIPLEX SCHEMES

	1 LEVEL	2 LEVEL
TRANSITION TIME	1.5 μ sec	0.25 μ sec
OUTPUT CAPACITANCE	180 pF	120 pF
OUTPUT LEAKAGE	40 nA	18 nA

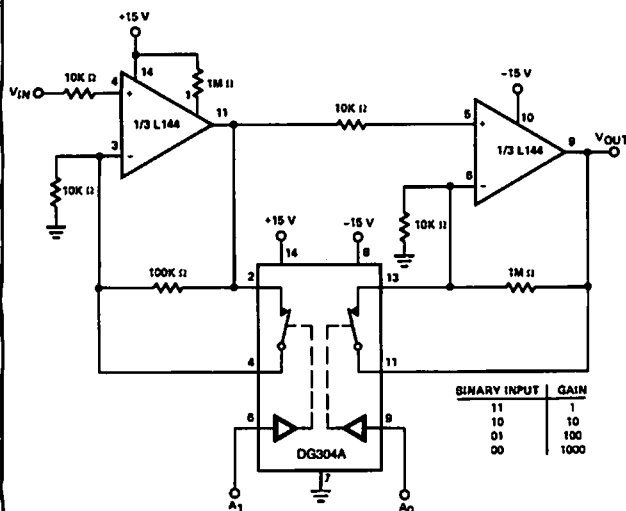


64-Channel 2-Level Multiplex System Using
DG304A as High Speed Switches

Figure 14



Device Power Dissipation vs Switching Frequency
Figure 15



Low Power Binary to 10^n Gain
Low Frequency Amplifier
Figure 16

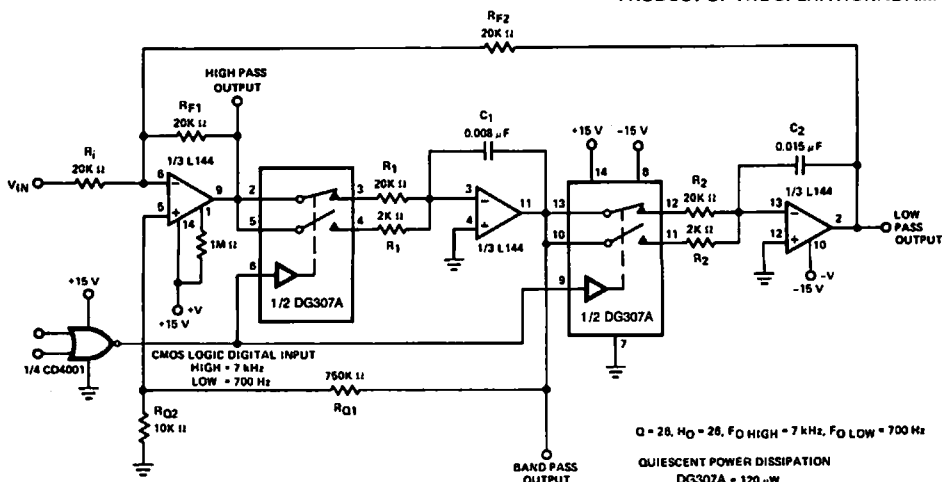
The low power of the DG307A also makes it ideal for use with the low power programmable triple op amp, the L144, in an active filter. Figure 17 shows the use of the DG307A in a switchable center frequency active filter, allowing a decade change in center frequency. Additional information on the L144 and the active filter circuit can be found in References 6 and 7.

Table 1
Design Procedure for the State Variable Active Filter
Given: f_0 (Resonant Frequency),
 H_0 (Gain at the Resonant Frequency) and Q_0
STANDARD DESIGN
(Assumes Infinite Op-Amp Gain)

1. CHOOSE $C_1 = C_2 = C$, A CONVENIENT VALUE
2. LET $R_1 = R_2 = R$
3. THEN $R = \frac{1}{2\pi \times f_0 \times C}$
4. CHOOSE $R_{11} = R_{12} = KR$,
WHERE $R_{11}, R_{12} = A$ CONVENIENT VALUE
AND $K = \frac{H_0}{Q_0}$
- IF H_0 IS UNIMPORTANT (i.e., GAIN CAN BE
ADDED BEFORE AND/OR AFTER THE
FILTER), CHOOSE $K = 1$
5. LET $R_{Q1} = A$ CONVENIENT VALUE
6. THEN $R_{Q2} = \frac{R_{Q1}}{(2 + K) \times Q_0 - 1}$

$A(f_0)$ = THE NOMINAL OP AMP GAIN AT
THE RESONANT FREQUENCY.

GBWP = THE NOMINAL GAIN-BANDWIDTH
PRODUCT OF THE OPERATIONAL AMPLIFIER.



Low Power Active Filter With Digitally
Selectable Center Frequency
Figure 17

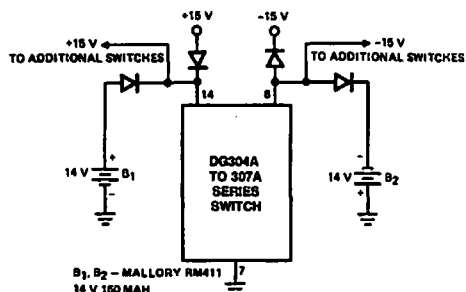
$Q = 28, H_0 = 28, f_0 \text{ HIGH} = 7 \text{ kHz}, f_0 \text{ LOW} = 700 \text{ Hz}$

QUIESCENT POWER DISSIPATION
DG307A = 120 μW
L144 = 18 mW

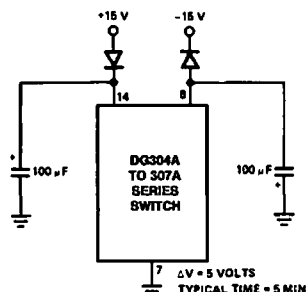
An advantage of the DG304A to DG307A family of switches due to their low power consumption is the ability to use batteries or capacitors to supply standby power to the switch. In this way errors at analog output and shorting of signals can be avoided when supply power fails. This method would also prevent loading

of the analog signal by the switch which could prevent the use of could prevent the use of the signal in other portions of a system. Figures 18 and 19 show methods of implementing standby power.

Battery lifetime should be well over 1 year with continuous standby.



Long Term Supply Standby
Figure 18

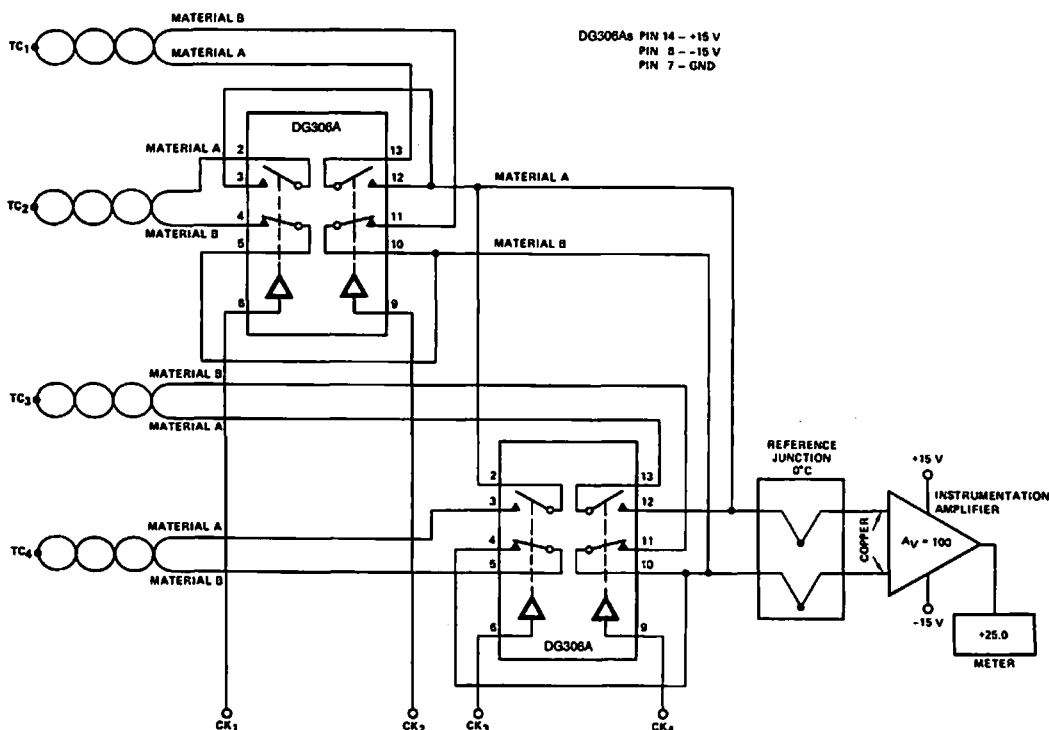


Short Term Supply Standby
Figure 19

Thermocouple Applications

Because silicon in contact with aluminum creates a thermocouple, low power dissipation by the integrated analog switch will mean lower offset voltages added to the thermocouple voltage. Thus, lower power dissipation translates into better potential accuracy. The DG300A series of analog switches do quite well in this type

of application. Figure 20 shows a typical schematic of a thermocouple switching circuit. It is necessary to switch the thermocouples differentially in order to cancel any thermal offsets due to the switch.

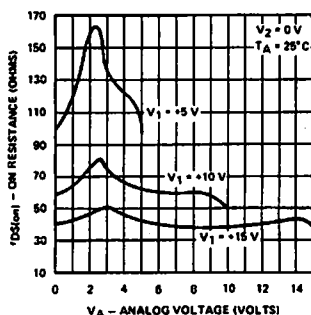


Thermocouple Multiplexing
Figure 20

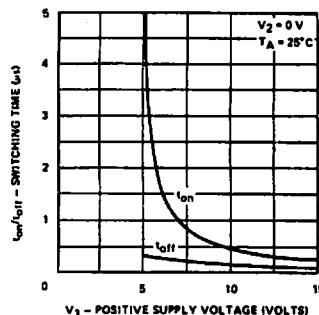
Single Supply Operation

The DG300A series of analog switches will switch positive analog signals while using a single positive supply. This will allow use in many applications where only one supply is available. The trade-offs or performance given up while using single supplies are: 1) Increased $r_{DS(on)}$; 2) slower switching speed. Typical

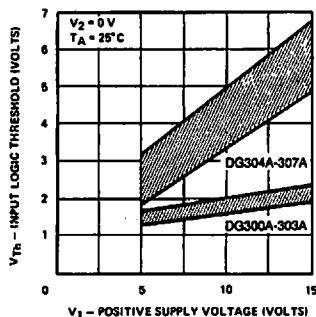
curves for aid in designing with single supplies are supplied in Figures 21 to 23. As stated in the absolute maximum ratings section of the data sheet, the analog voltage should not go above or below the supply voltages which in single supply operation are V_1 and 0 volts.



$R_{DS(on)}$ vs Analog and Positive Supply Voltage
With $V_2 = 0$ V
Figure 21



Switching Time vs V_1 - Positive Supply Voltage
Figure 22

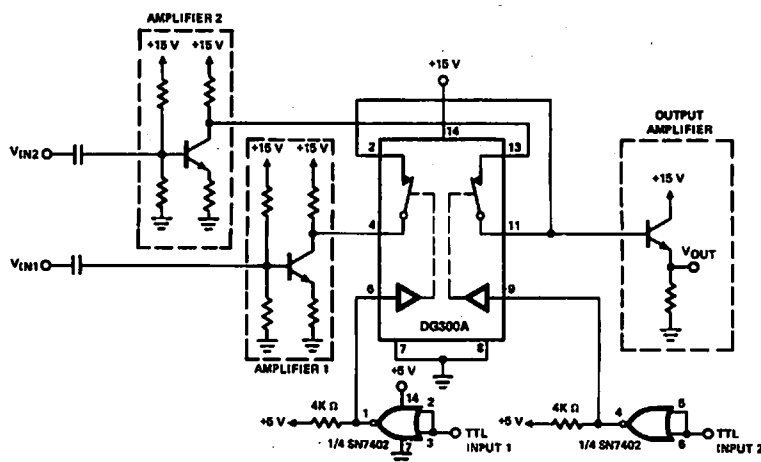


Input Threshold Voltage vs Positive Supply
Figure 23

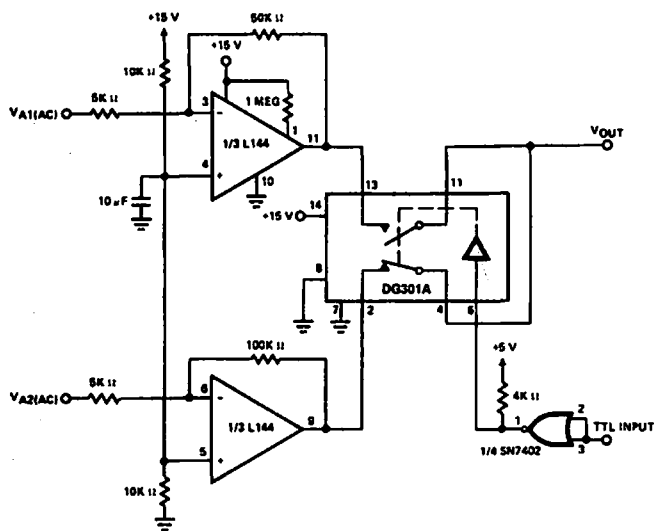
Single Supply Range:
(V_2 and GND Tied Together)
 V_1 : +5 V to +25 V

Analog Signal Range:
 $V_2 < V_{ANALOG} < V_1$

Figure 24 and 25 demonstrate methods of interfacing analog switches to single supply DC coupled amplifiers.



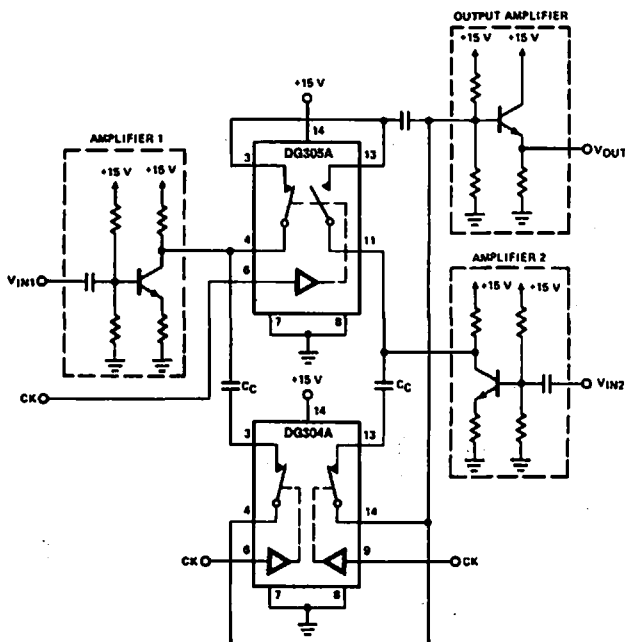
Switching Single Supply Amplifiers Using the DG300A
Figure 24



Single Supply Op Amp Switching
Figure 25

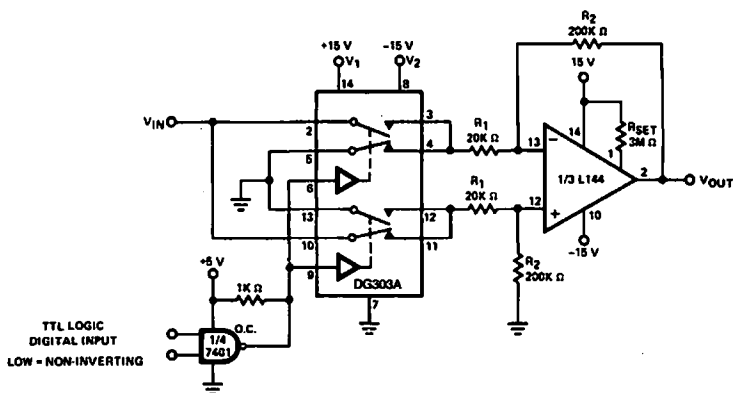
As shown in Figure 26 when switching capacitor-coupled analog signals, the coupling capacitor should appear either before or after but not on both sides of the switch. This is necessary to keep a

positive bias on the switch drain and source when the switch is turned on.

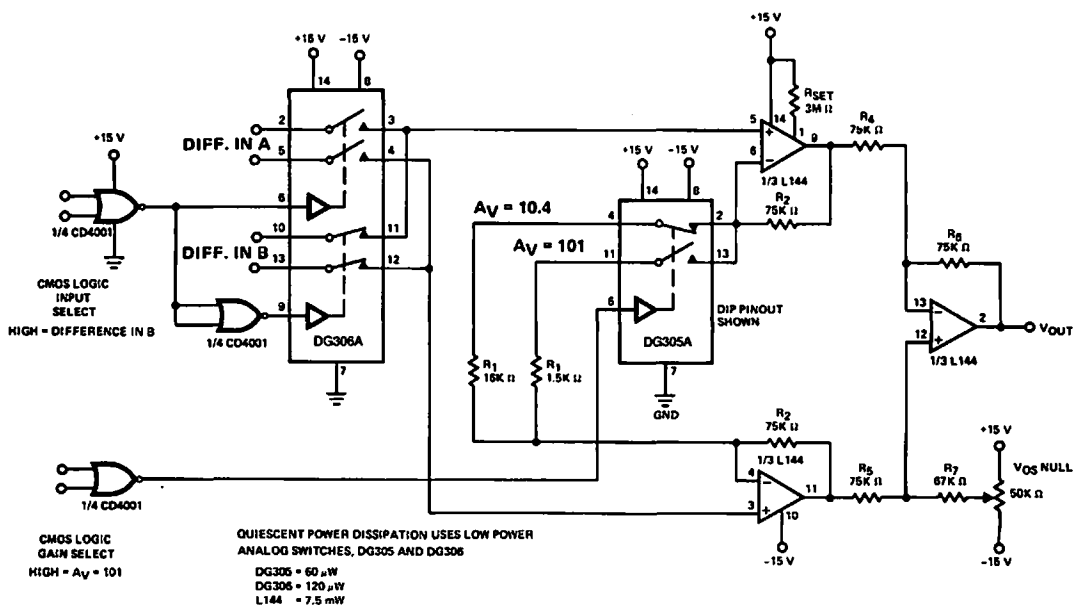


Proper Methods for Interfacing Capacitive Coupled
Outputs to Analog Switches
Figure 26





Polarity Reversing Low Power Amplifier
Figure 29



R_{SET} programs L144 power dissipation, gain-bandwidth product.
Refer to AN73-6 and the L144 data sheet.

Voltage gain of the instrumentation amplifier is:

$$A_V = 1 + \frac{2R_2}{R_1} \quad (\text{In the circuit shown, } A_{V1} = 10.4, A_{V2} = 101)$$

**Low Power Instrumentation Amplifier with
Digitally Selectable Inputs and Gain**
Figure 30

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1. Lee Shaeffer, "CMOS Analog Switches - A Powerful Design Tool," Siliconix Application Note AN75-1, July 1975.
2. Gary Dixon, "Analog Switches in Sample and Hold Circuits," Siliconix Application Note AN74-2, Jan. 1976.
3. Gary Grandbois, "Build an Autoranging DMM with the LD130 A/D Converter," Siliconix Design Aid DA76-3, June 1976.
4. "Siliconix Analog Switch Data Book," June 1976.
5. J. Jenkins, "IC Multiplexer Increases Analog Switching Speeds," Siliconix Application Note AN73-2, April 1976.
6. Marvin K. Vander Kooi, "L144 Programmable Micro-Power Triple Op Amp," Siliconix Application Note AN73-6, Jan. 1975.
7. Lee Shaeffer, "Op Amp Active Filters - Simple to Design Once You Know the Game," EDN Magazine, April 20, 1976.

The DG308A Digitally Switches Analog Signals

Walt Heinzer
September 1983

INTRODUCTION

The latch proof CMOS DG308A interfaces easily to system power supplies since it operates from $\pm 5\text{V}$ to $\pm 15\text{V}$, or it operates with a single supply from $+5\text{V}$ to $+25\text{V}$, all CMOS logic compatible. Additionally, the DG308A consumes negligible standby power and can switch in less than 200 ns. To minimize analog signal error the DG308A has a maximum $R_{DS(ON)}$ of 100Ω over the full analog signal range which extends to the positive and negative power supply, at the same time OFF state signal errors are kept small by low leakage currents.

MORE ABOUT THE DG308A:

One channel of the four channel DG308A is shown in Figure 1 which displays the input protection, logic interface, internal level shifting and switch contact circuitry. With $V_+ = 15\text{V}$ and $V_- = -15\text{V}$, a logic "1" control input ($V_{IH} = 11\text{ volt minimum}$) will close the switch, and a logic "0" ($V_{IL} = 3.5\text{ volt maximum}$) will open the switch. The ON resistance of the switch over the analog signal range has the characteristic double peaked curve shown in Figure 2. The OFF resistance plotted as a leakage current in Figure 3, combined with the ON resistance characteristic of Figure 2, guarantees full ON/OFF operation between the V_+ and V_- ($\pm 15\text{V}$) power supply rails.

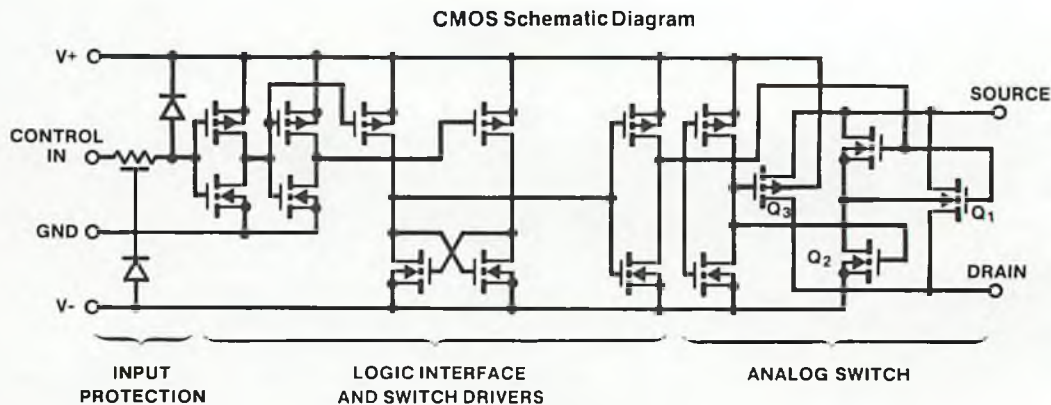


FIGURE 1

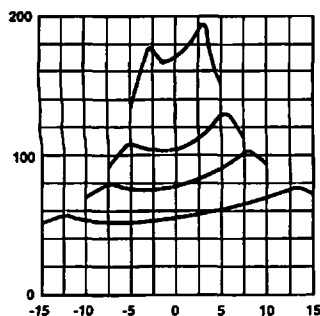
DG308A: $R_{DS(ON)}$ VERSUS V_D
AND POWER SUPPLY VOLTAGE

FIGURE 2

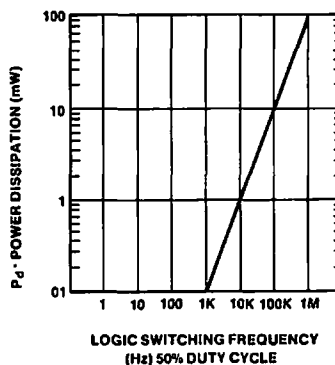
DG308A: DEVICE POWER DISSIPATION
V.S. SWITCHING FREQUENCY

FIGURE 4

Only residual leakage current flows when the circuit is either ON or OFF resulting in a power dissipation of less than 10 micro watts. However, as the switch toggles, the power consumption increases in proportion to the increasing toggle frequency. Figure 4 shows the increase in power dissipation as toggling rate increases.

The actual switching time to turn on (t_{ON}) and turn off (t_{OFF}) the switch consists of two distinct intervals: propagation delay and switch actuation. During the propagation delay interval, the CMOS logic input control signal amplifies, level shifts and begins to drive the output FET switch contacts. Switch actuation occurs rapidly as current through the switch begins or is interrupted generally occurring within twenty percent of the total switching time (see Figure 5). To a first approximation the turn on time (t_{ON}) is independent of the external circuit characteristics; however, turn off time (t_{OFF}) depends on external circuit time constants. The settling time portion of switch turn off calculates as:

$$t_{\text{settling}} = 2.2 R_L [C_L + C_{D(\text{off})}]$$

from 90% to 10% of V_0 (see Figure 6). For the load conditions $R_L = 1k\Omega$ and $C_L = 35pF$:

$$t_{\text{settling}} = 2.2 (1K) (35pF + 7pF) \\ = 92 \text{ nSec}$$

In order to minimize the external loading effects on the t_{OFF} parameter, the DG308A specification measures between 50% of the logic control input and 50% of the output voltage V_0 (Figure 5). Thus only a portion of the settling

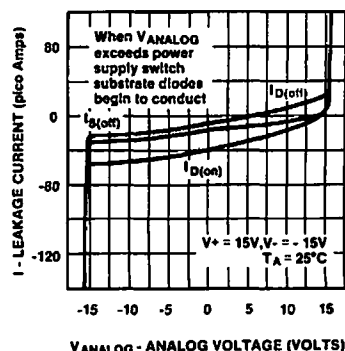
DG308A: $I_{D(ON)}$ & $I_{D(OFF)}$ VERSUS V_D 

FIGURE 3

time (70% of one time constant) is included in the t_{OFF} measurement. That is, the settling time to the 50% point of V_0 is 29 nSec. The remaining 50 nSec of the typical t_{OFF} is propagation time.

The turn on time exceeds the turn off time over the full temperature and analog signal range by design. This approach results in guaranteed break-before-make switch operation in multiplexing applications.

SWITCHING TIME TEST CIRCUIT

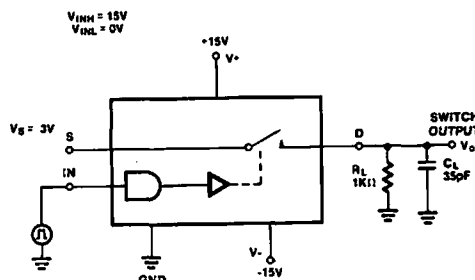
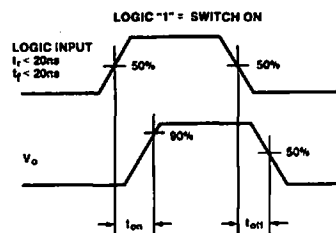


FIGURE 5

FOUR CHANNEL ANALOG MULTIPLEXER

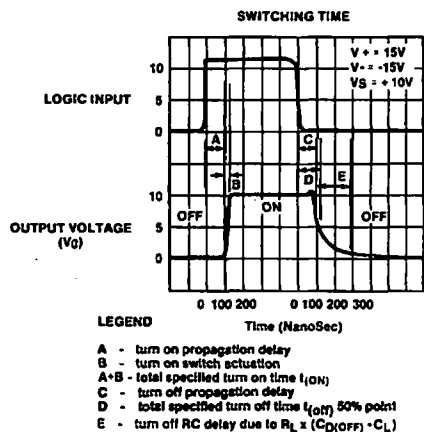


FIGURE 6

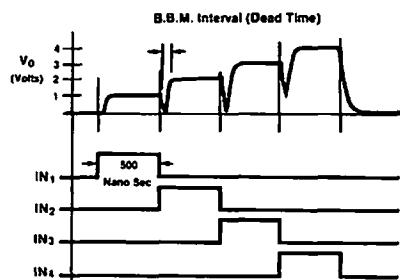
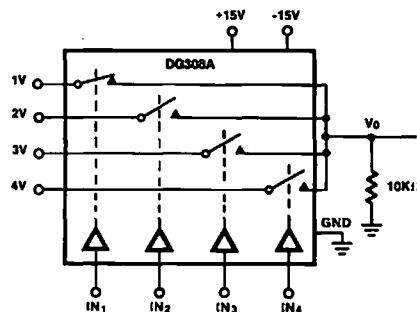


FIGURE 7

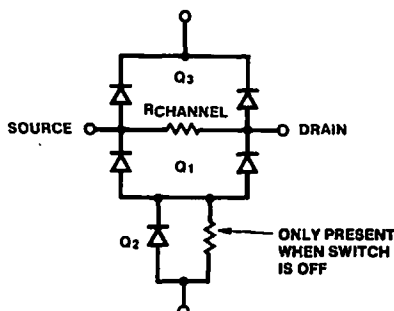
A FOUR CHANNEL ANALOG MULTIPLEXER:

The four channel input multiplexer (Figure 7) displays the characteristic dead time achievable between channel selections resulting from t_{ON} being longer than t_{OFF} . This desirable dead time (break-before-make operation) prevents transducer signal sources from being momentarily shorted together during channel selection.

While looking at multiplexing applications of the quad switch array, a few important comments apply to signals occurring outside of the normal analog signal range of V_+ to

V_- . Often analog multiplexers receive their input signals from sources located far away. The signal sources sometimes pickup transient signals which exceed the V_+ and V_- power rails. Under this condition the DG308A acts as a voltage clamp which can shunt transients up to 30mA to the V_+ or V_- power supplies. Figure 8 gives a working model of the transient clamping diodes during both switch ON and OFF states. Remember, the DG308A is constructed with a latch proof CMOS process (Reference 1).

TYPICAL SINGLE CHANNEL OVERVOLTAGE MODEL



$R_{CHANNEL} = 100\Omega$ Max when $IN_x = "1"$

$R_{CHANNEL} > 1000$ Meg Ohm when $IN_x = "0"$

FIGURE 8

When transient signals exceed the capability of the DG308A's clamping diodes, external protection circuits are required. One of the most often used and effective protection circuits are the clamped series input resistors (Figure 9). This circuit has some important subtleties worth mentioning. First, the series resistor combined with the switch input capacitance of 7 pico Farads provides a low pass filter action that rapidly attenuates very large fast transient voltages e.g., electrostatic discharge. Second, the series connection of diodes (zeners) tends to balance the individual leakage currents which could become a serious problem when the circuit operates at high ambient temperatures. Diode leakage current doubles every 10 degrees centigrade increase in temperature. The diode leakage current flowing in the signal path generates undesirable temperature sensitive offset voltages. These offsets cause problems with low level voltage switching applications, e.g. thermal couples. The diodes (zeners) perform the initial voltage clamping of a transient signal. It turns out that very fast transients (e.g. E.S.D.) are more effectively clamped by zeners than by forward biased diodes. Regarding placement for 8 bit and 12 bit A/D converters (0.2% and 0.01%), let's look at the accuracies attainable in programmable gain amplifiers.

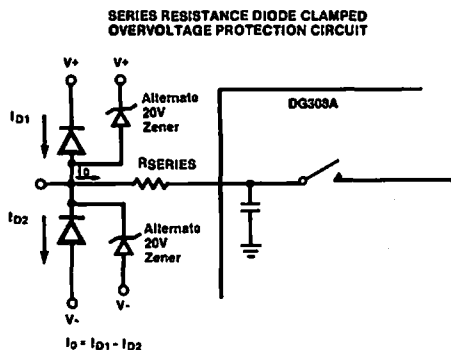


FIGURE 9

Figure 11 shows a common switchable gain amplifier. This circuit has two gain states X5 and X50. If the analog switch had zero ohms ON resistance ($R_{DS(ON)}$), the given values of R_{f1} , R_{f2} and R_i would produce the circuit gains of X5 when switch 2 was closed and X50 when switch 2 was open. The $R_{DS(ON)}$ of the analog switch produces a gain error of 0.19%.

Ideal switch gain calculation: $R_{DS(ON)} = 0\Omega$

$$AV(X50) = \frac{R_{f1}}{R_i} + 1 = \frac{2450K}{50K} + 1 = 50$$

$$AV(X5) = \frac{R_{f1}/R_{f2} + 1}{R_i} = \frac{2450K/217.78K + 1}{50K} = 5$$

Actual switch gain calculation: $R_{DS(ON)} = 100\Omega$

$$AV'(X50) = \frac{R_{f1}}{R_i + R_{DS(ON)}} + 1 = \frac{2450K}{50K + 100} + 1 = 49.9021$$

$$\% \text{ Gain Error} = \frac{AV - AV' \times 100}{AV} = 0.19\% \text{ error}$$

$$AV'(X5) = \frac{R_{f1}/[R_{f2} + R_{DS(ON)}] + 1}{R_i + R_{DS(ON)}} = \frac{2450K/(217.78K + 100) + 1}{50K + 100} = 4.99985 \text{ } 4.99376$$

$$\% \text{ Gain Error} = \frac{AV - AV' \times 100}{AV} = 0.003\% \text{ error } .012\%$$

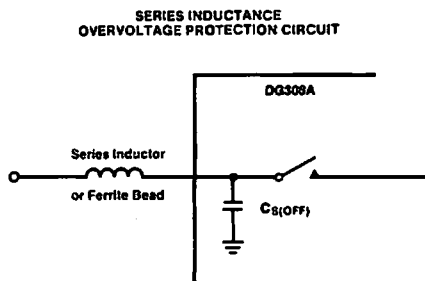


FIGURE 10

The low $R_{DS(ON)}$ of the DG308A allows us to meet the 0.2% accuracy requirement imposed by the 8 bit A/D converter. Note that the percent error in gain accuracy is larger in the high gain (X50) rather than low gain mode (X5).

The circuit of Figure 11 also has a dummy switch (SW1), which is always closed, to provide some temperature tracking between the feedback resistors and input resistors. The $R_{DS(ON)}$ of most analog switches has a positive temperature coefficient of 0.7% per degree centigrade. The $R_{DS(ON)}$ will double if the temperature increases by 140°C.

In order to achieve the 0.01% accuracy requirement of a 12 bit A/D converter measuring system, the programmable gain circuit can be rearranged which almost eliminates the $R_{DS(ON)}$ gain sensitivity. The circuit of Figure 12 achieves the required 0.01% gain accuracy by placing the analog switch in series with the high input impedance of the FET opamp. In this circuit gain accuracy is determined by the resistor ratios, which can be chosen to properly track over the operating temperature range. It turns out the weak component of the circuit Figure 12 becomes the opamp due to its input offset and common mode rejection capability.

The circuit Figure 12 also provides high input impedance and non-inverting operation. Additionally using a suitable wide-band width of the clamping diodes (zeners) between the series resistor and analog switch is not preferred since this would increase offset error generation due to the differential diode leakage flowing across the series resistor causing an IXR offset error voltage.

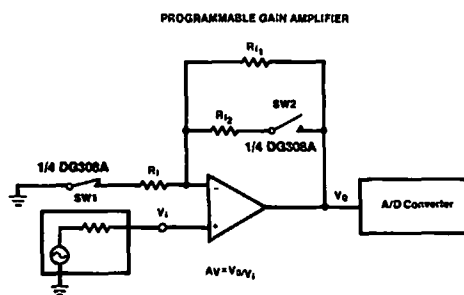


FIGURE 11

One disadvantage of the series input resistor protection circuit (Figure 9) is the increased total resistance in the signal path which will increase system noise pickup, degrading effective transducer signal-to-noise ratio. An alternate fast transient protection circuit shown in Figure 10 does not increase total transducer resistance but still damps fast transients. Taking advantage of the basic properties of lossy inductance, the ferrite bead allows signal frequencies generally close to D.C. (eg. thermal couple) to pass through the system to the amplifier. The low frequency resistance of the ferrite bead surrounding the signal lead is very low which minimizes the additional resistive contribution to the transducer signal-to-noise ratio. The high frequency operation of the series lossy inductance combined with the input capacitance of the analog switch provide a very effective damped two pole low pass filter. Basically the inductor blocks the high voltage transient from passing through to the analog switch. Additionally, the lagging current passing through the inductor to a first approximation integrates according to:

$$i_L = \text{transient time } V_{in} - V_{switch} \approx 0 \text{ dt.}$$

So far we have been discussing the transient handling capability of the DG308A at the source or drain terminals. The logic inputs (IN_X) have protection circuits shown in Figure 1. The protection circuit will stand off input voltage transients going positive by 22 volts or negative by 44 volts with respect to the $V+$ power supply terminal. The power supply terminals will handle 44 volt transients from $V+$ to $V-$, which translates to ± 22 volts for a dual supply application.

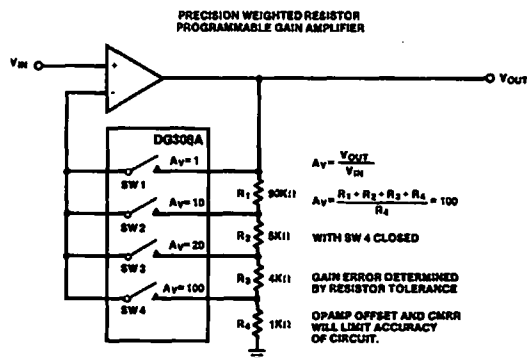


FIGURE 12

IMPORTANT APPLICATIONS OF THE DG308A.

The quad-single-pole-single-throw DG308A is a generalized building block found in several types of electronic test equipment. Some of the electronic equipment using analog switches include intelligent instruments, computer peripheral equipment, and automatic test equipment.

We will be looking at some of the basic circuits found in these applications, including programmable gain amplifiers, peak detection, velocity integrators, remote switching, and programmable filters.

PROGRAMMABLE GAIN CIRCUITS:

One of the most important analog circuits found in intelligent instruments and automatic test equipment are the programmable amplifiers and programmable attenuators. The programmable gain amplifier scales the measured signal into the full-scale range of the instruments analog-to-digital converter. Consequently the programmable gain amplifier should have better accuracy than one-half of the least significant bit of the system's A/D converter. For an 8 bit A/D converter, 1/2 LSB represents 0.2% of full-scale.

For a 12 bit A/D converter, 1/2 LSB represents 0.01% of full-scale. Keeping in mind the accuracy requirements, opamp frequency response and settling time can be easily optimized. In this circuit design it was not necessary to make $R_{DS(ON)}$ small compared to the gain setting resistor values. Consequently, the gain setting resistor values can be reduced until the opamp can no longer drive the total resistive load. Constructing Figure 13 (only resistor value changes from Figure 12) in the lab, I found that not only was settling time improved, but so was the magnitude of the ever present charge injection of the analog switch. Figure 14a to 14b shows the improvement in settling time when the total divider resistance is decreased by an order of magnitude. We quantify the magnitude of charge injection originating from the analog switch in terms of Q (pico-Coulombs). The DG308A injects approximately 35 pico-Coulombs of charge during every switch injection.

If the amplitude of the charge injection caused transients in Figure 14b is still objectionable, the addition of an extra buffer results in the charge compensated circuit of Figure 15.

PRECISION PROGRAMMABLE AMPLIFIER

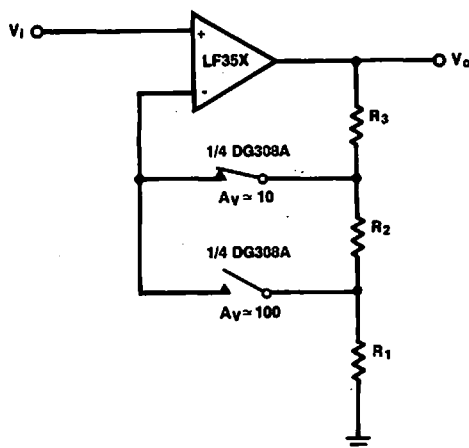


FIGURE 13

FIGURE 14a

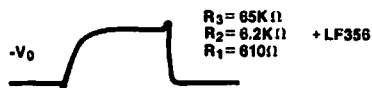
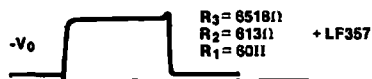


FIGURE 14b



LOGIC TIMING



FIGURE 14

CHARGE COMPENSATED INVERTING PROGRAMMABLE GAIN AMPLIFIER

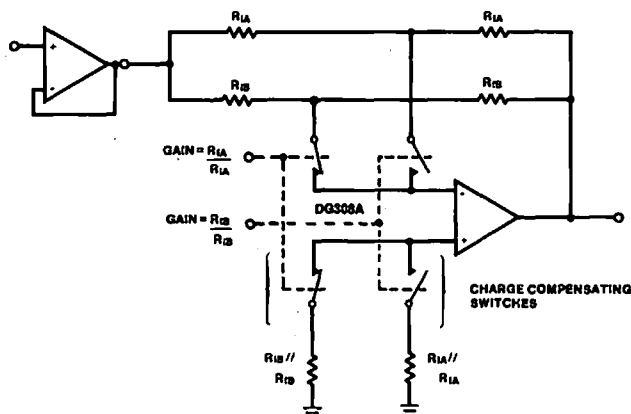


FIGURE 15

PEAK DETECTOR APPLICATIONS:

The basic peak detector circuit shown in Figure 16 utilizes the DG308A as a zero-offset reset switch. That is, no voltage will be left on the capacitor after reset. A maximum of plus or minus 10 volts may be discharged directly by the DG308A since it has a maximum switch current rating of 100mA for 1mSec. Capacitor values up to 10 μ F maximum are allowed. This peak detector circuit is commonly found in computer disk and tape drive equipment.

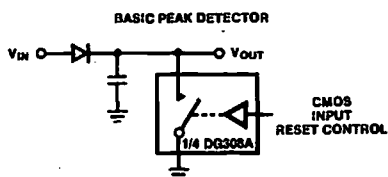


FIGURE 16

INTEGRATORS:

Velocity integration used in motor positioning circuits takes advantage of settable time integrators such as Figure 17. This circuit results in precise linear integration since the set point is determined by the set voltage and R_3/R_2 ratio.

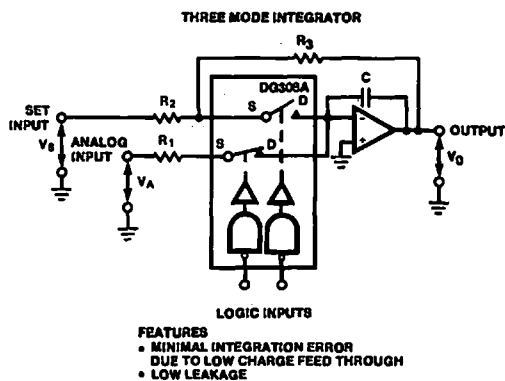


FIGURE 17

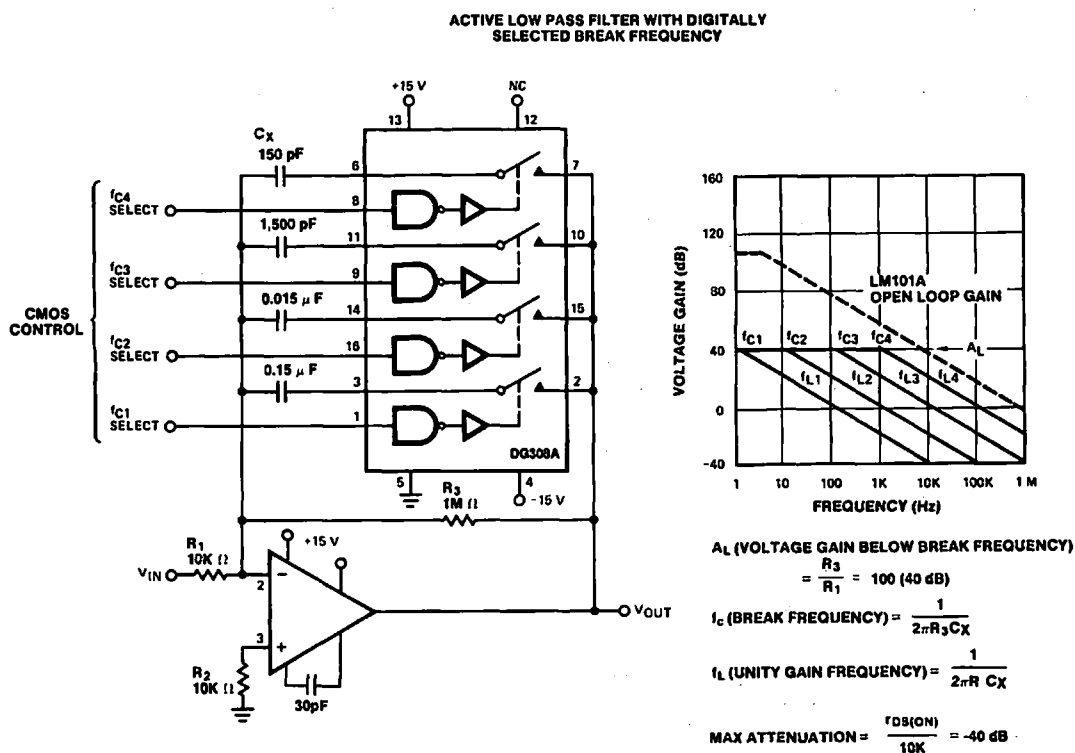
PROGRAMMABLE FILTERS:

An active filter is sometimes used at the front end of programmable test equipment. The first order active filter shown in Figure 18 can digitally select four different break frequencies. In order to minimize the effect of switch capacitance on frequency response, the DG308A is located between the low output impedance of the opamp and the frequency determining feedback capacitors.

100 ohm $R_{DS(ON)}$ of the DG308A results in an outside of selected frequency range maximum attenuation of 40dB.

REFERENCE:

1. Analog Switches and Their Applications, June 1980, AN75-1, pg. 7-57.



A MICROPROCESSOR COMPATIBLE ANALOG SWITCH MAKES INTERFACING EASY

Brian Wadsworth
September 1983

INTRODUCTION

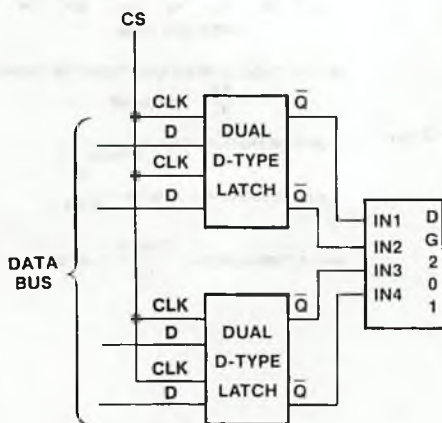
The advances made over recent years in the field of microprocessor programming have made the micro a very attractive tool for systems designers. Not only does the processor significantly reduce systems component count, but the increasingly complex algorithms developed give the microprocessor greater flexibility especially for the measurement or control of analog signals.

Until recently, to interface the digital world of the microprocessor to the "real world" of analog switches has meant the use of some type of memory device. If these memory devices are not used then the processor data bus had to remain tied to the logic inputs of the analog switch. This memory function employed one of the following devices: A shift register, a flip-flop, or a special peripheral interface adaptor. Some of these methods are shown in Figure 1.

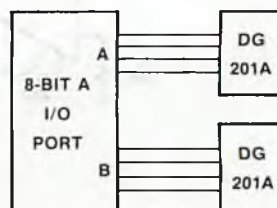
The DG221 Quad Latching Analog Switch combines both functions on a single chip. These latches eliminate the requirement of "WAIT STATES" used to accommodate slower I/O functions which compromise processor speed. This simplifies the interface methods and facilitates more efficient microprocessor performance.

The data latches are activated by the $\overline{WR}$ (WRITE BAR, active low) input. These latches become transparent whenever $\overline{WR}$ is driven to a logic 0. At this time, the DG221 is functionally identical to the popular DG201A to which it is also pin compatible, except for pin 12 which is used for the $\overline{WR}$ input. The logic truth table and pin configuration for the DG221 are shown in Figure 2.

TRADITIONAL METHODS OF INTERFACING USING MEMORY DEVICES



A. USING EXTERNAL LATCHES TO
MAINTAIN SWITCH CLOSURE



B. USING I/O PORT AS GATED BUFFER

FIGURE 1

CIRCUIT DETAILS

The circuit shown in Figure 3 is a simplified schematic for a single channel. It shows the logic interface circuitry, coupled with input protection, followed by D-type latches, level shift and driver circuitry, and finally the CMOS output switch.

The logic interface circuit has been designed to make microprocessor interfacing as simple as possible. The digital inputs, due to their CMOS construction, draw negligible current and provide extremely low capacitive loads (typ. 5 pF). Full TTL input compatibility is guaranteed without the external pull-up resistor. These features combine to ensure that the DG221 can be driven directly from the microprocessor data bus without overloading the bus. The input protection circuitry consists of internal diodes to both supply rails which forward bias to discharge any static

energy into the supply rails. A series resistor is included to limit the current to the forward biased diodes.

The D-type latches are driven from the $\overline{WR}$ input and which in its normal high state will isolate the output switches from excursions as the processor data change their state in response to the data present on the data bus.

The level shift and driver circuitry enables a full ± 15 volt analog signal to be switched by the CMOS output switch. The switch uses body snatcher transistors in its construction to improve switching performance by snatching the body of the N-channel MOSFET to different potentials, depending on the switch state. In the off-state, the body is snatched to the negative rail which improves off-isolation by providing a low impedance path for high-frequency signals. In the on-state, the body and source of the N channel MOSFET are shorted, which reduces the threshold value.

PIN CONFIGURATION

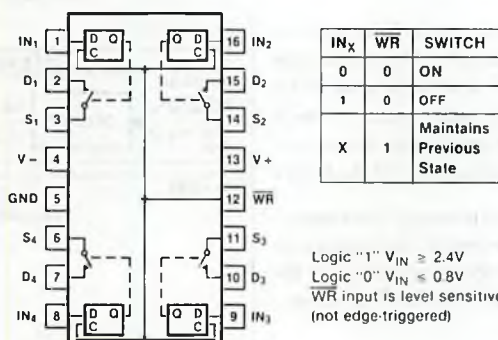


FIGURE 2

FUNCTIONAL SCHEMATIC (single channel shown)

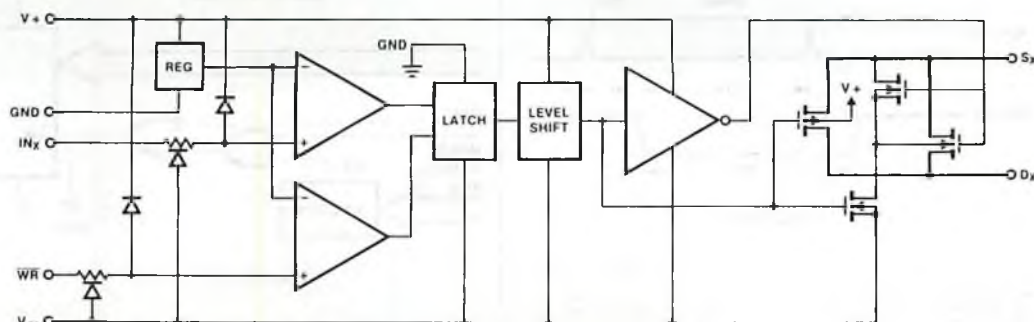


FIGURE 3

A measure of switch performance is the error voltages introduced by the switching element, often referred to as the VERROR figure of merit. This error is the product of RDS(on) and ID(on) maximum leakage quoted for the device. The extremely low leakage of 5nA max. (10pA typ.), combined with the low on-resistance of 90 ohms max. (60 ohms typ.) of the DG221, combine to give an error voltage of 0.45 uV maximum at room temperature. A signal level of 4.5 mV would remain 99% accurate. This switch is very suitable for low level signal switching applications.

Finally, the regulator used for the DG221 is a feature which is unique to the data latch analog switch range produced by Siliconix. It is used to maintain a constant internal reference voltage for defining digital input switching thresholds at 1.4 volts, allowing the device to maintain its TTL input compatibility over large power supply variations. The regulator has also been designed to reduce the effects of temperature on parameters such as switching threshold and switching speed, thus minimizing drift due to ambient conditions over the full military temperature range of -55 C to +125 C.

INTERFACING THE DG221

The latch timing arrangements have been designed to be fully compatible with the more popular NMOS microprocessors, e.g. 8085A, 6800, Z80. The timing arrangements for DG221 are given in Figure 4. The timing requirements of the 8085A have also been included for comparison to illustrate the full microprocessor compatibility of the DG221.

Although the DG221 was designed primarily to be compatible with the 8085A, it can also be used in conjunction with the MC6800 series and Z80 family of processors, as the interface circuits shown in Figures 5, 6 and 7 illustrate.

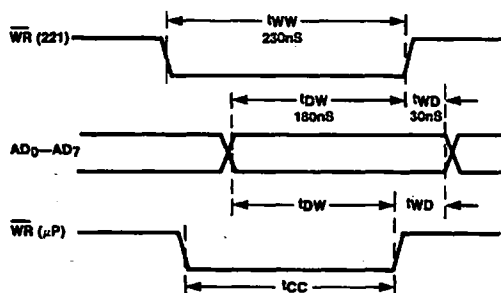


FIGURE 4

	8085A	8085A-2	DG221
t_WW Width of Control Low (WR)	400 (min)	230 (min)	230 (min)
t_DW Data Valid to Trailing Edge of Write	420 (min)	230 (min)	180 (min)
t_WD Data Valid after Trailing Edge of Write	100 (min)	80 (min)	30 (min)

This also illustrates how the DG221 more than meets the timing requirements of the faster 8085A-2.

All times are in nano seconds.

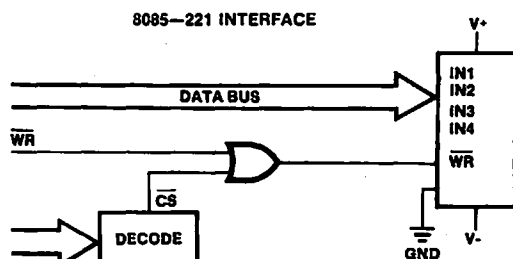


FIGURE 5

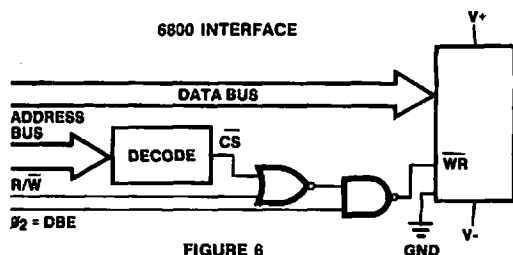


FIGURE 6

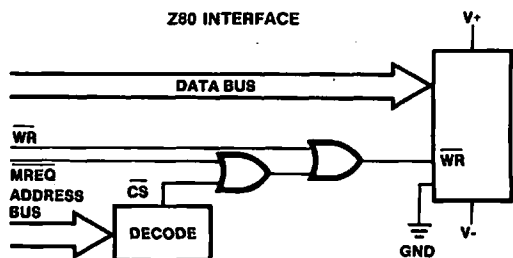


FIGURE 7

TYPICAL APPLICATIONS

The DG221 is intended for use in microprocessor applications where the data latch facility can be of great benefit. The circuits included in this article are intended to highlight the benefits offered by the DG221, while at the same time generating some ideas for design engineers.

Figure 8 shows the use of the DG221 in an alarm system. The low loading offered by the DG221 to processor outputs enables several DG221's to be operated in parallel without overloading the processor outputs. A lower component count results by using the DG221 as a MUX in the alarm sensor circuit.

The amplifier shown in Figure 9 has processor-controlled gain and inputs enabling analog signals of varying magnitudes to be switched to a common amplifier. This is achieved by ensuring the amplifier has the appropriate value of feedback resistor for the correct output level. The DG221 looks into the high input impedance of the op amp so the effects of RDS(on) are negligible. Furthermore, since the DG221 can handle positive and negative signals, the unity gain connection on the op amp is possible.

Figure 10 highlights the combined use of the DG221 and DG528 in a 32-channel MUX system. Because the timing arrangements for these devices are identical, they can be readily used together. The Reset facility on the DG528 is particularly useful for synchronization on channel 1 during "power up" conditions. The 2-level system has several advantages over the single-level system. These are:

- (i) reduced output capacitance.
- (ii) reduced output leakage current.
- (iii) much faster switching speed, giving higher data transmission rates.

The switching of intensity and position in a CRT with video display is simplified by using the DG221 in a processor-based system, as is illustrated in figure 11. This circuit can also be adapted for radar multiplexing because the DG221 allows both the radar trace and a marker to be displayed simultaneously since it can be "programmed" to have more than one switch closed at any one instant.

The final circuit shown in Figure 12 shows the use of the DG221 and the DG528 in a remote, processor-controlled measurement system.

The DG221 is used to condition the input signals to suit the input requirements of the A/D, allowing the system to be used to measure signals of various magnitudes.

The typical area where this may be of use is in automatic test equipment. In this application, the DG528 can be used as a demultiplexer to effect the illumination of the required status lamp to indicate the test result.

As was mentioned earlier, these are only example applications. Other application areas for the DG221 include: communication systems, home security, avionics, instrumentation, data acquisition, etc.

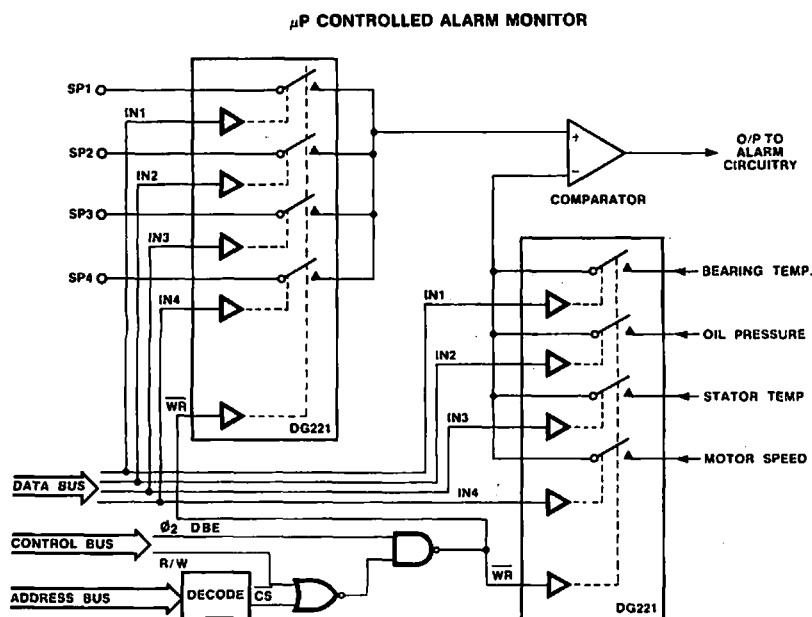


FIGURE 8

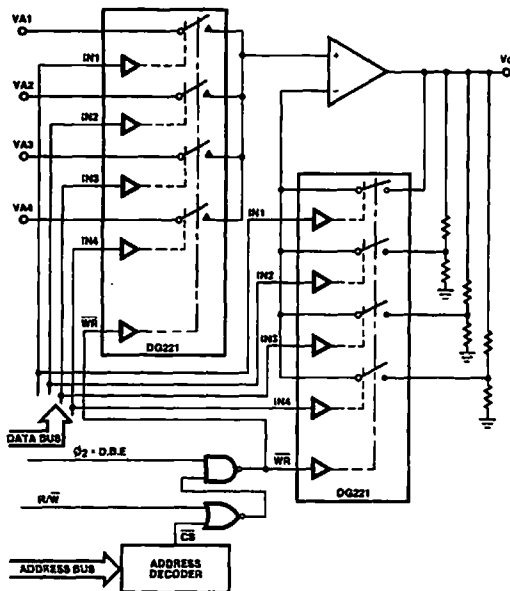
μ CONTROLLED VARIABLE GAIN AMPLIFIER

FIGURE 9

2 LEVEL 32 CHANNEL MUX SYSTEM.

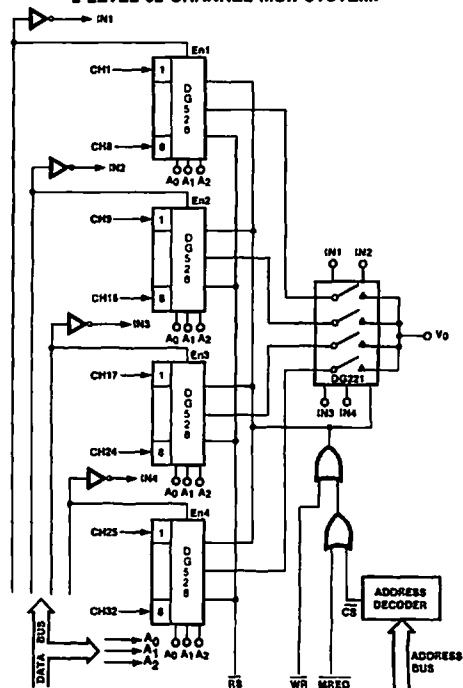


FIGURE 10

SIMPLE MUXING

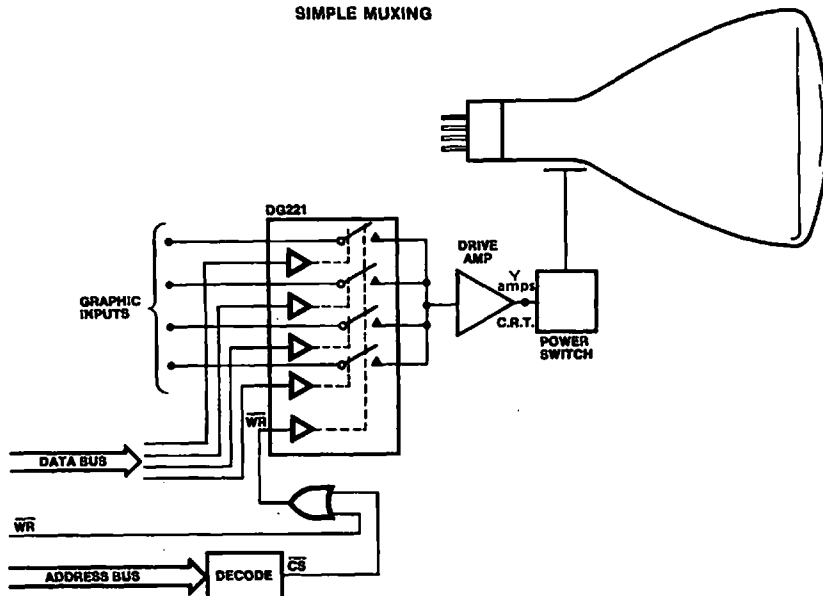


FIGURE 11

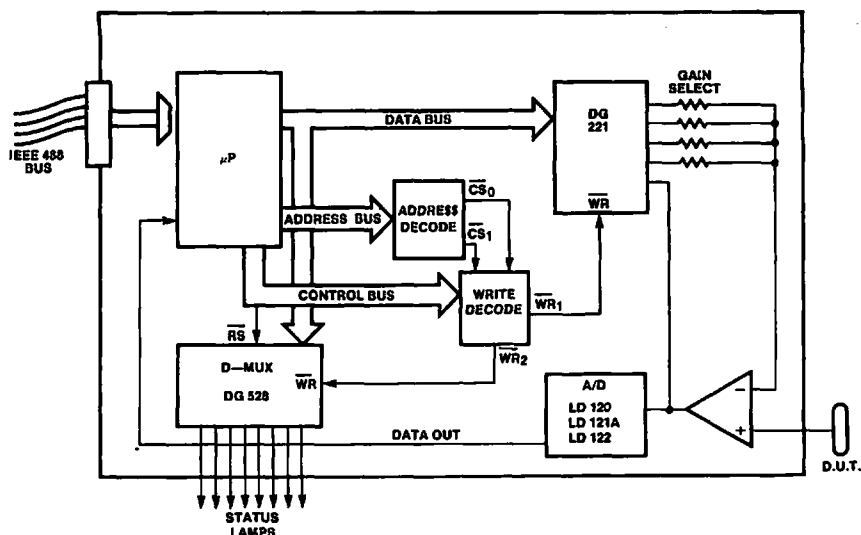


FIGURE 12

CONCLUSION

The DG221 Quad switch is an extremely reliable and rugged analog switch designed primarily for microprocessor applications. The on-chip latches have been designed to simplify microprocessor interfacing techniques while at the same time allowing more efficient processor use.

The on-chip regulator gives much greater stability against circuit and ambient conditions, while switch performance achieves very low switching errors.

In short, the DG221 is synonymous with high performance, real-world microprocessor applications.

THE PROCESS

The DG221 is fabricated on a new high voltage CMOS process developed by Siliconix called PLUS 40. This process continues to use the buried layer technique for prevention of CMOS latch-up. This new process was originally designed to provide a more rugged device in transient environments. To achieve this, first the gate oxides were made thicker to increase the DC rupture voltage by 33%. When this is

combined with the logic input protection and CMOS switch body-clamping diodes, an overall improvement in static damage immunity is achieved. Secondly, the increased voltage rating means normal operation is accommodated with less stress to the device. Thus, the PLUS 40 process improves reliability as well as the immunity to static damage.

To achieve this increase in process maximum breakdown voltage, an ion-implantation technique is used. This technique has the additional benefit of allowing greater process control to be achieved, which enables very uniform repeatable device parameters to be realized. One example of this is that switch-to-switch on-resistance variation has been improved to less than 2%.

Finally, due to its PLUS 40 CMOS structure and on-chip regulator, a much simpler power supply design has been facilitated. The 44V rating allows a greater margin for overvoltage while the on-chip regulator allows for large power supply variations.

A HIGH QUALITY AUDIO CROSSPOINT SWITCH

By Bob Zavrel
October 1983

INTRODUCTION

Recent advances in analog switch integrated circuits have made superior audio switch specifications possible. A crosspoint switch for the most demanding audio applications is described here. Although this switch may be used in recording studio and radio broadcast mixers where little compromise is acceptable, the low cost and small size makes this switch ideal for a much more diverse range of applications. Such applications can include audio follow switches found in video systems, audio synthesizers, high quality multiplexers, and home entertainment systems.

A high quality audio frequency switch should have the following features:

1. Reasonable cost
2. Unity or variable gain
3. Very low harmonic distortion ($< 0.01\%$)
4. Flat response (DC to > 1 MHz.)
5. Low crosstalk
6. High "Off" Isolation
7. Excellent phase linearity
8. High speed switching (< 1 ns.)
9. freedom from switch "popping"
10. Small size
11. Direct control by digital gates
12. Use of DC coupling only

The size of a complex audio switching array can be greatly reduced by using IC analog switches. The prototype array is an 8x2 stereo crosspoint switch mounted on a 4x7 inch board. Other switch configurations may be fabricated with little effect on the switch characteristics. This single board can replace a score of rotary switches and the bundles of audio cable often found in audio mixers. Furthermore, ground loop problems are reduced by eliminating the cable bundles.

Siliconix SD5002s were chosen because of low "on" resistance, low switch capacitance, and very fast switching times. The National Semiconductor LF347 quad op-amp was chosen for its excellent audio characteristics in a quad package. Two LF347s are used in this switch providing a summing and output amplifier for each of four channels. The SD5002s are held "normally open" by biasing the switch gates to ground potential through 10K ohm resistors. For any switch configuration, the appropriate switch(es) are closed by biasing the appropriate gate(s) to the positive voltage supply. In this circuit pairs of switches are controlled together to affect the left and right channels of a stereo input simultaneously. This is accomplished simply by tying the applicable switch gates together and using a common bias resistor. The ability to directly interface the SD5002 gates to digital integrated circuits opens up immense opportunities to the design engineer for switch control.

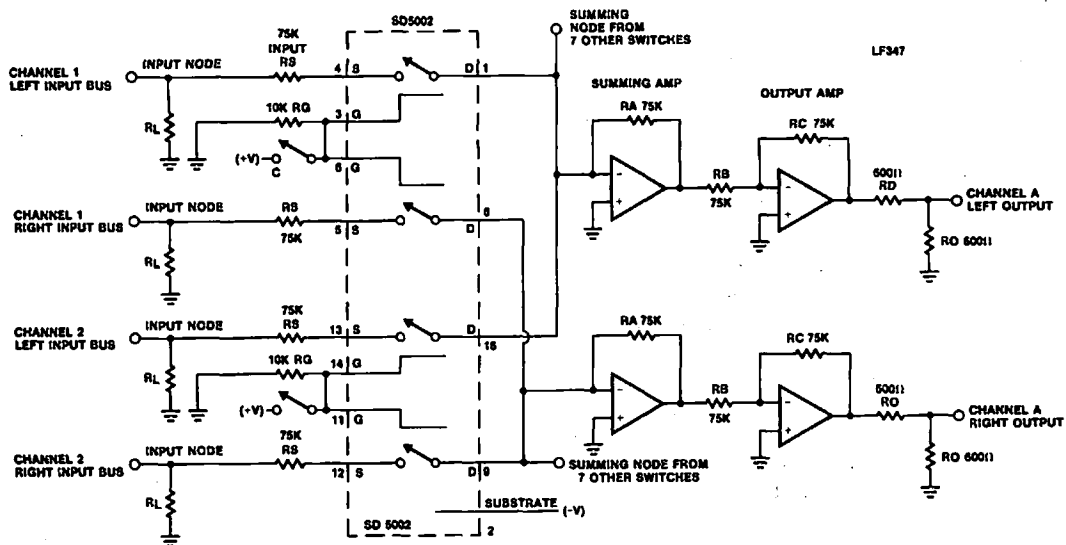


FIGURE 1

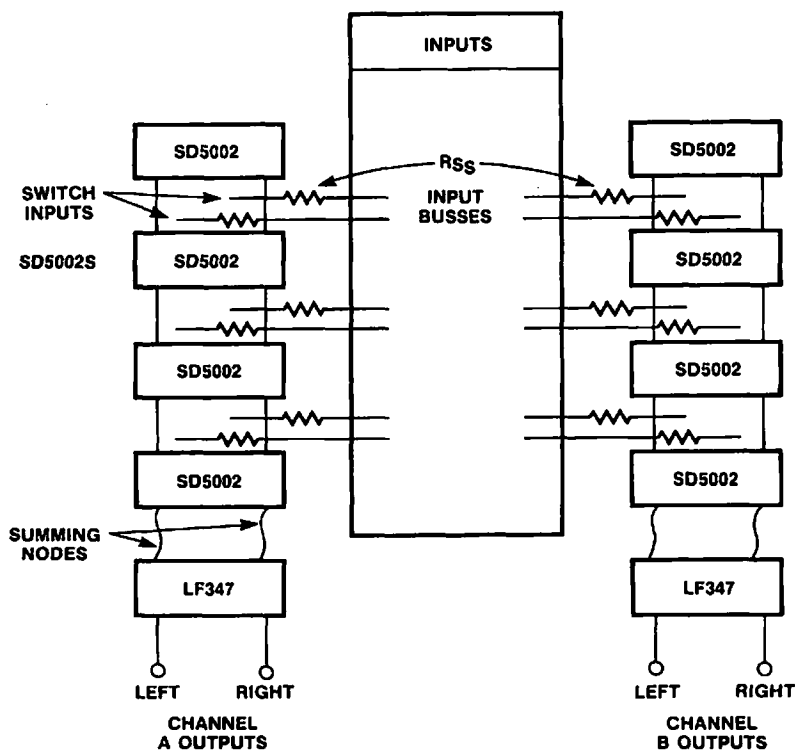


FIGURE 2

Figure 1 shows how a single SD5002 is configured as a 2x1 stereo switch. Figure 2 shows how the circuit can be expanded into a switch matrix. Eight SD5002s are required to construct the 8x2 stereo matrix array. One RL is required for each channel input for termination while separate RSs are employed to feed the signal from the inputs to the various switches. An input bus is consequently formed at the junction of these resistors.

The summing nodes are located at the inverting inputs of the summing amplifiers. The SD 5002 drains are connected to these summing nodes. A larger array will cause reduced system performance due to longer lead lengths and increased circuit capacitance. Nevertheless, large matrices can be configured with little performance compromise because of the low initial switch capacitance. RL's value should reflect the value of the source impedance. Deletion of RL will seriously degrade crosstalk and off isolation performance while lower values of RL will improve these specifications. RC may be adjusted for a wide range of system gain while a value of about 150K ohms will set the circuit to unity gain. RD sets the value of the output impedance and if the switch is to feed a high impedance load, RO should be included to maintain system performance.

Electrolytic and mica capacitors are used on the circuit board for bypassing the two power supply voltages. Supply voltage bypassing will reduce both high and low frequency noise and help stabilize the system. The entire circuit should be well shielded particularly if it will be exposed to strong RF or power line fields. Conductors carrying high currents should be kept away from the circuit. Double

sided PC board should be used creating a ground plain on the component side as an additional precautionary measure.

Table 1 shows the switch performance of the 8x2 cross-point configuration. RL was set to 10K ohms, reflecting the high impedance of the test oscillator's output. Regulated power supply voltages of plus and minus 9 to 15 volts may be used. The signal voltages should be kept under about 3.5 volts PTP to maintain switch performance.

TABLE 1

Frequency (Hz.)	Crosstalk	"Off" Isolation	%THD
50	-74db.	-75db.	.006
100	-74	-75	.005
200	-74	-75	.004
500	-74	-75	.003
1K	-74	-75	.003
2K	-73	-74	.003
5K	-70	-71	.003
10K	-67	-68	.004
20K	-62	-62	.006
50K	-55	-55	.020
100K	-50	-49	.045

Signal voltages: 3 volts PTP.

supply voltages: + and - 12 volts

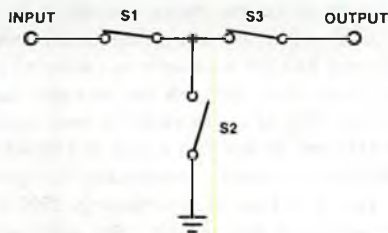
A HIGH PERFORMANCE VIDEO SWITCH USING THE SD5002

Bob Zavrel
December 1983

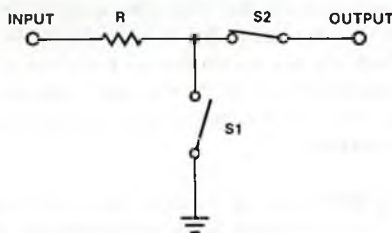
As the trend toward more advanced video systems accelerates, designers will need improved switching techniques. High resolution video and advanced computer graphics are only two areas demanding better switch performance. A high performance solution to this problem is presented here. The desirable characteristics of a high performance video switch include:

1. low cost
2. flat response from DC to VHF
3. minimal phase shift and group delay
4. constant input and output impedances
5. unity or variable switch gain
6. direct control by digital gates
7. minimum parts count
8. small size
9. very high switching speed (< 1 ns.)
10. low channel crosstalk
11. use of only DC coupling

The physical size of a video switch may be reduced and the design simplified by using integrated circuit analog switches. With this reduced size, however, increased crosstalk is introduced because of increased switch-to-switch capacitance. A fundamental goal of video switch design is to take advantage of the IC switch while minimizing crosstalk. The two popular schemes that have been developed to realize this goal are shown in Figure 1. In the "T" switch, S1 and S3 are used to route the signal to the load. S2 closes when the "T" configuration is "off" providing a near ground potential to the switch node and greatly reducing crosstalk. Unfortunately analog switches each have a channel capacitance which has an undesirable effect on frequency response and phase linearity. To minimize this capacitance, we can simply use fewer switches. The "L" configuration uses two switches but requires a loading resistor R (Fig. 1). R also serves as an isolation pad for the video source.



(a) T-SWITCH



(b) L-SWITCH

FIGURE 1
Equivalent circuits for a T-switch, a, and L-switch, b.

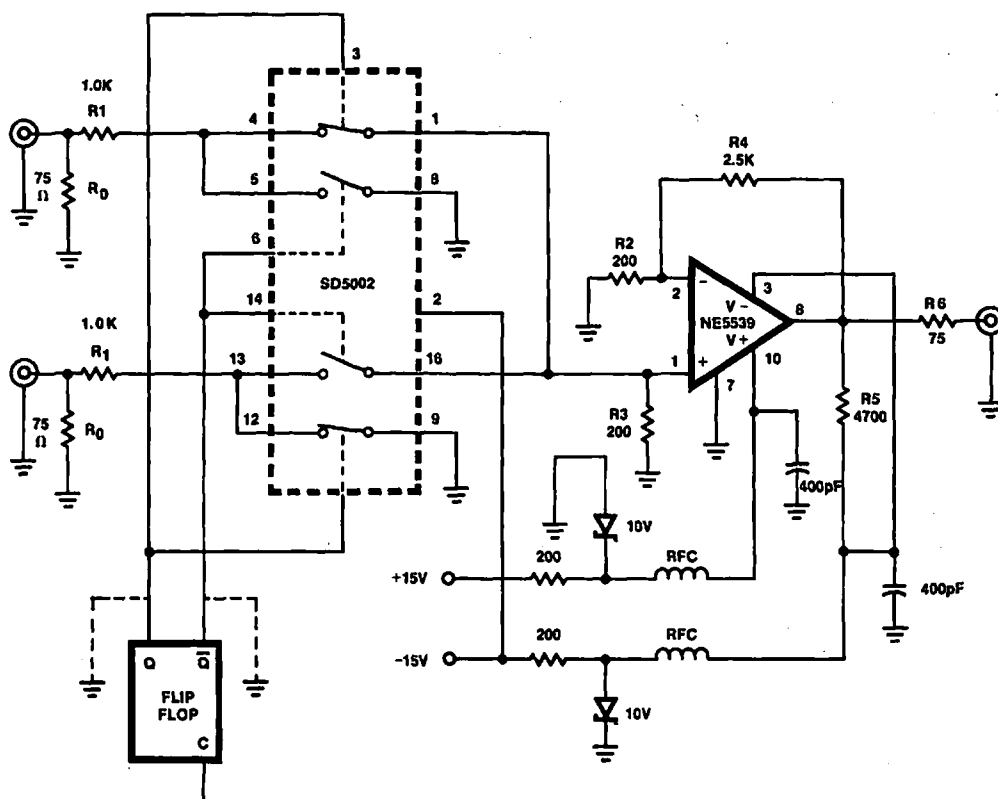


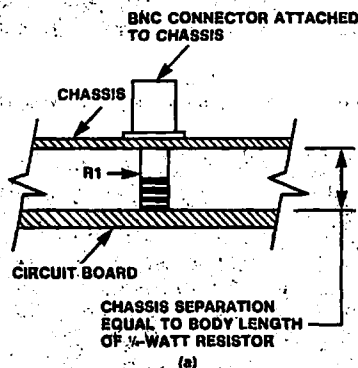
FIGURE 2
Actual circuit of a video switch with an L-configuration.

Figure 2. shows the completed circuit, a one-of-two switch with a summing amplifier. The video source's line can be terminated either externally or internally to the switch (R_0). With this termination resistor, a load change of less than 1 ohm will be "seen" by the source when the switch changes state. For this reason input isolation amplifiers are not necessary.

Siliconix SD5002 analog switches were chosen because of low "on" resistance, very low switch capacitance, and high switching speed. Also, the SD5002 can be directly controlled by standard CMOS logic gates or from TTL gates through standard interface techniques. The Siliconix

SD213 is the discrete equivalent to the SD5002 IC. Use of these discrete devices can reduce crosstalk at the expense of increased switch size and greater circuit complexity. The Signetics NE5539 was chosen as a summing amplifier because of its very high slew rate and gain bandwidth product. R_4 (Fig. 2) can be varied to control circuit gain but should never be less than a value of 1400 ohms since the NE5539 is internally compensated for gain values greater than 7. A value of approximately 2500 ohms for $4R$ will set circuit gain to near unity. Additionally, the circuit output impedance is set by R_6 while R_5 sets the output DC offset to near-zero.

Use of high quality components alone will not guarantee top performance. Circuit board layout and shielding are critical for meeting the desired specifications. The switch should be considered a subassembly with its own chassis even if included in a larger system. The designer should be ever mindful of stray capacitances and inductances. 1 pf of lead capacitance represents about 5K ohms of reactance at 30-MHz, which can ruin the crosstalk performance. The input and output BNC connectors should be mounted directly above or below the appropriate points on the circuit board (Fig. 3). Double sided PC board should be used with signal route leads etched as short as possible. The pin configurations of the SD5002 and NE5539 plastic DIP



Suggested method for mounting BNC connectors, a, printed-circuit pattern of the prototype board, b.

packages are very helpful to this end, which is evident on inspection.

Gate voltage control can be implemented by a very wide range of techniques including mechanical switches or logic gates. Since the two switches for each channel input in effect form a SPDT switch, a flip-flop logic circuit is a good choice for circuit control. Figure 2 shows the special case of a one-of-two channel switching circuit. The gate of the grounding switch of channel 1 is tied to the gate of the series switch of channel 2 and vice-versa. Thus in this unique case, one flip-flop may be used to control all four switches.

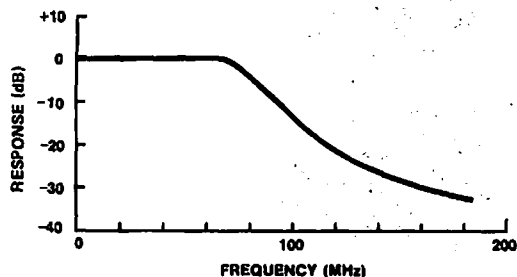


FIGURE 4

Frequency response for the circuit of Figure 2.

Figure 4 shows the response of the circuit from input to output with the applicable channel turned "on." Very good response linearity has been realized from DC to VHF which should prove to be quite adequate for the most demanding applications. Figure 5 shows channel-to-channel crosstalk isolation with equal input level signals and with channel 1 "on" and channel 2 "off." It can be seen that crosstalk isolation is better than 60 db. at 10 MHz. The switch was tested with a staircase test signal for various video response parameters. The photographs (Figs. 6 to 10) show the results while Chart 1 shows the test set-up used during this test. The photographs indicate imperceptible switch influences on the test signal.

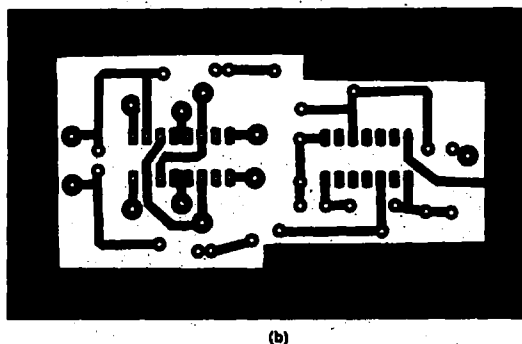


FIGURE 3

The switch specifications exceeded the resolution of the test equipment used. Chart 2 shows the test set-up used for the crosstalk and response tests.

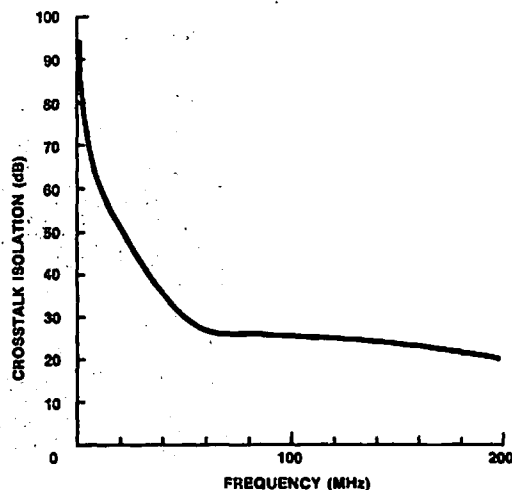


FIGURE 5

Channel-to-channel crosstalk isolation for the L-switch configuration.

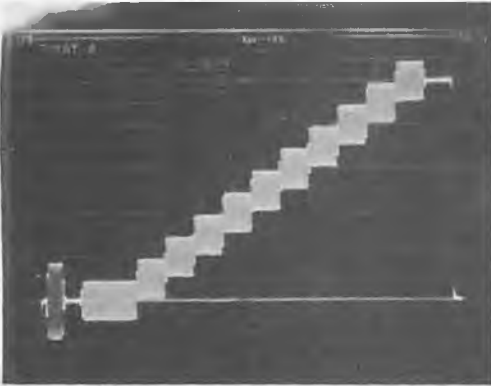


FIGURE 6
Staircase input test signal.

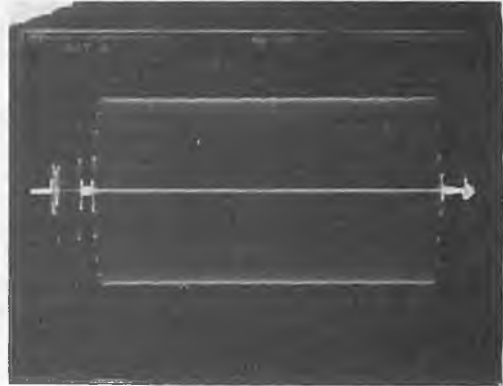


FIGURE 7
Small portion of the output video signal showing chroma.

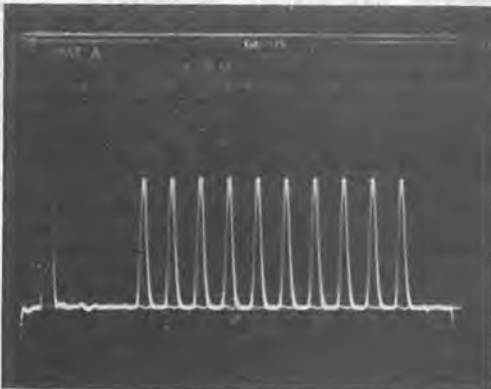


FIGURE 8
Risers (derivative) of the staircase input signal.

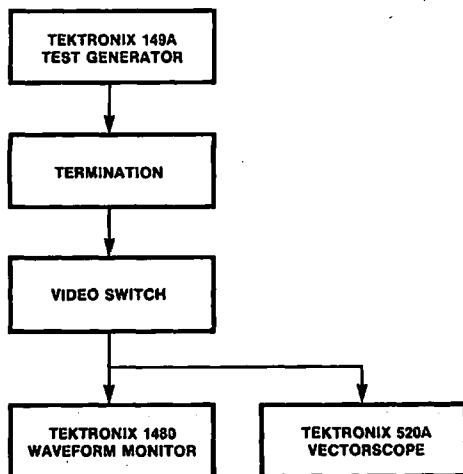


FIGURE 9
Vector scope of the color bars.



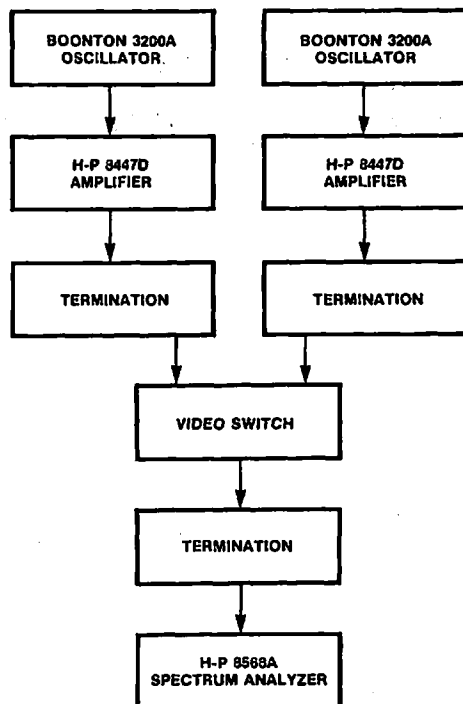
FIGURE 10
Phase shift test: parallel lines indicate no phase shift.

CHART 1



Instrumentation set-up for the video parameter tests.

CHART 2



Instrumentation set-up for the video crosstalk and frequency-response tests.

I.C. MULTIPLEXER INCREASES ANALOG SWITCHING SPEEDS

J. O. M. Jenkins
Revised April 1976

INTRODUCTION

A two-level IC multiplexing system, that has significant advantages over conventional single-level systems, can improve effective switching speeds of analog systems by approximately one order of magnitude.

Analog multiplexing is the simultaneous transmission of two or more analog signals on to a single transmission line. Time-division multiplexing is widely used, each analog input being sampled sequentially and conveyed into a common output line. The signals can be transmitted directly in their analog form or they can be digitally coded by means of A/D converters and then transmitted. The latter method is used in applications requiring a very high degree of transmission accuracy.

In a system having 'n' analog inputs, a multiplexing/demultiplexing system will generally require 1/n of the total transmitting and receiving circuitry of a nonmultiplexed system. Hence, system cost is reduced drastically in the former case.

Present-day requirements for analog multiplexers have necessitated the development of special circuits. These incorporate multichannel FET multiplexers which are now available in integrated-circuit form, and which possess numerous advantages over their discrete counterparts:

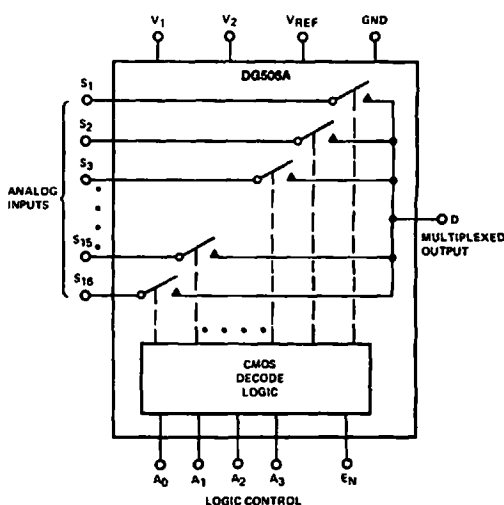
- (1) The use of IC's introduces a higher degree of circuit reliability;
- (2) Switch for switch, IC's are much more compact;
- (3) System layout cost is less;
- (4) The cost per switch is approximately the same as for a discrete FET switch.

Single-Level Multiplexing System

Fast IC multiplexers, having rapid open and close switch times, are required in many applications in which rapid

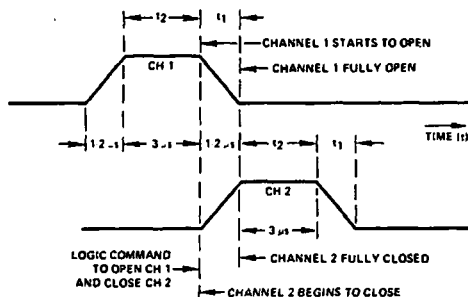
sampling of analog signals is required. In any application in which it is necessary to sample analog signals and convey them at maximum transmission rates, the ratio of $t_1:t_2$ must be as small as possible (where t_1 represents the time between samples and t_2 the sample duration time).

Applications requiring microsecond sample times clearly present considerable difficulty, because IC multiplexers which are commercially available have t_{ON} and t_{OFF} times in the region of 1-2 μs . When used in the conventional single-level mode, a substantial loss in transmission efficiency results. Figure 1 shows a simple single-level system for analog multiplexing.

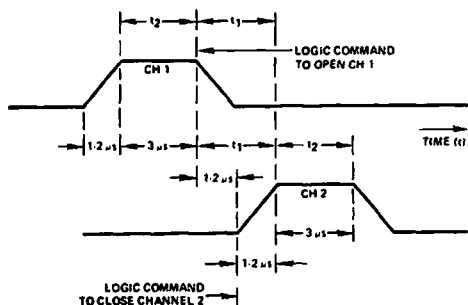


DG506 Used as a Single-Level Multiplex System
Figure 1

With a single-level system one can obtain either (a) the waveforms shown in Figure 2(a), and be faced with inter-channel interference due to overlapping samples or, (b) the waveforms of Figure 2(b) which result in delayed channel switching, in order to eliminate interference between channels.



Overlapping Channels
Figure 2(a)



Delayed Channel Switching
Figure 2(b)

If the analog sample time needed is $3 \mu\text{s}$, for example, system 2(a) would not be a practical proposition. System 2(b) would certainly be practical but would introduce a large wastage of transmission time due to the large ratio of $t_1:t_2$ (Figure 2(b), in fact, indicates a 50% loss in transmission efficiency).

This problem is manifest in all commercially available IC multiplexers used in single-level systems. Other problems that result from using a single-level system are:

- (1) With a large number of separate analog inputs, the leakage currents through the OFF switches can introduce an appreciable percentage voltage error into the common output line. This is important if the analog signal being conveyed through the closed switch is in the millivolt range.
- (2) The common node output capacitance increases with the total number of analog channels being multiplexed. With 64 channels (i.e., 4×16 channel DG506A), the common node output capacitance will be typically 160 pF .

The charging time (t_1) necessary for the analog signal to reach 0.25% of its final value (six time constants) will then be approximately

$$6 \times C_{\text{OUT}} (R_{\text{ds(on)}} + R_{\text{ANALOG SOURCE}}) \quad (1)$$

If the source resistance is $1 \text{ K} \Omega$, t_1 will be

$$6 \times (160 \times 10^{-12} \text{ pF}) \times (400 \Omega + 1 \text{ K} \Omega) = 1.35 \mu\text{sec} \quad (2)$$

This decreases the effective switching speed of the multiplexer.

Two-Level Multiplexing System

These problems can be overcome if a two-level multiplexer is used, which inherently provides a much faster switching system. Figure 3 shows an example of a two-level system capable of 32 channels. The first level consists of 16-channel DG506A multiplexers, the use of which offers the advantages stated in the introduction. The second level consists of two or more single channels of a DG181; this has switch open and close times of, typically, 100 ns , and has a break-before-make switching action. The DG181 is available as an integral dual-in-line package.

The two-level system uses the bank of high speed DG181 switches at the output to sequentially switch between the outputs of the DG506A's. Each DG506A is able to switch channels during the time the others are being interrogated. It contributes capacitance and leakage at the output only when it is switched into the output bus by a DG181.

The use of the two-level system achieves the following:

- (1) Effectively reduces the common output node capacitance of the system. It will consist of a single multiplexer output, DG506A (40 pF) and several DG181's (6 pF OFF , 15 pF ON). For a 64-channel 2-level system, for example, the output capacitance is reduced to 72 pF , compared to 160 pF of the single-level system.
- (2) Reduces the amount of error voltage developed as a result of leakage current flow through the OFF switches into the common output node. The leakage through the OFF switch of Figure 3 into the common output node is effectively that of a single OFF channel of the DG181 (from $\pm 40 \text{ nA}$ to $\pm 10 \text{ nA}$ in a 64-channel system).
- (3) Allows the system to operate in such a way that the ratio $t_1:t_2$ is very small. In the example, $t_1 = 200 \text{ ns}$ and $t_2 = 3 \mu\text{sec}$.

The switching speed of the system is dependent on the DG181, which is a high-speed 2-channel SPST ($t_{\text{ON}} \approx 100 \text{ nsec}$). The slower switching time of the DG506A ($\approx 1 \mu\text{sec}$) is not important because this switching transition can take place while the others DG506A's are being interrogated.

With the two-level system design, more data can be transmitted with a very fast multiplex system utilizing a large number of low-cost, moderate-speed multi-channel multiplexers and several high-speed SPST switches.

Details of the System

A 32-channel two-level multiplexing system is shown in Figure 3. Figure 4 shows the analog switching waveforms, including the segments of the multiplexer outputs being sampled. Notice that as one multiplexer is being sampled, the other is switching. The example of the output samples shows the edge-to-edge sampling achieved by the two-level system. The logic timing diagram for the system of Figure 3 is shown in Figure 5. This illustrates the timing used by the DG181 switches to give the two-level multiplexing.

Logic Control System

The digital control logic consists of a multi phase clock generator and recirculating binary counters. The number, N , of clock phases and binary counters necessary is equal to the number of multiplexers used in the first level of the system. With 16-channel DG506A's, 4-bit binary counters are needed (such as TTL DM7493) to give addressing to all 16-channels.

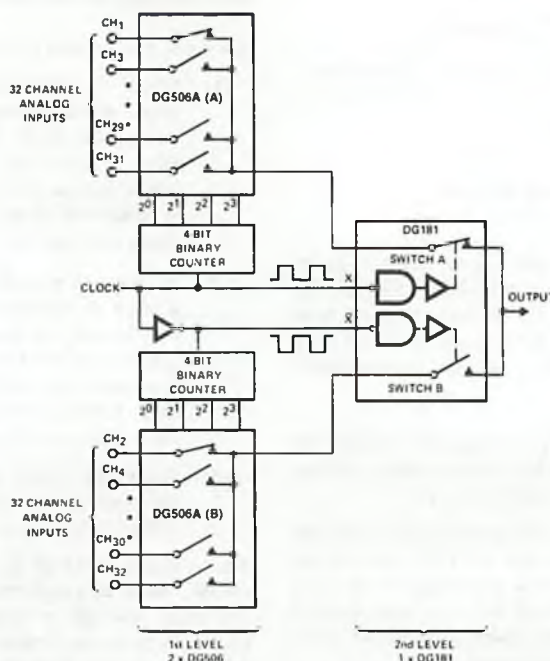
64-Channel Two-Level Multiplexer

Figure 6 shows a complete 64-channel two-level multiplex system. For the 64-channel system, $N = 4$ and the four clock

phases are generated with a two-bit counter and decoding logic (these four phases are also shown in Figure 6). Two J-K flip-flops (TTL DM7473) are connected as a two-bit counter and toggle on the high-to-low clock edge. The NAND gates (DM7400) decode the flip-flop outputs into the four clock phases shown. The low state of the clock phase is the ON state of the corresponding DG181 switch. As a clock phase goes from a low-to-high state, the DG181 it feeds turns off and the corresponding 4-bit binary counter (DM7493) is triggered to its next address state. This causes the multiplexer to change as the output of the next multiplexer is being sampled at the output. For synchronization there is a reset available to set the system to start on the first channel when power is first applied.

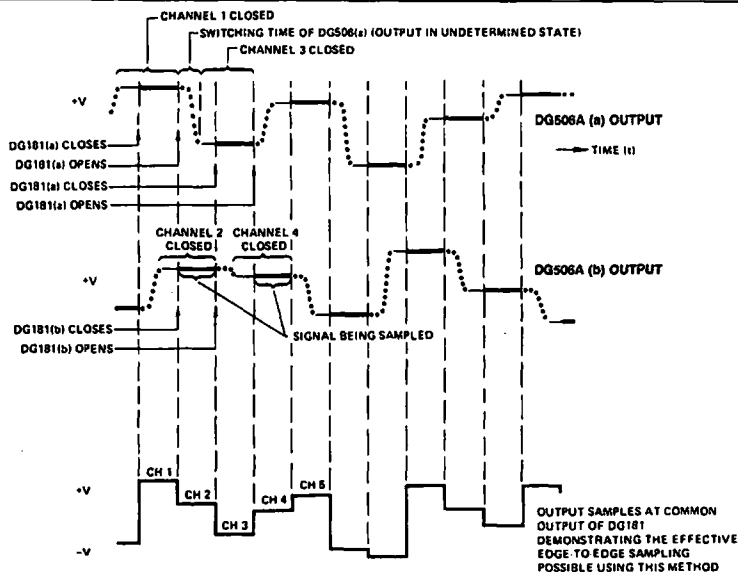
CONCLUSION

This system may be used for increasing data transmission rates in analog switching systems. One particular application is found in telephone switching where, for instance, it is necessary to multiplex 32 or more channels of analog information in the form of $4 \mu s$ samples (edge-to-edge) on to a common output line.

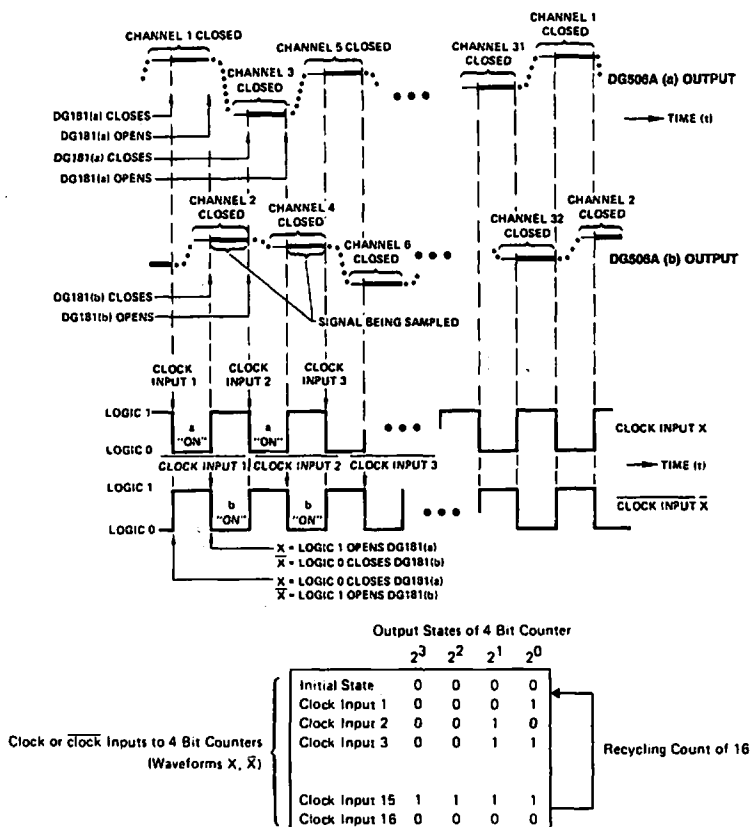


32 Channel, Two-Level Multiplex System, Comprising Two DG506's in the First Level, and a DG181 in the Second

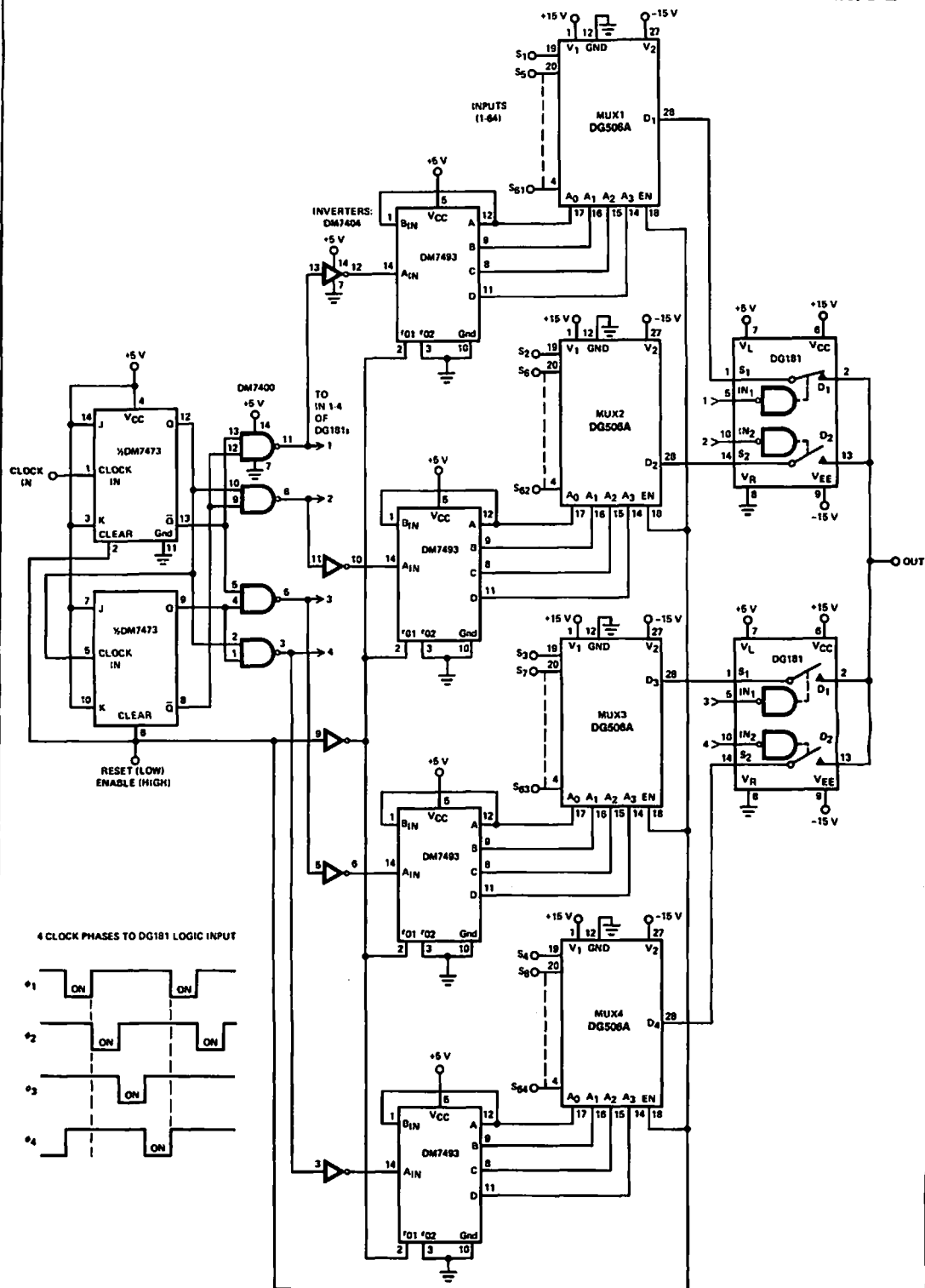
Figure 3



Two-Phase Timing Method That Eliminates the Switching Delays of the 16-Channel Multiplexers in a 32-Channel System
Figure 4



Logic Timing Diagram Showing Waveform Timing Sequences for a 32-Channel System
Figure 5



64-Channel 2-Level Multiplex System
Figure 6

MULTIPLEXER ADDS EFFICIENCY TO 32-CHANNEL TELEPHONE SYSTEM

Analog signals are time-division multiplexed by recently developed integrated circuits in a two-level switching scheme; the technique promises to add speed and efficiency to digital telephone systems

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□ Time-division multiplexing has gained wide acceptance in recent years as a means of combining multiple telephone channels on wire-pair transmission lines that previously accommodated only one channel. Combined with pulse-code-modulation (PCM) circuitry to convert the sampled signals to a digital format, the multiplexing techniques have generally reduced size, power consumption, and costs of plant equipment.

To achieve minimum signal loss and distortion in

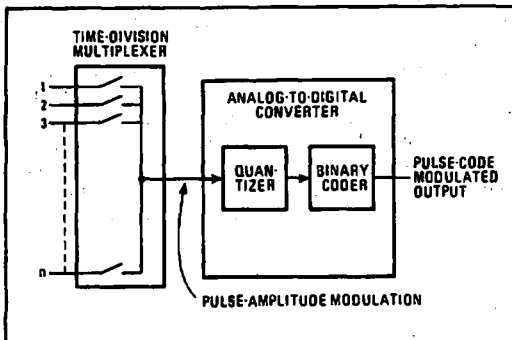
such systems, much effort has been directed toward building multiplexers that switch from channel to channel with minimum output rise and fall times. Such a multiplexer design recently built and tested provides 150-nanosecond switching time, an order of magnitude faster than presently available circuits.

This high-speed switching is achieved by applying biphasic control logic to a two-level multiplexer arrangement that takes advantage of the fast rise times and the break-before-make action of newly developed integrated-circuit multiplexers.

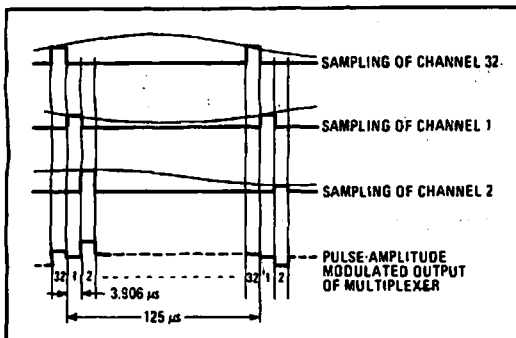
Telephone system requirements

A generalized system used to time-division multiplex voice signals is shown in Fig. 1. After the signals on each of analog channels have been sampled, each sample is quantized and coded into a PCM format. The new design focuses on the analog multiplexer, which feeds the analog-to-digital converter.

The sampling rate for each of the incoming channels is determined by the desired bandwidth of the voice signals being sampled, while sampling dwell time is fixed by the number of channels that must be sampled. Nyquist's sampling theory^{1,2} states that any transmitted waveform that is band-limited to a maximum frequency of f_L can be accurately reconstructed from periodic sam-



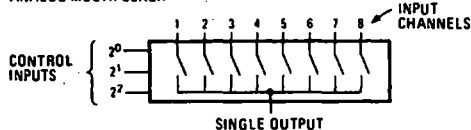
1. Telephone's answer. Problems in overcrowding of wire-pair telephone-transmission lines are lessened by using analog time-division multiplexers followed by a-d converters.



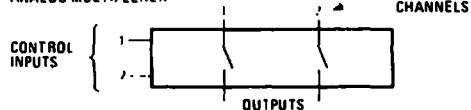
2. Tight fit. For accurate reconstruction of a 3.3-kHz telephone signal, it must be sampled at a rate of about 8 kHz, or once every 125 μs. The hierarchy of today's telephone system makes it highly desirable to multiplex 32 speech channels during this period.

CIRCUIT CHARACTERISTICS TABLE

DG501: 8-CHANNEL ANALOG MULTIPLEXER



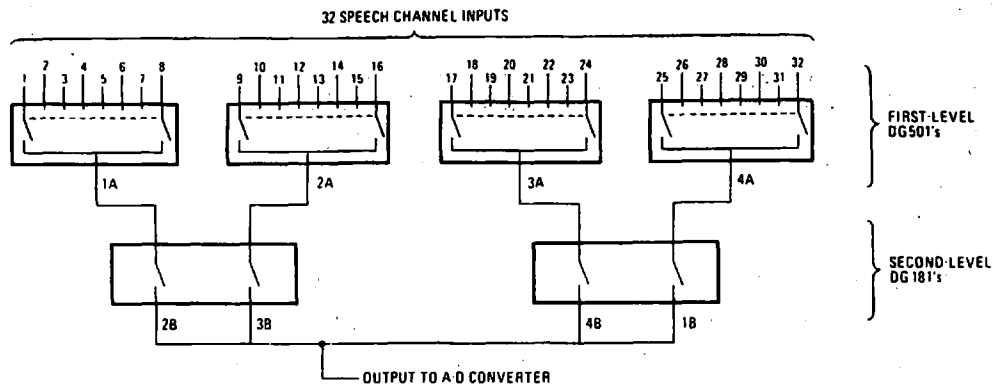
DG181: 2-CHANNEL ANALOG MULTIPLEXER



DG501
MIN I₂
1.5 μs
40 pF

SHIES RESISTANCE (ON CHANNEL)
SWITCHING TIME
OUTPUT CAPACITANCE

DG181
30 Ω
150 ns
20 pF



3. Two-level multiplexing. Output-node capacitance is significantly reduced when a second level of multiplexers is added. Interchannel switching time, however, is still determined primarily by the speed of the first-level switches.

ples taken at a rate as slow as $2f_s$.

In practice, however, filters do not provide ideal cut-off at f_s , and a somewhat higher sampling rate must be tolerated. For example, to achieve less than 1% error in reconstruction accuracy, the sampling rate must be at least twice the frequency at which the unwanted signals above cutoff are reduced by 40 dB.^{2,3} Thus, to relax difficult filtering requirements at the input-to-sampling circuitry, a voice bandwidth that is nominally limited to about 3.3 kHz is usually sampled at an 8-kHz rate, or once every 125 μ s.

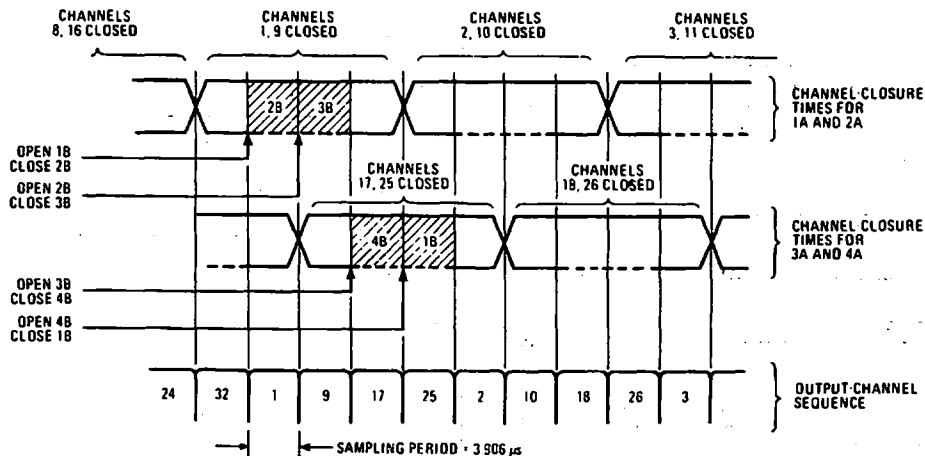
Single-level multiplexers

The standard configurations of today's telephone systems dictate that a fundamental group of 32 channels be multiplexed onto one line. Therefore, with a sample frame time of 125 μ s, each of 32 multiplexed channels is

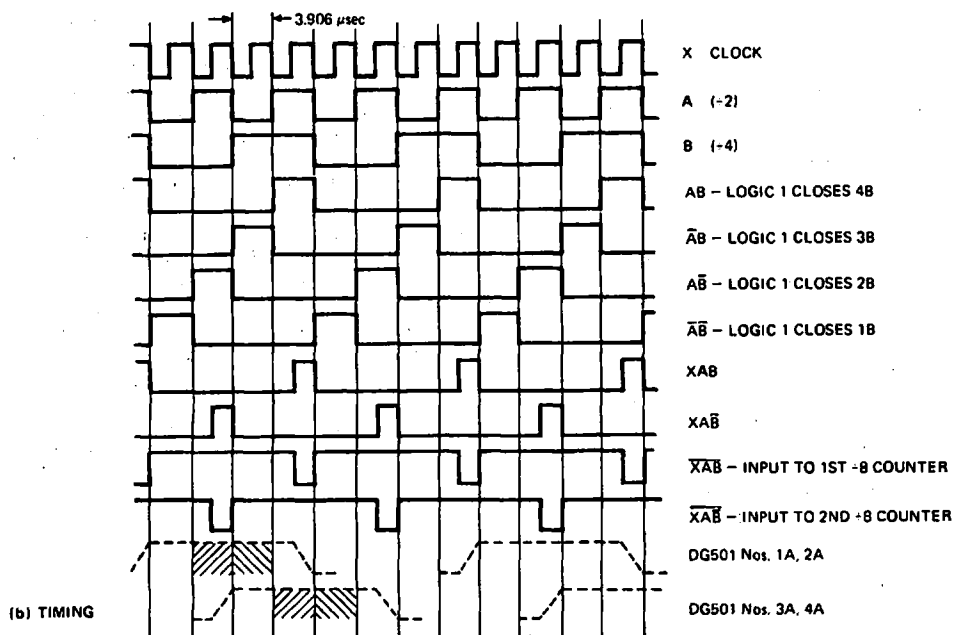
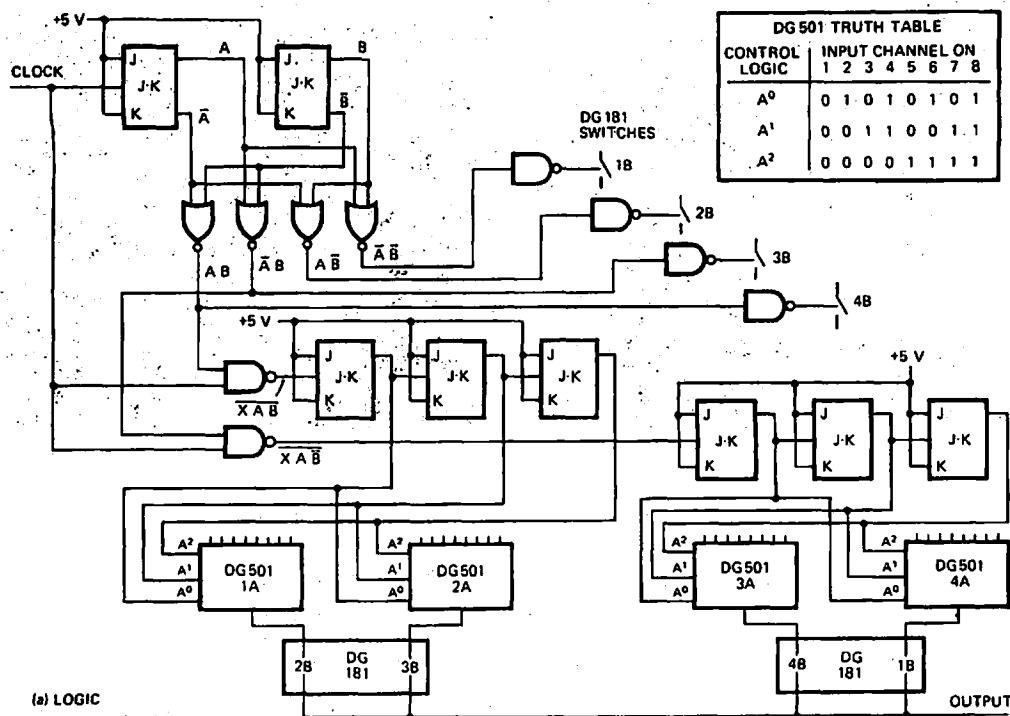
sampled for 125/32, or 3.906 μ s, as Fig. 2 indicates.

Conventional multiplexing networks can be implemented with either discrete components or integrated circuits, such as the Siliconix DG501 (see table). This circuit multiplexes eight input channels with a switching time between channels of 1 to 2 μ s. A 32-channel multiplexer is constructed simply by paralleling four DG501s. Thus, in single-level switching, each of the 32 analog input channels is multiplexed through a single switching bank.

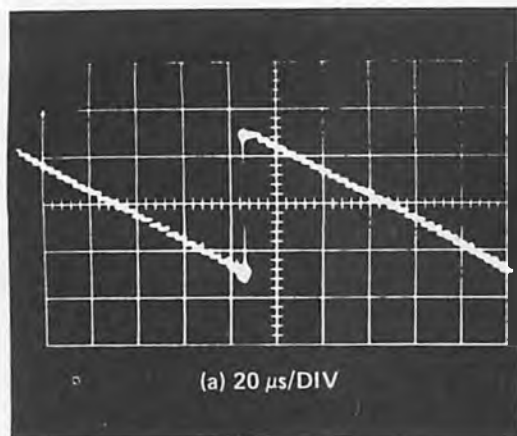
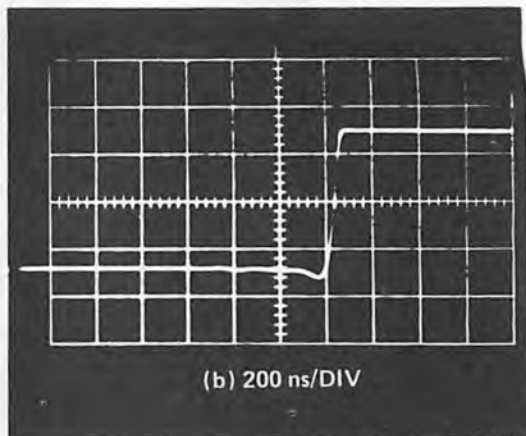
The problem with such a system stems from the relatively slow 1-2- μ s switching times between channels. Depending on the design of the particular multiplexer, there can either be an overlap between sampling pulses, which leads to crosstalk between channels, or a large separation between samples, which reduces the sampling time of a particular channel. The reduced



4. Phase II timing. By adding two-phase control logic to the two-level multiplexer of Fig. 3, the full advantage of the 150-ns switching speed of the DG181 circuits is realized. Channel numbers correspond with those in Fig. 3



5. Logic hardware. TTL control circuits (a) implement timing (b) required in two-phase, two-level multiplexing system. First-level DG501 switches are MOS circuits, and J-FET technology gives the faster switching times needed in the DG181 second-level switches.

(a) 20 μ s/DIV

(b) 200 ns/DIV

6. Quick switch. Thirty-two dc levels are sampled in a prototype multiplexer to demonstrate switching speed of the two-level two-phase design. Largest single transition, from -3 to $+3$ volts, is expanded in the lower trace. Vertical scale for both traces: 2 V per division.

sampling time results in lower multiplexer efficiency.

Added to the $1\text{--}2\text{-}\mu\text{s}$ switching time is a delay associated with the increased output-node capacitance when multiple channels are combined. For four DG501s (32 channels), the added delay is about 200 ns. These delays further reduce the effective sampling time and bring some uncertainty into the timing strobe for the a-d converter. The node-capacitance problem can be eased to some extent by a high-performance sample-and-hold circuit between the multiplexer and the a-d converter. However, the $1\text{--}2\text{-}\mu\text{s}$ switching times remain, and this problem becomes acute for signals obtained from sources with output impedances of 2 kilohms and above.

Two-level multiplexing

System-response time can be improved by reducing the output-node capacitance. This is achieved by using a two-level multiplexing system as shown in Fig. 3.⁴ Here, circuits with lower output capacitance (such as the DG181, with performance shown in the table) are placed in the second multiplexing level, which feeds the a-d converter.

The DG181 circuits can switch at a speed of 150 ns. The full advantages of these speeds, however, are not realized, since interchannel sampling time is still limited by the $1\text{--}2\text{-}\mu\text{s}$ rise times of the DG501s.

A timing sequence that makes maximum use of the switching rise times of the DG181s (and therefore results in extremely high sampling efficiency) can be achieved by applying control logic to the two-level multiplexer in a manner which will give the sampling sequence shown in Fig. 4. The faster switching speed and the break-before-make action of the DG181 virtually removes the possibility of overlap.

The problems caused by the relatively slow switching time of the DG501 are eliminated by ensuring that the first channels of multiplexer switches 1A and 2A (Fig. 3) are already fully closed when 2B and 3B, respectively, are closed, and that the first channels of switches 3A and 4A are fully closed when 4B and 1B, respectively, are closed. This sequence is then repeated for each of

the eight channels of the DG501s, and the complete cycle is again repeated.

Two-phase control logic

The timing requirement and logic-control layout for the complete circuit are shown in Figs. 5a and 5b. Waveforms A and B are obtained from the input clock waveform by an asynchronous divider. The A and B waveforms are combined to give AB , $\bar{A}\bar{B}$, $\bar{A}B$ and $A\bar{B}$ which are needed to close the DG181 gates sequentially. Functions XAB and $X\bar{A}\bar{B}$ then clock two three-bit asynchronous counters. A delay of two clock periods exists between XAB and $X\bar{A}\bar{B}$ so that the count sequence applied to the second and third multiplexer is suitably delayed.

A prototype multiplexer with two-phase control logic has been constructed and successfully tested. Series 7400 TTL circuitry is used to implement the timing and control logic. First-level DG501 switches are MOS circuits, while J-FET technology gives the faster switching times needed in the DG181 second-level switches.

To simulate all 32 analog inputs to the multiplexer, a voltage-divider network of series resistors is connected across a ± 3 -volt supply. Thus, 32 dc voltage levels are consecutively tapped off the network and applied to the multiplexer input. The multiplexer output is displayed on the oscilloscope, as shown in Fig. 6a. As can be seen, the largest transition is from -3 to $+3$ V. In Fig. 6b, this 6-V transition is demonstrated as being accomplished in less than 100 ns.

If low-power TTL or diode-transistor logic is used in the control circuits, synchronous counters may be necessary to eliminate cumulative flip-flop delays. Although the system shown is designed for negative-edge-triggered J-K flip-flops, the circuitry can be rearranged quite simply for almost any bistable logic element. $\square$

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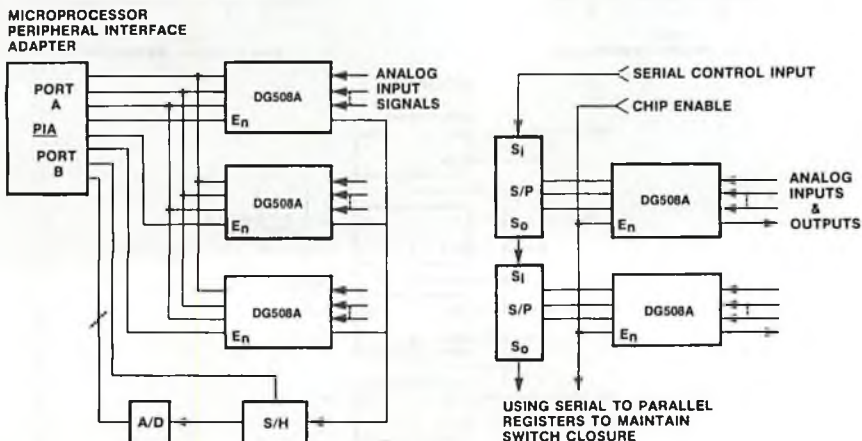
IMPROVED SYSTEM PERFORMANCE USING MICROPROCESSOR COMPATIBLE MULTIPLEXERS

Brian Wadsworth
Walt Heinzer
September 1983

INTRODUCTION

These new Siliconix multiplexers, the DG526, DG527, DG528 and DG529, feature the excellent characteristics of the DG506A-DG509A series with a bonus: latching logic. Microprocessor based systems are rapidly taking on more control tasks in electronic equipment. On chip latching logic in a multiplexer will, therefore, greatly simplify the microprocessor interface design and improve system performance.

When the micro is used in the "real world" of analog signals, it is often used in conjunction with analog multiplexers. Until recently, to interface the micro to the multiplexer has meant the use of some external memory device. These methods sometimes impaired system performance by compromising processor speed and always meant an increased component count. Two of these methods are illustrated in Figure 1.



Traditional Methods of Driving the DG508 MUX/DMUX with a Memory Device
FIGURE 1

With the introduction of these new multiplexers, the method of interface has been simplified. These devices have the memory function incorporated into the control circuitry of the multiplexer. Figure 2 illustrates functional diagrams of these multiplexers which show the memory devices in the form of latches.

These new devices are based upon the DG520 series of analog multiplexers. To examine the mode of operation, let us consider the DG528. The addition of the data latches on-chip has meant that two new control lines had to be introduced, i.e. $\overline{WR}$ and $\overline{RS}$. Figure 3 shows a detailed diagram of these input latches.

FUNCTIONAL DIAGRAMS

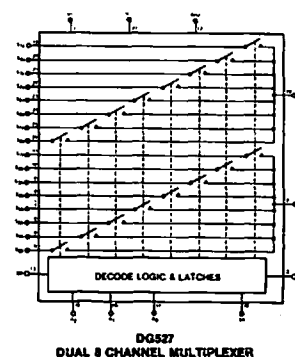
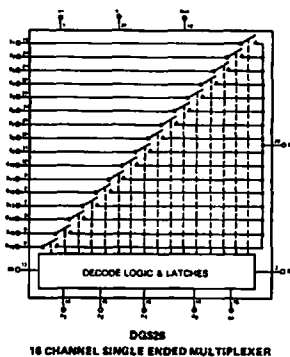
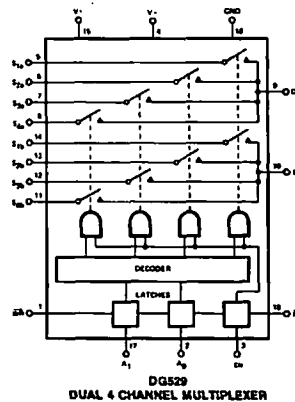
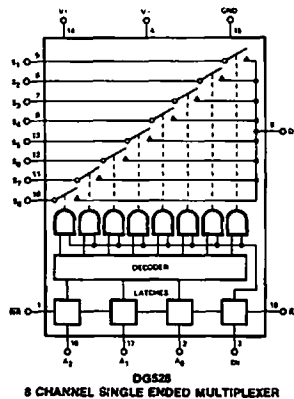


FIGURE 2

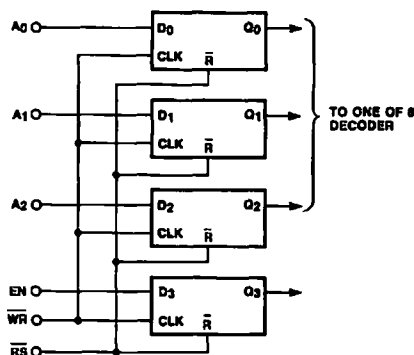


FIGURE 3

DECODE TRUTH TABLE - DG526

	A ₃	A ₂	A ₁	A ₀	EN	WR	RS	ON Switch
Latching	X	X	X	X	X	1	1	Maintains previous switch state
Reset	X	X	X	X	X	0	0	None (latches cleared)
	X	X	X	X	0	0	1	None
	0	0	0	0	1	0	1	1
	0	0	0	1	1	0	1	2
	0	0	1	0	1	0	1	3
	0	0	1	1	1	0	1	4
	0	1	0	0	1	0	1	5
	0	1	0	1	1	0	1	6
	0	1	1	0	1	0	1	7
Transparent Operation	0	1	1	1	1	0	1	8
	1	0	0	0	1	0	1	9
	1	0	0	1	1	0	1	10
	1	0	1	0	1	0	1	11
	1	0	1	1	1	0	1	12
	1	1	0	0	1	0	1	13
	1	1	0	1	1	0	1	14
	1	1	1	0	1	0	1	15
	1	1	1	1	1	0	1	16

DECODE TRUTH TABLE - DG528

A ₃	A ₂	A ₁	A ₀	EN	WR	RS	ON Switch
X	X	X	X	X	1	1	Maintains previous switch condition
X	X	X	X	X	0	0	None (latches cleared)
X	X	X	0	0	1	1	None
0	0	0	1	0	1	1	1
0	0	1	0	1	0	1	2
0	1	0	1	0	1	1	3
0	1	1	1	0	1	1	4
1	0	0	1	0	1	1	5
1	0	1	1	0	1	1	6
1	1	0	1	0	1	1	7
1	1	1	1	0	1	1	8

DECODE TRUTH TABLE - DG527

	A ₂	A ₁	A ₀	EN	WR	RS	ON Switch
Latching	X	X	X	X	1	1	Maintains previous switch state
Reset	X	X	X	X	0	0	None (latches cleared)
	X	X	X	0	0	1	None
	0	0	0	1	0	1	1
Transparent Operation	0	0	1	1	0	1	2
	0	1	0	1	0	1	3
	0	1	1	1	0	1	4
	1	0	0	1	0	1	5
	1	0	1	1	0	1	6
	1	1	0	1	0	1	7
	1	1	1	1	0	1	8

DECODE TRUTH TABLE - DG529

A ₁	A ₀	EN	WR	RS	ON Switch
X	X	X	1	1	Maintains previous switch condition
X	X	X	0	0	None (latches cleared)
X	X	0	0	1	None
0	0	1	0	1	1
0	1	1	0	1	2
1	0	1	0	1	3
1	1	1	0	1	4

Logic "1": V_{AH} ≥ 2.4V
 Logic "0": V_{AL} ≤ 0.8V

FIGURE 4

The first of these new control lines, $\overline{WR}$ (WRITE BAR, active low) is connected to the gating input of the latches. These latches become transparent whenever $\overline{WR}$ is driven to a logic low. During this state, data present on the address inputs is directly decoded and the appropriate switch closes. In fact, in this mode of operation ($\overline{WR}$ = low), the device functions identically to an earlier generation analog multiplexer, the DG508A. When $\overline{WR}$ returns to logic high, it will save the data present on the address lines in the data register. This ensures that the switches remain in their selected state irrespective of excursions on the address inputs.

The second new control line, $\overline{RS}$ (RESET BAR, active low), is an over-riding direct reset facility. When the reset input is activated, all data latch Q outputs are forced low and all switches opened. This reset facility is especially useful in processor based systems during power-up conditions. At this time all switches can be cleared, 'opened', preventing any undesirable switch action during initialization. If this initialization were left to software, it could easily take 10-30 instruction cycles to disable all switches. At an average 1.3 + μ secs each, it means 13 to 39 μ seconds of undesirable switch contact could take place. Therefore the direct reset facility provides a known safe power up initializing sequence.

The truth table shown in Figure 4 summarizes the logic

control functions of the DG520 series.

PERFORMANCE

Logic Inputs

The logic interface circuitry of the address inputs and control lines have been designed to simplify microprocessor interfacing. Each of these inputs, due to their CMOS construction, draws very low current (< 10 μ A) and provides extremely low capacitive loads (typ. 2.5 pF). Switching thresholds of these inputs have been designed to be fully TTL compatible. These features combine to ensure that each device can be driven directly from the microprocessor data bus.

All the logic inputs to the device carry input protection circuitry to protect the device against static damage. This input protection circuit consists of diodes to both positive and negative supply rails and a series resistor. The diodes forward bias to discharge any static energy into the supply rails while the resistor limits the current during this time to protect the diodes.

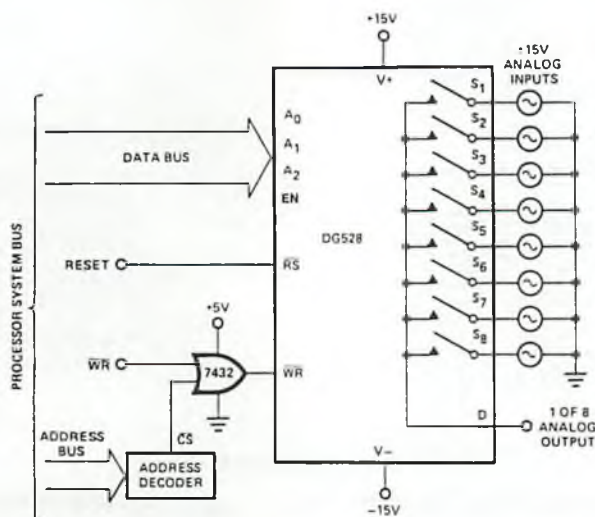
On-Chip Regulator

Also provided on-chip is a regulator which has been designed to provide stability against power supply and temperature variations. The design of this regulator ensures that:

- (a) TTL compatibility is maintained over a wide power supply variation.
- (b) Reduces the effects of temperature allowing the microprocessor timing specifications to be guaranteed over the full military temperature range, -55°C to $+125^{\circ}\text{C}$.

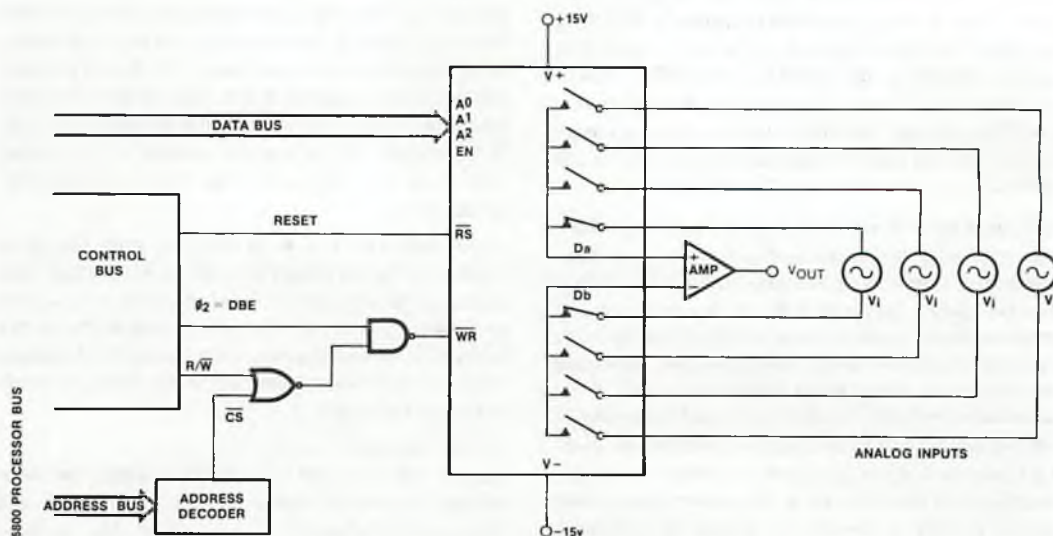
Interfacing

The DG520 series was designed to be fully compatible with the more popular NMOS microprocessors. In fact, the timing arrangements of the control lines were designed to be fully compatible with the 8085A-2 microprocessor. These minimum input timing arrangements are shown in Table 1. The diagrams shown in Figures 5 to 7 illustrate the ease with which these devices can be interfaced to various micros.



Complete 8085 Microprocessor to DG528 Interface

FIGURE 5



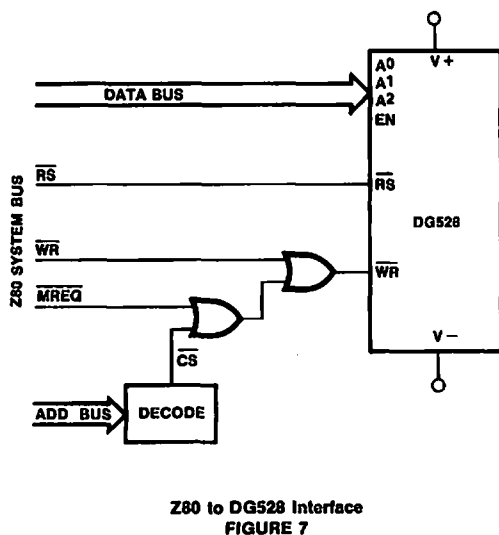
Complete 6800 Microprocessor Bus to DG529 Interface

FIGURE 6

Figure 5 illustrates the method of interfacing a DG528 to the 8085A processor. Notice that no additional bus buffering is required between the processor data bus and the multiplexer address inputs. A standard address decoder chip is still required to generate the chip select, $\overline{CS}$, signal. This $\overline{CS}$ is gated with the processor $\overline{WR}$ output to generate the $\overline{WR}$ signal for the DG528. These signals ensure that only when the DG528 is being addressed will information on the data bus affect switch states. This connection satisfies the processor's timing requirements since $\overline{WR}$ will only go active low once the information on the data bus has stabilized. Figure 5 also illustrates the direct connection between the processor system $\overline{RESET}$ and the multiplexer $\overline{RS}$.

The method of interface between the multiplexer and 6800 microprocessor bus is illustrated in Figure 6. In order to have a data valid signal, it is necessary to gate the ϕ_2 clock (often directly connected to the DBE) with $R/\overline{W}$ line. The gating of the chip select with the ϕ_2 , $R/\overline{W}$ combination is functionally identical to the 8080 connection.

The Z80 to multiplexer interface is shown in Figure 7. Simply by gating the $\overline{WR}$ and $\overline{MREQ}$ signals with the standard $\overline{CS}$ signal allows the correct $\overline{WR}$ signal for the multiplexer to be achieved.



The Process

These devices have been constructed using a new high voltage CMOS process called PLUS 40. This process was designed to provide a more rugged device while at the same time offer performance improvements over the original CMOS process. Basically, two features improve the ruggedness of the device:

- The gate oxides of the MOS transistors have been thickened, improving the DC rupture voltage by 33%. Combining this benefit with the improved input protection circuits and body clamped switch design results in improved static voltage immunity.
- The process maximum rating has been increased. PLUS 40 CMOS devices have an absolute maximum rating of 44V between supply rails. This means that devices can be operated at $\pm 15V$ supplies and still be within 75% of their maximum ratings.

Another important improvement achieved on the PLUS 40 process was the introduction of an ion-implantation technique. This technique allows much greater process control which results in very uniform, repeatable device parameters. In the case of analog multiplexers, for example, we achieve better matching characteristics switch to switch.

CHARACTERISTICS

Having discussed the performance of the device, we can now look at some of the important characteristics involved:

- First, the most critical specification of the device is its microprocessor timing arrangements. As was mentioned earlier, the timing of these devices was designed to be compatible with the 8085A. In actual fact the timings are such that the 8085A-2 can be operated on its maximum 5 MHz clock rate. The waveforms shown in Figure 8 illustrate the timing specifications for the DG520 series.

TIMING DIAGRAMS

Minimum Input Timing Requirements				
	Parameter	Measured Terminal	Min Limits over full temp range	Unit
t_{WW}	WRITE Pulse Width	$\overline{WR}$	300	ns
t_{Dw}	A, EN Data Valid to WRITE (Stabilization Time)	$A_0, A_1, (A_2), E_n$	180	
t_{WD}	A, EN Data Valid after WRITE (Hold Time)	$\overline{WR}$	30	
t_{RS}	RESET Pulse Width	$\overline{RS}$	500	

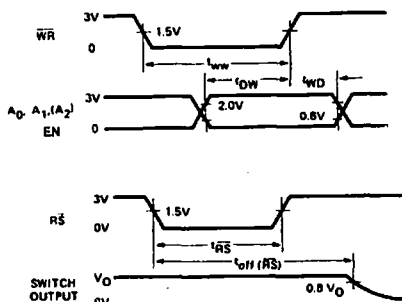


FIGURE 8

- Another parameter of importance, especially in such applications as sample and hold, is that of charge feedthrough. The graph shown in Figure 9 shows a typical curve for this parameter. In fact all PLUS 40 devices have compensation on the output switches to reduce switching errors due to charge feedthrough.

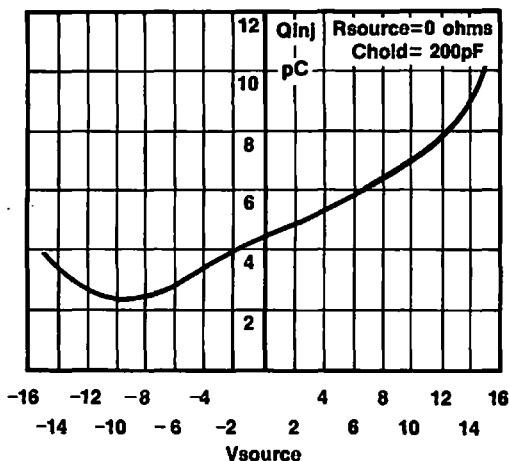


FIGURE 9

- The V error figure of merit is sometimes used as a parameter for evaluating switch performance. This parameter is the product of $R_{DS(on)}$ and $I_{D(on)}$ switch leakage current. It is a primary contributor to switch voltages errors when switching very low level signals such as thermo-couple voltages. The DG528 has a worst case specified V error of 100 microvolts at 125°C while at room temperature this figure reduces to 4 microvolts maximum.

SUMMARY

We are now in a position to analyze this information to identify user benefits. These benefits can be itemized as shown below:

- The ease of interfacing means that component count is reduced. This has the obvious benefit that overheads are reduced because component, inventory, manufacturing and production costs are reduced. Also, because component count is reduced, the systems reliability is increased.

- Because the timing arrangements are fully microprocessor compatible, then a more efficient system performance is obtainable.
- Much simpler power supply requirements are facilitated due to the on-chip regulator and the PLUS 40 construction.
- Its Plus 40 construction also means a more reliable, high performance device.

APPLICATIONS

Temperature Monitoring

In these systems, an array of transducers are switched one at a time to an analog-to-digital converter. Figure 10 illustrates the necessary steps in designing the front-end system. This system assumes that the transducers generate small differential signals upon which fairly large common-mode noise is superimposed. This common-mode signal can be assumed to be 50 Hz power line pick-up. Transducers with this type of characteristic would be thermistors wired in a bridge configuration.

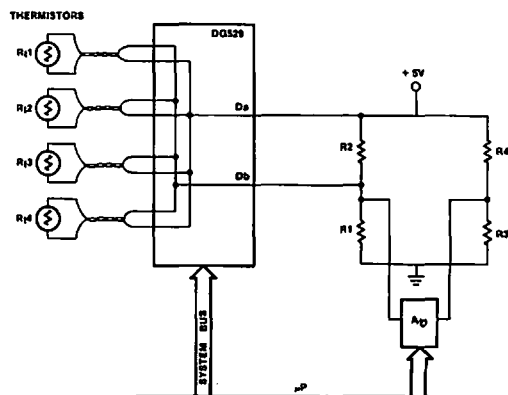


FIGURE 10

To calculate the errors introduced by the multiplexer, assumptions about the range of the differential signal, V diff, need to be made. A weighted thermistor bridge will easily have an output voltage swing of 0 to 100 mV, representing an input temperature range of 0 - 100°C. The second assumption is that the common mode noise pick-up is approximately 2V p-p. Finally, a measurement accuracy of 1%, or 1°C is required from a bridge with nominal output impedance of 500 ohms.

There are basically two sources of errors to analyze:

- DC errors contributed by the multiplexer. Figure 11 shows the steady-state differential voltage input path for one switch closed. As can be seen, the primary error source is the product of leakage currents in the signal path resistances. These leakage currents generate additional system offset voltages which, even though the bridge presents an unbalanced resistance, are acceptable.
- Common-mode voltage becoming a differential error due to the resistively unbalanced signal paths. This is the major contributor toward system error.

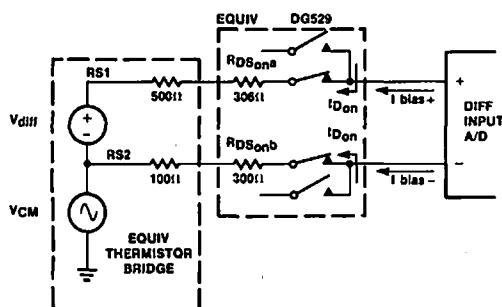


FIGURE 11
Steady State Errors

The total error voltage due to the DG529 is calculated as:

$$V_{\text{error}} = I_{D(\text{on})} \times (R_{DS(\text{on})a} + 500) - I_{D(\text{on})} \times (R_{DS(\text{on})b} + 100)$$

$$= 10\text{nA} \times (306 + 500) - 10\text{nA} \times (300 + 100) = 4.06\mu\text{V}$$

Thus the Multiplexer contributes negligible offset error.

The differential input A/D would contribute an additional offset of:

$$V_{\text{error}} = I_{\text{BIAS}} (+) \times (R_{DS(\text{on})a} + 500) - I_{\text{BIAS}} (-) \times (R_{DS(\text{on})b} + 100)$$

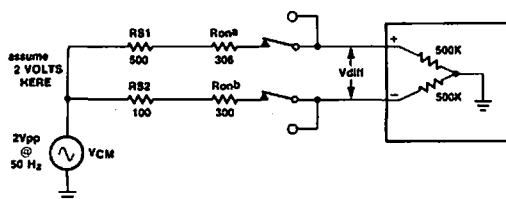


FIGURE 12

The instantaneous voltage appearing at the input to the A/D due to the 2 volt peak to peak common mode voltage is:

$$V_{\text{diff}} = (500k / (500 + 306 + 500k)) - 500k / ((100 + 300 + 500k)) \times 2 = 1.6\text{mV}$$

The 1.6mV adds to the thermistor output voltage signal as a superimposed 50Hz normal mode voltage. This signal can be rejected by using an integrating A/D converter sampling at an integer multiple of the 50Hz noise period.

Figure 12 shows how the common-mode voltage directly adds to the differential signal representing temperature. The net result is a 50 Hz differential error signal, superimposed on the DC temperature signal, of 1.6 mV p.p. This represents an error of 2°C which can be eliminated using an integrating A/D sampling at an integer multiple of the 50 Hz noise frequency.

It is worth pointing out at this point that if the bridge resistances were balanced, i.e. $RS1 = RS2 = 500$ ohms, then the multiplexer would only contribute a 0.024% error (assuming a 2% match for switch on-resistance). The dynamic characteristics of the switches are relatively unimportant in this application since temperature is a slowly varying signal.

AUTOMATIC TESTERS

In this application the dynamic performance of the switch is of importance. Figure 13 illustrates a PC board continuity tester, and this can be used to demonstrate the advantages of the DG528. To ensure that no paths (dendrites) for electro-migration are present, these testers require 30 volt bias between tracks.

Figure 14 shows a technique for applying the 30 volt bias to the PC board to perform the insulation test. The sense resistor is connected in series with the insulation resistance to form a voltage divider. The output of the divider is measured by the high input impedance sense amplifier. The sense amplifier output is then compared with a programmable limit to determine the test result. The critical multiplexer specifications in this application are leakage currents and capacitances. Leakage currents limit the maximum measurable resistances while capacitance increases the measurement settling time.

Switch leakage currents should be 10% of measured current to enable 100 Megohm resistances to be measured. Therefore maximum leakage should be:

$$\frac{10}{100} \times \frac{30}{100} \mu\text{A} = 30 \text{ nA}$$

The DG528 has a maximum $I_{D(\text{on})}$ leakage of 10 nA at +25°C

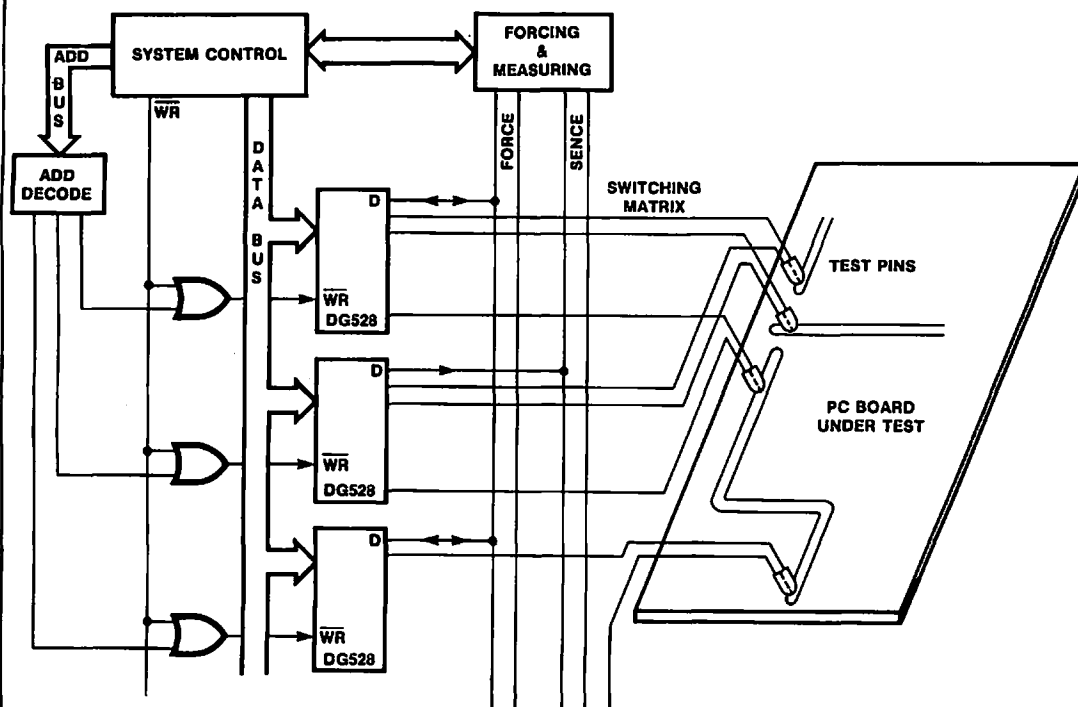
Capacitive loading is only critical for the test-node since it must charge through the insulation resistance. The force node is low impedance, therefore does not have a critical capacitance requirement. This capacitive loading on the test node defines the maximum achievable speed.

CD(off) is specified as 25 pF for the DG528. Assuming a 100 mΩ test limit, this loading results in a 2.5 mS circuit test time-constant. If multiplexers are being cascaded and sharing the test node then the time constant can be calculated using the formula: $N \times \text{Insulation Resistance} \times 25 \text{ pF}$, where N = number of multiplexers.

The second function of the tester is continuity testing, and this is illustrated in Figure 15. This circuit design uses 4 wire sensing to eliminate errors generated by $I \times R$ drops in

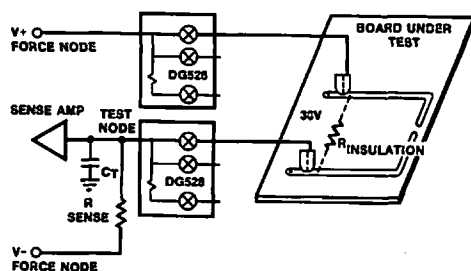
the forcing current path. Switch and probe-to-PC Board contact-resistance no longer limit the measurement of the copper foil continuity. Testing speed is fairly fast since all impedances are low, keeping circuit time constants short. To minimize the total test time a high slew rate sense amplifier should be used.

One final point is that because the DG528 has full bidirectional switching capabilities, the insulation and continuity tests share the same set of matrix switches.



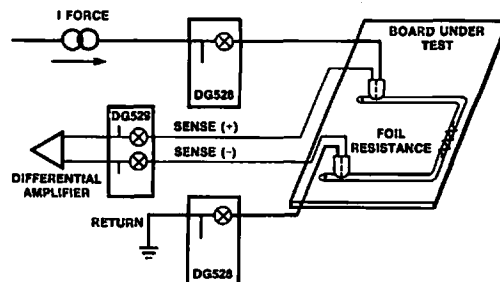
PC Board Continuity Tester

FIGURE 13



Simplified Circuit Highlighting the Insulation Test

FIGURE 14



Simplified Circuit Highlighting the Continuity Test Using Kelvin (4 wire) Sensing.

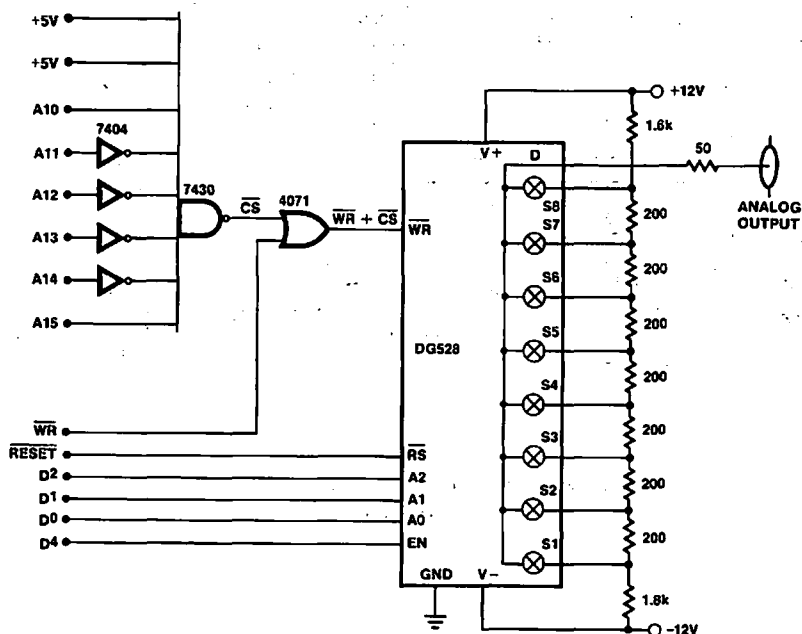
FIGURE 15

Conversely, the 'back-end' system utilized the DG528 as a demultiplexer where signal outputs from the D/A can be used for various functions. For example, it may be a corrective signal to a controller to reduce system error or simply a signal for an analog display.



Hex Add.	Hex Code	Assembler Code	Description
(20)00	31	LXI SP, 2080H	; Initialize stack pointer.
01	80		
02	20		
03	3E	MVI A, 0A	; Set interrupt register value.
04	0A		
05	30	SIM	; Set interrupt mask (loads interrupt register from accumulator).
06	FB	EI	; Enable interrupt at this point (when interrupt key is pressed, program runs until this point).
07	3E	MVI A, 0F	; Load the accumulator with the value 0F Hex (this represents "enable" switch 8).
08	0F		
09	32	STA, 8400H	; Store the accumulator value at memory location 8400 Hex.
0A	00		(8400H is the location of the 528 in this application.)
0B	84		
0C	3E	MVI A, 08	; Load accumulator with the value 08 Hex (this represents "enable" for switch 1).
0D			
0E	32	STA, 8400H	; Store the accumulator value at memory location 8400 Hex.
0F	00		
10	84		
11	C3	JMP, 2006H	; Jump (loop)back to the enable interrupt at location 2006 Hex and start again.
12	06		
13	20		
CE	FB	EI	; When interrupt (VECT INT) key is pressed, the monitor transfers control to location 20CE Hex.
CF	76	HLT	
D0	C9	RET	

Example Program Run in the Circuit Setup of Figure 16 with the SDK-85 Development System.



A Simple D/A Converter Constructed with the Intel SDK-85 Development System. See the Next Page for Some Demonstration Software.

FIGURE 17

Process Control

Figure 18 illustrates a novel use of the DG527. Differential multiplexers are generally used in process control applications to eliminate errors due to common mode signals. In this circuit however, advantage is taken of the dual multiplexing capability of the switch. This is achieved by using the multiplexer to select pairs of R.C. networks to control the pulse width of the multivibrator. This can be a particularly useful feature in process control applications where there is a requirement for a variable width sample "window" for different control signals.

The applications explained in this note highlight only a few of the intended uses of this new range of multiplexers. They are intended, basically, to act as a catalyst for design engineers to invent applications for their own areas.

Other areas where these devices may be used include security systems, air conditioning and heating control, food process machinery, petro-chemical production, avionics, and communications systems.

The circuit functions performed by the devices include analog multiplexing, demultiplexing, programmable gain switching, attenuation, simple D/A conversion and more.

Finally, the simple D/A converter shown in Figure 17, in conjunction with the 8085 based development system (SDK 85) helped define the necessary architecture of the DG528 and DG529. This circuit can easily generate very complex waveforms under processor software control.

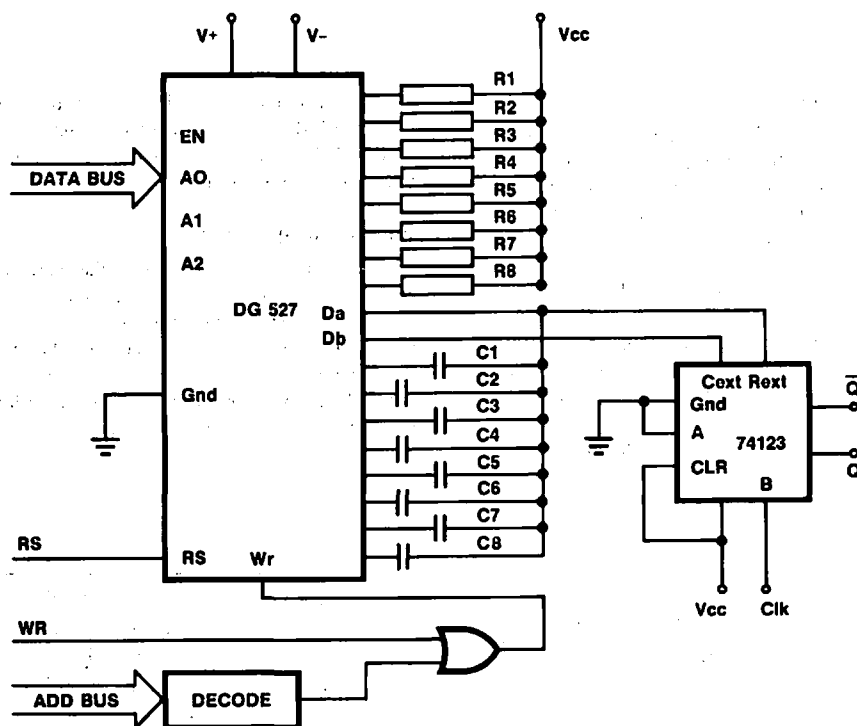


Figure 18.
μP Selected Pulse Width Control

References:

1. **Thermistors** — Thermometrics Catalogue No. 181-A, Edison N-J.
2. **Analog Switches and Their Applications** — Siliconix Applications Staff, June 1980.

FUNCTION/APPLICATION OF THE LD110/LD111A 3½ DIGIT A/D CONVERTER SET

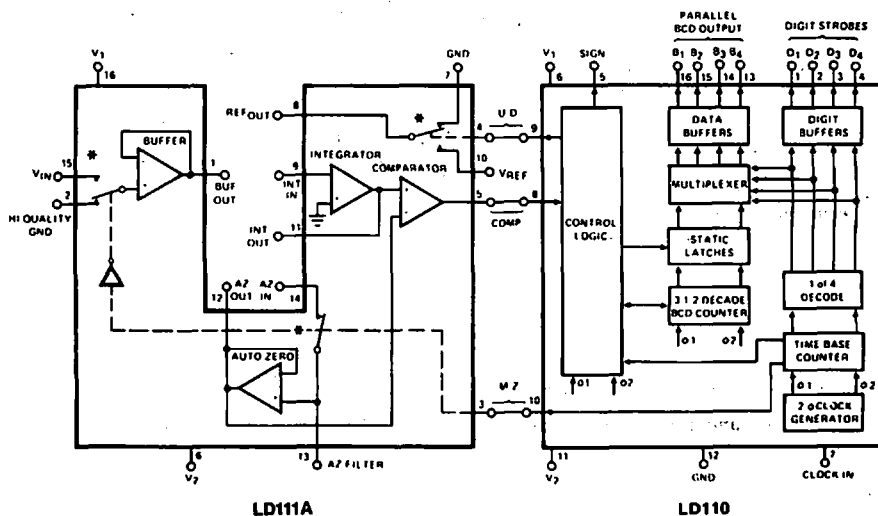
INTRODUCTION

The Siliconix LD110/LD111A 3½-digit A/D converter integrated circuit set offers high performance and versatility with a minimum of required external circuitry. The set consists of a monolithic PMOS synchronous digital processor (LD110) and a monolithic bipolar-PMOS analog processor (LD111A). The salient features of the A/D converter set include an accuracy of 0.05% (of reading) ± 1 count; a 4 pA typical input bias current; an input impedance of greater than 1,000 M Ω ; autozeroing; and a single reference voltage requirement. External user-selected components will allow for two different voltage ranges (2,000 V and 200.0 mV) and a wide range of sampling rates (1/3 to 12 samples per second) to accommodate a variety of applications.

This Application Note describes the functional operation of the LD110/LD111A A/D converter chip set, provides a basis for criteria in external component selection, and offers some practical circuit applications.

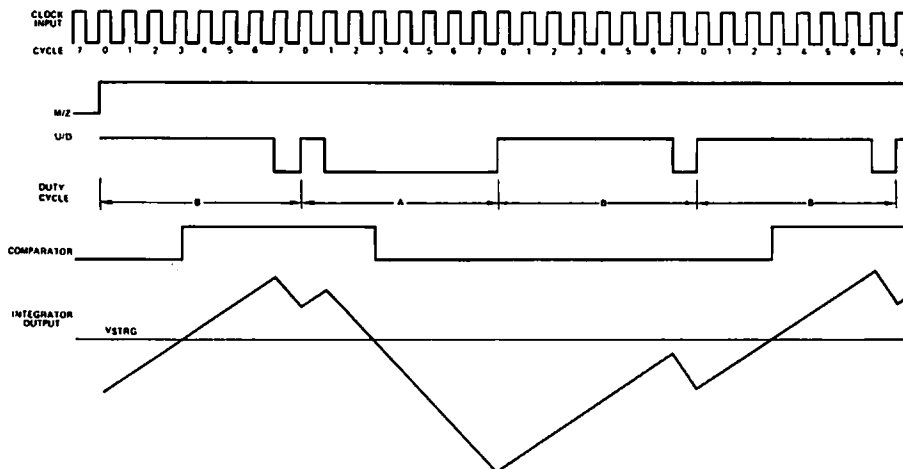
Functional Operation

The conversion technique balances the charge supplied by a current proportional to the input voltage, over a measure interval, with an accumulation of quantized charges equal to a BCD count. The units of quantized charge are provided through pulsewidth modulation of a reference current. In Figure 1, the A/D converter set is shown with the external RC components required to analyze the functional operation.



* P-channel Enhancement Mode MOS-FET Switches
U/D Shown in Down State (logic "0") M/Z in Zero State (logic "0")

Functional Diagram
Figure 1



Measure Interval Timing
Figure 2

The clock frequency is divided by the time-base counter of the LD110 digital processor into sampling intervals of 6144 cycles; 4096 cycles constitute the measurement interval and 2048 cycles make up the auto-zero interval.

The auto-zero interval allows the effects of offset, temperatures and drift to be impressed on the auto-zero storage voltage, V_{strg} , which is maintained as a reference by C_{strg} . Therefore, during the succeeding measure interval these effects will be balanced out. In addition, V_{strg} acquires a voltage component available at the AZ amplifier output, which provides a current equal to $-\frac{1}{2} V_{REF}/R_1$ through resistor R_3 . The net current provided to the integrator summing node by the sum of V_{strg}/R_3 and the current through R_1 is either + or $- V_{REF}/2R_1$, depending on the position of the Up/Down switch. The input of the buffer amplifier is grounded during this interval.

The input voltage V_{IN} is applied to the input buffer amplifier during the measure interval. This amplifier, in conjunction with R_2 , supplies an additional current V_{IN}/R_2 to the integrator summing node. The comparator transmits the state of the integrator output (with respect to V_{strg}) to the control logic. The control logic attempts to establish equilibrium in the circuit by operating the Up/Down switch at one of the two available duty cycles (7 clock cycles UP, one cycle DOWN; 1 clock cycle UP, 7 cycles DOWN) while the counter keeps track of the net UP count. The integrator output, Measure/Zero (M/Z), Up/Down (U/D) and comparator levels during the measure interval are shown in Figure 2.

The following equations describe the measurement technique:

$$\Delta Q = 0$$

WHERE:

$$\Delta Q = \frac{V_{IN}}{R_2} \Delta t_{measure} - \frac{V_{REF}}{2R_1 f_{IN}} (NU) + \frac{V_{REF}}{2R_1 f_{IN}} (ND) \quad (1)$$

WHERE:

$(NU) = (\# \text{ counts UP})$ and

$(ND) = (\# \text{ counts DOWN})$

BUT:

$$\# \text{ counts UP} + \# \text{ counts DOWN} = 4096 \text{ (clock cycles in the measure interval)} \quad (2)$$

$$\# \text{ counts UP} - \# \text{ counts DOWN} = \text{net count} \quad (3)$$

THEN:

$$0 = \frac{V_{IN}}{R_2} \Delta t_{measure} - \frac{V_{REF}}{2R_1 f_{IN}} (\text{net count}) \quad (4)$$

BUT:

$$\Delta t_{measure} = 4096/f_{IN} \quad (5)$$

Substituting and multiplying by f_{IN} yields

$$\text{Net count} = V_{IN} \cdot \frac{R_1}{R_2} \cdot \frac{8192}{V_{REF}} \quad (6)$$

Equation (6) is fundamental to the application of the LD110/LD111A A/D converter set.

Component Selection

Application of the LD110/LD111A A/D converter set should begin with the selection of power supplies and the clock frequency. The recommended supply voltages are $V_1 = 12 \text{ V} \pm 10\%$, $V_2 = -12 \text{ V} \pm 10\%$ and $V_{SS} = 5 \text{ V} \pm 10\%$. Clock frequencies between 2 kHz and 75 kHz are recommended. The duty cycle of the clock is not of particular importance; the logic "0" time should however, be greater than $5 \mu\text{sec}$. The sampling rate and clock frequency are related as follows:

$$\text{Sampling Rate} = f_{IN}/6144 \quad (7)$$

The clock frequency may be chosen to minimize line frequency interference. If the auto-zero and measurement periods are integral multiples of the line frequency (f_L) period, line frequency rejection will be maximized:

$$\Delta t_{ZERO} = 2048/f_{IN} \quad (\Delta t_{measure} = 2 \Delta t_{zero}) \quad (8)$$

$$\frac{2048}{f_{IN}} = \frac{n}{f_L}, \text{ where } n = 1, 2, 3, \dots 51 \quad (9)$$

THEN:

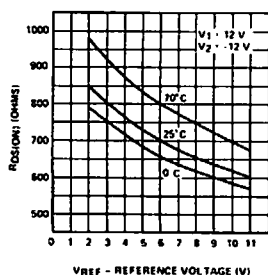
$$f_{IN} = \frac{2048 f_L}{n} \quad (10)$$

Once the clock frequency is chosen, the proper values for the external RC components may be determined.

Equation (6) defines the relationship between the ratio R_1/R_2 and the reference voltage V_{REF} when a full-scale voltage range V_{IN} (F.S.) is chosen. This relationship is:

$$\frac{R_2}{R_1} = \frac{V_{IN}(\text{F.S.})}{2000} \cdot \frac{8192}{V_{REF}} \quad (11)$$

It is usually more convenient to select V_{REF} before assigning resistance values because of the implications of temperature coefficients, availability, or other considerations. V_{REF} should be greater than 5 V, but less than V_1 . As V_{REF} is increased the U/D switch ON resistance decreases, as is shown in Figure 3. R_1 also increases with V_{REF} , thus decreasing the proportion of the total resistance provided by $r_{DS(ON)}$. Consequently, a large V_{REF} minimizes the effects of the U/D switch ON resistance. It is very important that V_{REF} have a low temperature coefficient to minimize drift and the resulting count error.



$R_{DS(ON)}$ (U/D Switch) vs. V_{REF} and Temperature
Figure 3

Equation (12) shows the change in count which will occur for a fractional change in V_{REF} (see Appendix A, Page 10)

$$\Delta \text{count} = -2000 \frac{V_{IN}}{V_{IN}(\text{F.S.})} \cdot \frac{\Delta V_{REF}}{V_{REF}} \quad (12)$$

Consequently, the count will decrease by 1 for each +0.05% change in V_{REF} , for $V_{IN} = V_{IN}(\text{F.S.})$

R_2 should be chosen to supply a full scale current of 20 μA into the integrator summing node (100 $\text{k}\Omega$ for 2.000 V and 10 $\text{k}\Omega$ for 200.0 mV). R_1 can then be determined by Equation (11). R_1 , R_2 and V_{REF} and the basic temperature-sensitive components of the system. The auto-zero interval makes the system essentially independent of changes in C_{INT} , R_3 , R_4 , R_5 , C_{strg} and the offset voltages of the amplifiers. In Figure 3, note that the U/D switch ON resistance has a temperature coefficient of about $0.2/^\circ\text{C}$. This temperature-dependent resistance must be considered as a part of R_1 , the reference resistor. The error in count resulting from a change in this total resistance R_1 is examined in Appendix B (Page 10) and found to be:

$$\Delta \text{Count} = 2000 \frac{V_{IN}}{V_{IN}(\text{F.S.})} \cdot \frac{\Delta R_1}{R_1} \quad (13)$$

Since the count is proportional to the ratio R_1/R_2 , equal temperature coefficients for these resistors should allow this ratio (and the count) to be maintained even with a change in the ambient temperature. It is desirable, however, to use resistors with low temperature coefficients for R_1 and R_2 to reduce any errors resulting from the differences in these coefficients.

The net error that can be attributed to temperature effects is the sum of the errors due to the changes in V_{REF} and the $R_{DS(ON)}$ of the U/D switch. Temperature compensation for the A/D converter circuit, then, can be approached in two different ways. The first method would be to provide a large V_{REF} (less than V_1 , however) with a very low temperature coefficient. This would require a large value of resistance for R_1 , reduce $R_{DS(ON)}$ and make changes in $R_{DS(ON)}$ negligible. The alternative method is to note that a reference voltage with a positive temperature coefficient produces an error in the count which tends to oppose the error caused by the positive temperature coefficient of $R_{DS(ON)}$. Thus the two effects can be used to counteract one another (an example is provided in Appendices A and B).

The specified accuracy of the A/D converter will be maintained if the integrator capacitor C_{INT} is chosen so that the voltage swing of the integrator is held to within 0.75 volt of V_{strg} . An analysis of this constraint, shown in Appendix C, (Page 11) results in the following relationship for C_{INT} :

$$C_{INT} = \frac{28.5 V_{IN}(\text{F.S.})}{R_2 f_{IN}} \quad (14)$$

This capacitor and the zener diode to be placed in parallel with it should have a combined leakage of less than 10 nA (see Appendix D, Page 11) to minimize this possible source of error.

The storage voltage, V_{strg} , should be maintained between -2 V and -5 V for normal operation. The ON resistance of

the auto-zero (AZ) switch is typically 11 K Ω at $V_{strg} = -4$ V ($V_2 = -12$ V), and will increase significantly with an increasingly negative storage voltage. Resistor R_3 can be selected to provide the desired V_{strg} by using Equation (17). The integrator output, which swings around V_{strg} during the measure and zero intervals, must always be more positive than -9 V to maintain the functionality of the analog processor. This can be accomplished by placing back-to-back Zener diodes in parallel with C_{INT} (the second diode is to prevent the Zener from being forward biased). It then becomes important that the integrator output voltage not exceed the breakdown voltage of the Zener diodes, for the maximum input voltage for which an accurate readout is desired. The relevant equations are:

$$V_{O(min)} > -V_{zener} \quad (15)$$

WHERE:

$$V_{O(min)} = V_{strg} - \frac{7}{f_{IN}C_{INT}} \left[\frac{V_{REF}}{2R_1} + \frac{V_{IN(max)}}{R_2} \right] \quad (16)$$

(see Appendix C)

$$V_{strg} = \frac{-V_{REF}}{2} \frac{R_3}{R_1} - \frac{R_3}{R_2} V_{Hi-Q} \text{ (If Hi-Q Gnd)} \quad (17)$$

is not at zero potential)

If $V_{O(min)}$ exceeds the breakdown voltage value of the selected Zener diodes, either V_{strg} or C_{INT} must be adjusted to maintain this inequality (see Equation (15)).

A number of engineering tradeoff considerations must be made in selecting RC components for the A/Z filter (R_4 , R_5 and C_{strg}). Some of these are covered in Appendix E. Various component values for different clock frequency ranges are presented in Table I, along with the recommended values for the integrator capacitor, C_{INT} .

TABLE I
Auto/Zero Filter Values

f_{IN} (kHz)	C_{INT} (μ F)	C_{strg} (μ F)	R_4 (K Ω)	R_5 (K Ω)
2 to 10	0.1	1.0	68	15
10 to 20	0.039	0.056	240	47
20 to 40	0.022	0.056	120	33
40 to 75	0.01	0.056	82	18

APPLICATIONS

Digital Voltmeters

The circuits shown in Figure 4 present the LD110/LD111A A/D converter set in typical ± 2.000 V digital voltmeter applications. The clock frequency of 24.5 kHz provides a sampling rate of 5 samples per second. Trimmer resistor R_6 calibrates the DVM. R_1 and R_2 are metal film resistors.

The illustrated connection of the analog circuit grounds (Pins 2 and 7 of the LD111A) and the digital circuit ground (Pin 12 of the LD110) is for schematic convenience only. The digital component grounds should be connected together and brought to a reference point such as the input voltage ground, and not directly to the pins of the LD111A.

The use of a seven-segment LED for Digit 4 will allow the DVM to be employed up to the maximum count of 3100. The output of the BCD-to-seven-segment decoder will be erroneous during Digit 4 time, however, because under-range information is encoded on bit 4 during Digit 4 time. The bit 4 input of the decoder in Figure 4a (bit 4 is the most significant bit) should be clamped to ground during Digit 4 time to provide the correct Digit 4 readout, as in:

$$\text{Input D of decoder} = B_4 \cdot \bar{D}_4 \quad (18)$$

where B_n is the nth BCD data bit and D_n is the nth digit.

The display will blink at a rate equal to the sampling rate when the count exceeds 1999. If the grounding system is poor, erroneous readings will result for counts of 2000 and above.

The data output format is an interlaced scan of Digits, 1, 3, 2 and 4 with Digit 4 as the most significant digit. This permits the use of Sperry displays with clock frequencies of 25 kHz or less. All outputs are active high and TTL-compatible.

The overrange and underrange signals may be obtained by external logic, i.e.,

$$\text{MUX Underrange} = B_4 \cdot D_4 \text{ (5\% of full scale)} \quad (19)$$

$$\text{MUX Overage} = \bar{D}_1 + \bar{D}_2 + \bar{D}_3 + \bar{D}_4 \text{ (100\% of full scale)} \quad (20)$$

Autorangeing DVM

The circuit in Figure 5 shows how the decoded underrange and overrange signals can be used to make an automatic-ranging DVM. The circuit will cycle through five ranges (200 mV to 2,000 V), starting with the most sensitive range and proceeding through the less sensitive ranges until the proper operating range is attained.

When the cycle proceeds from the most sensitive to the least sensitive range, the proper range will be achieved for voltages which will provide a count between 1000 and 2000. If the cycle began at the least sensitive range, a voltage such as 15.0 V would be read on the 200 V range, since the count of 150 would not initiate an underrange signal to advance the circuit to a more sensitive range.

The two-input NOR gate decodes the underrange signal to preset the shift register with a "1" logic at each of the parallel bit outputs. A Siliconix DG201A quad SPST CMOS



Figure 4A

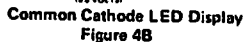
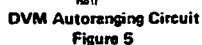


Figure 4B



analog transmission gate is employed in the circuit so that each of the four switches of the DG201A will be OFF when a logic "1" signal appears at the appropriate input.

Diodes D_1 and D_2 clamp the input of the LD111A processor at ± 5 V to prevent damage which could result from large input voltages. The presence of the overrange signal (Equation (20)), decoded by the combination of the five inverters and NAND gate 1, transfers the logic "0" signal which appears at NAND gate 2 into the shift register. Logic "0" appears at the A output of the shift register and turns on the DG201A switch which is associated with R_2 , producing a voltage division of 10:1. The serial input of the shift register remains at logic "1" when any of the outputs are at logic "0"; this insures that only one of the four DG201A switches is ON at a given time. The logic "0" signal is shifted through the register until the proper range is acquired. When the input voltage is removed the decoded underrange signal returns the shift register to the initial state.

The current-sinking capability of the shift register can be used to turn on the appropriate decimal point cathode of the LED display, with the only additional required component being a 150 Ω current-limiting resistor. Inverters 1 through 4 can be used as inverters 1-4 of the DVM circuit shown in Figure 4. The filter $R_6 C_1$ insures that there will be only one range change for each overrange signal, while the filter comprised of $R_7 C_2$ eliminates an erroneous underrange signal which can occur if bit 4 of Digit 2 time overlaps into Digit 4 time.

The $R_6 C_1$ and $R_7 C_2$ filters are optimized for the 24.5 kHz clock frequency of the DVM circuit in Figure 4. Clock frequencies of less than 10 kHz or greater than 40 kHz may require the adjustment of C_1 and C_2 .

The ON resistance of the four switches in the DG201A quad transmission gate is typically 160 Ω with ± 12 V supplies. This resistance has been considered in determining the values of range resistors R_2 , R_3 , R_4 and R_5 . Some trimming may, however, be necessary.

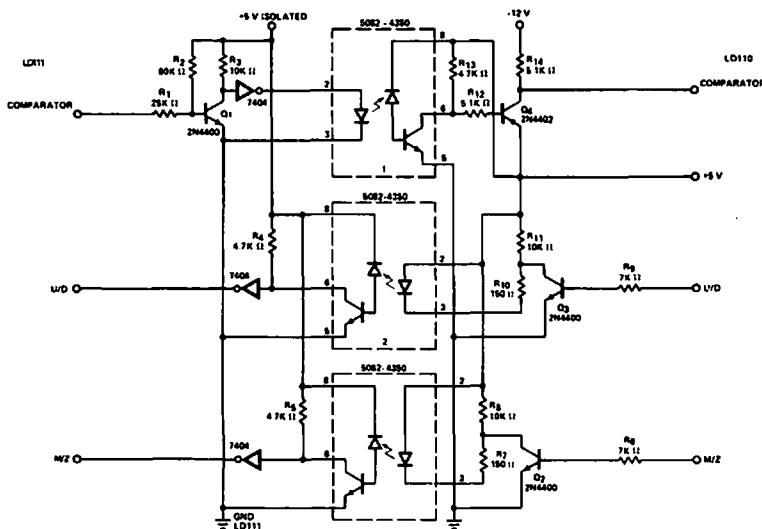
The input impedance is greater than 10 M Ω on all ranges. Since the circuit changes range once every sampling period, the time required to attain a reading on the highest range is $30720/f_{IN}$.

Isolated Analog Processor

The isolation circuit shown in Figure 6 provides a floating analog processor for measurement of off-ground signals such as those found in medical, nuclear, and process control instrumentation.

The three analog-to-digital interface signals (M/Z, U/D and comparator) are isolated via high-speed optical couplers with a 2,500 V insulation. Transistors Q_1 , Q_2 and Q_3 provide TTL level drive capability to interface the optical couplers with the LD110/LD111A system signals. The isolators in the M/Z and U/D channels are used in the non-inverting mode while the isolator in the comparator interface is used in the inverting mode. Transistor Q_4 shift the TTL level signal to the MOS level required at the LD110 comparator input.

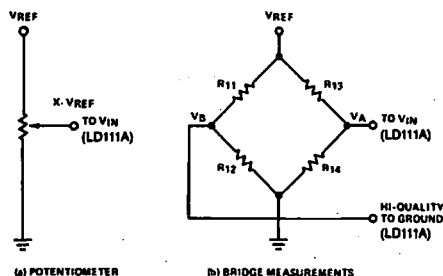
Although the isolators tend to shorten the pulse length of the LD110/LD111A system signals, the unique conversion technique of the system automatically compensates for this, and no additional adjustments are necessary.



Optical Isolation Circuit
Figure 6

Ratio Measurements

Equation (6) shows that the LD110/LD111A A/D converter measures input voltage as a ratio: the count is proportional to the ratio of the input voltage and the reference voltage. This system conversion technique is ideally suited to the measurement of ratio. Ratio measurements using a reference voltage which is also the excitation voltage of the ratio device allows measurements to be independent of variations in the excitation voltage. Typical ratio-measuring circuits are shown.



Ratio Measurements
Figure 7

The output of the potentiometer in Figure 7A (which can represent position, level, etc.) can be substituted in Equation (6) to demonstrate this capability:

$$\text{Count} = X V_{\text{REF}} \cdot \frac{R_1}{R_2} \cdot \frac{8192}{V_{\text{REF}}} = \frac{R_1}{R_2} \cdot 8192 X \quad (21)$$

Bridge transducer measurements, as shown in Figure 7B, can also be normalized to an external reference. The Hi-Q ground input of the LD111A functions as the inverting input of a difference amplifier to provide a count proportional to the difference of the two input voltages V_A and V_B .

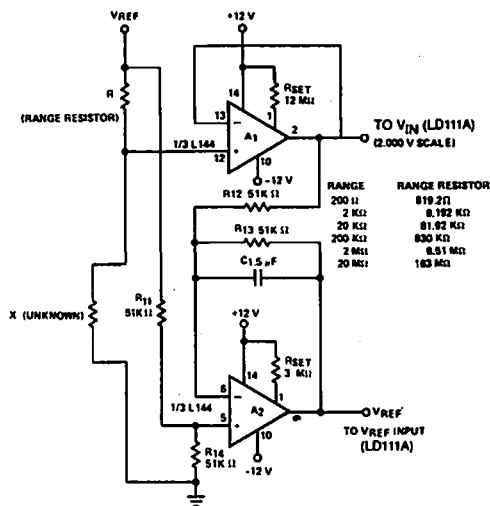
$$\begin{aligned} \text{Count} &= \frac{R_1}{R_2} \cdot \frac{8192}{V_{\text{REF}}} (V_A - V_B) \\ &= \frac{R_1}{R_2} \cdot 8192 \left(\frac{R_{14}}{R_{13} + R_{14}} - \frac{R_{12}}{R_{11} + R_{12}} \right) \end{aligned} \quad (22)$$

Ratio measurement techniques can also be extended to resistance measurement. The resistance-measuring circuit shown in Figure 8 will measure accurately to 20 MΩ when associated with a buffer amplifier (A1) having a low input bias current ($I_{\text{IN}} < 30 \text{ nA}$). The circuit illustrated uses two of the three amplifiers contained in the Siliconix L144 micropower triple op amp.

This circuit exhibits a very high reference voltage rejection ratio, as shown by the following pertinent equations. (1)

$$V_{\text{IN}} = V_{\text{REF}} \left(\frac{X}{R + X} \right) \quad (23)$$

$$V_{\text{REF}}' = V_{\text{REF}} \left[1 - \frac{X}{R + X} \right] \frac{R_{14}}{R_{11}} \quad (24)$$



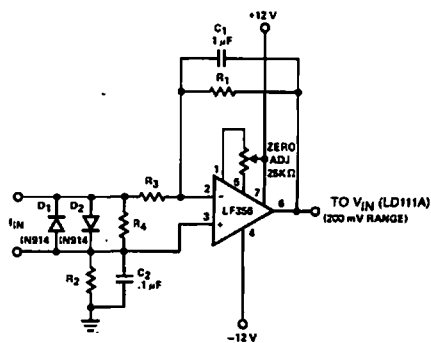
Resistance To Voltage Converter
Figure 8

Substituting into Equation (6) yields

$$\text{Count} = 8192 \cdot \frac{X}{R} \cdot \frac{R_{11}}{R_{14}} \cdot \frac{R_1}{R_2} \quad (25)$$

Current-To-Voltage Converter

A current-to-voltage converter featuring eight decades of current range is shown in Figure 9. The circuit is intended to be used with the 200.0 mV range of the DVM.



CURRENT RANGE	R ₁	R ₂	R ₃	R ₄
200 nA	500 KΩ	500 KΩ	0	∞
2 μA	50 KΩ	50 KΩ	0	∞
20 μA	5 KΩ	5 KΩ	0	∞
200 μA	1 KΩ	0	0	∞
2 mA	50 KΩ	0	5.0 K	10.0 Ω
20 mA	50 KΩ	0	5.0 K	1.0 Ω
200 mA	50 KΩ	0	5.0 K	.1 Ω
2 A	50 KΩ	0	5.0 K	.01 Ω

Current To Voltage Converter
Figure 9

The arrangement actually comprises two different circuits, as examination of the table of resistance values in Figure 9 will show. The more sensitive ranges (up to 200 μ A) use the amplifier in a differential mode to give an output equal to $-2 I_{IN} R_1$. This configuration effectively cancels the contribution of the input bias currents to the output voltage. (Since this error would be insignificant on the 200 μ A range, R_2 is eliminated.)

The less sensitive ranges (2 mA to 2 A) use the amplifier in an inverting configuration to provide an output equal to $-I_{IN} R_4 R_1/R_3$.⁽²⁾ Input protection is provided by diodes D_1 and D_2 .

AC-To-DC Converter

When an AC-to-DC converter is designed using the LD110/LD111A converter set, the input impedance and input bias currents should approximate those of the LD111A input buffer amplifier. This is particularly true if the autoranging circuit of Figure 5 is used so that the same range resistors can be employed for both AC and DC measurements. The AC-to-DC converter shown in Figure 10 fulfills these requirements. The circuit includes a PMOS enhancement-mode

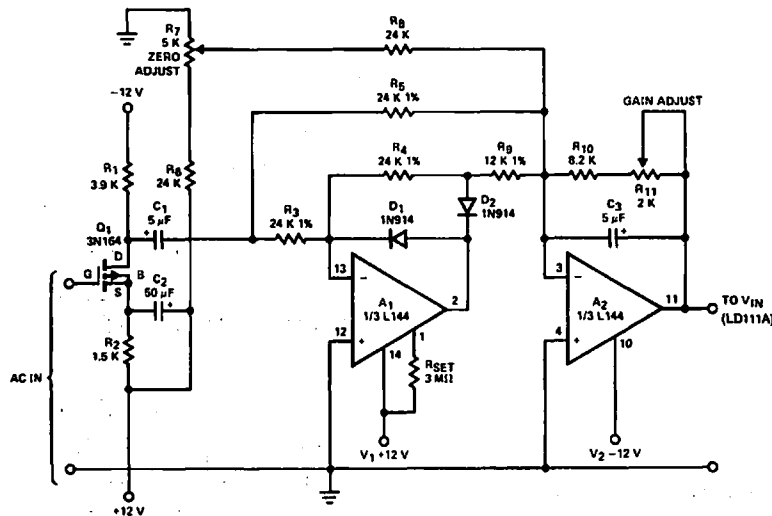
FET input buffer amplifier, coupled to a classical absolute value circuit which essentially eliminates the effect of the forward voltage drop across diodes D_1 and D_2 .

A filter removes the DC component of the rectified AC, which is then scaled to RMS. The output is linear from 40 Hz to 10 kHz or higher.

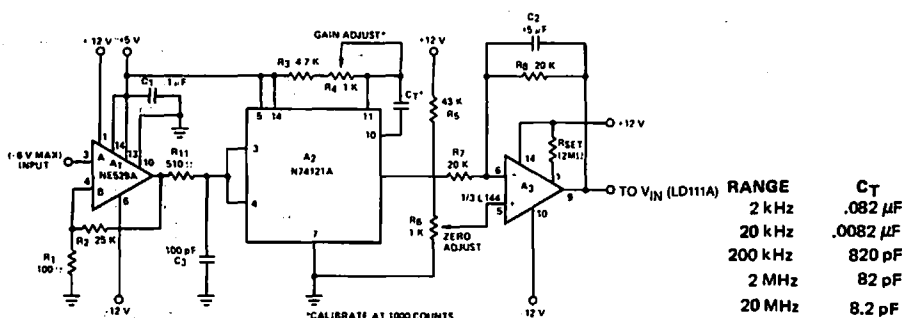
Digital Frequency Meter

A digital frequency meter can be fashioned by using the circuit shown in Figure 11 with the basic 2-volt DVM circuit shown in Figure 4.

The circuit converts frequency to voltage by taking the average DC value of the pulses from the 74121 monostable multivibrator. The one-shot is triggered by the positive-going AC signal at the input of the 529 comparator. The amplifier acts as a DC filter, and also provides zeroing. This circuit will maintain an accuracy of 2% over 5 decades of range. The input signal to the comparator should be greater than 0.1 volt peak-to-peak, and less than 12 volts peak-to-peak for proper operation.



AC to DC Converter
Figure 10

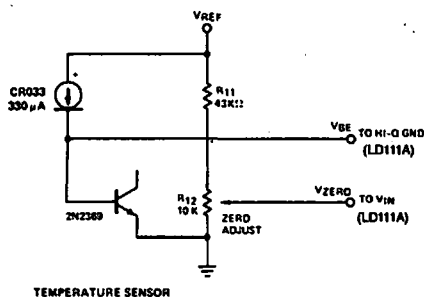


Frequency To Voltage Converter
Figure 11

RANGE	C_T
2 kHz	.082 μ F
20 kHz	.0082 μ F
200 kHz	820 pF
2 MHz	82 pF
20 MHz	8.2 pF

Digital Thermometer

A digital thermometer can be constructed by using the change in forward voltage drop across a PN junction as the temperature-sensitive element in the circuit. This change is typically $-2.3 \text{ mV}/^\circ\text{C}$. The circuit shown in Figure 12 has the base-emitter junction of a bipolar transistor biased with a $470 \mu\text{A}$ current source.



NOTE:
THE DVM SHOWN IN FIGURE 4 MUST BE CHANGED
IN THE FOLLOWING WAYS FOR THIS APPLICATION

1. $R_3 = 51 \text{ K}$;
2. $R_2 = 23 \text{ K}$; (CENTIGRADE SCALE)
(11 R_2 ; (FAHRENHEIT SCALE)
3. HI-QUALITY GND NO LONGER CONNECTED TO
GROUND

Temperature To Voltage Converter
Figure 12

The junction voltage V_{BE} is applied to the input buffer amplifier of the analog processor which functions as a differential amplifier. The buffer resistor R_2 is scaled to give a count proportional to temperature as shown by the following equations:

$$\text{Count} = \frac{R_1}{R_2} \frac{8192}{V_{REF}} [V_{ZERO} - V_{BE}(T)] \quad (26)$$

AND SO:

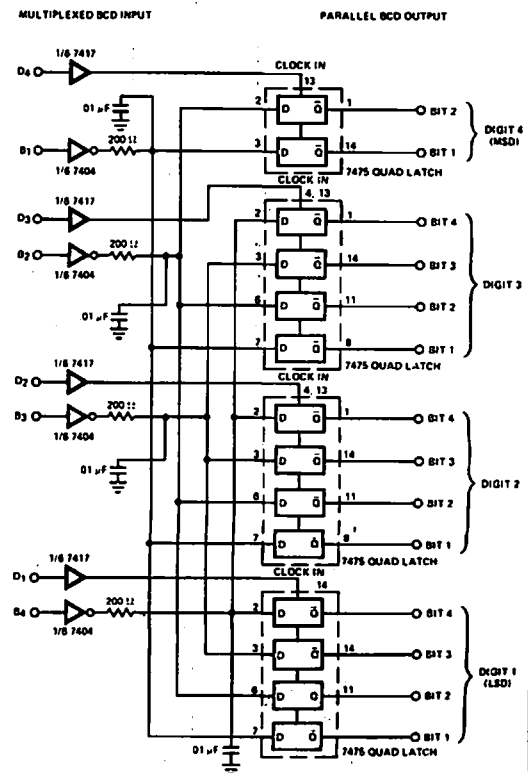
$$\text{Count} = 1000 A [V_{ZERO} - V_{BE}(T)] \quad (27)$$

Gain A must be approximately 5 for the Centigrade scale and 9 for the Fahrenheit scale.

Multiplexed BCD To Parallel BCD Converter

Although the multiplexed BCD output of the LD110/LD111A A/D converter set is useful for digital displays, there are applications (such as printer inputs) in which the BCD data for all four digits should be available in a parallel format. The multiplexed BCD-to-parallel-BCD converter shown in Figure 13 will provide the proper interface for such applications.

The converter consists of 4 quad bistable latches activated in the proper sequence by the digit strobe output of the LD110. The complemented outputs ($\bar{Q}$) of the quad latch set will reflect the state of the bit outputs when the digit strobe goes high, and will maintain this state when the digit strobe goes low. The latches will be updated with the next digit strobe. This parallel BCD output will not then be affected by the blinking-off of the digit strobes when the count exceeds 1999 (overrange), and can be used to drive a non-blinking display up to a full scale of 3000 counts. The parallel BCD output can be put in a "hold" state by lamping all digit strobes to ground to prevent the updating of the latches.



Multiplexed BCD To Parallel BCD Converter
Figure 13

CONCLUSIONS

The LD110/LD111A A/D converter integrated circuit set lends itself to a wide range of applications in which analog information is desired in digital format. High accuracy and long term stability combined with a minimum of external circuitry and calibration requirements make this converter set a superior choice for any application. The circuit examples presented are intended to be of general interest, and do not touch upon the wide variety of more specialized applications.

REFERENCES:

- (1) R. Milner, "Integrate with a DMM?", Electronic Design, October 25, 1973, pp. 93-96.
- (2) M.K. Vander Kooi, "Simple IC Meter Amplifier Circuit Measure 100 Nanoamps Full-Scale", ED/EEE, April 15, 1972, pp. 40-41.
- (3) J. D'Azzo and C. Houpis, Feedback Control System Analysis and Synthesis, McGraw-Hill Co. New York, 1960, pp. 81-83.

APPENDIX A: ERROR ANALYSIS FOR V_{REF}

Equation (6) will be used to derive the count error to be expected for changes in the reference voltage V_{REF} due to temperature changes or load regulation.

$$\text{Count}' = V_{IN} \frac{R_1}{R_2} \frac{8192}{V_{REF}'} \quad (6)$$

WHERE:

$$\text{Count}' = \text{Count (Ideal)} + \Delta \text{Count (Error)} \quad (28)$$

AND

$$V_{REF}' = V_{REF} + \Delta V_{REF} \quad (29)$$

Substituting (28) and (29) into (6) yields

$$\text{Count} + \Delta \text{Count} = V_{IN} \frac{R_1}{R_2} \frac{8192}{(V_{REF} + \Delta V_{REF})} \quad (30)$$

OR:

$$\begin{aligned} \text{Count} \cdot V_{REF} + \text{Count} \cdot \Delta V_{REF} + \Delta \text{Count} \cdot V_{REF} \\ + \Delta \text{Count} \cdot \Delta V_{REF} = V_{IN} \frac{R_1}{R_2} 8192 \end{aligned} \quad (31)$$

The quantity $\Delta \text{Count} \cdot \Delta V_{REF}$ is very small in relation to the other factors and can be eliminated. The product $\text{Count} \cdot V_{REF}$ is equal to $V_{IN} \frac{R_1}{R_2} 8192$ and so these factors can be eliminated from both sides of equation (31) leaving

$$\text{Count} \cdot \Delta V_{REF} + \Delta \text{Count} \cdot V_{REF} = 0 \quad (32)$$

THEREFORE:

$$\Delta \text{Count} = - \text{Count} \frac{\Delta V_{REF}}{V_{REF}} \quad (33)$$

This can be related to V_{IN} by noting that the full-scale count is 2000, thus:

$$\Delta \text{Count} = -2000 \frac{V_{IN}}{V_{IN} (F.S.)} \frac{\Delta V_{REF}}{V_{REF}} \quad (34)$$

The reference supply shown in Figure 4 has a typical temperature coefficient of ± 20 ppm/ $^{\circ}\text{C}$. Therefore the reference voltage would change by 0.1% for an increase in temperature of 50°C (20°C to 70°C). The maximum error will occur when V_{IN} equals the full scale voltage $V_{IN} (F.S.)$ as shown below.

$$\Delta \text{Count} = -2000 \frac{V_{IN} (F.S.)}{V_{IN} (F.S.)} (.001) \quad (35)$$

$$\Delta \text{Count} = -2 \quad (36)$$

If no other effects were present, the DVM in Figure 4 will show a decrease of 2 in the count for a 50°C increase in temperature, if the reference Zener diode has a positive 20 ppm/ $^{\circ}\text{C}$ temperature coefficient.

APPENDIX B: TEMPERATURE EFFECT OF $R_{DS(on)}$ (U/D SWITCH)

The analysis of the readout error caused by a change in the $R_{DS(on)}$ of the U/D switch will proceed along similar logic as that of Appendix A. Again we look at Equation (6).

$$\text{Count}' = V_{IN} \frac{R_1'}{R_2} \frac{8192}{V_{REF}} \quad (6)$$

WHERE

$$\text{Count}' = \text{Count (Ideal)} + \Delta \text{Count (Error)} \quad (28)$$

AND

$$R_1' = R_1 (\text{Ideal}) + \Delta R_1 \quad (37)$$

Substituting (28) and (37) into (6) yields,

$$\text{Count} + \Delta \text{Count} = V_{IN} \frac{R_1}{R_2} \frac{8192}{V_{REF}} + V_{IN} \frac{\Delta R_1}{R_2} \frac{8192}{V_{REF}} \quad (38)$$

Eliminating Equation (6) from (38) gives the change in count (ΔCount).

$$\Delta \text{Count} = V_{IN} \frac{\Delta R_1}{R_2} \frac{8192}{V_{REF}} \quad (39)$$

BUT:

$$V_{REF} = V_{IN} \frac{R_1}{R_2} \frac{8192}{\text{Count}} \quad (40)$$

so that by substituting (40) into (39) yields

$$\Delta \text{Count} = \frac{\Delta R_1}{R_1} \text{Count} \quad (41)$$

or by relating the count to the input voltage V_{IN} we see that:

$$\Delta \text{Count} = 2000 \frac{V_{IN}}{V_{IN}(\text{F.S.})} \frac{\Delta R_1}{R_1} \quad (42)$$

We can now examine how the temperature dependency of $R_{DS(on)}$ (U/D Switch) will affect the accuracy of the DVM application circuit of Figure 4. Using Figure 3, it can be seen that $R_{DS(on)}$ will increase by 100Ω when the ambient temperature changes by about 50°C ($V_{REF} = 6.8$ volts). The maximum error ($V_{IN} = V_{IN}(\text{F.S.})$) will be:

$$\Delta \text{Count} = \frac{100 \Omega}{83 \text{ K}\Omega} 2000 = 2.41 \quad (43)$$

The net count error will then be due to the sum of the error associated with V_{REF} and the error due to the change in $R_{DS(on)}$ which is:

$$\text{Net Count Error} = \Delta \text{Count}(V_{REF}) + \Delta \text{Count}(R_1) \quad (44)$$

$$\text{Net Count Error} = -2 + 2.41 = .41 \text{ counts} \quad (45)$$

If the reference resistor R_1 and the input resistor R_2 have the same temperature coefficients, the temperature effects of these resistors will be balanced out.

APPENDIX C: PROPER SELECTION OF THE INTEGRATOR CAPACITOR C_{INT}

In order to maintain good accuracy, the integrator output V_o should not be allowed to deviate from V_{strg} by more than 0.75 volts. The maximum deviation from V_{strg} will occur when the maximum input current $\frac{V_{IN}(\text{F.S.})}{R_2}$ is of

the same sense as the reference current. These considerations are shown in the following mathematical expressions:

$$|\Delta V_o| = \frac{1}{C_{INT}} \int_0^{7/f_{IN}} \left(\frac{V_{IN}(\text{F.S.})}{R_2} + \frac{V_{REF}}{2R_1} \right) dt \quad (46)$$

SO

$$|\Delta V_o| = \frac{7}{C_{INT} f_{IN}} \left[\frac{V_{REF}}{2R_1} + \frac{V_{IN}(\text{F.S.})}{R_2} \right] \quad (47)$$

BUT:

$$R_1 = \frac{2000 V_{REF} R_2}{8192 V_{IN}(\text{F.S.})} \quad \text{See Eq. (6)} \quad (48)$$

Substituting (48) into (47) yields

$$|\Delta V_o| = \frac{7}{C_{INT} f_{IN}} \left[\frac{2.048 V_{IN}(\text{F.S.})}{R_2} + \frac{V_{IN}(\text{F.S.})}{R_2} \right] \quad (49)$$

AND

$$|\Delta V_o| = \frac{21.336 V_{IN}(\text{F.S.})}{R_2 C_{INT} f_{IN}} \quad (50)$$

Setting this absolute deviation equal to 0.75 volts gives

$$C_{INT} = \frac{28.45 V_{IN}(\text{F.S.})}{R_2 f_{IN}} \quad (51)$$

For the application circuit of Figure 4:

$$R_2 = 100 \text{ K}\Omega$$

$$f_{IN} = 24.5 \text{ kHz}$$

$$V_{IN}(\text{F.S.}) = 2.000 \text{ volts}$$

From equation (51) then:

$$C_{INT} = 0.0232 \mu\text{F} \quad (52)$$

and we choose the closest standard value which is $0.022 \mu\text{F}$.

APPENDIX D: ERROR DUE TO C_{INT} LEAKAGE

In order to determine how much leakage from integrator capacitor C_{INT} is tolerable we must first find the relationship between read-out error and leakage current I_L . From Equation (1) it can be seen that the charge Q proportional to 1 count is:

$$Q \text{ per count} = \frac{-V_{REF}}{2 R_1 f_{IN}} \quad (53)$$

Therefore, to maintain an error of less than 1 count, the net charge leaked from C_{INT} during the measure interval must be less than the charge associated with 1 count.

$$I_L \Delta t_{\text{measure}} < \frac{V_{REF}}{2 R_1 f_{IN}} \quad (54)$$

OR

$$\frac{4096 I_L}{f_{IN}} < \frac{V_{REF}}{2 R_1 f_{IN}} \quad (55)$$

THUS

$$I_L < \frac{V_{REF}}{8192 R_1} \quad (56)$$

Given the values for the application circuit of Figure 4,

$$R_1 = 83 \text{ K (after trimming)}$$

$$V_{REF} = 6.8 \text{ volts}$$

THEN:

$$I_L < 10 \text{ nA to have less than 1 count error}$$

APPENDIX E: RC TIME CONSTANTS FOR AZ FILTER

The component values for the RC time constants of the AZ Filter (R_4 , R_5 and C_{strg}) are derived from a consideration of the following transfer functions:

1. The low pass filter composed of R_4 , R_5 , C_{strg} and the AZ amplifier has a transfer function $G_1(S)$

$$G_1(S) = \frac{V_{AZ}}{V_o} = \frac{R_5}{R_4 + R_5} \frac{S + 1/R_5 C_{strg}}{S + 1/C_{strg} (R_4 + R_5)} \quad (57)$$

which is of the form

$$G_1(S) = \alpha \frac{S + 2\pi f_2}{S + 2\pi f_1} \quad (58)$$

where α is the high frequency gain of this filter and f_1 and f_2 are the pole and zero frequencies respectively.

2. The closed-loop system composed of the integrator and AZ amplifier has the transfer function $G_2(S)$ shown below:

$$G_2(S) = \frac{V_o}{V_{IN}} = \frac{S C_{STRG} (R_4 + R_5) + 1}{S^2 R_3 C_{INT} C_{strg} (R_4 + R_5) + S (R_3 C_{INT} + R_5 C_{strg}) + 1} \quad (59)$$

which is of the form

$$G_2(S) = \frac{S T_1 + 1}{\frac{1}{\omega_n^2} S^2 + \frac{2\zeta}{\omega_n} S + 1} \quad (60)$$

SO THAT

$$\omega_n^2 = \frac{1}{R_3 C_{INT} C_{strg} (R_4 + R_5)} \quad (61)$$

AND

$$4\zeta^2 = \frac{R_5^2 C_{strg}^2}{R_3 C_{INT} (R_4 + R_5)} + \frac{2R_5}{R_4 + R_5} + \frac{R_3 C_{INT}}{C_{strg} (R_4 + R_5)} \quad (62)$$

where ω_n is 2π times the natural frequency and ζ is the system damping factor.

With these equations, R_4 and R_5 can be determined. C_{INT} should already be chosen (see Appendix C) and C_{strg} can be somewhat arbitrarily chosen (.1 μF is a good choice to keep R_4 and R_5 at useful resistance values). The following procedure evolved from a desire to decrease the high frequency gain α of the low pass filter while maintaining a well damped Auto-Zero system. The procedure is as follows:

- a) From Equations (57) and (58) it can be found that:

$$f_1 = \frac{1}{2\pi C_{strg} (R_4 + R_5)} \quad (63)$$

The total resistance ($R_4 + R_5$) can be solved for by setting f_1 equal to 2 times the sampling rate.

- b) Since the sum $R_4 + R_5$ is known, R_5 can be found by setting the damping factor equal to 0.4 and solving for R_5 using Equation (62).

- c) R_4 can then be found now that R_5 is known.

These AZ filter component values will be valid if:³

$$\frac{2048}{f_{IN}} \zeta \omega_n \geq 5 \quad (64)$$

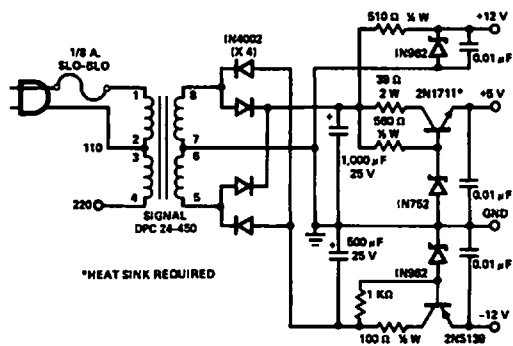
This assures that V_{strg} settles properly during the auto-zero period. If the values determined for R_4 and R_5 do not meet this criteria, a higher value of damping factor should be chosen and the determination of R_5 , as delineated in step b, should be repeated.

DESIGN AID OF THE LD110/LD111A 3½ DIGIT DVM DEMONSTRATOR BOARD

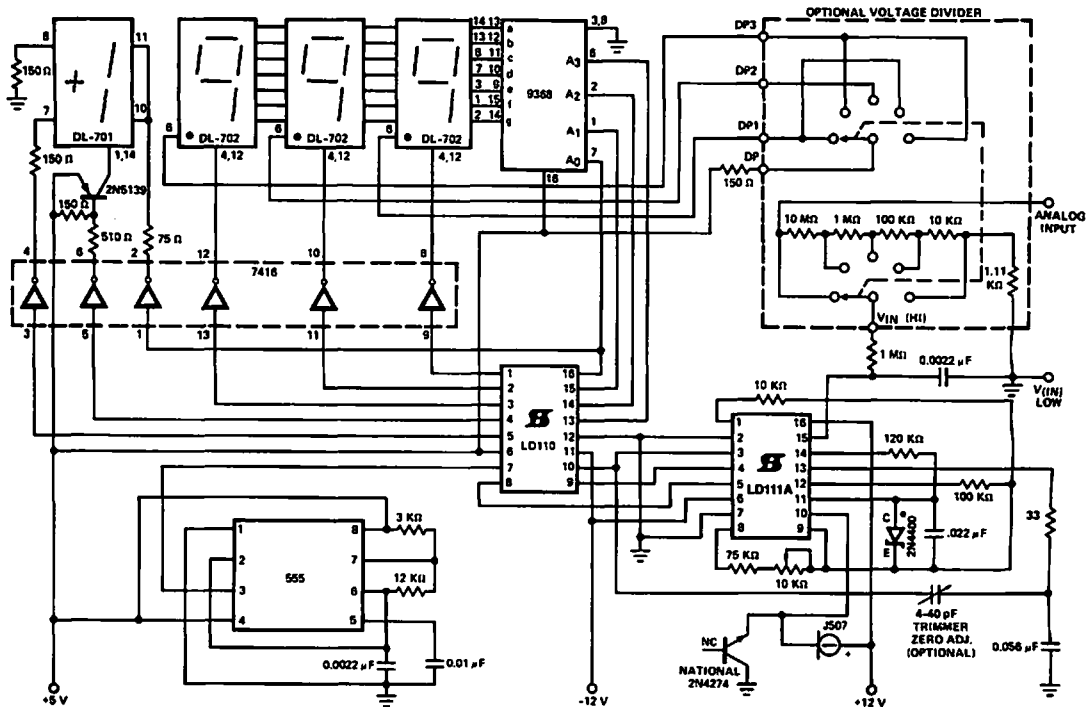
INTRODUCTION

The schematics, parts-list and art-work for a DVM demonstrator board are presented on the following pages. Inexpensive reflective-bar LEDs are used in the basic DVM circuit which features 100 μV resolution and an accuracy of $\pm 0.05\%$ of reading ± 1 count. A five range voltage divider shown on the schematic can further extend the usefulness of this instrument. An optional power supply circuit is incorporated into the P.C. board to give line operation if desired.

The metal pattern diagram and component placement diagram are both to 1:1 scale. The component placement art is intended to be silk-screened on the top side of the board to provide easy component installation. It can, however, be used simply as a loading diagram.



OPTIONAL POWER SUPPLY

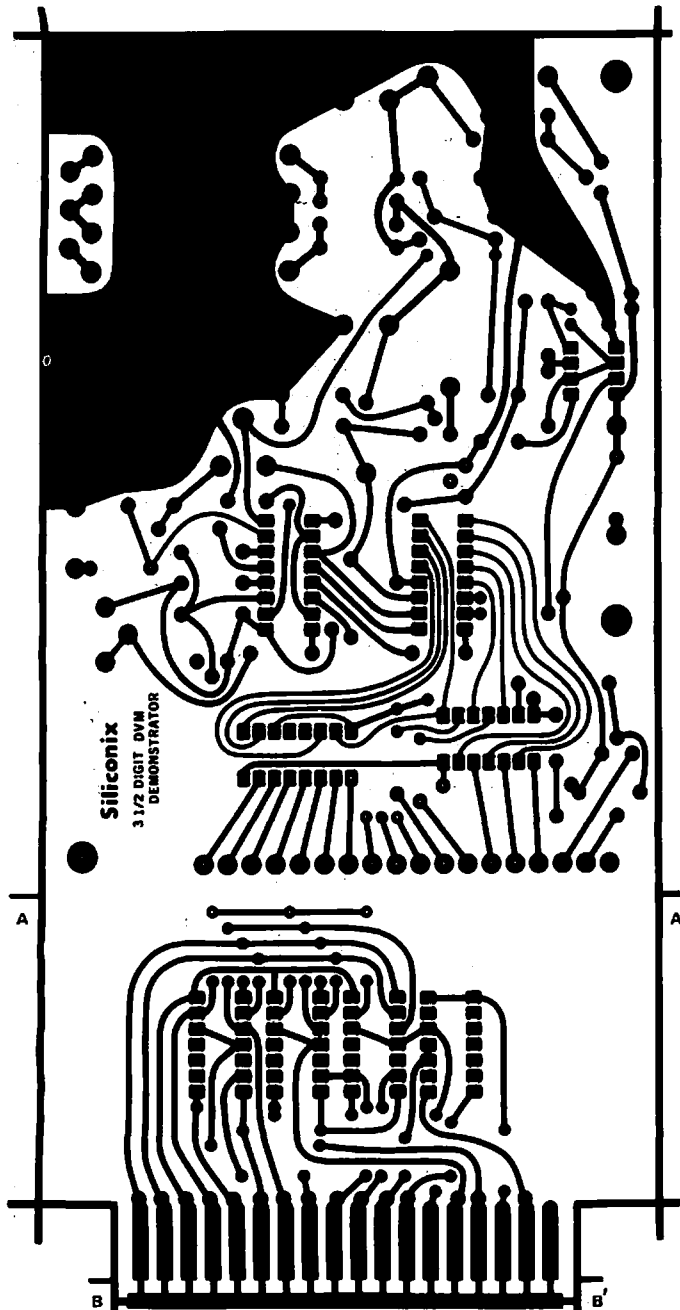


SILICONIX DVM DEMONSTRATOR

*2N4400 not required when using LD111A.

METAL PATTERN FOR DVM BOARD

(refer to last page of design aid for 1:1 P.C. pattern)



FABRICATION HINTS

1. All holes require a #60 drill except for the following holes which require a #54 drill.
 - a) Transformer
 - b) AC input
 - c) Power Supply filter capacitors
 - d) $39\ \Omega$ Resistor in Power Supply
 - e) Trimmer Resistor (10K)
 - f) Trimmer Capacitor
 - g) Edge Connector (labeled A thru Q)
 - h) V_{IN} (Hi and Lo)

The location of these holes may be determined from the component placement diagram and the adjacent metal pattern.

2. Shear board along lines A-A' and B-B'.

CIRCUIT BOARD
(Bottom View)SHEAR
HERELED DISPLAY BOARD
(Back View)

1. A solid line between two holes requires a jumper wire.
2. The dotted area denotes the optional power supply. If bench power is to be used, it can be attached to the pads marked +12 V, -12 V and +5 V.
3. AC line input to "COM" and "110" for 110 VAC 50-60 Hz and to "COM" and "220" for 220 VAC 50-60 Hz.
4. Pin 1 of the transformer should be aligned with hole marked "1".
5. Filter Caps, whether axial or radial lead type should be upright.
6. Anode of E507 denoted by flat spot.
7. 2N1711 requires a heat sink.
8. Display board can be directly wired to main board if desired — thus eliminating connector.
9. Use Molex strip sockets for LD110/LD111A
10. If the readout has a slight negative offset with a grounded input, an optional trim capacitor can be added to the board (where TRIM is marked). This can be a 4-40 pF trimmer or a fixed capacitor as needed to zero the reading.

[illegible]

Siliconix

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DL-701 DL-702 DL-702 DL-702

A
B
C
D
E
F
G
H
I
J
K
L
M
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P
Q

The AC line voltages associated with the board can be fatal to human life. Proper precautions for operating this instrument must be observed by the user. Silicon assumes no liability for unsafe operation.

BASIC DVM Electrical Parts List

Quantity Required	Description	Recommended Manufacturer And Part Number
1	Analog IC	Siliconix LD111A
1	Digital IC	Siliconix LD110
1	BCD to 7 Segment Decoder/Driver	Fairchild 9368DC
1	Timer IC	Signetics NE555V
1	Hex Buffer/Inverter	National DM7416N
1	±1 Overflow LED Display	Litronix DL-701
3	7 Segment LED Display	Litronix DL-702
1	NPN Transistor	Motorola 2N4400
1	NPN Transistor	National 2N4274
1	PNP Transistor	Fairchild 2N5139
1	Current Limiting Diode	Siliconix J507
1	0.022 μ F 80 Volt Mylar Cap.	Sprague 192P2239RB
1	0.056 μ F 80 Volt Mylar Cap.	Sprague 192P5639RB
1	0.0022 Ceramic Cap.	
1	4-40 pF Trimmer Cap. (Optional)	Johanson 9304
1	0.01 μ F Ceramic Cap.	
1	10K Potentiometer	CTS X201R103B
1	75 Ω 1/2 watt 5% Resistor	Allen-Bradley
4	150 Ω 1/2 watt 5% Resistor	Allen-Bradley
1	510 Ω 1/2 watt 5% Resistor	Allen-Bradley
1	3 K Ω 1/2 watt 5% Resistor	Allen-Bradley
1	10 K Ω 1/2 watt 5% Resistor	Allen-Bradley
1	12 K Ω 1/2 watt 5% Resistor	Allen-Bradley
1	33 K Ω 1/2 watt 5% Resistor	Allen-Bradley
1	75 K Ω 1/2 watt 5% Resistor	Allen-Bradley
1	100 K Ω 1/2 watt 5% Resistor	Allen-Bradley
1	120 K Ω 1/2 watt 5% Resistor	Allen-Bradley
1	1 M Ω 1/2 watt 5% Resistor	Allen-Bradley
32	Socket Pins (use for LD110 and LD111)	Molex
1	18 pin Edge Connector	Amphenol 143-018-03

OPTIONAL POWER SUPPLY Electrical Parts List

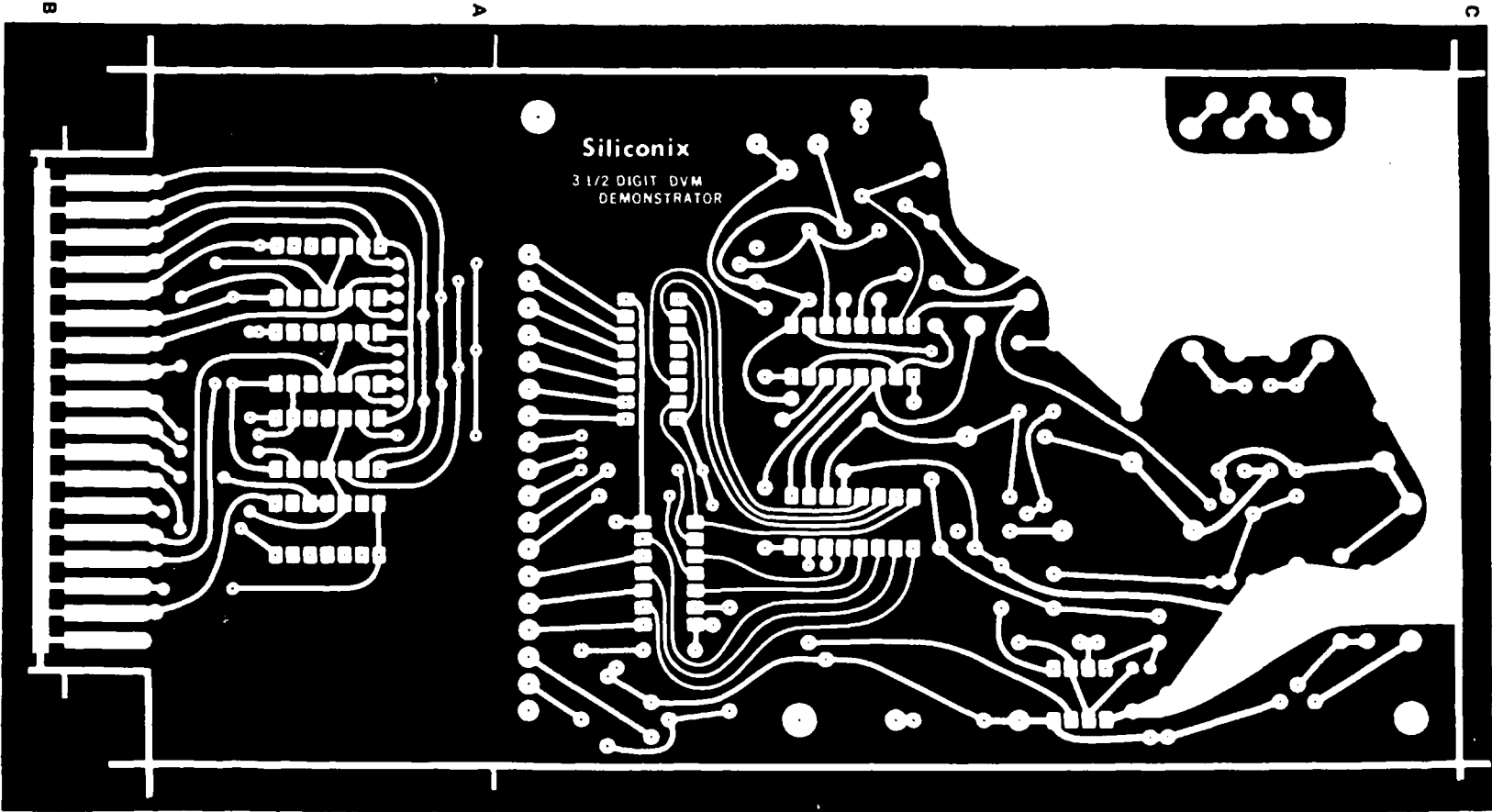
Quantity Required	Description	Recommended Manufacturer And Part Number
1	Supply Transformer	*Signal or EWC DPC24-450
1	PNP Transistor	Fairchild 2N5139
1	NPN Transistor	Motorola 2N1711
1	5.6 Volt Zener Diode	Motorola IN752
2	11 Volt Zener Diode	Motorola IN962
4	100 Volt Rectifier Diode	Motorola IN4002
1	1,000 μ F 25 Volt Electrolytic	Sprague 503D108G025EU
1	500 μ F 25 Volt Electrolytic	Sprague 503D477G025EK
3	0.01 μ F Ceramic Cap.	
1	100 Ω 1/2 watt 10% Resistor	Allen-Bradley
1	39 Ω 2 watt 10% Resistor	Allen-Bradley
1	510 Ω 1/2 watt 5% Resistor	Allen-Bradley
1	560 Ω 1/2 watt 10% Resistor	Allen-Bradley
1	1 K Ω 1/2 watt 5% Resistor	Allen-Bradley
1	Power Cord, 2 Wire	
1	Fuse Holder	Little-fuse 357-001
1	1/8 Amp Slo-Blo Fuse	
1	Heat Sink (for 2N1711 transistor)	Wakefield 205-CB

OPTIONAL 5 RANGE VOLTAGE DIVIDER

1	10 M Ω	0.1%	1/2 watt Resistor	The divider resistors should be mounted on the rotary range switch.
1	1 M Ω	0.1%	1/2 watt Resistor	
1	100 K Ω	0.1%	1/2 watt Resistor	
1	100 K Ω	0.1%	1/2 watt Resistor	
1	1.11 K Ω	0.1%	1/2 watt Resistor	
1	2 Pole 5 Position Rotary Switch		Centralab PA-3 and 30° Index	
2	Banana Jacks			

*This transformer may be ordered from:
Signal Transformer Co.
1 Julius Street
Brooklyn, NY 11212
(only direct from factory)

EWC, inc (#DPC-24-450B19)
725 Federal Avenue
Kenilworth, NJ 07033
(available through factory or
West coast distributors)



Circuit Board
(Bottom View)

LED Display Board
(Bottom View)

LD110/111A 3 1/2 Digit DVM Demonstrator

PC Board Art

Component
Placement
Diagram

Scale 1:1

Circuit Board
(Top View)

LD110/LD111A 3½ Digit DVM Demonstrator

Siliconix

Siliconix

LED Display Board
(Top View)

Siliconix

FUNCTION /APPLICATION OF THE LD120 /LD121A 4½ DIGIT A/D CONVERTER SET IN MEASUREMENT SYSTEMS

INTRODUCTION

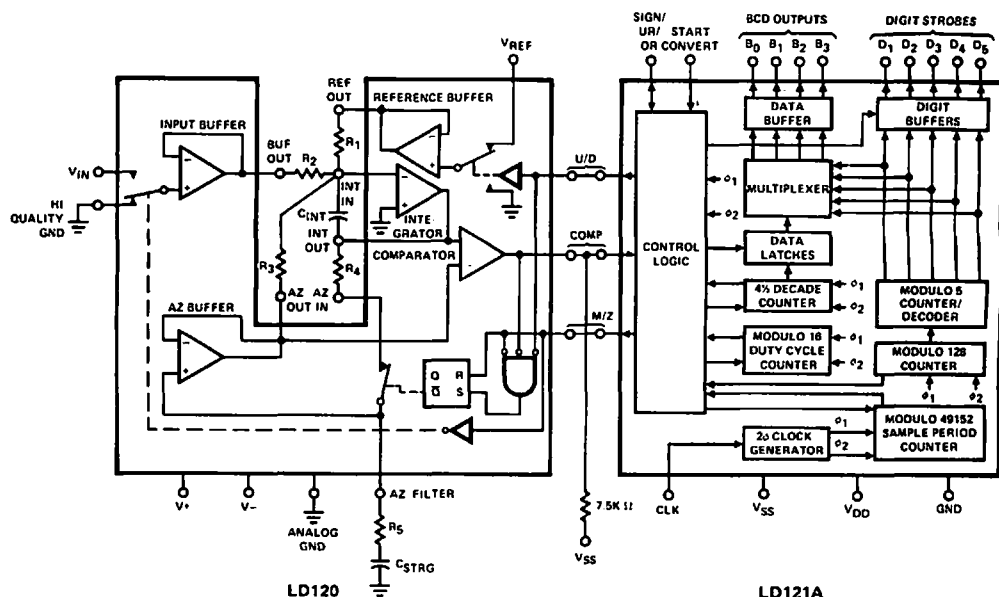
The Siliconix LD120 and LD121A Integrated Circuits permit the building of low cost and physically small 4-1/2 digit panel meters, voltmeters, and other A/D conversion systems where resolution and accuracy are of prime importance. The set can provide basic ranges of ± 2 V and ± 200 mV full-scale and, with an external amplifier and analog switch, can read ± 20 mV full-scale. The quantized feedback algorithm of A/D conversion provides inherent auto-polarity and auto-zero operation, and the PMOS/Bipolar technology of the LD120 analog chip provides $>10^9 \Omega$ input impedance and buffered reference input. The set is flex-

ible with regard to analog signal range, external voltage reference level, and output display format.

This application note will describe the basic operation and circuit constants, and will develop some typical applications circuits.

Description of Operation

There are two main periods in a sample of analog data, the auto zero period and the measure period. Descriptions of these periods will be referred to Figure 1.



Connection Diagram
Figure 1

Auto-Zero Interval

In the auto-zero period, the input buffer is connected to high-quality ground and the auto-zero buffer is connected to the integrator output. Ignoring up/down and transient waveforms for the moment, the DC currents presented to the integrator are:

$$I_{INT} = I_{BIAS} \cdot INT \equiv \frac{V_{OFFSET, INPUT BUFFER}}{R_2} + \frac{V_{OFFSET, AZ BUFFER}}{R_3} + \frac{V_{OFFSET, REFERENCE BUFFER}}{R_1} + \frac{V_{AZ, OFFSET}}{R_3} + \frac{V_{HI-Q}}{R_2}$$

$V_{AZ, OFFSET}$ is the fraction of the auto-zero voltage across C_{AZ} which will null all the other quantities mentioned above. Also being injected into the integrator input is $V_{REF}/2R_1$ since the up/down line is being toggled at 50% duty cycle by the LD121A. When the dynamics of the system settle out toward the end of the zero period, C_{AZ} will have the voltage

$$V_{AZ} = V_{AZ, OFFSET} - \frac{R_3}{2R_1} V_{REF}$$

$-V_{REF} R_3/2R_1$ provides a reference quantity of exactly negative one-half the integrator input current injected by the reference current through R_1 .

The auto-zero period is 16,384 clock times long.

Measure Interval

During the measure interval, the input buffer is connected to V_{IN} and the auto-zero capacitor is disconnected from the integrator output. The quantity $V_{AZ, OFFSET}$ remains on C_{AZ} , and analog offsets are nulled out. Due to the quantity $-V_{REF} R_3/2R_1$ being held on C_{AZ} , an effective $V_{REF}/2$ or $-V_{REF}/2$ is applied through R_1 when U/D is 0 and 1, respectively.

Referring to Figure 2, the U/D waveforms are of 2 kinds: 1 clock time up and 15 down; and 15 clock times up and 1 down. The LD121A logic generates these waveforms in response to the LD120 comparator output. The system attempts to return the integrator output to V_{AZ} regardless of the input. Since the integrator sees both input and reference currents simultaneously, its output does not vary far from V_{AZ} .

The BCD counter counts up once per clock time when U/D=1 and down once per clock time when U/D=0, causing the displayed count to be proportional to the amount of $V_{REF}/2R_1$ that was required to null V_{IN}/R_2 during the

measure interval. The charge balancing in the measure interval calculates so:

$$Q = \frac{V_{IN} - V_{HI-Q}}{R_2} \Delta t \equiv \text{Count} \frac{1}{f_{OSC}} \frac{V_{REF}}{2R_1}$$

where $\Delta t = 32,768/f_{OSC}$ and is the measure period.

Rearranging,

$$\text{Count} = \frac{V_{IN} - V_{HI-Q}}{V_{REF}} \frac{R_1}{R_2} \cdot 65,536.$$

The measure interval cannot resolve single counts; it can only resolve multiples of 14 counts. Immediately after the measure and into the auto-zero period is the override period. The input buffer is reconnected to V_{HI-Q} and the C_{AZ} switch is left open. The LD121A sends the integrator positive with respect to V_{AZ} (see Figure 3), then returns it to V_{AZ} potential, stopping when the LD120 comparator changes states, keeping track of the count in single clock times. The override period can exist a maximum of 56 clock times into the zero period, assuming a non-overload V_{IN} .

Since only 14 of the 16 counts in the U/D waveform produce net counts, there are $\pm 28,672$ counts maximum out of the 32,768 clock times available.

Component Selection

R_1 and R_2 : The nominal currents into the integrator are 20 μA full-scale through R_2 and 80 μA through R_1 . These values are chosen for minimum system noise consistent with maximum amplifier linearities. Then

$$R_2 = \frac{V_{IN} (F.S.)}{20 \mu A}, \quad R_1 = \frac{V_{REF}}{80 \mu A}$$

V_{REF} should be in the range of 2 V to 8 V, for reasons of system gain stability and noise characteristics. Some trimming of either R_2 or R_1 is required for exact full-scale reading.

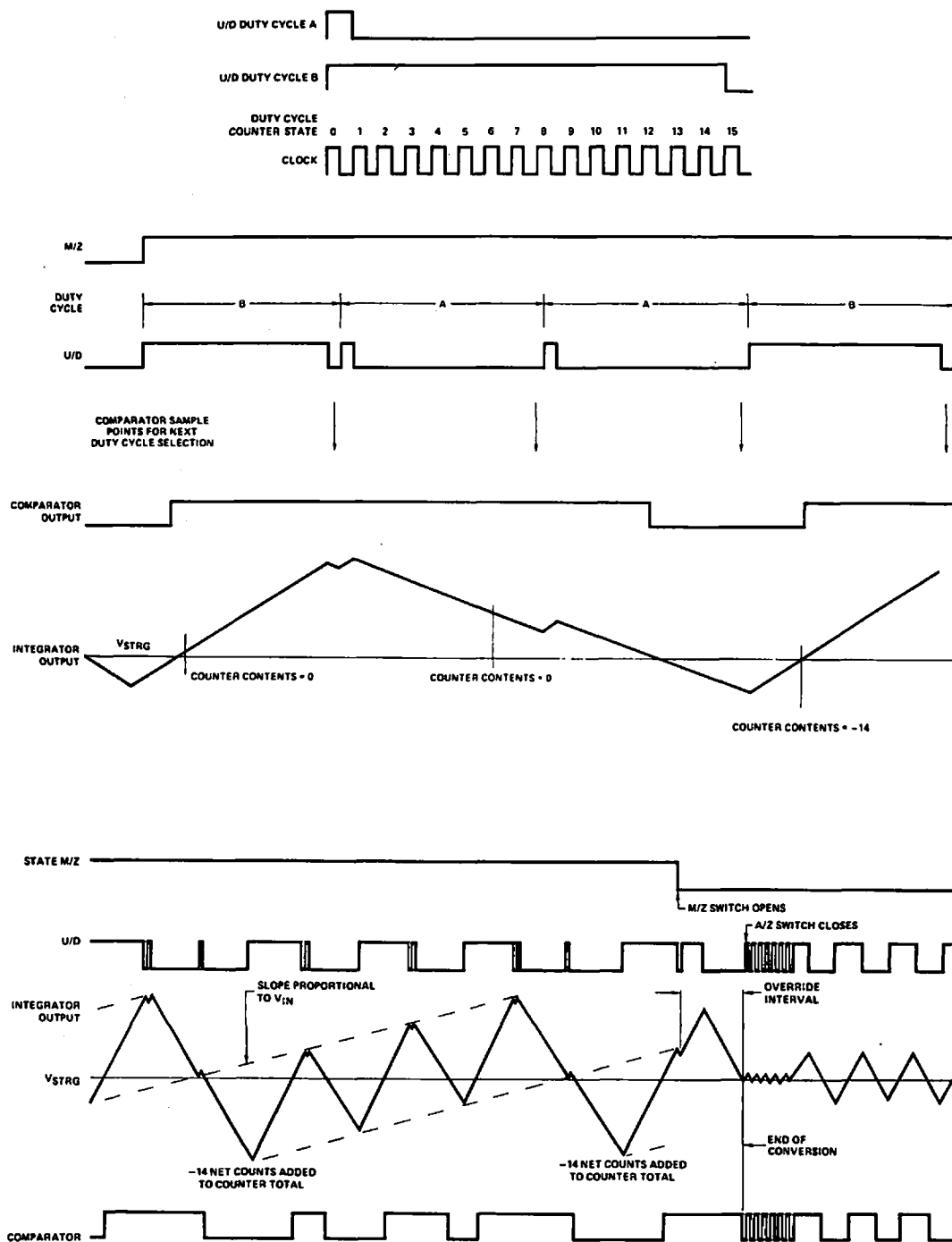
R_2 is determined by the equation previously given

$$R_2 = 65,536 R_1 \left[\frac{V_{IN} (\text{FULL-SCALE}) - V_{HI-Q}}{V_{REF} \text{ Count} (\text{FULL-SCALE})} \right]$$

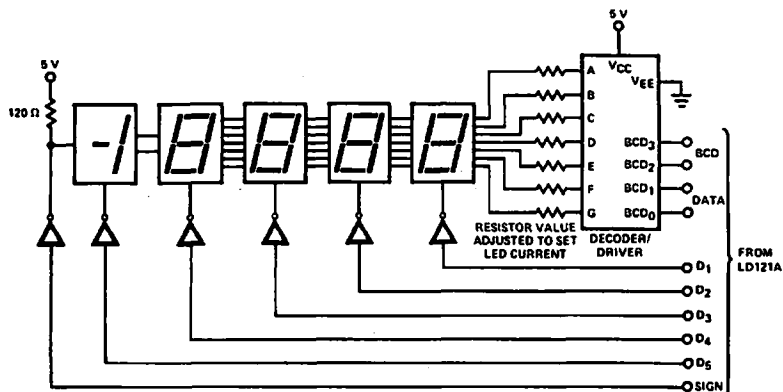
The oscillator frequency is determined from $f_{OSC} = 49,152 \times \text{Sample Rate}$.

Values of R_3 and C_{INT} are derived from the consideration that the integrator output should be at least 3 V from either supply rail. The negative rail is the one of interest, since V_{AZ} is negative. A starting point is to set the integrator AC swing at about 6 V p-p. Then

$$C_{INT} \equiv \frac{V_{REF}}{R_1} \cdot \frac{1}{6 V} \cdot \frac{30}{f_{OSC}}$$



Up/Down and Integrator Waveforms
Figure 2



APPROPRIATE INVERTERS: MC75452 (MOTOROLA)
DS8892 (NATIONAL)
DS8893 (NATIONAL)
*9907 (FAIRCHILD)
ANY NPN DARLINGTON TRANSISTOR

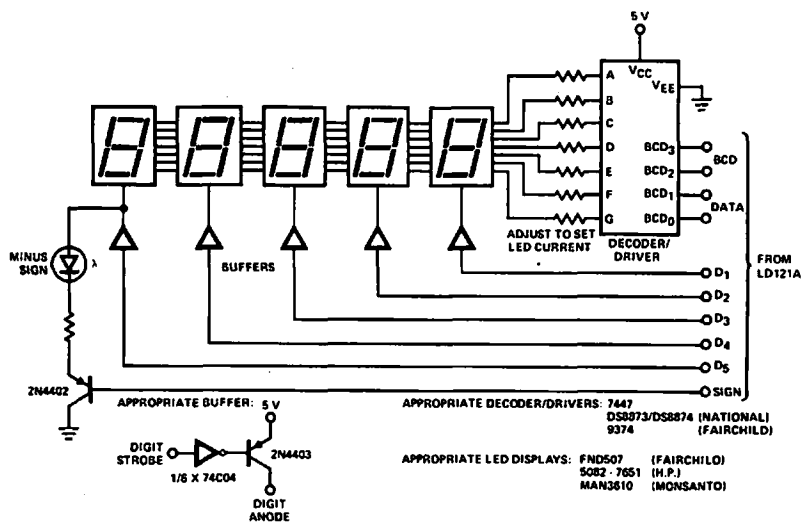
APPROPRIATE DECODER/DRIVERS: DS8857
74C48

APPROPRIATE DISPLAYS:

7 SEGMENT		
FND70	FND71	(FAIRCHILD)
5082 - 7653	5082 - 7656	(H.P.)
MAN3840	MAN3840	(MONSANTO)

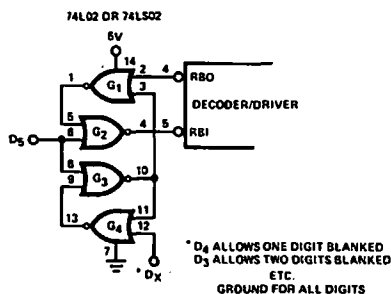
Common Cathode LED Display ($\pm 19,999$ Counts max. with Blinking)

Figure 4



Common Anode LED Display ($\pm 28,672$ Counts max. without Blinking)

Figure 5a



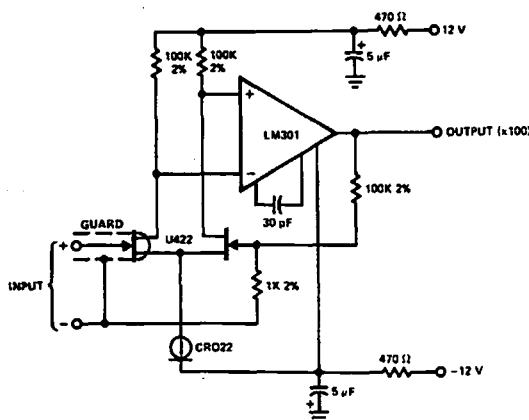
Leading Zero Blanking

Figure 5b

Figure 7 shows the arrangement for a 20 mV full-scale front end. If an extremely low source impedance were used, such as thermocouple, then an amplifier such as the LM201A could be used for A₁. For higher impedances, lower bias currents are required until at about 1K Ω or above, a JFET amplifier will be required. Note that MOS input op-amps are not quiet enough.

A feature of the quantized-feedback conversion is the ability to use external preamplifiers within the auto-zero loop. This allows a preamp that is quiet but has poor DC



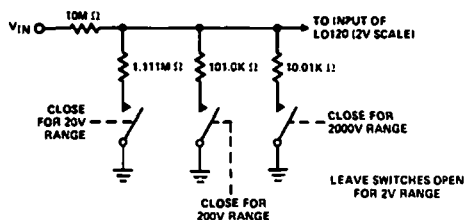


Ultra-Low-Leakage Preamp
Figure 8

Even the BI-FET op-amps are only good for a 20K Ω input resistance up to 75°C. The circuit of Figure 8 has an input leakage of only 2 pA typical at 75°C and would be usable with 1M Ω input resistance. Although not covered here, there are ways to reduce leakage effects over temperature by a factor approaching 10.

Auto-Ranging Voltmeter

The usual auto-ranging voltmeter simply has an input attenuator whose division ratio is controlled by analog switches:



The problem with this approach is that only 10 pA of total leakage at the divider node causes 1 count of offset on the 2 V range. 10 pA is not easily met over temperature.

The circuit of Figure 9 is another approach to the problem. The input signal is fed through a $10\text{M}\ \Omega$ input resistor to the summing junction of an inverting-gain op-amp whose gain is controlled in 2 ranges. The output of the op-amp is fed through 2 R_2 resistor paths to the integrator input of the LD120; the input buffer amplifier and switch of the LD120 are not used. Here is a table of the resistance paths used in each scale excluding the trimmers:

Range	Op-Amp Feedback	R_2 to integrator
2 V	3.9M Ω	390K Ω 43K Ω
20 V	3.9M Ω	390K Ω
200 V	3.9M Ω 39K Ω	390K Ω 43K Ω
2000 V	3.9M Ω 39K Ω	390K Ω

The U426 JFET monolithic pair has extremely low leakage and is used as the input measure/zero switch. During the zero period Q₁ is on and Q₂ is off so that the op-amp sees $10\text{M}\Omega + \text{RDS FET } 1$ to ground as an input. During the measure interval, Q₁ is OFF and Q₂ is ON so that the op-amp sees $10\text{M}\Omega + \text{RDS FET } 2$ in series with the input voltage. Since the input (and feedback) resistances are identical in measure and in zero the auto-zero voltage of the LD120 suppresses input offsets over temperature.

Digital control of the range switches is accomplished by decoding the LD121A overrange and underrange outputs and driving a 2-bit counter with the resulting "count up" and "reset downward" signals.

Although not tried here, a 200 mV range seems possible, but does require 5 scale ranges.

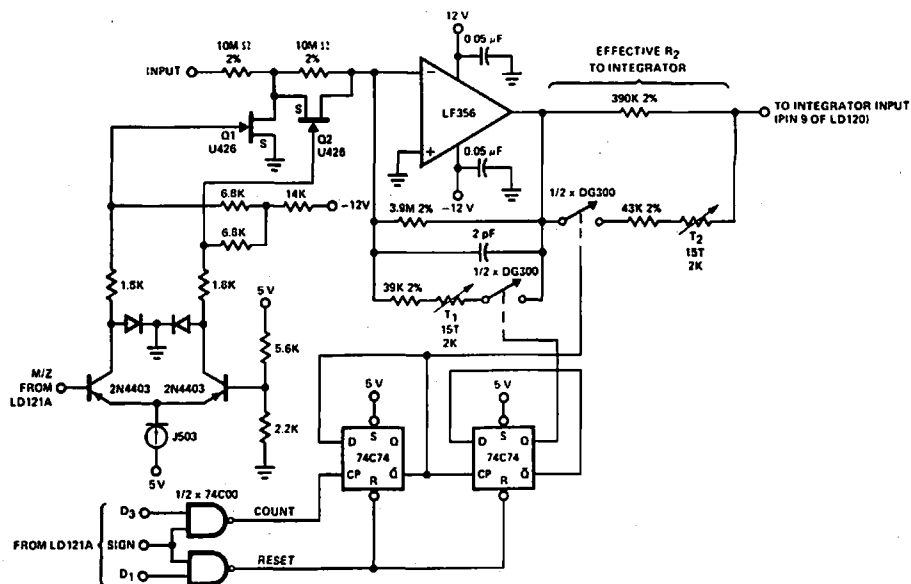
Calibration is done in this order:

- (1) Offset zero is set with input shorted.
- (2) The LD120 scale factor is adjusted with the auto ranger in the 20 V range.
- (3) Trimmer 2 is adjusted for scale factor in the 2 V range.
- (4) Trimmer 1 is adjusted on the 200 V range.

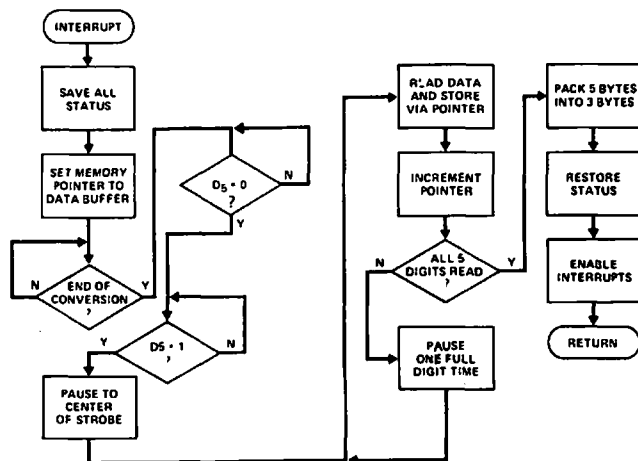
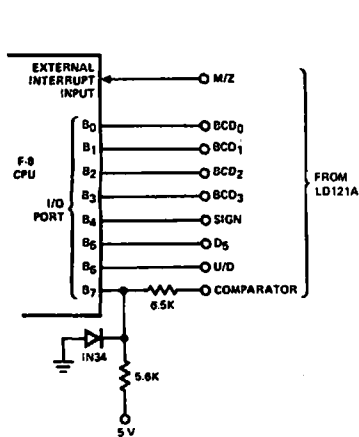
Microprocessor Interface

This circuit is used with the F8 series microprocessor, but the general approach taken is applicable to many processors.

Figure 10 shows the port wiring and flowchart. The falling edge of the M/Z line is used to request an interrupt from the processor, whereupon the I/O program waits for a decoded end of conversion. This end of conversion signal occurs when $U/D = 0$, $M/Z = 0$, and $comp. = 0$. The program then waits for D_5 to occur to synchronize subsequent data pickup. A delay causes the actual BCD data to be read in the middle of the strobe, and all subsequent strobes are sampled in the middle of their intervals. After 5 strobes have been read in, the data is packed and left in a location of memory.



Auto-Ranging Amplifier: 2–2000 V Ranges
Figure 9



F-8/LD121A Interface
Figure 10

APPENDIX A: ERROR TERMS

Zero Drift – The main source of zero drift is leakage from the input and auto zero buffers. Figure 11 shows typical input and auto zero leakages over temperature. The error component due to I_{IN} is simply

$$\Delta V_{IN} = \Delta I_{IN} \cdot R_{SOURCE}$$

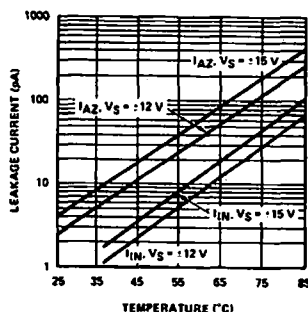
For a $1M\ \Omega$ input resistance, and $\Delta I_{IN} = 30\text{ pA}$ at 75°C , $\Delta V_{IN} = 30\ \mu\text{V}$, corresponding to a 0.3 bit offset at 2 V full-scale, and 3 count offset at 200 mV full-scale. This offset can be reduced by reducing R_{SOURCE} or by inserting a compensating R_{SOURCE} between V_{HI-Q} and ground.

The drift due to I_{AZ} is independent of scale factor, and is caused by the voltage on C_{AZ} drifting during the measure interval. The magnitude of drift will be

$$\Delta V_{AZ} = \frac{I_{AZ} \cdot T_{MEASURE}}{C_{AZ}} = \frac{I_{AZ} \cdot 32,768}{C_{AZ} \cdot f_{OSC}}$$

This will cause an effective input current to the integrator of $\Delta V_{AZ}/2R_3$, the factor two resulting from the fact that the ramp of auto-zero drift is averaged by the algorithm. This input current due to drift is analogous to an input signal of $\Delta V_{AZ} R_2/2R_3$, so the count drift is

$$\Delta \text{Count} = \frac{\Delta I_{AZ}}{C_{AZ} f_{OSC} V_{REF}} \cdot \frac{R_1}{2R_3} \cdot 2.15 \times 10^9$$



Typical Leakage Over Temperature
Figure 11

So given $\Delta I_{AZ} = 100\text{ pA}$ when up at 70°C , $R_1 = 60K = R_3$, $C_{AZ} = 0.1\ \mu\text{F}$, $f_{OSC} = 150\text{KHz}$, and $V_{REF} = 6.2\text{ V}$, $\Delta \text{Count} = 1.16$ due to ΔI_{AZ} only.

The drift caused by thermocouple junctions on the LD120 is much less than that caused by leakages.

Gain Drift – Full-scale gain drift is caused mainly by changes in V_{REF} . One count in 20,000 stability per degree C is 50 ppm/ $^\circ\text{C}$, so the zener reference should have at least 10 ppm/ $^\circ\text{C}$ stability and the system burned-in to reduce long term drift.

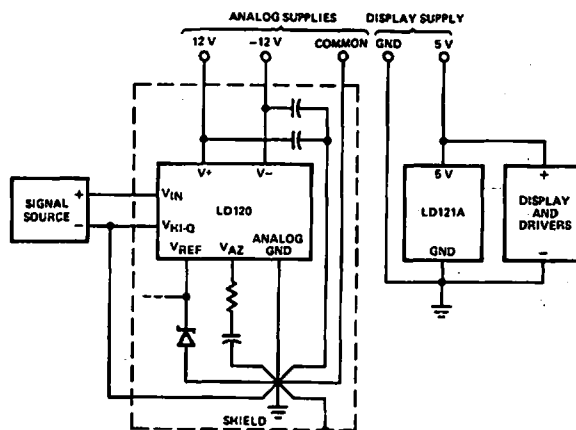
The resistors at R_2 and R_1 should track each other over temperature at least as well as the tempco of the reference.

APPENDIX B

Grounding – The optimum grounding scheme is shown in Figure 12.

The main considerations are: analog ground is common to V_{REF} , C_{AZ} , $\pm 12\text{ V}$ commons, $\pm 12\text{ V}$ bypass, ground of the signal source, common power ground, case ground; isolation of currents in the 5 V circuits from those of analog grounds; a 3-wire input connection for remote signal sources.

These connection methods will alleviate AC and DC pickup in signal inputs and integrator positive input (analog ground) from noise currents caused by the display and AC environment.



LD120/LD121A Grounding System
Figure 12

APPENDIX C: TROUBLESHOOTING

Problem	Causes
Jittery Display	f_{OSC} is not stable (short-term) AC voltage on V_{IN}, V_{HI-Q}, power supplies, or V_{REF} AC fields passing through unshielded circuit board R_1, R_2, or R_3 being carbon composition type Excessively small full-scale sensitivity implemented V_{AZ} or V_{REF} too small
Offset Drift	Excessive input resistance or C_{AZ} too small (see appendix A) Circuit board leakages excessive due to flux or moisture absorption A variable offset in grounding system Poor quality capacitors for C_{INT} or C_{AZ} Sample rate too slow (< 1 sec) Thermocouple junctions in the 200 mV range
Poor Linearity	Poor quality C_{INT} V_+ or V_- less than 10 V Circuit board leakages to C_{INT} Noise pickup on U/D or loading of U/D V_{REF} modulated by display ground currents
No digit strobes from LD121A	Clock not functioning Some terminal of the LD121A more positive than V_{SS}

DESIGN AID OF THE LD120/LD121A 4½ DIGIT DVM

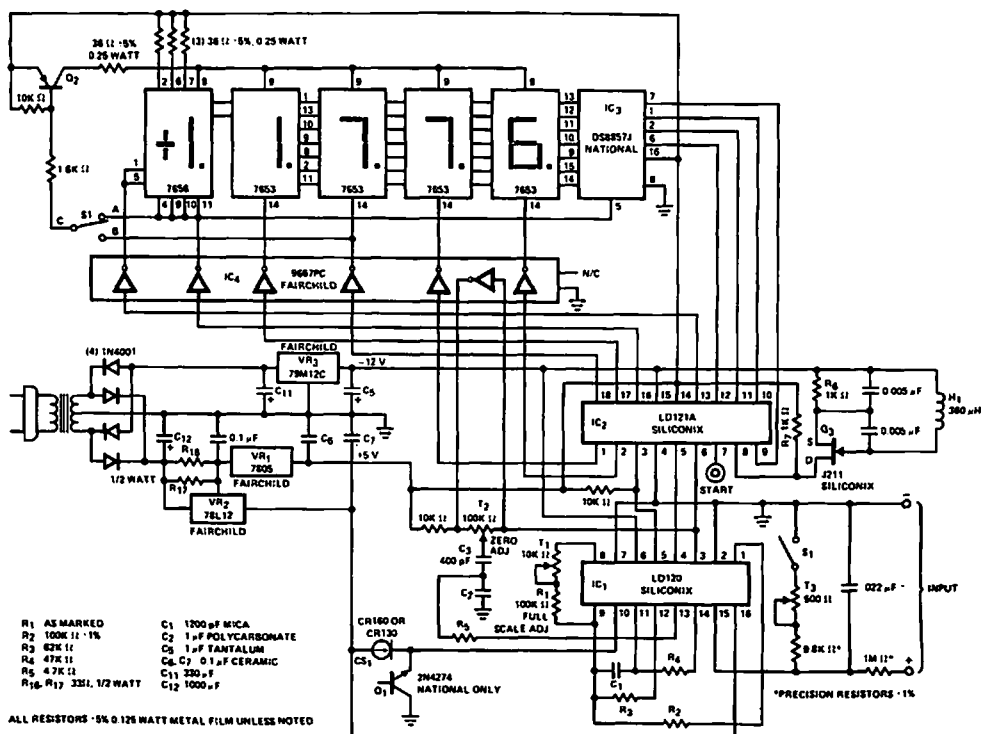
INTRODUCTION

The 4 1/2 Digit AC powered DVM schematic, P.C. board layout and parts list are intended to aid and speed the evaluation of the Siliconix LD120/LD121A precision A/D converter. As all converters of this resolution are sensitive to trace layout, this pattern demonstrates proper grounding and signal protection. A switchable 100:1 input signal divider is provided to enable the demonstrator to become a useful laboratory DVM after the evaluation of the system has been completed.

The metal pattern and component placement diagram are both printed to a 1:1 scale. The component placement art is intended to be silk-screened on the top side of the board to provide easy component installation. It can, however, be used simply as a loading diagram.

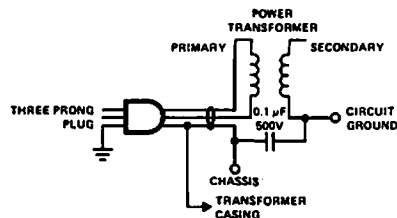
The demonstrator DVM features,

- ± 1 count linearity
- 0.75 count LSD count stability (2 V scale)
- $1\text{M}\Omega$ source impedance seen by converter input
- Auto Polarity
- Auto Zero cycle
- 200 mV F.S. range with:
 - less than 2 counts instability
 - ± 1 count linearity
 - $10\mu\text{V}$ resolution



CONSTRUCTION HINTS

1. A solid line between two holes represents a jumper wire.
2. A copper dot is placed by pin one of the IC's.
3. The dotted area denotes the power supply. If bench power supplies are available, connect to the pads marked +15 and -15. The positive source must supply 300 mA. The negative source must supply 30 mA.
4. The tab of the CR160 aligns to + mark.
5. The LD120 should be socket mounted
6. The 2N4274 voltage reference must be selected for a reference voltage equal to or greater than 6.6 V. A 6.6 V to 6.8 V zener reference may be substituted.
7. The CR160 current source may be replaced with a 36K Ω resistor. Some degradation in stability and gain tempo may result.
8. The display board may be directly soldered to the circuit board, eliminating the edge connector.
9. C₃ is a mica dielectric.
C₁ may be mica or polycarbonate dielectric.
C₂, and C₆ may be mylar or polycarbonate dielectric.
C₁₀ is tantalum dielectric.
C₁₁ and C₁₂ are electrolytic dielectric.
C₄, C₅, C₇, C₈ and C₉ are ceramic disc capacitors.
10. All resistors are $\pm 5\%$ metal film unless otherwise noted.
11. Regulators VR₁ and VR₂ operate too hot to touch $\approx (85^{\circ}\text{C}$ or 185°F)
12. Total power dissipation is 6 watts.
13. Break off steel screw tab from transformer nearest analog input. Connect other tab to earth ground wire from the power cord.
14. **CLEAN BOARD THOROUGHLY** after assembly. Any salts, finger oil, or solder flux remaining in analog circuitry may allow leakage currents detrimental to high quality performance.
15. LED displays are intensity coded. To avoid an unattractive display, check these codes for uniformity.



LAYOUT PRECAUTIONS

The following layout precautions have been taken and should be observed on the user's P.C. board:

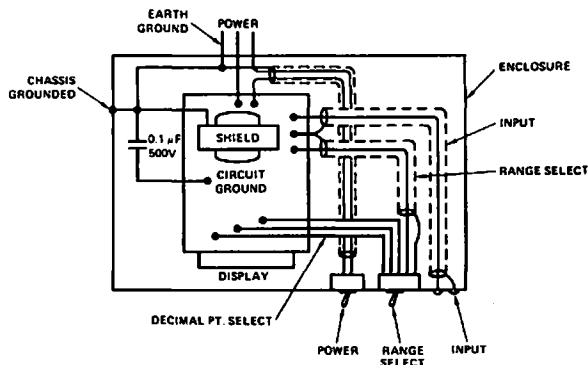
1. $V_{IN}^{(+)}$ trace is adjacent to ground only.
2. Traces from LD120 pins 9, 13, 15 are not adjacent to signal traces carrying AC signals.
3. U/D and comp. signals (LD120 pins 4 and 5) are separated by digital ground.
4. Digital circuitry ground paths return to the transformer (or power supply) via a different path than analog grounds from LD120.
5. The path from $V^{(-)}$ input to Hi-Quality ground (pin 2) does not carry any other currents.
6. The ground path from the reference and CSTRG (C2) travel directly to Analog Ground (pin 7 of LD120).
7. Int Input (LD120, pin 9) node connections are kept short and compact. This node has a relatively high impedance and is therefore subject to AC line noise pick up.
8. The +5 V supply to the LD121A should not share a current path with the display currents.

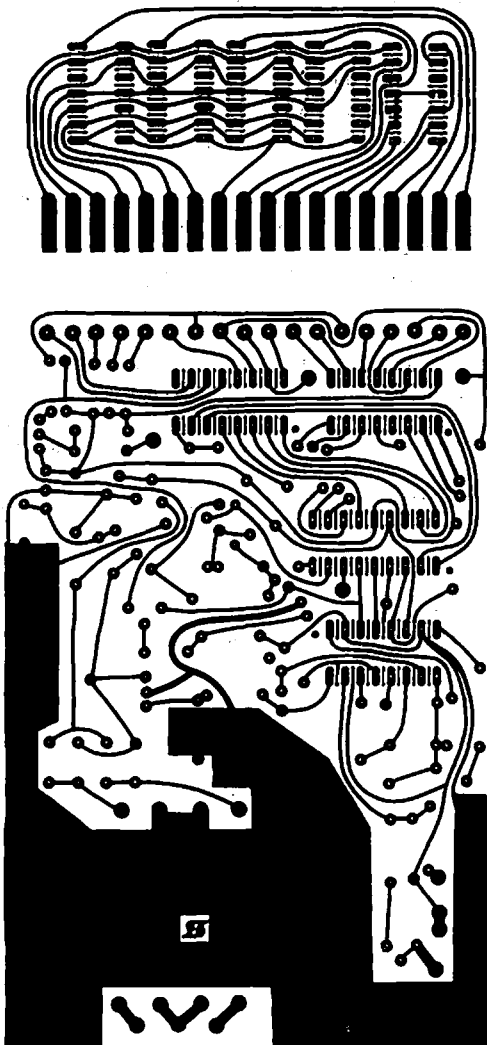
AC SHIELDING

Improper AC shielding will result in excessive LSD run around. Therefore, the following precautions should be taken:

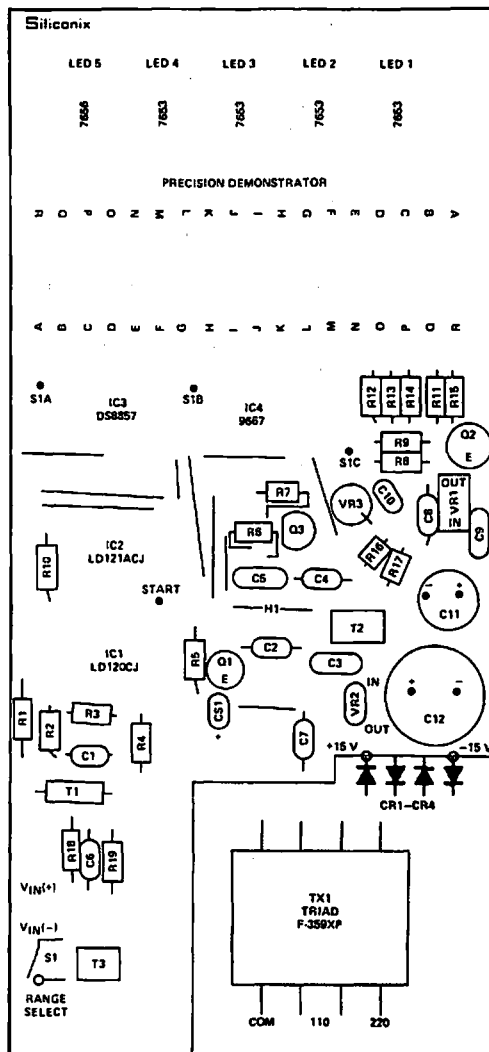
1. Use coaxial wire for the input and range select leads to the chassis front panel.
2. Enclose DVM in a metal enclosure.
3. Keep decimal point select wires separated from the input leads.
4. Keep AC line cord enclosed in box to a minimum and close to the chassis.
5. Shield the power switch leads with earth ground.

The diagram below illustrates good packaging practice:





Metal Pattern for DVM Board
(Bottom View)



Component Placement Diagram
(Top View)

(refer to last page of design aid for 1:1 P.C. pattern)

CAUTION: The AC line voltages associated with this board can be fatal. Proper precautions for operating this instrument must be observed by the user! Siliconix assumes no liability for unsafe operation.

FABRICATION HINTS

All holes require a #60 drill except for the following holes which require a #54 drill:

- Transformer
- AC inputs
- Edge connector
- V_{IN} (+ and -)
- Range control pins
- Decimal point select

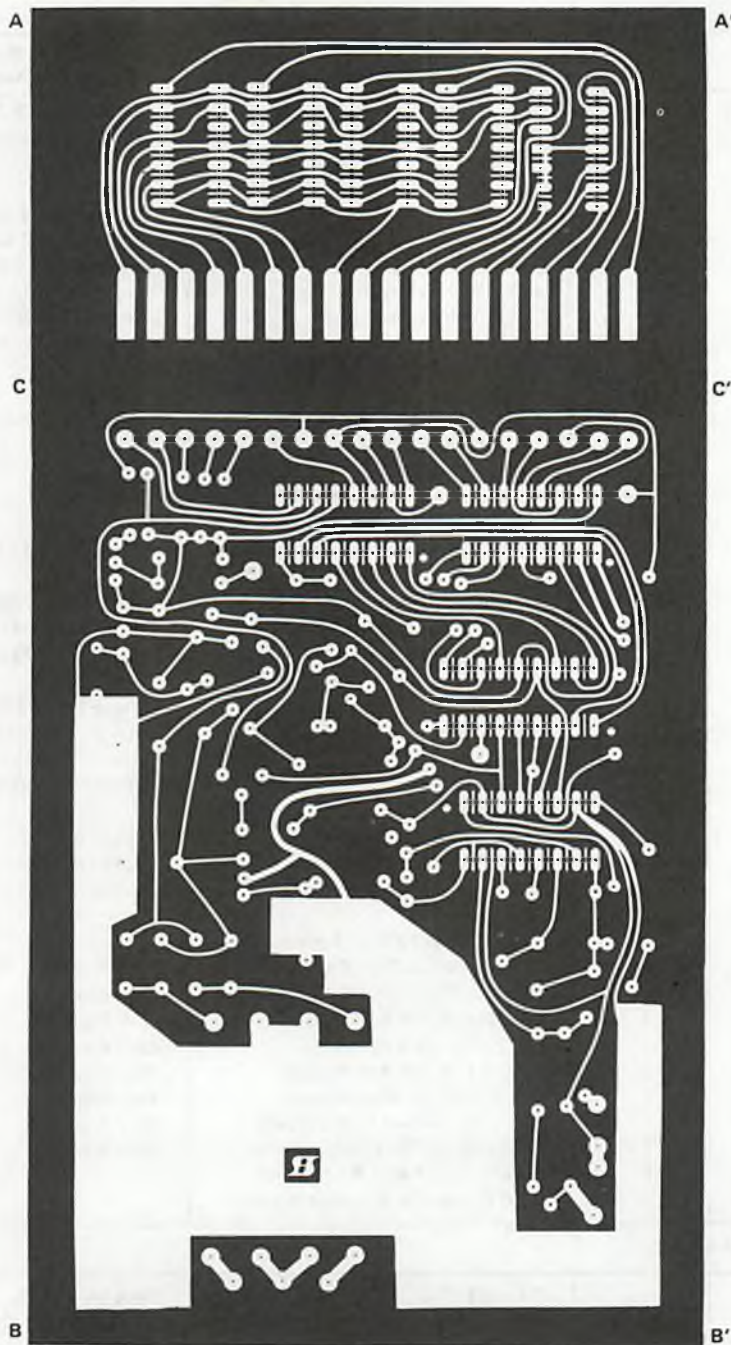
PARTS LIST

Part Numbers	Quantity	Description	Recommended Manufacturer and Part Number
IC ₁	1	Analog Processor IC	Siliconix LD120CJ
IC ₂	1	Digital Processor IC	Siliconix LD121ACJ
IC ₃	1	Display Decoder/Driver	National DS8857J
IC ₄	1	Seven Buffer/Driver	Fairchild 9667PC
LED 1-4	4	Seven Segment 0.43" LED Display	Hewlett-Packard 5082-7653
LED 5	1	±1 Overflow 0.43" LED Display	Hewlett-Packard 5082-7656
VR ₁	1	+5 V Voltage Regulator	Fairchild μ A7805UC
VR ₂	1	+12 V Voltage Regulator	Fairchild μ A78L12AWC
VR ₃	1	-12 V Voltage Regulator	Fairchild μ A79M12HC
Q ₁	1	NPN Transistor	National (Only) 2N4274
Q ₂	1	PNP Transistor	Motorola 2N4402
Q ₃	1	N-Channel JFET	Siliconix J211
CS ₁	1	1.3 or 1.6 mA Current Source	Siliconix CR130 or CR160
H ₁	1	360 μ H Inductor $\pm 5\%$	—
S ₁	1	DPDT Miniature Toggle Switch	C & K 7201
S ₂	1	SPST Miniature Toggle Switch	C & K 7101
C ₁	1	1200 pF Mica Capacitor	—
C ₂	1	1 μ F Polycarbonate Stocked Foil Cap.	Siemens B32 541-1.00/5/100
C ₃	1	400 pF Mica Capacitor	—
C ₄	1	.0047 μ F Mylar Capacitor	Sprague 192P4729R8
C ₅	1	.047 μ F Mylar Capacitor	Sprague 192P504739R8
C ₆	1	.022 μ F Mylar Capacitor	Sprague 192P2239R8
C ₇₋₉	3	0.1 μ F Ceramic Disc Capacitor	—
C ₁₀	1	1.2 μ F Tantalum Cap - 10 V	Sprague 198D125X90225H1
C ₁₁	1	330 μ F Electrolytic Cap - 25 V Radial Lead	Mallory VTT330J25
C ₁₂	1	1000 μ F Electrolytic Cap - 25 V Radial Lead	Mallory VTT1000M25
T ₁	1	5K Ω Multiturn Trimpot	Spectrol 43P502
T ₂	1	100K Ω Multiturn Trimpot	Spectrol 64Y104
T ₃	1	500 Ω Multiturn Trimpot	Spectrol 64Y501
—	2	Bannana Jacks	—
R ₁₋₂	2	100K Ω $\pm 1\%$, 1/8 Watt Resistor	—
R ₃	1	62K Ω $\pm 5\%$, 1/8 Watt Resistor	Allen Bradley
R ₄	1	47K Ω $\pm 5\%$, 1/8 Watt Resistor	Allen Bradley
R ₅	1	4.7K Ω $\pm 5\%$, 1/8 Watt Resistor	Allen Bradley
R _{6, R7}	2	1K Ω $\pm 5\%$, 1/8 Watt Resistor	Allen Bradley
R ₈	1	1.6K Ω $\pm 5\%$, 1/8 Watt Resistor	Allen Bradley
R ₉₋₁₁	3	10K Ω $\pm 5\%$, 1/8 Watt Resistor	Allen Bradley
R ₁₂₋₁₅	4	36 Ω $\pm 5\%$, 1/4 Watt Carbon Comp.	Allen Bradley
R ₁₆₋₁₇	2	33 Ω $\pm 5\%$, 1/2 Watt Carbon Comp.	Allen Bradley
R ₁₈	1	1M Ω $\pm 1\%$, 1/8 Watt Wire Wound	—
R ₁₉	1	9760 Ω $\pm 1\%$, 1/8 Watt Wire Wound	—
AC Power Supply Parts			
TX 1	1	24 V C.T. Transformer	TRIAD F-359XP
CR ₁₋₄	4	Rectifier Diodes	Motorola IN4002
—	1	3-Wire Power Cord w/Plug	—

Metal Pattern

Scale 1:1

PC Board Art

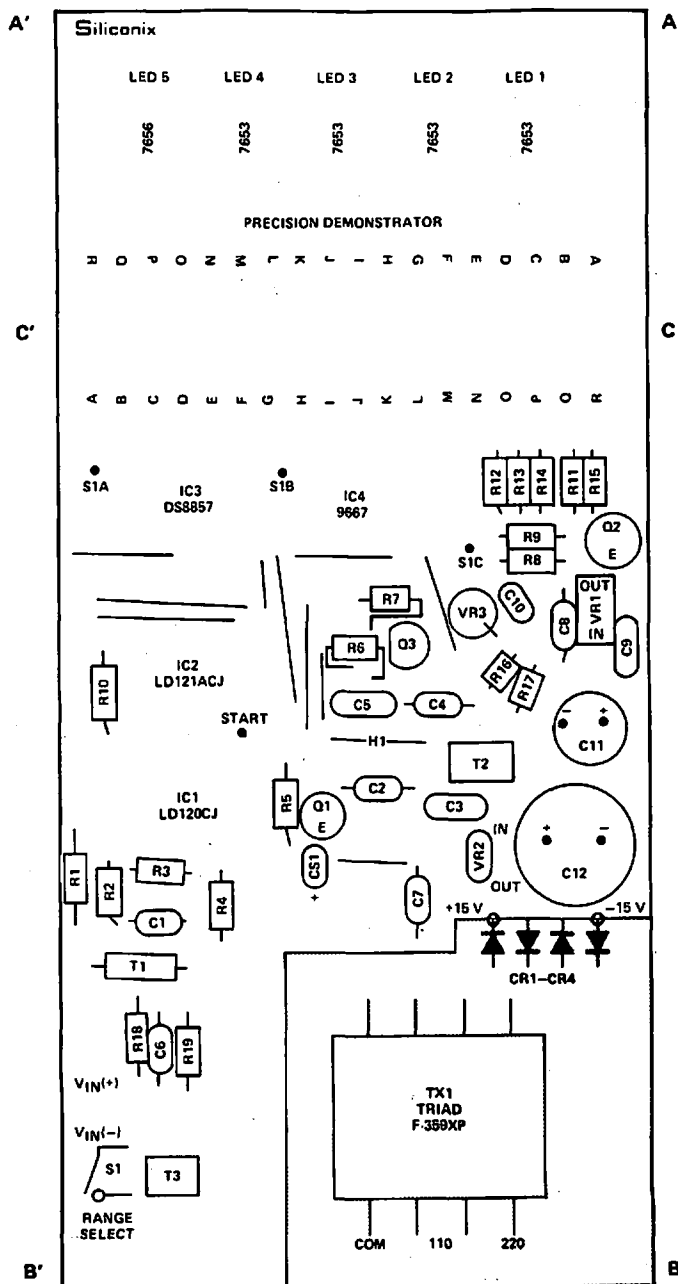


LD120/LD121A 4 1/2 Digit DVM

PC Board Art

Component Placement Diagram

Scale 1:1



LD120/LD121A 4 1/2 Digit DVM

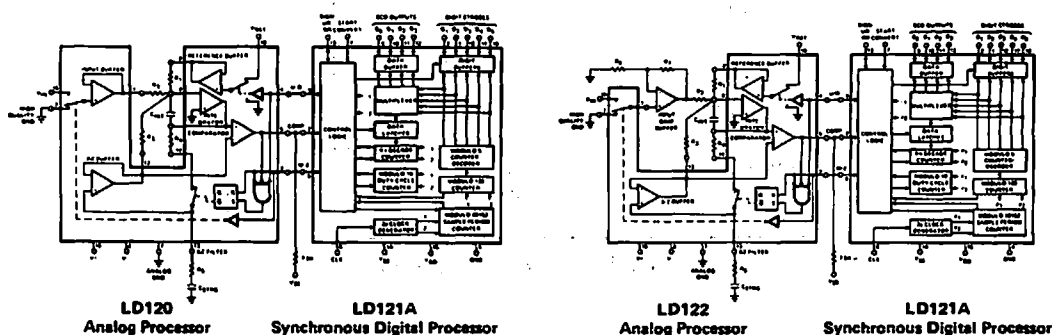
FUNCTION /APPLICATION OF THE LD122 /LD121A $\pm 4\frac{1}{2}$ DIGIT A/D CONVERTER SET IN MEASUREMENT SYSTEMS

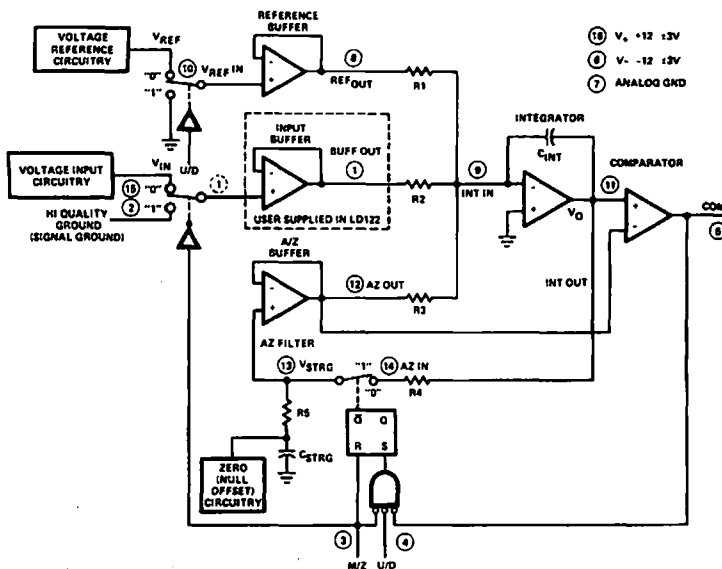
INTRODUCTION

The Siliconix LD122/LD121A combination extends system resolution capability beyond the $10\ \mu\text{V}$ maximum possible with the LD120/LD121A to literally the state of the art in low noise op-amps. All the while however, retaining the features of the LD120/LD121A system such as $4\frac{1}{2}$ digit precision, Auto-Polarity, Auto-Zero and ratiometric operation. Typical low voltage measurement applications of the LD122 include thermocouples, resistance bridges, and strain gauges.

As the functional block diagrams show in Figure 1, the two A/D converters are identical except for the input gain buffer which is user supplied in the LD122. Although it's

theoretically possible to manipulate the LD120 resistor ratios to accommodate any input voltage range, the $1/F$ noise characteristics of the LD120 unity input PMOS buffer make it impossible to obtain better than $10\ \mu\text{V}/\text{LSB}$ resolution capability. A $10\ \mu\text{V}/\text{LSB}$ resolution capability corresponds to a 200 mV fullscale range. However by using an external op-amp with good noise characteristics as diagrammed with the LD122, low voltage resolution capability becomes essentially a function of the external op-amp's performance. For instance it's currently possible to obtain op-amps with noise levels on the order of $1\ \mu\text{V}$, enabling our system to have $1\ \mu\text{V}/\text{LSB}$ (or 20 mV full scale) measurement capability.





Analog Processor Expansion Diagram
Figure 2

Since the LD122/LD121A converter is essentially a LD120/LD121A system suitably modified (in Figure 2) and numerous dissertations on the quantized feedback technique can be found in the Siliconix LSI Data Book, discussion of basic converter operation will be foregone in favor of specific precautions, guidelines and applications to follow when doing very low voltage measurements. For those desiring basic operational information I refer you to the LD120/LD121A data sheet and application note AN77-1.

APPLICATIONS INFORMATION

Features and Applications

With its long list of high performance features:

- Wide choice of input voltage ranges
- High resolution 4½ digit operation
- 0.005% ± 1 count accuracy
- Highly linear operation with simultaneous unknown-reference integration
- Auto Polarity operation with only 1 external reference
- Fully buffered inputs
- TTL output drive
- Automatic Zeroing cycle

Applications Tailor Made for the LD122/LD121A include:

- Microvolt Digital Volt Meters
- Thermocouple Temperature Measurement Systems
- High Precision strain gauge measurement systems
- Scientific Instrumentation and others

LD122-LD120 Similarities

Probably the best way to think of the LD122 is as if it were an LD120 with the V_{IN} input amplified. So anywhere you see an expression for the differential LD120 input ($V_{IN} - V_{HI-Q}$) substitute $X(V_{IN} - V_{HI-Q})$ where X is the gain of the user supplied input buffer. Doing so, our A/D output count relation becomes:

$$\text{Output Count} = \frac{X(V_{IN} - V_{HI-Q})}{V_{REF}} \cdot \frac{R_1}{R_2} \cdot 65,536$$

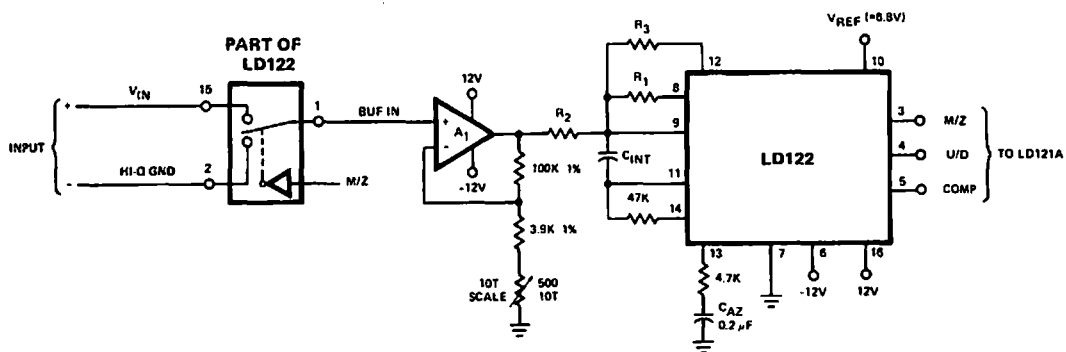
Now in addition to being able to scale the converter for different input ranges by changing the R_1/R_2 ratio, we can also alter the input buffer gain = X.

Figure 3 shows a typical application of the LD122/LD121A chip set. The system is set up to indicate full scale if 2V (100 $\mu\text{V}/\text{LSB}$) is applied to R_2 by the input gain buffer. However the input gain X is 100 so that a 20mV (1 $\mu\text{V}/\text{LSB}$) signal applied to the input buffer results in a fullscale reading. If the input gain were only 10, then a 200mV (10 $\mu\text{V}/\text{LSB}$) signal would be necessary to cause a full scale reading.

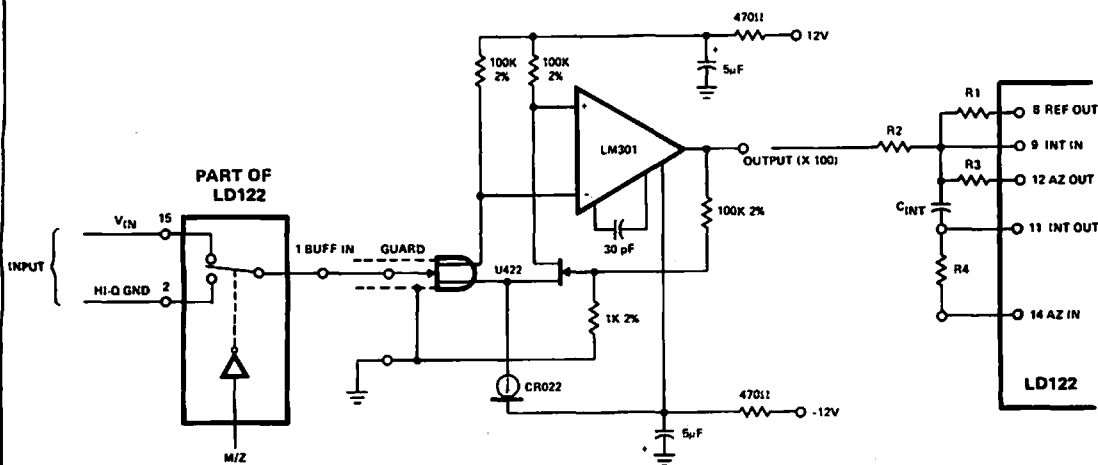
Input Gain Buffers

Figure 5 shows the arrangement for a 20 mV full-scale front end. If an extremely low source impedance were used, such as thermocouple, then an amplifier such as the LM201A could be used for A_1 . For higher impedances, lower bias currents are required until at about $1\text{K}\Omega$ or above, a JFET amplifier will be required. Note that MOS input op-amps are not quiet enough.

Even the BI-FET op-amps are only good for a $20\text{K}\Omega$ input resistance up to 75°C . The circuit of Figure 6 has an input leakage of only 2pA typical at 75°C and would be usable with $1\text{M}\Omega$ input resistance. Although not covered here, there are ways to reduce leakage effects over temperature by a factor approaching 10.



20 mV F.S. Meter (Front End)
Figure 5



Ultra-Low-Leakage Preamp
Figure 6

Input Buffer Selection Considerations

Ideally we would like the user supplied input buffer to have constant gain over the entire input voltage range so that the converter's linearity and accuracy can be preserved. Unfortunately real life op-amp characteristics, principally common mode voltage, prohibit such an ideal situation and must be reckoned with when choosing an op-amp.

Consider first of all the following unity gain voltage follower configuration in Figure 7.

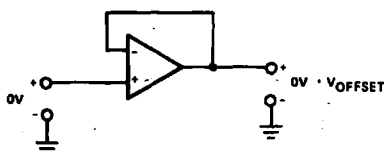


Figure 7

With an ideal op-amp, inputting 0V should give us a 0V output. With a real amplifier though, there is a small error offset V_{OFFSET} present as shown. Assuming that this offset is constant over the entire input voltage range, it is easily taken care of by the LD122 in the Auto-Zero interval where such error offsets are easily corrected for.

Suppose that we now input a 20 mV signal to our unity buffer. See Figure 8.

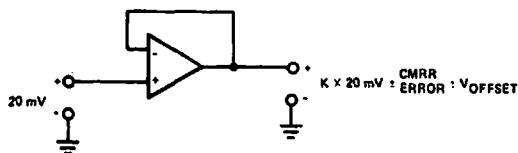


Figure 8

If our circuit is ideal, then $K=1$ for a unity gain. Realistically though, it's slightly less than 1, so just considering our voltage gain (no other errors) we don't quite get a 20 mV output. Such a loss in gain means that we don't quite get the output range that we'd like from our A/D when a full scale input voltage is applied.

This gain loss, if constant, is easily corrected for by slightly trimming the LD122 R_1/R_2 ratio for a full scale reading with a full scale voltage input. The one error that we cannot compensate for however, is the common mode error, CMRR, which is non-linear and varies depending on the input-voltage. This being the case, we'd like the maximum error attributable to CMRR to be less than 1 count of the A/D. If we were using the above buffer with an LD122/LD121A to measure down to $1 \mu\text{V}/(\text{count or LSB})$ (20 mV range) then the maximum CMRR error must be less than $1 \mu\text{V}$.

If we now use a buffer with a gain of 100 as diagrammed in Figure 9, a full scale input (20 mV) to the buffer will result in a 2 volt output signal. Since we would like to resolve to 1 part in 20,000 ($1 \mu\text{V}$ input, $100 \mu\text{V}$ output) the output

CMRR error must be less than $\frac{1}{20,000} \cdot 2\text{V}$ (i.e. for ± 1

count operation CMRR better than 86 dB over the input voltage range) or $100 \mu\text{V}$ over the entire voltage range. If noise is significant, (thermal, junction, etc.) the sum of

CMRR error and noise must be less than $\left[\frac{1}{20,000} \times \text{output buffer voltage} \right]$ for ± 1 count resolution.

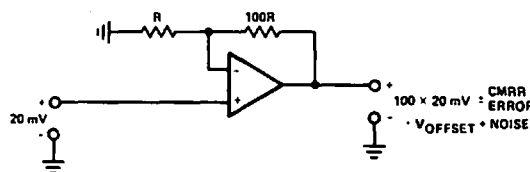


Figure 9

System Layout Guidelines and Precautions

When operating in the microvolt region extreme care must be taken with system layout and component selection, particularly in the front end, to minimize stray noise pick up. For instance the voltage inputs to the A/D should be shielded and put through a low pass filter as illustrated in Figure 10.

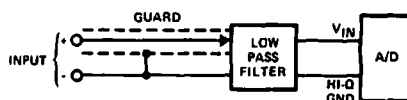


Figure 10

In laying out a printed circuit board, good layout technique should be observed with particular emphasis placed on possible problems due to grounding, capacitive coupling, leakage and thermocouple effects between pins and traces as follows.

Grounding considerations are presented in detail in Appendix B and as discussed there, minimum system noise requires that analog and digital grounds be kept separate until terminated at the power supply.

Capacitive coupling and leakage problems are particularly noticeable with the LD122 analog chip, but can be minimized through the use of a 2 sided glass-epoxy board, with guard traces driven from low impedance sources. Of foremost concern with the LD122 is capacitive coupling between pins 4 (U/D in) and 5 (COMP out) as diagrammed in the chip pin out below. As shown, a digital ground trace between pins 4 and 5 is recommended to reduce these inter-pin effects. The general rule of thumb to follow here is to guard [high impedance analog inputs and pulse width critical digital waveforms] from [voltage supplies and digital signals] by driving [the guard rings and traces] with [low impedance sources having potentials close to the guarded pins].

Following this approach it might also be wise to isolate pin 10 (V_{REFIN}) with traces from pin 8 ($REFOUT$) and pin 13 (A/Z filter) with a trace from pin 12 (A/Z out) as shown in Figure 11.

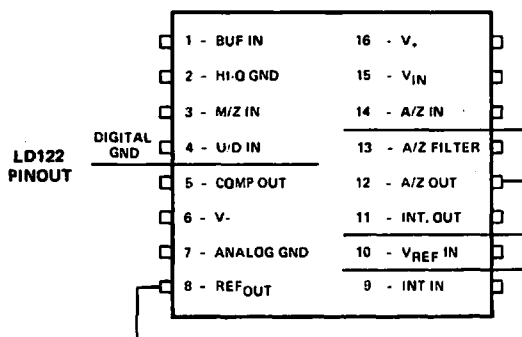


Figure 11

Down in the microvolt region ordinarily insignificant sources of noise can become major problems unless adequately accounted for in the system layout. Probably the most insidious of which are thermal effects in the form of thermocouple junctions and board temperature gradients. Recall that 2 dissimilar metals placed together form a thermocouple junction and when heated can supply a small output voltage. Even at room temperature the effects are

appreciable in the microvolt region and numerous junctions are possible on a circuit board where we go from gold plated edge connector to tin plated copper trace to solder to kovax IC lead to semiconductor interface. Board temperature gradients can effect minute resistance and thermocouple changes resulting in unequal voltage potentials and noise over even the most carefully balanced signal paths. Therefore, layout in terms of optimum package placement, minimum input lead length and minimizing temperature gradients should be considered. Generally speaking, the input gain buffer as well as any input circuitry should be electrically and thermally shielded for best results.

In any measurement application component quality and stability is always a question and a few words concerning LD122 resistor and capacitor selection are appropriate here. Ordinarily R1 and R2 quality are critical to proper circuit operation and they and any accompanying trimming components are recommended to be wirewound or metal film since carbon and oxide film resistors can generate large amounts of thermal noise.

In addition, since we are talking about gain setting resistances, they should track each other over the operational temperature range lest a gain error result.

When a user supplied input buffer of appreciable gain is used, the burden of quality becomes shifted to the input buffer components since any noise there is appreciably magnified, while R2 now faces a large input signal in relation to its possible noise contribution. The gain setting resistors must therefore be of appropriate quality. In either case, resistor quality should be appropriate to its relative noise contribution.

The integrator capacitor C_{INT} should be mylar or better quality. The autozero capacitor C_{STRG} should be mylar, polystyrene, polycarbonate, or polypropylene, the latter being best with regards to dielectric absorption. Resistors R3, R4, R5 quality is not critical, but should be long term stable. Above all, capacitive losses (leakage, dielectric absorption, etc.) must be kept to a minimum for proper operation as Appendix A explains.

APPENDICES

APPENDIX A: ERROR TERMS

Zero Drift – The main source of zero drift is leakage from the input and auto zero buffers. Figure 12 shows typical input and auto zero leakages over temperature. The error component due to I_{IN} is simply

$$\Delta V_{IN} = \Delta I_{IN} \cdot R_{SOURCE}$$

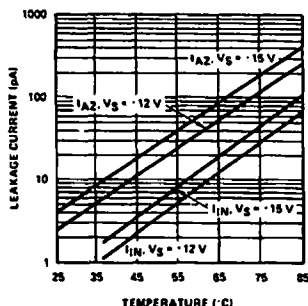
For a 1M Ω input resistance, and $\Delta I_{IN} = 30$ pA at 75°C, $\Delta V_{IN} = 30$ μ V, corresponding to a 0.3 bit offset at 2 V full-scale, and 3 count offset at 200 mV full-scale. This offset can be reduced by reducing R_{SOURCE} or by inserting a compensating R_{SOURCE} between V_{HI-Q} and ground.

The drift due to I_{AZ} is independent of scale factor, and is caused by the voltage on C_{AZ} drifting during the measure interval. The magnitude of drift will be

$$\Delta V_{AZ} = \frac{I_{AZ} \cdot T_{MEASURE}}{C_{AZ}} = \frac{I_{AZ} \cdot 32,768}{C_{AZ} \cdot f_{OSC}}$$

This will cause an effective input current to the integrator of $\Delta V_{AZ}/2R_3$, the factor two resulting from the fact that the ramp of auto-zero drift is averaged by the algorithm. This input current due to drift is analogous to an input signal of $\Delta V_{AZ} R_2/2R_3$, so the count drift is

$$\Delta \text{Count} = \frac{\Delta I_{AZ}}{C_{AZ} f_{OSC} V_{REF}} \cdot \frac{R_1}{2R_3} \cdot 2.15 \times 10^9$$



Typical Leakage Over Temperature
Figure 12

So given $\Delta I_{AZ} = 100$ pA when up at 70°C, $R_1 = 60K = R_3$, $C_{AZ} = 0.1$ μ F, $f_{OSC} = 150KHz$, and $V_{REF} = 6.2$ V, $\Delta \text{Count} = 1.16$ due to ΔI_{AZ} only.

The drift caused by thermocouple junctions on the LD120 is much less than that caused by leakages.

Gain Drift – Full-scale gain drift is caused mainly by changes in V_{REF} . One count in 20,000 stability per degree C is 50 ppm/°C, so the zener reference should have at least 10 ppm/°C stability and the system burned-in to reduce long term drift.

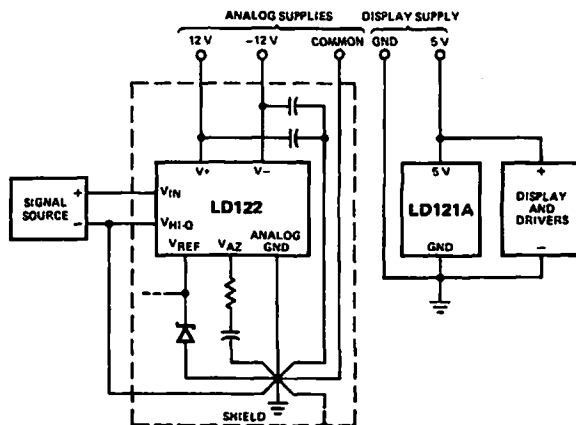
The resistors at R_2 and R_1 should track each other over temperature at least as well as the tempco of the reference.

APPENDIX B

Grounding – The optimum ground scheme is shown in Figure 13.

The main considerations are: analog ground is common to V_{REF} , C_{AZ} , ± 12 V commons, ± 12 V bypass, ground of the signal source, common power ground, case ground; isolation of currents in the 5 V circuits from those of analog grounds; a 3-wire input connection for remote signal sources.

These connection methods will alleviate AC and DC pickup in signal inputs and integrator positive input (analog ground) from noise currents caused by the display and AC environment.



LD120/LD121A Ground System
Figure 13

APPENDIX C: TROUBLESHOOTING

Problem	Causes
Jittery Display	f_{OSC} is not stable (short-term) - AC voltage on V_{IN}, V_{HI-Q}, power supplies, or V_{REF} - AC fields passing through unshielded circuit board R_1, R_2, or R_3 being carbon composition type - Excessively small full-scale sensitivity implemented V_{AZ} or V_{REF} too small - Insufficient power supply bypass capacitor
Offset Drift	- Excessive input resistance or C_{AZ} too small (see appendix A) - Circuit board leakages excessive due to flux or moisture absorption - A variable offset in grounding system - Poor quality capacitors for C_{INT} or C_{AZ} - Sample rate too slow (< 1 sec) - Thermocouple junctions in the 200 mV range
Poor Linearity	- Poor quality C_{INT} V_+ or V_- less than 10 V - Circuit board leakages to C_{INT} - Noise pickup on U/D or loading of U/D V_{REF} modulated by display ground currents
No digit strobes from LD121A	- Clock not functioning - Some terminal of the LD121A more positive than V_{SS}

MICROPROCESSOR INTERFACE TECHNIQUES AS APPLIED TO THE SILICONIX A/D CONVERTER FAMILY

INTRODUCTION

When attempting to interface a microprocessor system with a peripheral device (in this case an A/D) that operates at a substantially slower speed, the communications process between the system and peripheral can be thought of as lying between two extremes, synchronous and asynchronous operation. Either mode of operation will offer trade-offs between speed or throughput, and hardware complexity. For instance, in a synchronous communications approach, overall system speed is effectively reduced to that of the slow peripheral as the system must wait for a response or handshake from it. In an asynchronous approach however, both the system and the peripheral are able to operate at their own respective clock rates, with the speed differential problem being solved through the use of an interface buffer between the two. Hardware complexity is considerably higher here though than in a handshaking synchronous interface because such an asynchronous buffer is usually implemented through the use of latches to retain all of the data.

More often than not in A/D application notes or data sheets where an interface to a microprocessor is shown, the ap-

proach taken is the use of a peripheral interface chip such as an 8255 PPI or a 6820 PIA. While this approach will ultimately get the job done, it's extremely costly in terms of all of the negative features of both asynchronous and synchronous approaches (high hardware cost - peripheral interface chips aren't cheap; slowness - we are essentially operating synchronously with the A/D). As an added drawback, there's the software overhead necessary to initialize the chip and implement the synchronizing software routines. It's possible however, as we'll soon see, to construct totally synchronous and asynchronous interfaces out of common TTL parts costing only 1/3 to 1/2 the price of a peripheral interface chip and requiring none of the software overhead.

The circuits to be presented were built with the LD121A, but are of a sufficiently general nature that they can easily be modified to accommodate the other A/D's in the Siliconix product line.

LD121A DATA FORMAT

Just to review, Figure 1 shows the output data format of the LD121A digital controller and as you can see, data is BCD and sent out digital serial - bit parallel, perfect for multiplexed displays for which it was designed. The sequence in which the BCD digits are sent out is D5, D4, D3, D2, D1, repeating continuously as indicated. Note that the BCD data for a particular digit is available (16 LD121A clock cycles) both before and after the digit strobe comes on, a feature of which we shall make good use. Sign data appears 250 ns after the D5 strobe and is valid for the duration of D5. Although not shown here, a means of deter-

mining that the A/D has completed a measurement and has new data available is the positive edge of a signal called M/Z which occurs once every measurement interval. Complete LD120/LD121A operational information may be obtained by consulting the data sheet. All of the LD121A digital output signals can drive 1 standard TTL load and the M/Z line - 1/2 a load, a factor which contributed to the use of 74LS parts as much as possible in my circuits.

Since the synchronous interface is the simpler of the two, let's start with it first.

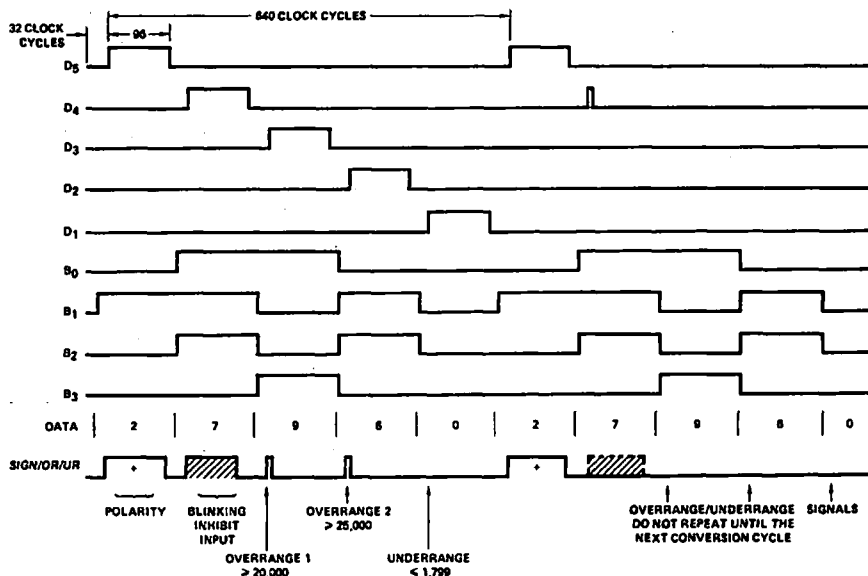


Figure 1. LD121 Digital Output Timing Diagram

SYNCHRONOUS A/D INTERFACE

In Figure 2 we have the schematic of an LD121A synchronous interface which was built and operated in an Intel SDK-85 system. Key to the operation of this circuit is the READY line which can be found on Intel, MOS Technology and other microprocessors. For those not familiar with it, the READY line is an input to the processor through which slow memories and in this case, slow peripherals can make the processor wait while data to be read in is being placed on the data bus. In this way the processor can be SYNCHRONIZED to the rate at which the slow peripheral is giving data, while running at full speed when other, faster, memories and peripherals are being accessed. The operation of the circuit is as follows. Normally the output to the READY input, A5 pin 5 is high, permitting full-speed processor operation. To accomplish this, all of the inputs to A5 must be low, which is possible if none of the first 5 outputs of the 4 to 10 line decoder are active (low). Although the A,

B, C inputs of A2 may change continuously, by using the D input as a chip enable, the outputs in question will remain high. However when a valid chip select (read peripheral operation) comes along, the tristate bus buffer A1 will be enabled as well as the 4 - 10 line decoder. Now depending on the valid address on ADR 0, 1, 2 one of the decoder outputs, corresponding to a particular LD121A digit, will go low. Assuming that all of the digit strobes are low (inactive), the READY line goes low causing the processor to wait up. As soon as the digit strobe in question goes high, indicating valid data is available, the READY line rises again allowing the processor to continue its read operation. Note that the digits may be read in any order as the synchronization is accomplished automatically. However the processor does have to wait for the right digit strobe to come along. The 74LS74 D type F.F. in the circuit is used as an interrupt indicator latch, generating a latched high level interrupt

signal when the positive M/Z edge comes along (new data ready) and resetting when a data read occurs. Depending on how the chip select is generated, the circuit may be set up as regular or memory mapped I/O, the choice is up to the user. As set up, the BCD data is located in the low data nibble and the sign is the high order data bit. However considerable latitude is possible both in data word configuration and parts selection, particularly in choosing the tristate bus buffer and decoder chips.

Lastly, after receipt of a valid chip select there's only a 3 gate delay in generation of a correct READY signal, permitting the circuit to be used with even the fastest of processors providing that they have a READY input.

ASYNCHRONOUS A/D INTERFACE

In Figure 3 we have the schematic of an asynchronous LD121A interface, also built and operated with an SDK-85. Although it's somewhat more complex than the previous circuit, relatively common parts are used and hardware costs are still well below that of a peripheral interface chip. Briefly, this circuit uses a 2101A memory as a 5 word X 4 bit latch to store the BCD data for immediate access later on by the microprocessor (i.e. no wait states). The 2101A was chosen because of its separate data inputs and outputs and is relatively cheap as far as memories go. Ordinarily LD121A BCD data is being written into the 2101A memory at addresses determined by encoding the LD121A digit strobes into 3 bit binary. The encoding is done by the A4 OR gates and the address is gated to the memory by the A2, A3 AND-NOR gates.

Note that 1/2 of the A3 AND-NOR chip is used to permit the storage of sign information as data bit D₁₄ during digit strobe 5. The memory write pulse is generated by A7 and A8 and is a low level pulse of minimum duration so as not to interfere during microprocessor reads (i.e. lock up the A5 read-write arbitrator logic unnecessarily). Note the 0.01 μ F capacitor on the trigger input to the A8 monostable. It's used to delay the generation of the write enable pulse so that the sign information which is slightly delayed from D5 (by 250 ns) will be valid. A5 is arbitration logic which determines whether a microprocessor read or LD121A data write is to be performed on the 2101A memory. The A5 outputs, pins 3, 6 control the A2, A3 AND-NOR gates and determine whether the 2101A memory address is to be supplied by the system address bus (read) or encoded digit strobes (write). A5 is also set up so that if a data write pulse is present from the monostable, its output pins 3, 6 will not change state (i.e. lock up). However when the write pulse ends, A5 will change state if necessary to reflect whether or not we have a valid chip select present (microprocessor read). If so, it will enable the memory data bus drivers, lock out monostable write pulses and gate the system address bus to the 2101A memory so that the read can be performed. When the chip select is in control of the A5 logic, further updating of the memory by the LD121A is

inhibited until the chip select is removed.

Although I was using a 2101A-2N with a 250 ns access time, measurements showed that data could be obtained within 250 ns after application of a valid chip select, providing that there was no monostable write pulse to lock up the A5 logic at the time. In which case it would have taken 250 ns plus the width of the monostable write pulse. However I found it very difficult to coincidence the chip select and write pulse since the write pulse is so short and so infrequent. So except on very rare occasions, my read access time from application of a valid chip select was at most 250 ns. By being careful about how and when the processor determines that there is new data to be read in (i.e. further qualify the interrupt signal) any possible coincidence of chip select and write pulse can be totally avoided.

As in the previous circuit, the A9-74LS74 is used as an interrupt latch. The entire circuit is of sufficiently general purpose design that the only real limitation to using it with any processor is its 250 ns access time. Again, depending on how the chip select is generated the circuit may be set up as either regular or memory mapped I/O.

Through careful examination of both the asynchronous and synchronous schematics it can be seen that in each, the correspondence between a system address supplied and the BCD digit read is:

ADR 2	ADR 1	ADR 0	Digit
0	0	0	D1
0	0	0	D2
0	1	0	D3
0	1	1	D4
1	0	0	D5

A rough estimate of the savings in time possible using an asynchronous rather than an synchronous interface approach in this application would be something on the order of 1 complete LD121A data output cycle each time we read in all 5 digits. For a LD121A running at maximum clock frequency (250 KHz, 5 conversions/second) this is a savings of about 2.5 milliseconds each and every time. Since the asynchronous circuit acts as though it were memory as far as the processor is concerned, the amount of time necessary to read in new data from it is essentially how quickly the processor can execute memory or I/O read commands, as the case may be, providing of course that read access times are met.

REFERENCES

1. Intel MCS-85 Users Manual, September 1980 Intel Corporation.



A SYSTEM SOLUTION TO HP-IL EQUIPMENT INTERFACE

Robert J. Zavrel Jr.
December 1983

INTRODUCTION

Siliconix manufactures several high performance components which lend themselves nicely to portable equipment. For a 4-½ digit HP-IL compatible DVM, Siliconix now offers a "systems solution" to the designer of such a device. With the exception of a few standard 4000 series CMOS ICs, all the special integrated circuits are offered by Siliconix. The DVM is based on the Si7135, a high-quality, single chip, dual-slope integrating A/D converter. The circuit used to interface the Si7135 to the HP-IL contains 23 standard 4000 series CMOS ICs. This hardware interface solution will be simplified to a 28 pin DIP interface IC. This IC allows direct connection to the Hewlett-Packard HP-IL standard "GPIO". Additionally, Siliconix offers three devices which complete the specialized DVM IC requirement. The DF412 provides a local LCD driver which will allow the DVM to operate as a stand-alone device. Two SD5002 analog switches are arranged to provide an analog input multiplexer which boasts over 100 db. channel-to-channel isolation. Finally, an Si7661 voltage converter eliminates the need for a negative power supply, thus a single 5 volt supply is all that is necessary.

The HP-IL "interface loop" is a data communications system designed as a portable, low cost, and high quality instrument controller. It is quite suitable for lab environ-

ments where easy programming is desirable. The powerful and popular HP-41 handheld computer or the HP-75C portable computer can be used as controllers for up to 31 "HP-IL devices" in the loop. Hewlett-Packard manufactures a wide variety of HP-IL compatible devices including a printer, timer, video interface, and DVM (Reference 1). For convenience the HP-41 will be used as the controller in this paper. A detailed description of HP-IL is beyond the scope of the paper, but a basic understanding of HP-IL is necessary to render this interface technique meaningful.

HP-IL INTERFACE CIRCUIT/INTERFACE IC HANDSHAKING

Care must be taken to avoid confusion of terms. The HP-IL interface circuit contains two basic ICs. It is this circuit which takes the serial IL pulses and routes the data to the two-way data bus, the appropriate handshake and other control pins. Taken together this assemblage of data and control pins is called "GPIO" or "general purpose input/output". Hewlett-Packard offers four approaches to realizing the HP-IL interface circuit. Details of these approaches are available from Hewlett-Packard. The "Interface IC" interfaces the Si-7135 digital outputs to the GPIO bus. (Figure 1).

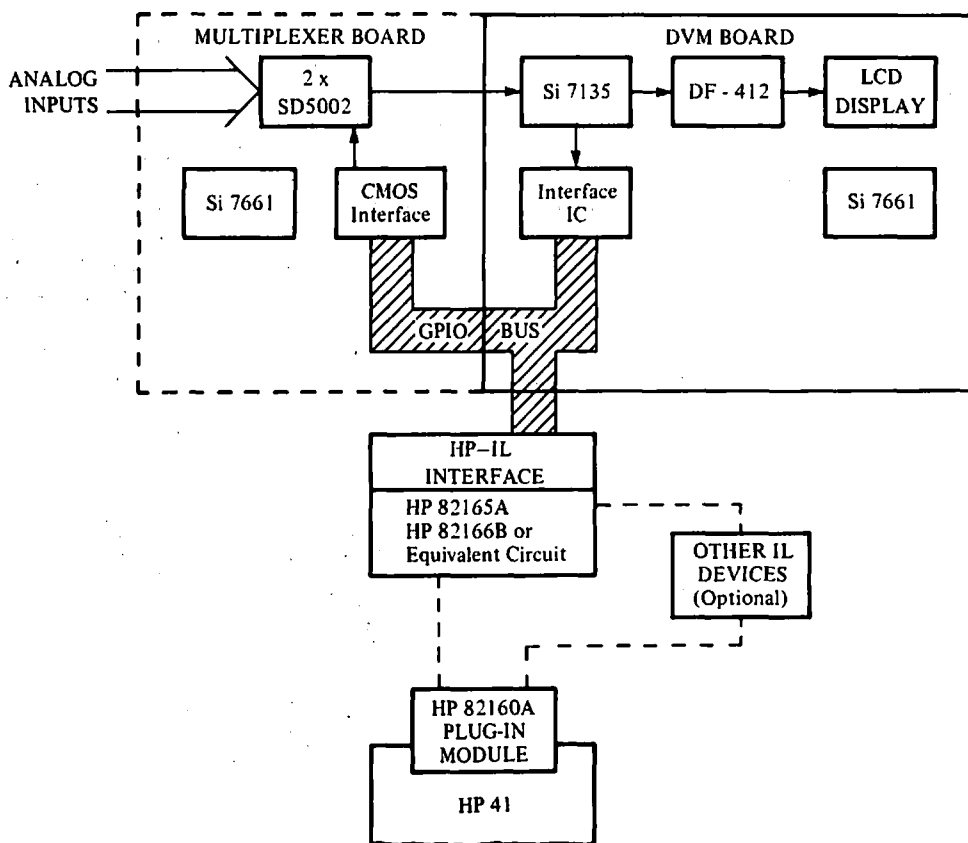


Figure 1
HP-IL Multiplexer/DVM System

Contained within the HP-IL interface circuit are the 28 pin DIP ILB3-0003 from Hewlett-Packard and the Mostek 1820-2810 40 pin single chip microcomputer. The ILB3-0003 contains multiple registers and extensive circuitry for the HP-IL interface. The microcomputer acts as an HP-IL device controller and provides the GPIO data and control pins later to be discussed in detail. This Mostek microcomputer is made with a special mask for HP-IL and must be purchased from Hewlett-Packard. These ICs are arranged around two 8-bit data busses labeled as DA and DB. In the DVM and multiplexer circuits, the DB bus is used only for data transfers between the 1820-2810 and the ILB3-0003. The DA is used as the bi-directional bus between the 1820-2810 and the DVM. Because ASCII characters are seven-bit words, the eighth bit of the eight-bit bus should be held low when ASCII is being transmitted. The circuits described here link the GPIO standard interface to the specialized data and control pins of the Si7135 4 1/2 digit DVM chip and a multiplexer. The multiplexer

circuit is also relatively simple, needing only a few standard CMOS ICs.

ASCII characters are used for all data transfer in HP-IL. Data transfer can flow to an external device such as a printer or from an external device such as a DVM. Two device modes are consequently defined as listener and talker. Data transfer between an HP-IL station and its corresponding peripheral device can utilize six "handshake" and additional command pins located on GPIO. Three handshake pins are used for the listener mode, and three are used for the talker mode. The two handshake modes are very similar. When listener is ready to accept data, a "Ready" pin is taken low (logic true). The talker may respond at this point if it has data to send with an ASCII character on the data bus and a low "Data Valid" pin. Finally, if the listener receives the data, it sets the "Data Confirmed" pin low completing the handshake sequence.

Several levels of handshaking are possible using the three handshake pins in different combinations. For the Siliconix DVM, the talker handshaking is very simple. "Data confirmed" is not used, and the "Ready" and "Data Valid" pins are hardwired together. "Ready" and "Data Valid" correspond to the $\overline{\text{RDY0}}$ and $\overline{\text{DAV1}}$ pins for the talker handshake. In addition, the $\overline{\text{GET0}}$ pin is used to initialize a reading which is fed to the controller. The $\overline{\text{GET0}}$ pin is set low by a "TRIGGER" command in the computer software program. The "IND" command is used after the "TRIGGER" command to actually read in decimal data from the HP-IL device. The low $\overline{\text{GET0}}$ pin sets a latch in the interface IC in turn allowing a counter to sequence seven ASCII characters to the HP-IL. The counter is sequenced as the $\overline{\text{RDY0}}$ pin is set low if three conditions are met. Sequencing is prevented during the $\overline{\text{GET0}}$ pulse by the first of three con-

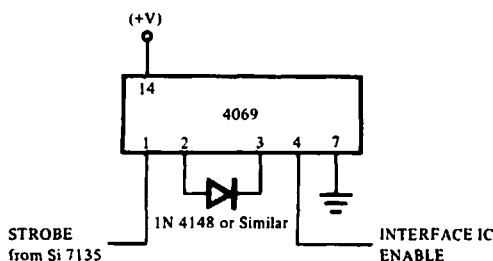


Figure 2
Optional Condition Circuit

ditional "AND" gates controlling the counter. The second gate is activated by the "TRIGGER" latch. In addition, an optional third gate is provided by the interface IC's ENABLE pin to be discussed later.

The seven ASCII characters provide for a polarity character, five digits, and a hardwired ASCII "LF" command. This character is recognized by the controller as an "End of Data" statement. The counter is allowed to sequence one more step after the "LF" command which resets itself and the "TRIGGER" latch. The read cycle is now complete, and the interface IC is ready to send another reading. A very simple seven line program in the HP-41 will initialize the DVM, read in the data, display the data, and loop back to take another reading. This program is shown in Table 1.

Figure 1 shows a functional block diagram of the system that contains several levels of asynchronism. The HP-41 is asynchronous to HP-IL; HP-IL is asynchronous to the interface IC; and the interface IC is asynchronous to the Si7135. The interface IC must account for random events

at all three levels and convert the polarity and strobed BCD outputs to the proper ASCII characters. A subtle but desirable trait of the interface is that it should not allow a reading by the HP-IL while the Si7135 is latching in new data. Additionally, the interface should not allow the latching of data while the HP-IL is reading. Either condition would result in an invalid entry. The ENABLE pin when used with the circuit in Figure 2 will prevent the counter from sequencing the ASCII characters. The result will be a repetition of a single character which will fill the HP-41 X Register. In turn, this may be checked with HP-41 software, and the data will be deleted preventing an HP-IL read during a latch change. Alternatively, this gate may be held high if an occasional invalid reading is permissible. With this configuration, about 3% of the readings will be invalid. "Invalid" is used here to describe the condition of reading

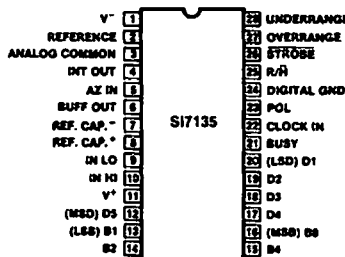


Figure 3
Si7135 Pin Out

in the five digit number from two separate Si7135 writings. For example, if the Si7135 latches in new data to the interface IC while the HP-IL is reading, perhaps the first two digits may be from the old voltage reading while three would be from new data. The other invalid condition is prevented by stopping the Si7135 with the "TRIGGER" activated latch. This is accomplished by setting the RUN/HOLD pin low and thus stopping the Si7135 cycle until the reading is complete.

Si7135/INTERFACE IC HANDSHAKING

Data is latched into the interface IC from the Si7135 by means of the four BCD data lines (Figure 4). They are routed to the proper character latch by the digit strobe pins. The polarity and most significant digit are simultaneously latched with Digit Strobe One. The STROBE pin, which should not be confused with the five digit strobe pins, goes low five times after each voltage measurement in tandem with the sequencing five digit strobes. Thus, the latching of Si7135 data into the interface IC occurs only once during each measurement cycle as a condition of the

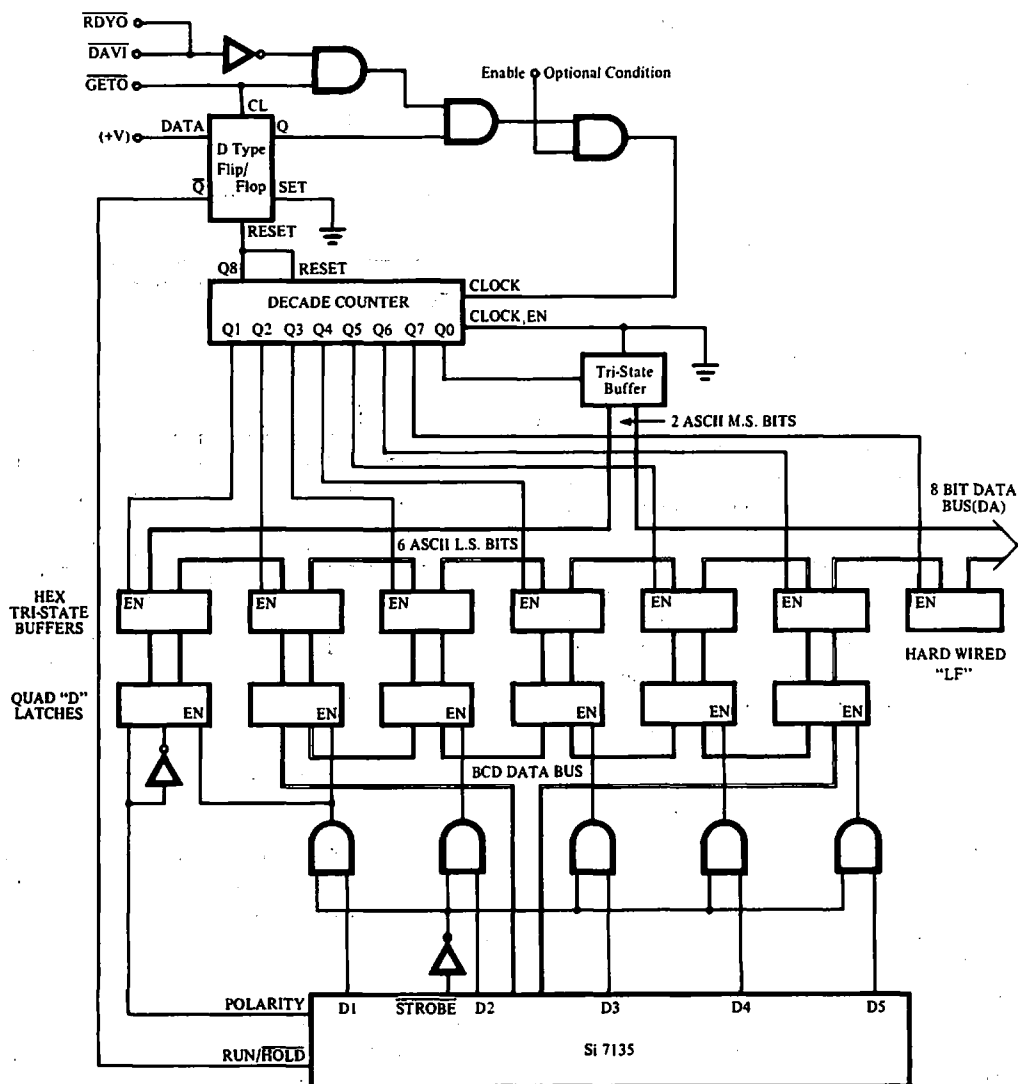


Figure 4
Simplified Circuit of Interface IC

Digit Strobe pins and the STROBE pin. There is one latch for each variable bit of the six variable ASCII characters. Non-variable bits, including the entire "LF" command, are hardwired. These latches and hard wires feed tri-state buffers which are sequentially activated by the counter and consequently present their data to the ASCII output bus (DA) on GPIO.

Autoranging or multiple input select functions can be implemented using similar straightforward programming techniques. The under-range and over-range pins of the Si7135 are connected to the most significant digit buffer.

Valid readings on the Si7135 range from -19999 to +19999. The under-range and over-range pins on the Si7135 are tied to the second and third bits of the most significant digit latch. Thus, during under-range, a numerical value slightly greater than or equal to 20,000 will be read, and 40,000 will be read during an over-range condition. These values along with the full register condition of the invalid reading discussed earlier can be checked by software. In the case of over or under-range, a subroutine can be called selecting an appropriately higher or lower scale. The scale called can also indicate the proper coefficient for correct

numerical display and decimal placement. Therefore, meter calibration may take place in software if the sensor cannot be adjusted. Under and Overrange as well as other Si7135 functions are optionally used by the designer. The interface IC was designed to allow customizing the interface for a given set of functions and applications. The interface IC is also useful with other A/D converters including the Siliconix "LD" family. Additionally, the great flexibility afforded by the software allows special readings such as dbm, db gain, and radian measure, etc. Indeed, applications of this system seem infinite.

HP-IL/MULTIPLEXER INTERFACE

In the case of input selection, autoranging and function select, etc., the circuit in Figure 5 may be used. Here, eight inputs are used to feed the Si7135. When the multiplexer is receiving instructions, it actually becomes a listener. A relatively simple circuit is required for the interface between the SD5002s and the HP-IL; furthermore, this SD5002 circuit may be used as a stand-alone circuit for a wide range of analog switching functions. SD5002s can be configured into superior video, audio, or RF switching circuits featuring excellent cross-talk and distortion performance (Ref. 2 & 3). Additionally, Siliconix offers a wide range of analog switches and multiplexers to suit any application. Power control is possible with up to 650 volt power FETs and simple standard control circuits. Thus, Siliconix can be a single supplier of specialized components from the HP-IL interface IC to HP-IL controlled high voltage FETs!

Three 4000 series CMOS ICs are required to interface data from HP-IL to the switch control gates. A separate Si7661 is shown on the multiplexer circuit in case the multiplexer is built independently of the DVM. (Figure 1) If it is built independently, a higher supply voltage can be used. This will allow higher analog voltages to be switched. Siliconix also manufactures the SD210 series which are discrete switch devices; these devices may be used if superior channel isolation is required and/or higher signal voltages must be switched.

HP-IL/multiplexer handshaking is very straightforward. The $\overline{\text{DAVO}}$ pin is used to enable a CMOS latch which stores the last three bits of the transmitted ASCII character. The $\overline{\text{RDYI}}$ pin is not used while the $\overline{\text{DACI}}$ pin is tied to ground. This is the simplest handshake scheme possible with HP-IL.

In the multiplexer, the three least significant bits of the ASCII character taken from the DA bus are used to select one of the eight analog inputs. The "OUTA" command in HP-41 software sends the contents of the Alpha Register to the IL device. The very simple hardware interface requires some special compensation in software. The most impor-

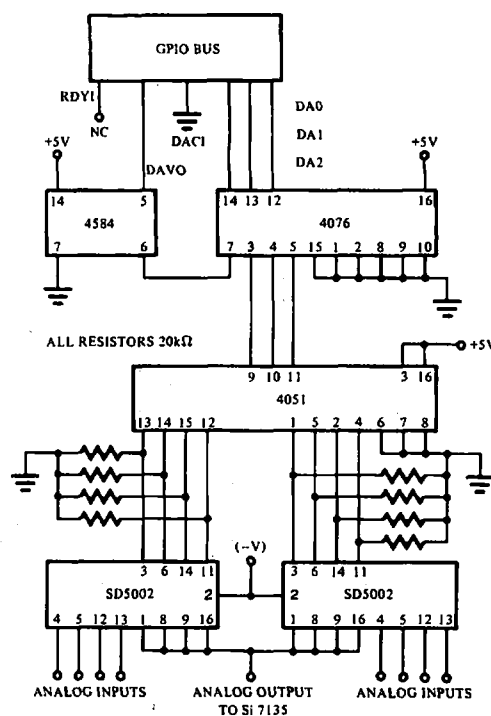


Figure 5
Multiplexer Schematic Diagram

tant constraint with this circuit is to send only one ASCII character at a time. This will prevent "glitches" and false data from being latched. In its normal operations mode, the HP-41 will automatically send an "End of Data" ASCII character at the end of an alpha string. The last ASCII character sent is the one which is latched into the multiplexer. For this reason, the "End of Data" character must be restrained. This is accomplished by setting Flag 17 "SF17" in the software. A more complex problem involves mathematical manipulations of numbers specifying the multiplexer channel. Such manipulations must take place with digital information—not alpha characters. Since HP-IL can only send data from the Alpha Register, these digital characters must be sent to the Alpha Register for transmission to the multiplexer. A problem arises because a decimal point "rides along" with the number to the Alpha Register. The decimal point is consequently read by the IL interface and sent as a ASCII character to the multiplexer causing a "glitch" or an invalid latch. This problem can be solved by clearing Flag 29 "CF29" and not displaying fraction data "FIXO". With these two additional simple commands, the desired numeric ASCII character will be latched into the multiplexer.

SOFTWARE EXAMPLE

Table 2 shows a simple program which will sequence the eight input multiplexer, display the input channel number, read in the voltage, display the voltage, and loop back. It is included to provide a sample program to get the system working and illustrate how the necessary commands can be arranged. The power of the HP-IL system may be appreciated when one sees only 29 lines of programming! The user will in most instances modify or rewrite programs to meet individual needs.

Details of HP software are contained in the literature provided with the applicable HP devices. The HP 82166C Inter-

face Kit includes a very comprehensive system description of HP-IL contained in multiple volumes. One word of caution to the hardware designer: there are numerous errors and misleading diagrams in the HP booklet entitled "HP 82166A HP-IL Converter Technical Manual" (Nov. 81). The corrections to these errors are in a follow-up booklet "HP-IL/GPIO Interface HP-IL Converter Manual Supplement".

In conclusion, Siliconix now offers the necessary integrated circuits to easily facilitate HP-IL interface to a low cost DVM design. This solution reduces the problem of such an interface to an easy lay-out task.

Table 1

```

01 LBL DVM1
02 LBL 01
03 TRIGGER
04 IND
05 VIEW X
06 GTO 01
07 END

```

Table 2

```

01 LBL DVM1      16 -
02 0             17 X=0?
03 STO 01        18 GTO 03
04 LBL 02        19 RCL 01
05 VIEW X        20 1
06 TRIGGER       21 +
07 IND           22 LBL 03
08 .0001         23 STO 01
09 *             24 CLA
10 FIX 4         25 ARCL 01
11 VIEW X        26 SF 17
12 FIX 0         27 OUTA
13 CF 29         28 GTO 02
14 RCL 01        29 END
15 7

```

REFERENCES:

1. *Electronic Design*, Parzybok, Hanson, Dec. 24, 1981.
2. Siliconix Application Note: "A High Performance Video Switch", Zavrel.
3. Siliconix Application Note: "A High Quality Audio Crosspoint Switch", Zavrel.

Si520 DATA ACQUISITION SYSTEM INTERFACES FOR I/O OR MEMORY MAPPED OPERATION

By Doyle L. Slack
December 1983

INTRODUCTION

The Siliconix Si520 is an 8 channel, 8-bit silicon gate CMOS Data Acquisition System containing an 8 channel multiplexer, an A/D converter, and an output latching circuit. The A/D converter uses a binary weighted capacitor successive approximation technique allowing fast conversion time with low power consumption. The 8 channel multiplexer offers great flexibility by providing multi-channel data collection with only one A/D converter. However, the outstanding advantage of this device is its ease of interfacing to microprocessor systems. Both the address inputs and data outputs are latchable which minimizes the time that the microprocessor and the data acquisition system must dedicate to data transfer. The outputs are tri-state, allowing direct connection to the system data bus for memory mapping. Since the Si520 is easily wired for either I/O or memory mapped operation, interfacing hard-

ware and associated software for both schemes are presented here.

The Si520 can be easily interfaced to the Intel 8085, an inexpensive 8-bit microprocessor with many available peripheral devices. The 8085 was chosen for interfacing because it makes a good example for wiring to any one of the several other similar microprocessor architectures.

The Intel 8155 RAM-I/O and 8755 EPROM-I/O chips provide both memory and I/O ports for the 8085 system and can be used to interface the Si520 and the 8085. If the A/D converter output of the Si520 is to be monitored at an I/O port, it can be left running constantly. The port can be sampled whenever a reading is desired. On the other hand, the memory mapped data acquisition system costs less to build because there is no need for an I/O port.

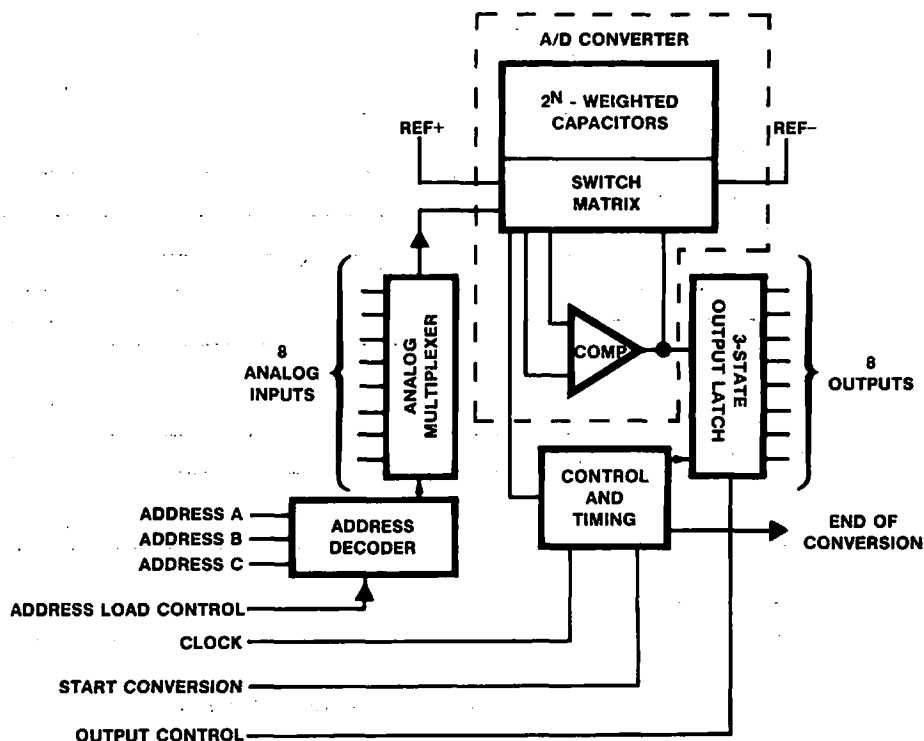


FIGURE 1
Block diagram of the Si520 Data Conversion System

CIRCUIT DESCRIPTION

Figure 1 shows a block diagram of the Si520. Address inputs A, B, and C allow selection of the 8 channels of the multiplexer. Each channel has a single-ended input which has an analog range from $-REF$ to $+REF$, giving a conversion range from 3 to 6.5 Volts. Note that only a 5 Volt VCC and $+REF$ will allow TTL compatibility. The $-REF$ input allows separation of analog and digital grounds which helps to keep noise spikes that might be present on the digital system ground from affecting the accuracy of the analog input to the Si520. The eight tri-state data outputs provide the data to the microprocessor. A 200 kHz square wave signal is needed for the CLOCK input. The OUTPUT CONTROL (OC), START CONVERSION (START), and ADDRESS LOAD CONTROL (ALC) provide the means for the microprocessor to control the Si520. The END OF CONVERSION (EOC) output goes high when the conversion is finished and when the output is available at the data pins. Figure 2(a) shows the pin diagram of the Si520, and Figure 2(b) gives the relationship of the input and output signals of the data acquisition system.

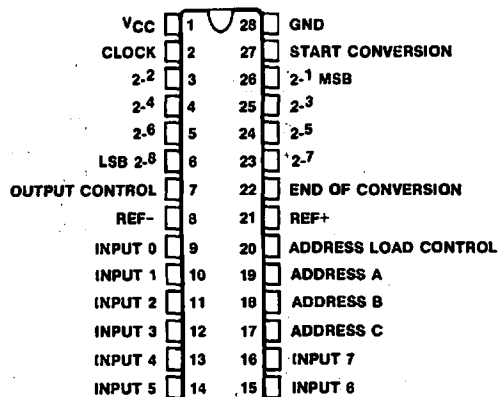


FIGURE 2(a)
Pin Diagram of the Si520 8 channel Data Acquisition System

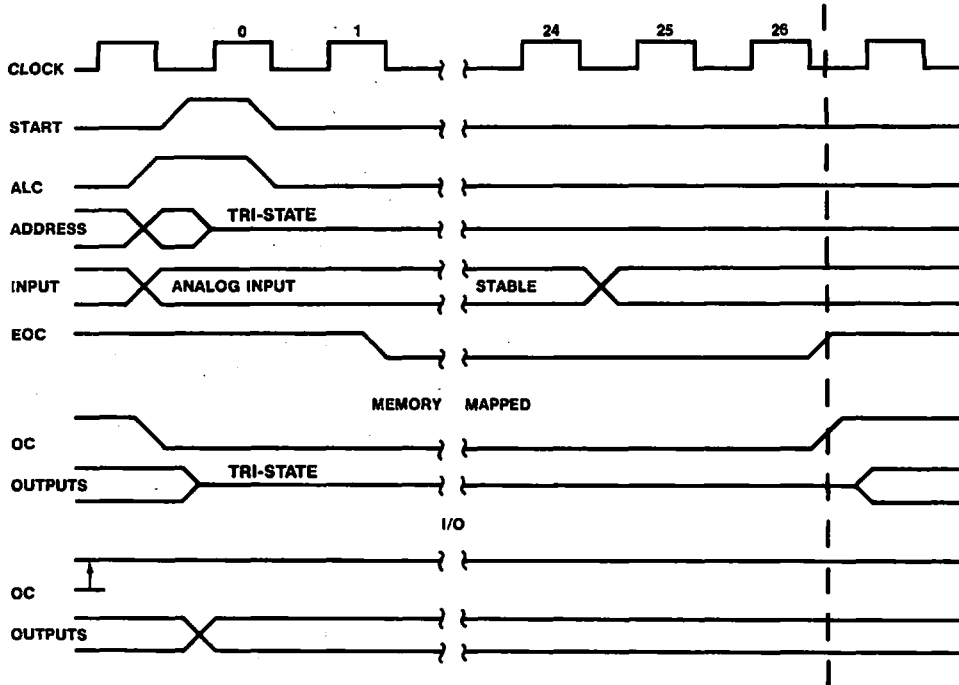


FIGURE 2(b)
Timing diagram of the SI520 Data Acquisition System

I/O OPERATION

In the I/O mode, the Si520 is in a free-running loop; the data outputs of the A/D converter are always enabled. The data outputs and address inputs of the data acquisition system are connected to the I/O port, and the START input is tied to the EOC line so that the system is constantly measuring the selected input channel (see Figure 3). The

data handling is then accomplished by a machine language program that reads in the converted data and processes it in whatever way desired by the user. The data transfer is verified in the program by checking the EOC pin for data stability before accepting the next input

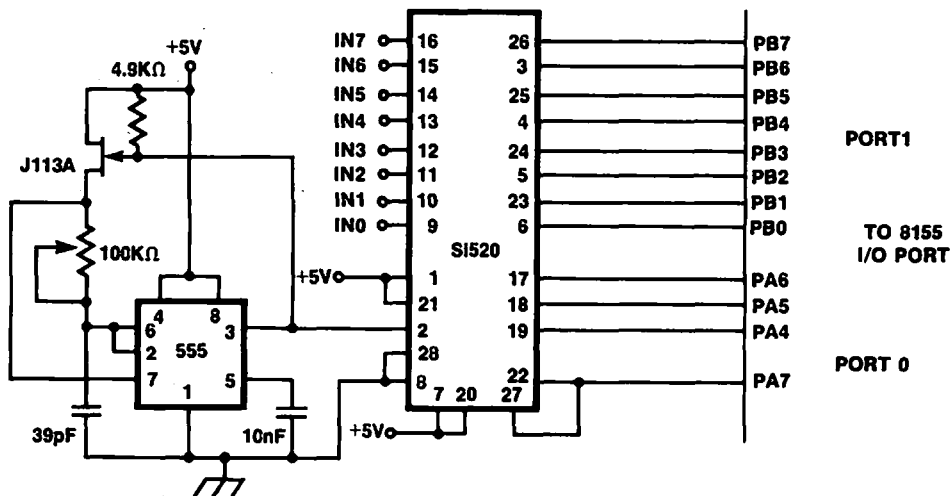


FIGURE 3
Schematic diagram of the I/O version of the SI520 interface

MEMORY MAPPED OPERATION

When operating in the memory mapped mode, the data outputs and address inputs are tied directly to their corresponding busses. The OC, START, and ALC lines are used to tri-state the Si520 when appropriate. Figure 4 shows the schematic diagram of the memory mapped data acquisition system. Note the A15 is the only address decoding line used for this example. To eliminate memory map redundancy, a more sophisticated address decoding circuit would be needed. The NOR gates of the 4001 combine the address decoding, READ, and WRITE signals to control the

The I/O oriented programs are shown in Tables 1 (a) and 1 (b). Table 1 (a) shows a simple routine that reads in and displays a single channel selected by the data stored at location 20A0H. The program in Table 1 (b) reads each of the channels and displays them for approximately 1/3 second each. Since the I/O system is constantly running, the EOC pin is monitored by the program, and data is only taken if EOC is high (data is valid).

The memory mapped system must be started when a reading is desired. This is done in Tables 2 (a) and 2 (b) by

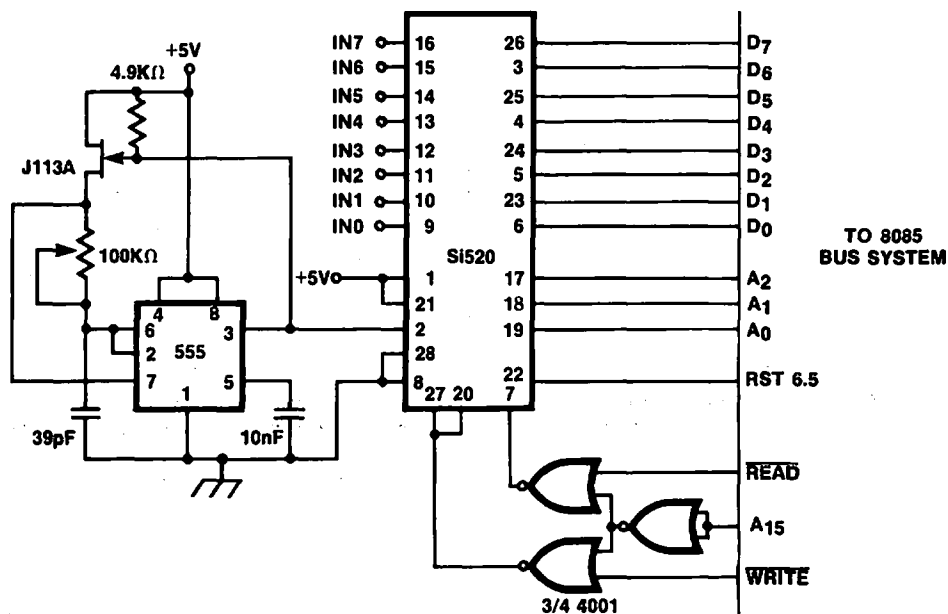


FIGURE 4
Schematic diagram of the memory mapped version of the SI520 interface

data acquisition system. The EOC pin is tied to RST 6.5 of the 8085 to notify the microprocessor when the conversion has been completed and when the data outputs are ready to be read.

SOFTWARE

The software shown here was written for use with the Intel SDK-85 development system monitor with the 8 channels of the Si520 memory mapped at 8000H-8007H and I/O mapped through ports 0 and 1. The UPDDT and UPDAD routines are used to display the contents of the A, D, and E registers. Both programs are written in subroutine form so they can be utilized by more than one calling program. If data storage or comparison is desired, minor changes or additions to the software shown here will be necessary.

writing to the desired memory location, which starts the conversion. The EOC line signals an interrupt for the microprocessor, making it jump to the READ subroutine and then return back to the main program. Table 2 (a) uses the H and L registers to point to the desired channel and then displays the reading from that channel. Table 2(b) reads all 8 channels and displays each one for approximately 1/3 second.

Note the asterisks in Table 1 (a) and 2(a). These mark the locations where the desired input channel is selected. Figure 5 gives the locations of the channels in both the I/O and memory mapped configurations.

TABLE 1 (a)

Program for reading one channel
of the SI520 in the I/O configuration

	ADDRESS	MNEMONIC	OP-CODE	COMMENTS
Calling Program	2000	LXI SP, 20C2H	31 C2 20	Load stack pointer
	2003	LXI H, 20A0H	21 A0 20	Reserve location for channel selector
	2006	MVI M, 00H*	36 00	Load channel selector with desired input
	2008	MVI A, 00H	3E 00	Set up data direction registers for I/O ports
	200A	OUT 03	D3 03	
	200C	MVI A, 7FH	3E 7F	
	200E	OUT 02	D3 02	
	2010	CALL READ	CD 16 20	Read the I/O port
	2013	JMP 2003H	C3 03 20	Start over
Subroutine READ	2016	MOV A, M	7E	Start conversion
	2017	OUT 00	D3 00	
	2019	IN 00	0B 00	Check to see if conversion is finished, if done, read in data
	201B	RLC	07	
	201C	JNC 2019H	D2 19 20	
	201F	IN 01	0B 01	Read in data
	2021	CALL UPDDT	CD 6E 03	Display data
	2024	RET	C9	Return

TABLE 1 (b)

Program for reading all 8 channels
of the SI520 in the I/O configuration

	ADDRESS	MNEMONIC	OP-CODE	COMMENTS
Calling Program	2000	LXI SP, 20C2H	31 C2 20	Load stack pointer
	2003	LXI H, 20A0H	21 A0 20	Reserve location for channel selector
	2006	MVI M, 00H	36 00	Load channel selector with desired input
	2008	MVI A, 00H	3E 00	Set up data direction registers for I/O ports
	200A	OUT 03	D3 03	
	200C	MVI A, 7FH	3E 7F	
	200E	OUT 02	D3 02	
	2010	CALL READ	CD 16 20	Read the I/O port
	2013	JMP 2003H	C3 03 20	Start over
Subroutine READ	2010	MOV A, M	7E	Start conversion
	2011	PUSH PSW	F5	
	2012	OUT 00	D3 00	
	2014	IN 00	0B 00	Check to see if conversion is finished, if done, read in data
	2016	RLC	07	
	2017	JNC 2014H	D2 14 20	
	201A	IN 01	0B 01	Read in data
	201C	CALL UPDDT	CD 6E 03	Display data
	201F	POP PSW	F1	Restore channel selector
	2020	SUI 70H	D6 70	Check to see if all channels have been read, if not, keep going
	2022	JZ 2029H	CA 29 20	
	2025	INR M	34	Increment channel selector
	2026	JMP 2010H	C3 10 20	Read next channel
	2029	RET	C9	Return

TABLE 2 (a)

Program for reading one channel
of the SI520 in the memory mapped configuration

	ADDRESS	MNEMONIC	OP-CODE	COMMENTS
Subroutine BGNCNVSN	2000	MOV M, A	77	Start conversion
	2001	MVI A, 0CH	3E 0C	Enable the interrupt system
	2003	SIM	30	
	2004	EI	FB	
	2005	EXI D, 0FFFFH	11 FF FF	Delay while conversion takes place
	2008	CALL DELAY	CD F1 05	
	2008	RET	C9	Return
Subroutine READ	2010	MOV A, M	7E	Read in results of the conversion
	2011	CALL UPDDT	CD 6E 03	Display the results
	2014	RET	C9	Return
Calling Program	2020	LXI SP, 20C2H	31 C2 20	Load stack pointer
	2023	LXI H, 6000H*	21 00 60	Load channel selector
	2026	CALL BGNCNVSN	CD 00 20	Start conversion
	2029	LXI D, 0FFFFH	11 FF FF	Delay between readings for approximately 1/3 second.
	202C	CALL DELAY	CD F1 05	
	202F	JMP 2023H	C3 23 20	Repeat

TABLE 2 (b)

Program for reading all 8 channels
of the SI520 in the memory mapped configuration

	ADDRESS	MNEMONIC	OP-CODE	COMMENTS
Subroutine BGNCNVSN	2000	MOV M, A	77	Start conversion
	2001	MVI A, 0CH	3E 0C	Enable the interrupt system
	2003	SIM	30	
	2004	EI	FB	
	2005	LXI D, 0FFFFH	11 FF FF	Delay while conversion takes place.
	2008	CALL Delay	CD F1 05	
	2008	RET	C9	Return
Subroutine READ	2010	MOV A, M	7E	Read in results of the conversion
	2011	CALL UPDDT	CD 6E 03	Display the results
	2014	RET	C9	Return
Calling Program	2020	LXI SP, 20C2H	31 C2 20	Load stack pointer
	2023	LXI H, 8000H	21 00 80	Load channel selector
	2026	PUSH H	E5	Save channel selector
	2027	CALL BGNCNVSN	CD 00 20	Start conversion
	202A	POP H	E1	Restore channel selector
	202B	MOV A, L	7D	Check to see if all channels have been read, if they have, start over
	202C	SUI 07H	D6 07	
	202E	JZ 2023H	CA 23 20	
	2031	INR L	2C	Increment channel selector
	2032	JMP 2026H	C3 26 20	Go to next channel for a reading

INPUT CHANNEL	I/O LOCATION	MEMORY MAPPED LOCATION
0	00	8000H
1	10	8001H
2	20	8002H
3	30	8003H
4	40	8004H
5	50	8005H
6	60	8006H
7	70	8007H

FIGURE 5
Channel locations for the Si520 in both I/O and memory mapped configurations

CONCLUSION

The Si520 Data Acquisition System features built-in multi-channel capability with easy interface to most microprocessor systems. The 8085 is just one example of how this system can be constructed using only an external clock

circuit and the Si520. It has a 70 μ S conversion time and extremely low power consumption which makes it ideal for battery powered monitoring of multiple parameters or conditions in the field.

A SIMPLE APPROACH TO Si7135/8085 INTERFACING

By Doyle L. Slack
December 1983

INTRODUCTION

Many A/D conversion designs in use today are both complex and confusing, and for these reasons, they are often overlooked for use in more simple applications. Up to now, many Analog-to-Digital (A/D) converter chips have not been microprocessor compatible; the interfacing schemes to make them so have been unnecessarily complicated. But now a simple, straightforward A/D converter can be constructed using only the Siliconix Si7135 and one other IC. It can be easily interfaced to most machine level or high level language computer systems using I/O ports. This system would be ideal for remote/field monitoring or storage of slowly changing conditions with minimum maintenance requirements.

CIRCUIT COMPONENTS

The Siliconix Si7135 IC is a $4\frac{1}{2}$ digit integrating A/D converter intended for use as a digital volt meter (DVM) chip. Using the dual slope method of conversion, it can achieve an accuracy of ± 1 count in 20,000. Some of the other features are overrange, underrange, and polarity indications, allowing autoranging and a measurement range of -1.9999 volts to $+1.9999$ volts. At the optimum clock rate of 120 kHz, approximately 3 conversions per second are possible. Figure 1 gives the pin diagram of the Si7135.

The other half of the A/D system is the Intel 8085 microprocessor—an inexpensive 8-bit general purpose Central Processing Unit (CPU) that can be operated with a minimum of peripheral devices. With its internal clock circuitry, the only external devices needed to make a working system are address demultiplexing, I/O ports, and memory. The latter two are supplied by the Intel 8155 RAM-I/O and 8755 EPROM-I/O chips. By connecting the data and control lines of the Si7135 A/D system to the I/O lines of the microprocessor system, the data can be read and processed in whatever way the user chooses via software.

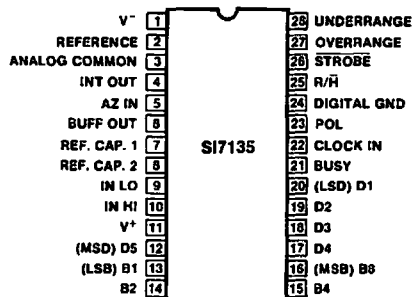


Figure 1
Pin diagram of the Si7135 $4\frac{1}{2}$ digit A/D converter.

CIRCUIT DESCRIPTION

Figure 2 shows the schematic diagram of the Si7135 A/D converter circuit connections to an Intel 8085 microprocessor system. The Si7135 outputs are straightforward in their functions. The **OVERRANGE** output goes to a logic 1 when an overrange condition (down count exceeds 20,000) has occurred on the previous measurement. The **UNDERRANGE** output goes to a logic 1 when the input measurement is less than 10% of full scale. The **POLARITY** output goes high for positive readings and goes low for negative signals. **RUN/HOLD** is the only control signal from the microprocessor and can be used to stop the measurement cycle of the 7135 and hold the last reading for as long as the line is held low. The other direct outputs from the Si7135 are the data lines which provide the data in BCD format for each of the 5 digits. The tricky part of the interface is the digit strobe decoding circuitry between the A/D converter and the microprocessor.

Figure 3 gives a simplified timing diagram of the A/D system. When the Si7135 **BUSY** line (PA7) goes high, either the

data from the last reading is valid or the **OVERRANGE** line (**PBO**) is high. If an overrange is indicated, the microprocessor displays OL and waits for the next reading. If the data is valid, each of the digit drive signals from the Si7135 goes high one at a time, sequencing from D5 to D1 repeatedly. The 4532 priority encoder condenses the 5 digit drive signals into 3 bits (PA4-PA6) which are combined with **BUSY** to make up the upper nibble of the input data. The BCD data lines (PA0-PA3) make up the lower nibble, and the BCD data presented corresponds to the digit drive that is high at the time. This byte, containing both status and data information, is read by the microprocessor. The status information is decoded, and the port is read again to verify the data for the particular digit being input. After the entire voltage reading has been input, the **POLARITY** line (**PB1**) is checked, and the reading and polarity are displayed by the microprocessor. The system then waits for the next conversion. For more details on how the microprocessor handles the data, see **SOFTWARE**.

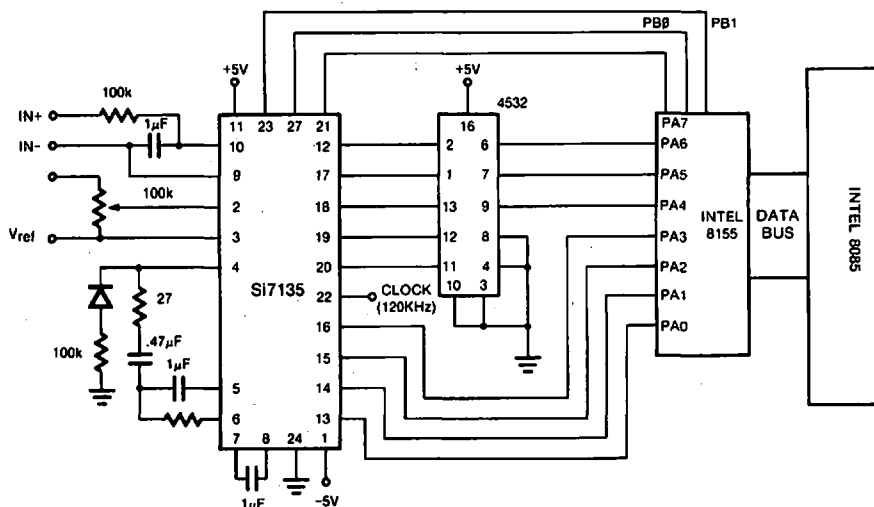


Figure 2
Schematic diagram of the Si7135 to 8085 system interface.

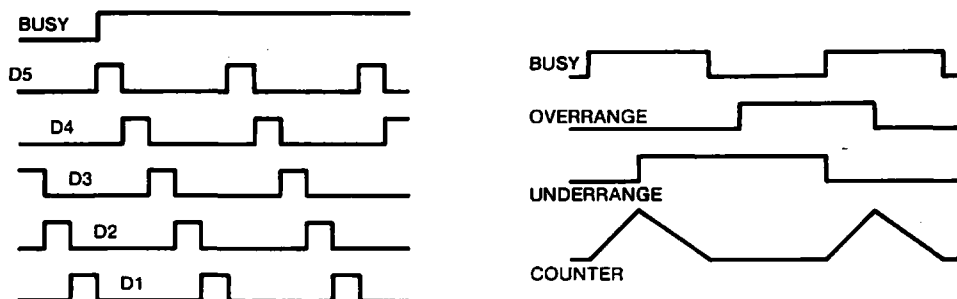


Figure 3
Timing diagram of the Si7135 A/D conversion system.

MULTIPLEXING SI7135 SYSTEMS

It would be desirable to be able to monitor more than one analog signal at a time, since often several different events or conditions of interest occur simultaneously. Since the conversion time of integrating converters is relatively slow, the outputs of several A/D converters can be multiplexed without the loss of time that multiplexing the inputs of a single A/D converter entails. The Si7135 system lends itself to this type of use very easily without tying up a large number of additional I/O lines. By multiplexing the outputs of each of the A/D converters, many inputs can be monitored with little additional hardware.

Figure 4(a) shows how the A/D converter systems can be

multiplexed quite simply by using tri-state buffers. The RUN/HOLD line of the desired converter is pulled low when a reading is needed from that particular A/D system. The buffers for that system are then enabled, and the data from the Si7135 is read in the same manner as before. The RUN/HOLD line is then sent high, and the other converters are read sequentially in the same way. This method uses only two extra I/O lines and two 4503 buffer chips for each additional A/D converter added to the system. Figure 4(b) shows a detailed schematic of 1/3 of the multiplexed system. Each section that is added to the system is wired identically and connected to the I/O bus.

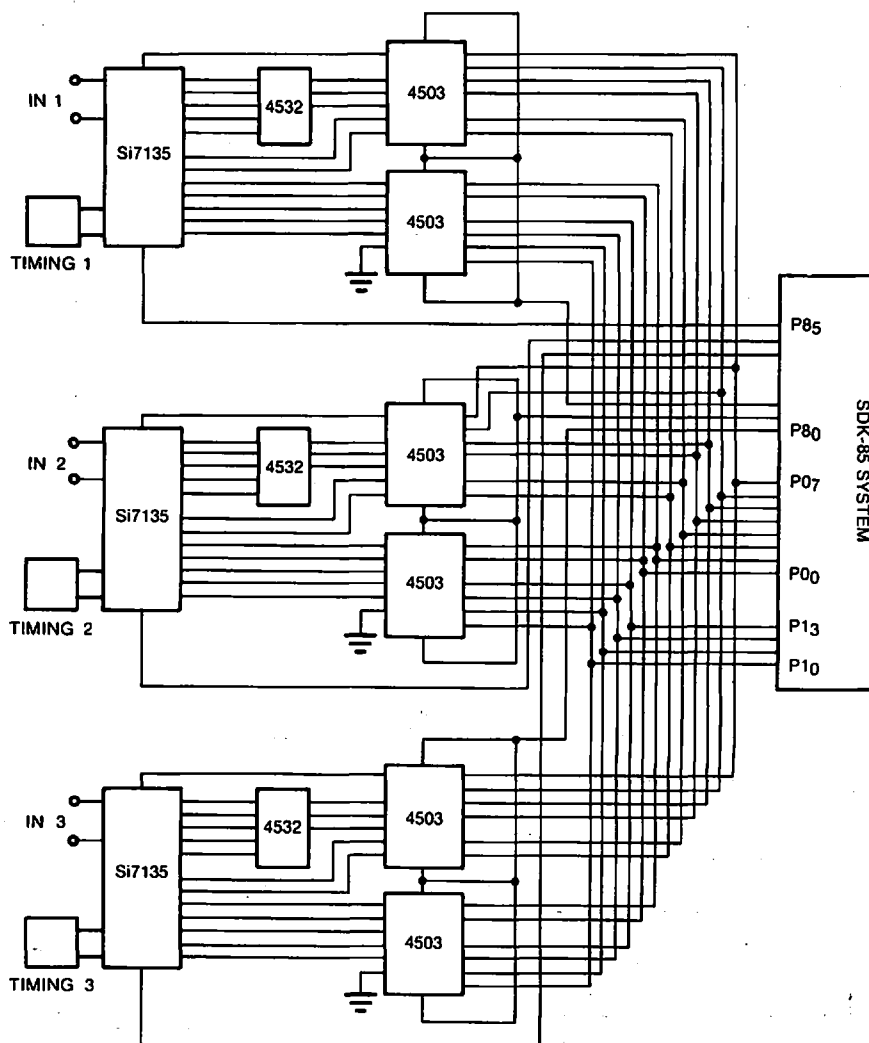


Figure 4 (a)
Schematic diagram of the multiplexed Si7135 A/D converter system.

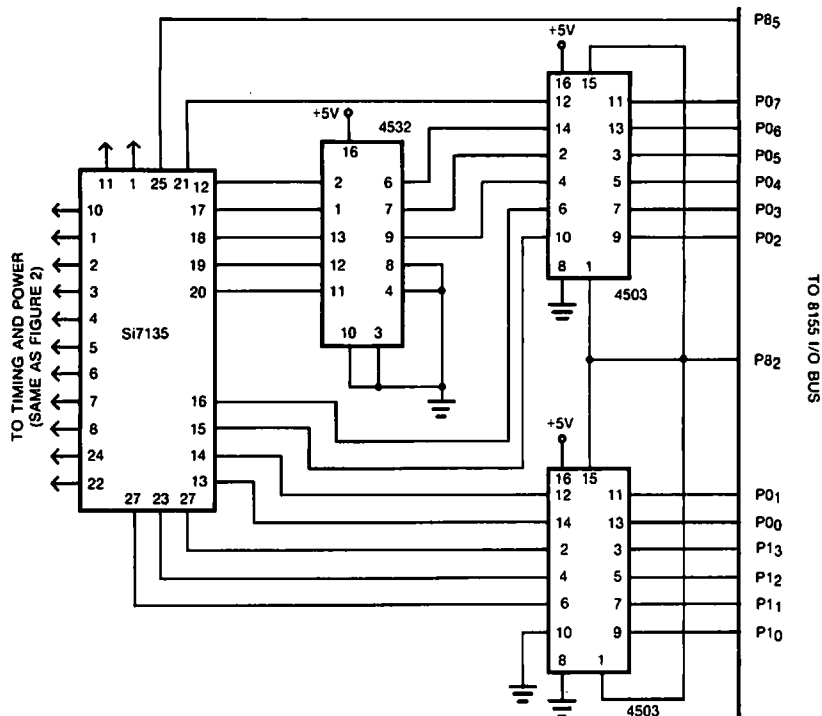


Figure 4 (b)

Schematic diagram of 1/3 of the multiplexed A/D system shown in Figure 4 (a) including pin diagrams of the components.

SOFTWARE

The software used to read the data from the Si7135 system is shown in Table 1 along with comments on what each command does. This software was written for the Intel SDK85 monitor. The UPDAD and UPDDT subroutines display the data by writing to the 8279 display controller. The OUTPT subroutine outputs the data stored at the location pointed to by the H and L registers. Only minor changes or additions to the software shown here would be required to store large amounts of readings or read several different inputs simultaneously. Also, this program does not utilize the RUN/HOLD or UNDERRANGE lines.

Table 1.
Program for reading in and displaying
the data from the Si7135 A/D converter system.

ADDRESS	MNEMONIC	OP-CODE	COMMENTS				
2000	LXI SP, 20C2H	31 C2 20	Load stack pointer	2014	IN 01	0B 01	Check for OVERRANGE if
2003	MVI A, 00H	3E 00	Set up data direction	2016	RRC	0F	not, continue with
2005	OUT 02	D3 02	registers for I/O ports	2017	JNC 203AH	D2 3A 20	reading
2007	MVI A, 08H	3E 08		201A	MVI A, 01H	3E 01	Output 01 to display
2009	OUT 03	D3 03		201C	MVI B, 00H	06 00	
200B	IN 00	DB 00	Check for BUSY; if	201E	LXI H, 2082H	21 82 20	
200D	ANI 80H	E6 80	not, wait	2021	CALL OUTPT	CD B7 02	
200F	SUI 80H	D6 80		2024	MVI A, 00H	3E 00	
2011	JNZ 200BH	C2 0B 20		2026	MVI B, 00H	06 00	
				2028	LXI H, 2084H	21 84 20	
				202B	CALL OUTPT	CD B7 02	
				202E	IN 00	DB 00	Wait for next measure-
				2030	ANI 80H	E6 80	ment cycle
				2032	SUI 80H	D6 80	
				2034	JZ 202EH	CA 2E 20	
				2037	JMP 200BH	C3 0B 20	Return
				203A	MVI B, 0D0H	06 0D	Set pointer to value of
							first strobe
				203C	CALL DIGIT	CD A0 20	Get first digit and put it
				203F	MOV D, A	57	in the proper register
				2040	MVI B, 0C0H	06 C0	Set pointer to value of
							second strobe
				2042	CALL DIGIT	CD A0 20	Get second digit and put
				2045	RLC	07	it in the proper register
				2046	RLC	07	
				2047	RLC	07	
				2048	RLC	07	
				2049	MOV E, A	5F	
				204A	MVI B, 0B0H	06 B0	Set pointer to value of
							third strobe
				204C	CALL DIGIT	CD A0 20	Get third digit and put it
				204F	ADD E	83	with the second digit
				2050	MOV E, A	5F	
				2051	MVI B, 0A0H	06 A0	Set pointer to value of
							fourth strobe

Table 2
Program for reading in and displaying
the data from the multiplexed SI7135 A/D converter system.

				ADDRESS	MNEMONIC	OP-CODE	COMMENTS
2053	CALL DIGIT	CD A0 20	Get fourth digit and put it in the proper register				
2056	RLC	07		2080	LXI SP, 20C2H	31 C2 20	Load stack
2057	RLC	07					
2058	RLC	07		2083	MVI A, OFFH	3E FF	Set up data direction registers for I/O ports
2059	RLC	07		2085	OUT 0A	D30A	
205A	MOV C, A	4F		2087	OUT 08	D3 08	
205B	MVI B, 90H	06 90	Set pointer to value of fifth strobe	2089	MVI A, 00H	3E 00	
				208B	OUT 02	D3 02	
				208D	OUT 03	D3 03	
205D	CALL DIGIT	CD A0 20	Get fifth digit and put it with the fourth digit	208F	MVI A, 0DFH	3E DF	Hold present
2060	ADD C	81		2091	MVI B, 0DBH	06 DB	A/D converter
2061	PUSH PSW	F5	Save the lowest two digits	2093	OUT 08	DB 08	
				2095	RRC	0F	Set pointer to next A/D converter
2062	CALL UPDAD	CD 63 03	Display the upper three digits				
2065	POP PSW	F1	Restore the lowest two digits	2096	PUSH PSW	F5	Save pointer data
				2097	LXI D, 0A700H	11 00 A7	Delay for 1/3 second
2066	CALL UPDDT	CD 6E 03	Display the lowest two digits	209A	CALL DELAY	CD F1 05	
				209D	MOV A, B	78	Enable buffers
2069	IN 01	DB 01	Check polarity bit for positive or negative sign	209E	OUT 08	D3 08	
206B	ANI 02H	E6 02		20A0	RRC	0F	Set enable to next A/D converter
206D	SUI 02H	D6 02		20A1	MOV B, A	47	
206F	JNZ 207AH	C2 7A 20		20A2	PUSH B	C5	Save enable data
2072	MVI A, OFFH	3E FF	Blank the polarity position.	20A3	CALL READ	CD 00 20	Read data from A/D converter
2074	STA 1800H	32 00 18					
2077	JMP 202EH	C3 2E 20	Return	20A6	POP B	C1	Restore enable data
207A	MVI A, 0FBH	3E FB	Put a minus sign in the polarity position	20A7	RLC	07	Check if all A/D converters have been read
207C	STA 1800H	32 00 18		20A8	RRC	0F	
207F	JMP 202EH	C3 2E 20	Return	20A9	JC 2080H	DA B0 20	
2082	data	00		20AC	POP PSW	F1	Restore pointer data
2083	data	11		20AD	JMP 208FH	C3 8F 20	Return
2084	data	15		20B0	POP PSW	F1	Clear the stack
2085	data	15		20B1	JMP 2093H	C3 93 20	Start over
2086	data	15					
2087	data	15					
Subroutine DIGIT				Subroutine READ			
20A0	IN 00	DB 00	Read port	2000	IN 01	DB01	Check for OVERRANGE if not, continue with reading
20A2	ANI 0F0H	E6 F0	Mask lower byte of data	2002	RRC	0F	
20A4	SUB B	90	Compare byte to pointer, if not equal then wait	2003	JNC 201AH	D2 1A 20	Output 0L to display
20A5	JNZ 20A0H	C2 A0 20		2006	MVI A, 01H	3E 01	
20A8	IN 00	DB 00	Read port	2008	MVI B, 00H	06 00	
20AA	ANI 0FH	E6 0F	Mask upper byte of data	200A	LXI H, 2062H	21 62 20	
20AC	RET	C9	Return	2000	CALL OUTPT	CD 87 02	
				2010	MVI A, 00H	3E 00	
				2012	MVI B, 00H	06 00	
				2014	LXI H, 2064H	21 64 20	
				2017	CALL OUTPT	CD 87 02	
				201A	MVI B, 000H	06 00	Set pointer to value of first strobe
				201C	CALL DIGIT	CD 70 20	Get first digit and put it in the proper register
				201F	MOV D, A	57	
				2020	MVI B, 0C0H	06 C0	Set pointer to value of second strobe
				2022	CALL DIGIT	CD 70 20	Get second digit and put it in the proper register
				2025	RLC	07	
				2026	RLC	07	
				2027	RLC	07	
				2028	RLC	07	
				2029	MOV E, A	5F	
				202A	MVI B, 080H	06 B0	Set pointer to value of third strobe
				202C	CALL DIGIT	CD 70 20	Get third digit and put it with the
				202F	ADD E	83	
				2030	MOV E, A	5F	Second digit
				2031	MVI B, 0A0H	06 A0	Set pointer to value of fourth strobe

This program was written to run by itself on the Intel SDK85 system. However, if the A/D converter routine is to be used as a subroutine of another program, the starting address of the subroutine should be changed to 2003H, or NO-OPs (00) should be placed in locations 2000-2002H to eliminate unintentional resetting of the stack pointer. Also, RET (C9) should replace the JUMP instructions at address locations 2037H and 207FH. The instructions at locations 202EH through 2037H should be deleted.

If multiple A/D units are to be connected to the microprocessor, a routine like the one shown in Table 2 would work well. The program shown in Figure 5 has been modified and named READ for this example, and ports 0, 1, and 8 of the SDK85 system are used for the data transfer.

2033	CALL DIGIT	CD 70 20	Get fourth digit and put it in the proper register	Subroutine DIGIT		
2036	RLC	07		2070	IN 00	DB 00
2037	RLC	07				Read port
2038	RLC	07		2072	ANI 0F0H	E6 F0
2039	RLC	07				Mask lower byte of data
203A	MOV C, A	4F		2074	SUB B	90
						Compare byte to pointer, if not equal then wait
203B	MVI B, 90H	06 90	Set pointer to value of fifth strobe	2075	JNZ 2070H	C2 70 20
203D	CALL DIGIT	CD 70 20	Get fifth digit and put it with the fourth digit	207B	IN 00	DB 00
2040	ADD C	81				Read port
2041	PUSH PSW	F5	Save the lowest two digits	207A	ANI 0FH	E6 0F
						Mask upper byte of data
2042	CALL UPDAD	CD 63 03	Display the upper three digits	207C	RET	C9
						Return
2045	POP PSW	F1	Restore the lowest two digits			
2046	CALL UPDDT	CD 6E 03	Display the lowest two digits			
2049	IN 01	DB 01	Check polarity bit for positive or negative sign			
204B	ANI 02H	E6 02				
204D	SUI 02H	D6 02				
204F	JNZ 205AH	C2 5A 20				
2052	MVI A, 0FFH	3E FF	Blank the polarity position			
2054	STA 1800H	32 00 18				
2057	RET	C9	Return			
205A	MVI A, 0FBH	3E FB	Put a minus sign in the polarity position			
205C	STA 1800H	32 00 18				
205F	RET	C9	Return			
2062	data	00				
2063	data	11				
2064	data	15				
2065	data	15				
2066	data	15				
2067	data	15				

CONCLUSION

The Siliconix Si7135 is an inexpensive, simple integrated circuit that can solve the problems associated with a design that is far too complex for the job it is intended to do. Note that the Intel 8085 is not the only microprocessor one could interface to the Si7135. This scheme is easily adaptable to other microprocessor architectures. However it is also important to know that the comparatively slow conversion time makes multiplexing of several Si7135's to one microprocessor more practical than multiplexing the inputs to a single Si7135. With multiplexed converters, a fast, easy method of data acquisition can be achieved for a reasonable price.

Si8021 DIGITAL-TO-ANALOG CONVERTER INTERFACE FOR MICROPROCESSOR SYSTEMS

By Doyle L. Slack
December 1983

INTRODUCTION

The Siliconix Si8021 is a CMOS 12-bit multiplying Digital-to-Analog Converter (DAC) with byte addressable input latches. Utilizing low-drift compatible thin-film R-2R ladder and full-scale/offset resistors on chip for stable and linear operation over a wide temperature range, the Si8021 is capable of full four-quadrant multiplication. The control inputs of the DAC are level triggered, allowing transparent operation if desired. The digital inputs are designed to allow easy interface to microprocessor systems, and its control logic arrangement makes the Si8021 ideal when minimum microprocessor dedication to perform the conversion function is required. In this application, the Si8021 is interfaced to an 8085 microprocessor system to demonstrate the ease of interfacing and simple software requirements.

CIRCUIT DESCRIPTION

Figure 1 is a block diagram of the Si8021. Each nibble of the 12-bit input has a latching input register to hold the data until conversion occurs. The latching and conversion operations are synchronized by the control logic circuitry which includes the strobe inputs (LBE, MBE, HBE), LDAC and $\overline{CE}$. Figure 2 depicts the control operations, and Figure 3 shows the timing diagram for the Si8021. If one of the strobe inputs goes high while $\overline{CE}$ is low, the data present at the corresponding input register is loaded. When either the strobe goes low or the $\overline{CE}$ line returns high, the data is latched. When the LDAC line is brought high, the DAC register loads the information held in the input registers, and the 12-bit DAC starts the conversion process.

The low capacitance current outputs I_{01} and I_{02} are

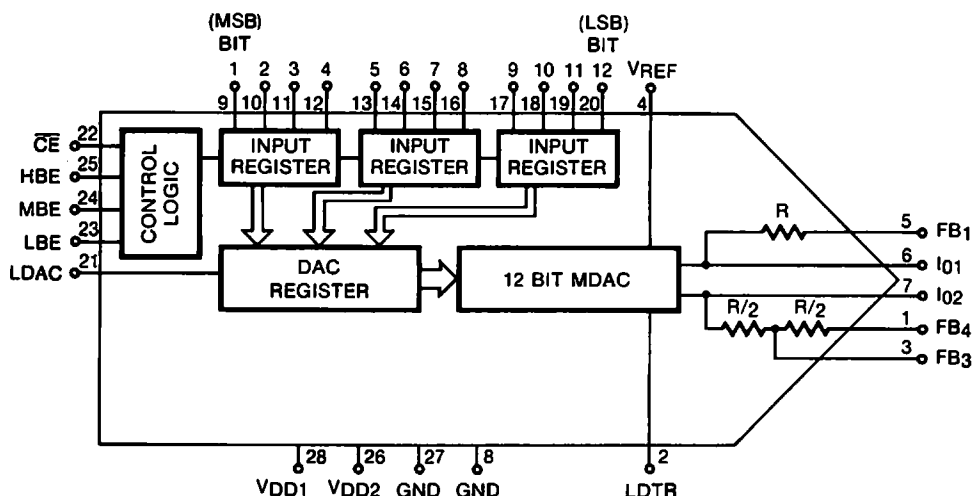


Figure 1
Block diagram of the Si8021 Digital-to-Analog Converter (DAC).

designed to drive the inputs of high speed op-amps for faster settling times and greater bandwidth while the feedback lines (FB1, FB3, FB4) help stabilize the output gain by providing an internal precision feedback resistor network which promotes low gain drift. The multiplying action of the Si8021 produces an output equal to V_{ref} times the ratio of the digital input to the full-scale digital value. The V_{ref} pin allows selection of the full-scale output voltage for the maximum digital input and can accept either an AC or DC signal. The importance of this is that an AC signal can be introduced through the V_{ref} pin, and the analog output will be the AC signal times whatever attenuation factor is supplied by the microprocessor. Another important fact is that V_{ref} cannot equal the op-amp supply voltages if maximum linearity is desired, due to the inability of most op-amps to swing all the way to the power

supply rails. Figure 4 illustrates the pin diagram of the Si8021.

CIRCUIT OPERATION

Figure 5 demonstrates how the Si8021 can be connected to any 8-bit microprocessor system. The address decoding circuitry can be as simple as a single address line or as complex as a collection of logic gates required to reduce the number of memory map redundancies. The $\overline{WR}$ line of the microprocessor is tied to the $\overline{CE}$ line of the Si8021 so that a memory-write operation to the appropriate address triggers the desired operation. High speed op-amps must be used on the outputs if fast settling time and/or high bandwidth are desired. Also, good grounding of the entire system is essential for proper operation.

Figure 6 and 7 show how the Si8021 can be connected to an 8085 microprocessor system. The SDK-85 microprocessor trainer was used to test the interface to the Si8021. The two possible output modes for the Si8021 are unipolar and bipolar. The unipolar configuration allows analog output swings of 0 volts to $-V_{ref}$ as shown in Figure 6. The bipolar configuration shown in Figure 7 allows the analog output to vary from V_{ref} to $-V_{ref}$. Note that the inverting action of the output op-amps for both circuits requires that the V_{ref} voltage for the Si8021 be negative for a positive full-scale analog output. The equations necessary to calculate the output voltage for any given digital input in either the unipolar or bipolar configurations are given in Figure 8.

Si8021 INPUTS					Si8021 OPERATION
HBE	MBE	LBE	LDAC	$\overline{CE}$	
0	0	1	0	0	LB data in
0	1	0	0	0	MB data in
1	0	0	0	0	HB data in
0	0	0	1	X	Start conversion
X	X	X	0	1	No operation

Figure 2
Control operation for the Si8021.

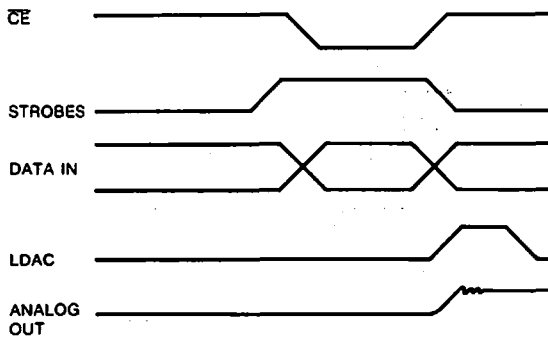


Figure 3
Timing diagram for the digital inputs of the Si8021

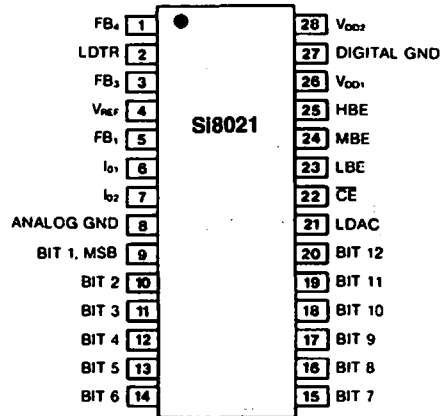


Figure 4
Pin diagram of the Si8021.

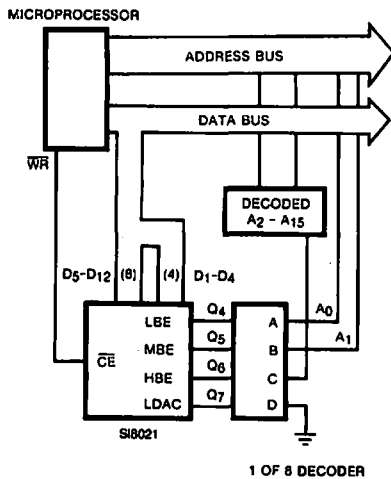


Figure 5
An example of microprocessor interfacing for the Si8021.

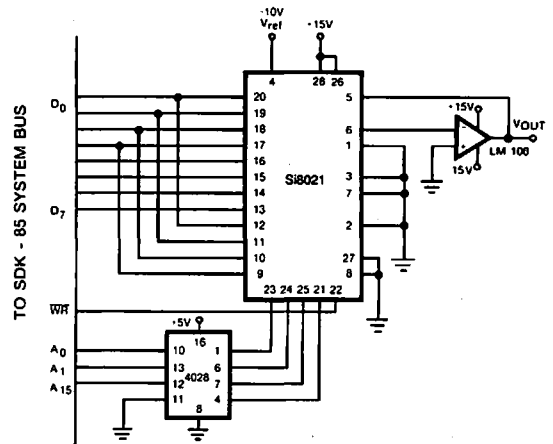


Figure 6
Schematic diagram of the SDK-85 interface for unipolar operation.*

*NOTE: The op-amps used in these circuits must have low offset to insure proper linearity. Also, inrush current for some op-amps may overload the current outputs. If this is a problem, Schottky diodes should be used to protect I₀₁ and I₀₂.

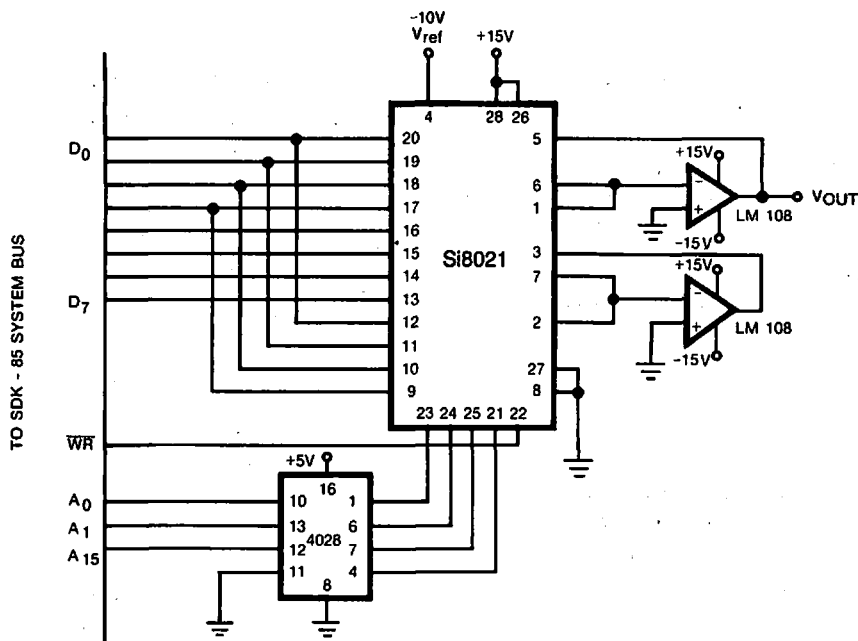


Figure 7
Schematic diagram of the SDK-85 interface for bipolar operation.*

*NOTE: The op-amps used in these circuits must have low offset to insure proper linearity. Also, inrush current for some op-amps may overload the current outputs. If this is a problem, Schottky diodes should be used to protect I_{O1} and I_{O2} .

UNIPOLAR OPERATION

$$V_{OUT} = -V_{ref} * (X/N)$$

BIPOLAR OPERATION

$$V_{OUT} = -[2V_{ref} * (X/N)]$$

where: X = decimal equivalent of the binary input

$$N = 2^{12} - 1 \text{ for 12 bit operation}$$

$$2^{11} - 1 \text{ for 11 bit operation}$$

$$2^{10} - 1 \text{ for 10 bit operation}$$

Figure 8
Equations for calculation of the analog outputs for unipolar and bipolar operation.

SOFTWARE

Basic I/O Programs

The software required to drive the systems shown in Figures 6 and 7 is quite simple since all that is required to access the Si8021 is a memory-write operation. Table 1 shows a program that will read digital data from memory (address locations 20A0H and 20A1H) and then output it to the DAC. The software was written for the SDK-85 system monitor, and the programming is the same for both the unipolar and bipolar configurations. The only difference is that for a given digital input, the output will vary between 0 volts and $-V_{ref}$ for the unipolar system and between V_{ref} and $-V_{ref}$ for the bipolar system.

Table 1.

Program for converting the contents of a memory location to an analog output.

ADDRESS	MNEMONIC	OP-CODE	COMMENTS
2000	LXI SP, 20C2H	31 C2 20	Initialize stack pointer
2003	LXI H, 20A0H*	21 A0 20	Set memory pointer
2006	MOV A, M	7E	Load high nibble
2007	STA 8002H	32 02 80	into DAC
200A	INX H	23	Increment memory pointer
200B	MOV A, M	7E	Load middle and low
200C	STA 8001H	32 01 80	nibbles into DAC
200F	STA 8000H	32 00 80	
2012	STA 8003H	32 03 80	Start conversion
2015	HLT	76	Halt

* The order of binary data for the conversion is:
 20A0H 20A1H
 XXX HHHH MMM LLL X = don't care

Function Generation

Another possible use for the Si8021 DAC is function generation. Table 2 shows how a simple variable frequency sawtooth signal could be generated. Again, the software for both configurations is the same.

With the Si8021 almost any function that can be approximated by the microprocessor system can be generated. The limiting factor of the system is the speed of the op amp. If the rate of the digital data is greater than the settling time of the op amp, the analog output will be distorted from the original digital input. Also, the sampling theorem states that the frequency of the samples used to reconstruct the analog signal must be at least twice the desired signal's maximum frequency component. Even with these restrictions, the Si8021 can reproduce signals well above the audio frequency range.

Table 2.

Program for generating a variable frequency sawtooth output.

ADDRESS	MNEMONIC	OP-CODE	COMMENTS
2000	LXI SP, 20C2H	31 C2 20	Load stack pointer
2003	LXI H, 0000H	21 00 00	Load function start point
2006	MOV A, L	7D	Output low nibble and
2007	STA 8000H	32 00 80	middle nibble to DAC
200A	STA 8001H	32 01 80	
200D	MOV A, H	7C	Output high nibble to
200E	STA 8002H	32 02 80	DAC
2011	STA 8003H	32 03 80	Start conversion
2014	PUSH H	E5	Save function counter
2015	LXI H, 20A0H*	21 A0 20	Get frequency constant
2018	MOV D, M	56	and move it to the D
2019	INX H	23	and E registers
201A	MOV E, M	5E	
201B	CALL DELAY**	CD FI 05	Delay for the period
			determined by the
			frequency constant
201E	POP H	E1	Restore function
201F	INX H	23	counter
2020	JMP 2006H	C3 06 20	Increment function
			counter
			Do it again

* The order for storing the frequency constant is:

20A0H - high byte
 20A1H - low byte

** This is an SDK-85 subroutine that counts down through the D and E register pair to generate a timed delay before resuming execution of the program.

CONCLUSION

Teaming up the Si8021 with any microprocessor system results in a simple, flexible, yet powerful conversion system which could be used for applications such as programmable power supplies, programmable variable attenuators, programmable amplifiers, and function generators. The basic block diagrams of these systems are shown in Figure 9 through 12. The simple software requirements of these circuits allow easy expansion or alteration of existing programming to include the new capabilities provided by the addition of the Si8021 to your computer system.

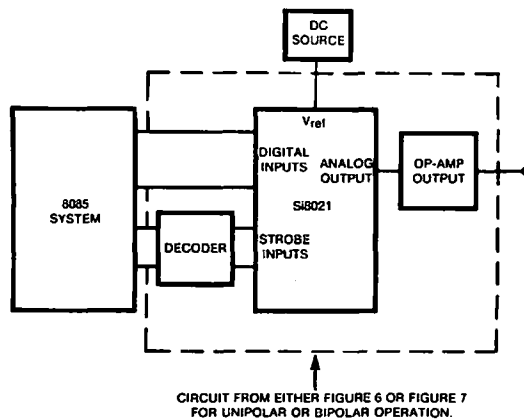


Figure 9
Block diagram of the Si8021/8085 programmable power supply.

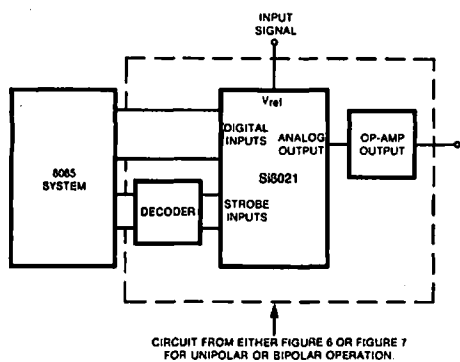


Figure 10
Block diagram of the Si8021/8085 programmable variable attenuator.

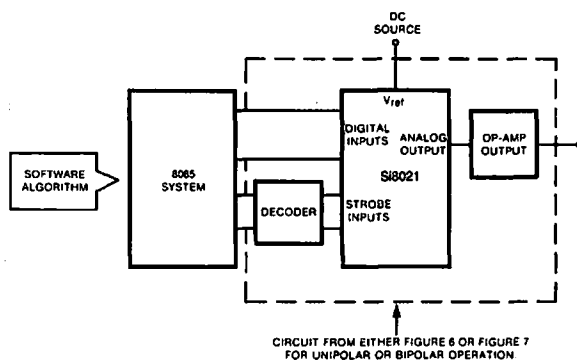


Figure 11
Block diagram of the Si8021/8085 function generator.

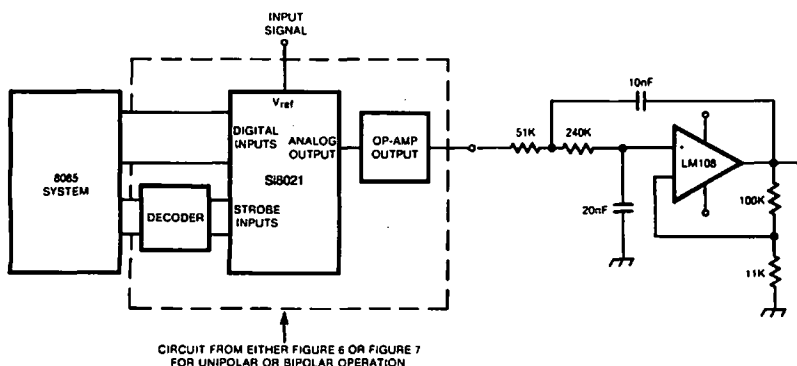


Figure 12
Block diagram for the Si8021/8085 programmable audio amplifier.

FUNCTION / APPLICATION OF THE L144 PROGRAMMABLE MICROPOWER TRIPLE OP AMP

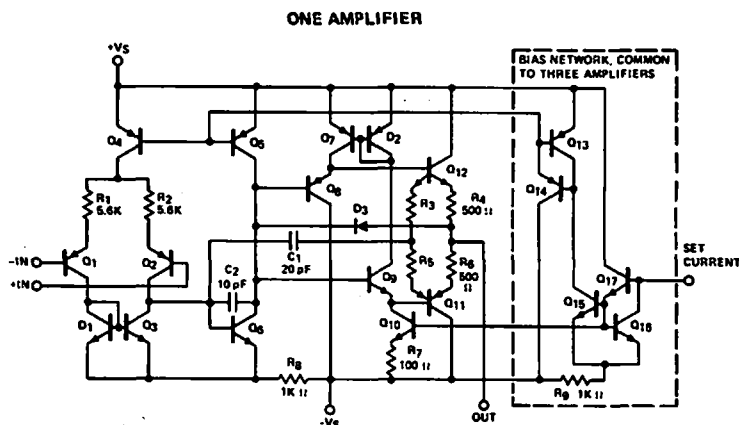
INTRODUCTION

The L144 is a monolithic triple operational amplifier circuit with an external programming feature for power dissipation and input bias current control. It finds application in RC active filters, instrumentation amplifiers, micropower comparators, and numerous general signal processing circuits. The L144 is a practical industry standard op amp wherever low current drain, low voltage, low power, or very small physical size are the controlling criteria.

This Application Note describes the L144, how to program it, what the effects of slew rate limiting are, and some practical circuit applications.

The L144 has three operational amplifiers programmed by one external current setting resistor. It operates from power

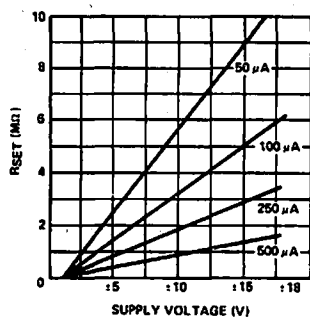
supplies ranging from ± 18 V to as low as ± 1.5 V with quiescent supply currents of from $10\text{ }\mu\text{A}$ to greater than 1 mA independent of supply voltage. The schematic shown in Figure 1 reveals a general-purpose PNP input transistor op amp with an outstanding difference. The master bias current is not set by an internal resistor strung from V^+ to V^- , but is brought out to an external pin. This allows the user to determine the operating currents of each stage through a system of current mirrors. Of special interest to the designer are the equal collector currents of Q_1 and Q_2 , which are derived from the output of Q_4 . These collector currents, divided by a beta of approximately 50, determine the input bias currents for each amplifier. The ratio between the set current and the collector current of Q_4 is unity, which allows one to program the input bias current simply by changing the set current input of the device.



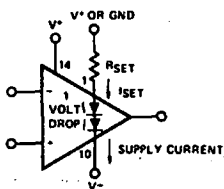
L144 Schematic
Figure 1

Input Bias Current and Supply Current

The relationship between supply current, supply voltage, and the setting resistor is shown in the graph and set current model of Figure 2. The two diodes of the set current model correspond to the base-emitter junctions of Q_{16} and Q_{17} .



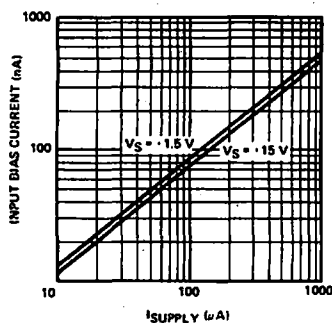
L144 SET CURRENT MODEL



Supply Current vs Bias Resistor and Supply Voltage
Figure 2

Figure 3 shows the essentially linear relationship between input bias current and total quiescent supply current for the L144. The low input bias currents at low supply current levels allow the L144 to maintain good input specifications even with the large feedback and load resistor values normally encountered in micropower applications.

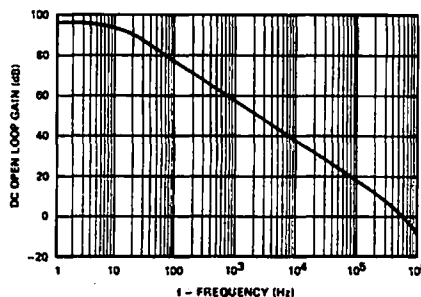
The slightly lower input bias currents at the higher supply voltages are due to the narrower base width and higher beta encountered at $V_S = \pm 15$ V.



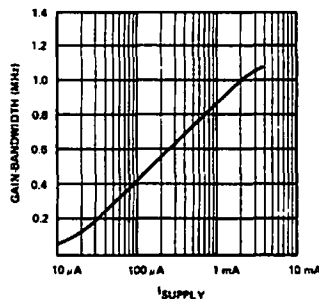
Input Bias Current vs Supply Current
Figure 3

Frequency Response

At the data sheet standard supply current of $250 \mu\text{A}$ the typical Bode plot is as shown in Figure 4. The low frequency gain of approximately 95 dB rolls into a uniform -20 dB/decade slope until after the 0 dB unity gain crossing point. The variation of open loop gain with temperature is typically -2 dB per 100°C of temperature rise. The 600 kHz unity gain crossover gives a gain bandwidth product (GBWP) of 600,000. Figure 5 shows the variation of GBWP with supply current.



L144 Open Loop Gain vs Frequency
Figure 4

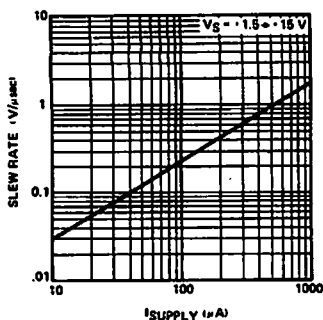


L144 Gain Bandwidth Product vs Supply Current
Figure 5

The vertical axis is linear whereas the horizontal I_{CC} axis is logarithmic, demonstrating that the GBWP does vary with I_{CC} , but at much less than the 1-to-1 ratio observed for other parameters.

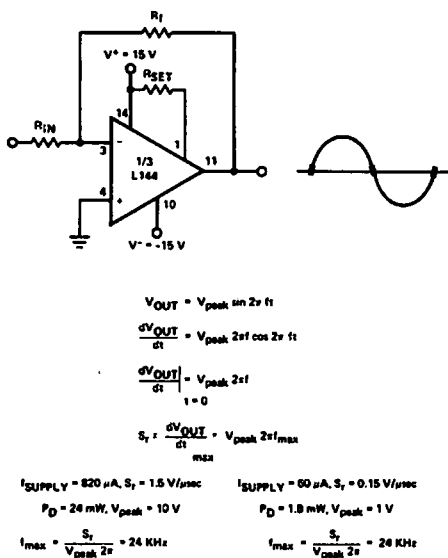
Slew Rate

Slew rate is almost a direct function of supply current as shown in Figure 6. This follows from the fact that slew rate limiting is actually caused by the finite limits of the internal current sources (which charge and discharge the second stage compensation capacitor) varying with the externally-determined set current. An amplifier output changes from the small signal response shown on the Bode plot to a slew-rate-limited response when the rate of change of the output voltage exceeds the rate of change determined by slew rate limit of the amplifier. Since the maximum rate of change of



Slew Rate Limits vs Supply Current
Figure 6

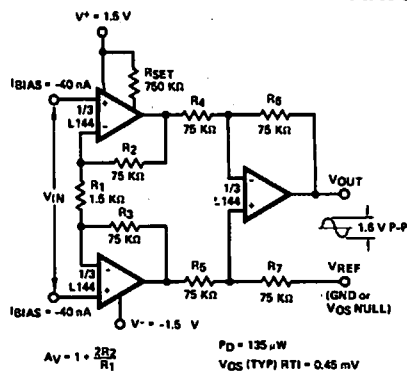
a sine wave is a function of peak amplitude it is possible to trade maximum frequency for peak signal amplitude when operating at low power dissipation levels. Figure 7 shows the derivation¹ of an equation relating slew rate S_r , sine wave amplitude V_{PEAK} , and frequency. The zero crossing of a sine wave is the point of maximum rate of change as shown after the derivative is taken and maximized. In both of the examples shown the maximum undistorted operating frequency is kept constant while juggling power dissipation, slew rate, and peak amplitude in an engineering tradeoff.



Slew Rate Limiting
Figure 7

Instrumentation Amplifier

Figure 8 shows a single L144 chip used to construct a three-amplifier classical instrumentation amplifier. The entire circuit consumes only 135 μ W of power from a ± 1.5 V power supply. With a gain of 101 the instrumentation amplifier is ideal in sensor interface and biomedical preamplifier applications.

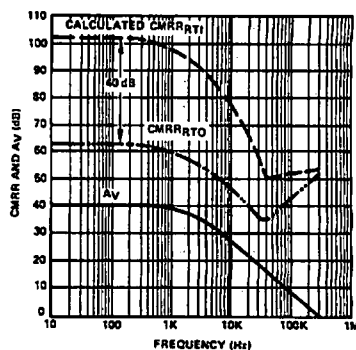


L144 Instrumentation Amplifier
Figure 8

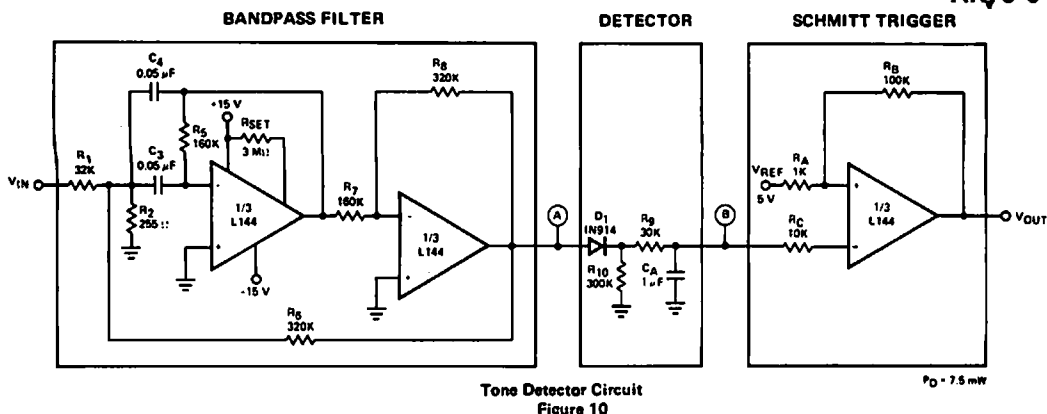
The first stage provides all of the gain while the second stage is used to provide common mode rejection and double-ended to single-ended conversion. The resistor R_1 determines the gain of the circuit according to the equation:

$$A_V = 1 + \frac{2R_2}{R_1} \quad (1)$$

The reference point at the base of R_7 can be used to determine the quiescent output voltage when there is no differential input voltage. This provides an easy single point to zero any net offset voltage (typically 0.45 mV referred to input) and/or to insert a trim resistor to improve common mode rejection ratio (CMRR). The CMRR depends heavily on the match between R_4/R_6 and R_5/R_7 and can be nulled if R_7 is broken into a resistor and a small-value trim potentiometer. Figure 9 shows the voltage gain and CMRR versus frequency for a typical instrumentation amplifier. The upper curve shows a calculated CMRR referred to input. The falloff and final rise in CMRR is due to the mismatch in gain rolloff between amplifiers in the first stage followed by a falloff in gain and consequent increase in rejection of the second stage.



Common Mode Rejection Ratio and Gain vs Frequency
Figure 9



Tone Detector Circuit
Figure 10

Tone Detector

Another example of a single L144 providing the amplifiers for an entire system is shown in Figure 10. This tone detector circuit is made up of a two-amplifier multiple feedback bandpass filter followed by an AC-to-DC detector section and a Schmitt Trigger. The bandpass filter (with a Q of 25) passes only 500 Hz inputs which are in turn rectified by D_1 and filtered by R_9 and C_A . This filtering action in combination with the trigger level of 5 V for the Schmitt device insures that at least 55 cycles of 500 Hz input must be present before the output will react to a tone input. The actual integrating capacitor waveform shown in Figure 11 was taken with a 1 volt peak 500 Hz sine wave input. The ratio between capacitor C_A charge and discharge is 1:11, due to resistors R_9 and R_{10} .

For frequencies other than the 500 Hz center frequency shown in the example the relevant bandpass filter² equations are:

$$\text{GIVEN: } Q, f_0, H_0 \text{ (Q normally from 10 to 50)} \quad (2)$$

$$\begin{aligned} \text{LET: } C &= C_3 = C_4 \\ 1 &\leq k \leq 10 \text{ (k chosen for component} \\ &\text{value convenience)} \end{aligned} \quad (3)$$

$$\text{THEN: } R_7 = \frac{Q}{2\pi f_0 C} \quad (4)$$

$$R_7 = R_5 \quad (5)$$

$$R_1 = \frac{k R_7}{H_0} \quad (6)$$

$$R_2 = \frac{R_7}{Q^2 - \frac{H_0 + 1}{k}} \quad (7)$$

$$R_8 = k R_7 = R_6 \quad (8)$$

In the example shown in Figure 10 the chosen value of $k = 2$ and the passive components used resulted in a measured Q of 23.1. The center frequency of 495.7 Hz and H_0 of 9.9 were close to the calculated values of 500 Hz and 10.

The detector RC was designed to have a 3 dB down frequency of:

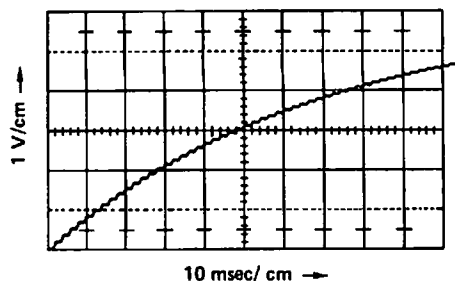
$$f_{3dB} = \frac{f_0}{100} \quad (9)$$

while the Schmitt trigger operated around the reference voltage with trip points determined by:

$$V_{HIGH} = \frac{V_{REF} R_B + 14 R_A}{R_A + R_B} \quad (10)$$

$$V_{LOW} = \frac{V_{REF} R_B - 14 R_A}{R_A + R_B} \quad (11)$$

where ± 14 V is the output swing with ± 15 V supplies. The measured trip points agreed with the calculated values of 5.089 V and 4.81 V within 0.2% in the circuit of Figure 10.



Detector Output Voltage vs Time
Figure 11

3 Amplifier Active Filter

The active filter shown in Figure 12 is a state variable filter with band-pass, high-pass and low-pass outputs. It is a classical analog computer method of implementing a filter using three amplifiers and only two capacitors. With the L144 triple op amp it becomes cost-effective to use this configuration with its attendant high Q values and low sensitivities.³ The practical maximum value of Q is:

$$Q_{\max} = \frac{A_{f0}}{3} \quad (12)$$

where A_{f0} is the open loop gain of amplifier A_1 at the resonant frequency.

The controlling design equations are:

GIVEN: Q , f_0 , and H_0 (bandpass output) (13)

LET: $R_5 = R_6 = R_7$ (Chosen for component value convenience) (14)
 $C_1 = C_2$

THEN: $\frac{R_4}{R_3} = 3H_0 - 1$ for $H_0 \ll \frac{A_{f0}}{3}$ (15)

$$R_2 C_2 = \frac{H_0}{2\pi f_0 Q} \quad (16)$$

$$R_1 C_1 = \frac{Q}{2\pi f_0 H_0} \quad (17)$$

The design example shown in Figure 12 was calculated as follows:

LET: $Q = 26$
 $f_0 = 1 \text{ kHz}$
 $H_0 = 26$
 $R_5 = R_6 = R_7 = 20 \text{ k}$ (18)
 $C_1 = C_2 = .008 \mu\text{F}$
 $R_3 = 10 \text{ k}$

THEN: $R_4 = (3H_0 - 1) R_3 = 770 \text{ k} \approx 750 \text{ k}$ (19)

$$R_2 = \frac{H_0}{2\pi f_0 Q C_2} = 19.9 \text{ k} \approx 20 \text{ k} \quad (20)$$

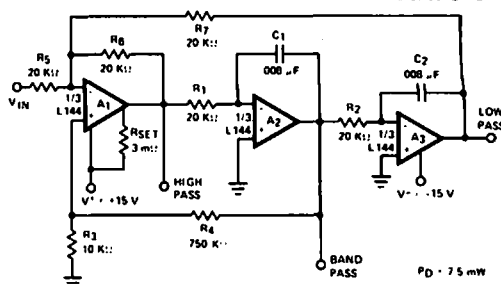
$$R_1 = \frac{Q}{2\pi f_0 H_0 C_1} = 19.9 \text{ k} \approx 20 \text{ k} \quad (21)$$

giving an actual calculated f_0 and H_0 of

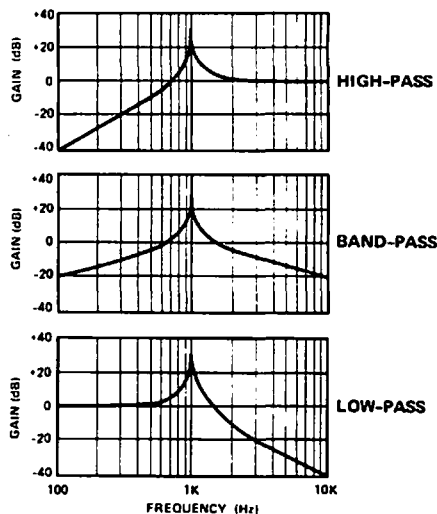
$$H_0 = 1/3 \left(1 + \frac{R_4}{R_3} \right) = 25.3 \quad (22)$$

$$f_0 = \frac{Q}{2\pi R_1 C_1 H_0} = \frac{H_0}{2\pi R_2 C_2 Q} = 994.7 \text{ Hz} \quad (23)$$

The measured values of Q , H_0 , and f_0 using 1% components were 26.9, 26.3 and 996 respectively. Figure 13 shows the Bode plots of the high-pass, band-pass, and low pass outputs.



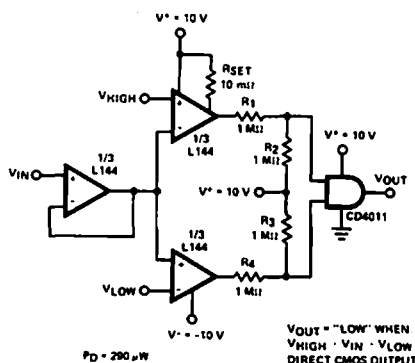
3 Amplifier Active Filter
Figure 12



Bode plots of Active Filter Output
Figure 13

Micropower Double-Ended Limit Detector

The double-ended limit detector shown in Figure 14 uses three sections of an L144 and a DC4011 type CMOS NAND



Micropower Double-Ended Limit Detector
Figure 14

gate to make a very low power voltage monitor. If the input voltage V_{IN} is above V_{HIGH} or below V_{LOW} the output will be a logical high. If (and only if) the input is between the limits will the output be low. The $1\text{ M}\Omega$ resistors R_1 , R_2 , R_3 and R_4 translate the bipolar $\pm 10\text{ V}$ swing of the op amps to a 0 to 10 V swing acceptable to the ground-referenced CMOS logic.

Total power dissipation is typically $290\text{ }\mu\text{W}$ while in limit and $330\text{ }\mu\text{W}$ while out of limit. Within the $\pm 9\text{ V}$ input range of the circuit the comparator resolution is typically 2 mV with the offset adjust determined by trimming V_{HIGH} and V_{LOW} . Since the L144 is operating at only $14.5\text{ }\mu\text{A}$ of supply current the slew rate is a corresponding low $.063\text{ V}/\mu\text{sec}$.

CONCLUSION

The preceding practical circuit examples are intended to show a few of the many possible applications of the L144 micropower triple op amp.

REFERENCES

1. M.K. Vander Kooi, "Slew Rate Limiting of IC Op Amp is Easy to Predict and to Avoid," EDN, October, 1972; pp. 36-37.
2. J.G. Graema, G.E. Tobey, and L.P. Huelsman; "Operational Amplifiers Design and Application," McGraw-Hill Co., New York, N.Y., 1971, pp.293-295.
3. S.K. Mitra, "Active Inductorless Filters," IEEE Inc., New York, N.Y., 1971, pp. 74-78.

FUNCTION / APPLICATION OF THE L161 MICROPPOWER COMPARATOR

INTRODUCTION

The L161 is a monolithic quad micropower comparator with an external control for varying its AC and DC characteristics. The variation of a single programming resistor will simultaneously alter parameters such as supply current, input bias current, slew rate, output drive capability, and gain. By making this resistor large, operation at very small supply current levels and power dissipations — typically in the low microwatt region — is possible. The L161 is therefore ideal for systems requiring minimum power drain, such as battery-powered instrumentation, aerospace systems, CMOS designs, and remote security systems.

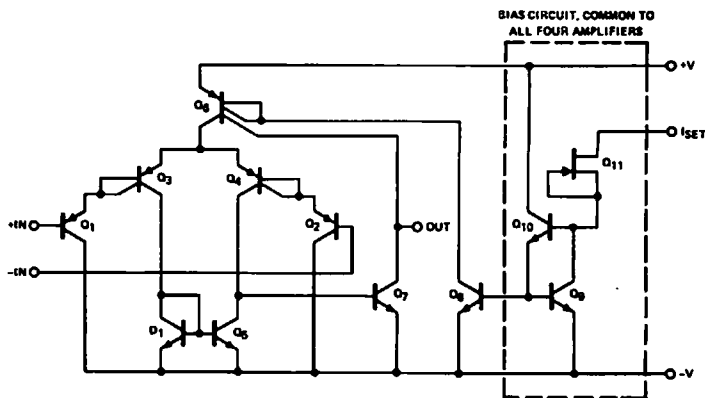
Description

The L161 is fabricated on a 48 x 54 mil chip using standard bipolar processing. The circuit (Figure 1) is composed of five major blocks — four comparators and a common bias

network. Q_1 - Q_6 and D_1 form a darlington differential amplifier with double-to-single ended conversion. Q_6 is a dual current source whose outputs are exactly twice the current flowing through Q_8 . The collector current of Q_8 is a function of the current supplied externally to Q_9 - Q_{10} , which in turn is known as the set current or I_{SET} . This set current is established by a resistor connected between the I_{SET} terminal and a voltage source, most commonly the positive supply. Q_{11} prevents excessive current from flowing through Q_9 and Q_{10} in the event the I_{SET} terminal is shorted to the positive supply; it has no effect on circuit operation under normal conditions.

The set current can be expressed as:

$$I_{SET} = \frac{[(+V) - (2V_{BE}) - (-V)]}{R_{SET}} \quad (1)$$



Schematic of One Channel of the L161
Plus the Common Bias Network
Figure 1

where $+V$ is the voltage to which the control resistor is connected, $-V$ is the negative supply voltage, V_{BE} is the base emitter drop of Q_9 or Q_{10} (about 0.7 V), and R_{SET} is the value of the external control resistor or set resistor. Equation 1 is simply a derivative of ohms law. There is also an analytical relationship between I_{SET} and the total supply current:

$$\begin{aligned}
 I_{SUPPLY} &= [I_{SET} \text{ (current sourced by } Q_6 \text{ to } Q_8) \\
 &\quad + 2 I_{SET} \text{ (current sourced to the differential amplifier by } Q_6) \\
 &\quad + 2 I_{SET} \text{ (current sourced to the comparator output by } Q_6)] \\
 &\quad \times 4 \text{ (the total numbers of comparators)} \\
 &\quad + I_{SET} \text{ (current sourced through } Q_{11}, Q_{10}, \text{ and } Q_9 \text{ to } -V) \\
 &= [I_{SET} + 2 I_{SET} + 2 I_{SET}] \times 4 + I_{SET} \\
 &= 21 I_{SET}
 \end{aligned}$$

The output current pulldown capability (I_{OL}) of the L161 is about 2 orders of magnitude greater than the high output drive current, (I_{OH}), which allows wire-ORing the outputs. I_{OH} is simply the current sourced by Q_6 :

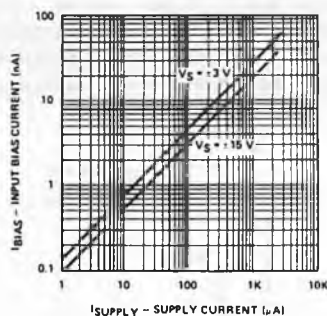
$$I_{OH} = 2 \times I_{SET} \quad (3)$$

I_{OL} is found by multiplying the current sourced by the collector of Q_6 by the gain of Q_7 :

$$I_{OL} = \beta(Q_7) \times 2 I_{SET} \quad (4)$$

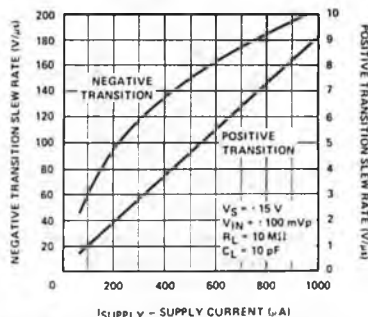
The beta of Q_7 is about 75-150.

Input bias current is a function of the betas of input devices Q_1 - Q_2 and I_{SET} . This is difficult to express analytically because β varies greatly with both processing and collector current; however it is roughly proportional to the set current and can easily be determined experimentally (see Figure 2).

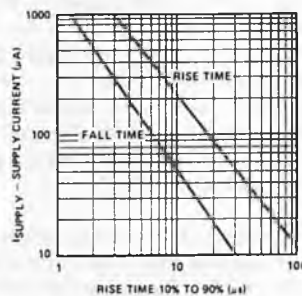


Input Bias Current vs Supply Current
Figure 2

Gain varies logarithmically with changes in supply voltage and linearly with changes in set current. Primary causes are the decrease in output impedance of Q_7 with decreasing supply voltage and an increase in transistor betas with increasing set current. Other AC parameters such as slew rate and transition time are also effected by set current; however current dependent parameters such as beta and chip capacitances make mathematical expressions imprecise. These relationships have been determined empirically and are presented in Figures 3 and 4.



Slew Rate vs Supply Current
Figure 3

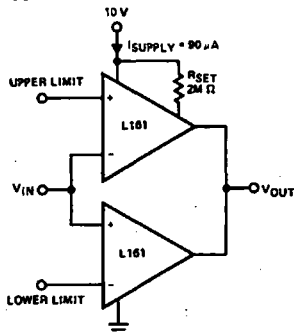


Rise and Fall Times vs Supply Current
With One CMOS Load
Figure 4

The designer's ability to program the key parameters of the L161 enables him to program just enough supply current to meet his design objectives. This coupled with the L161's performance using only microwatts of power makes it ideal for any micropower or battery-powered system, as well as a replacement for existing higher power comparators. The following applications illustrate the flexibility and unique capabilities of the L161.

Micropower Applications

A classic comparator application is the double-ended limit detector or window comparator shown in Figure 5. V_{OUT} is high whenever the input voltage is within the two limits. Because the Darlington input stage extends the common-mode input range below the negative supply, the lower limit may be as low as -0.4 V with the V_- terminal at ground. A comparison about ground is therefore possible with only one supply.

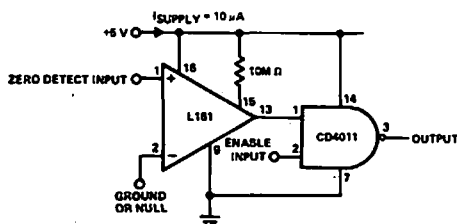


Double-Ended Limit Comparator
With Wire OR'd Outputs
Figure 5

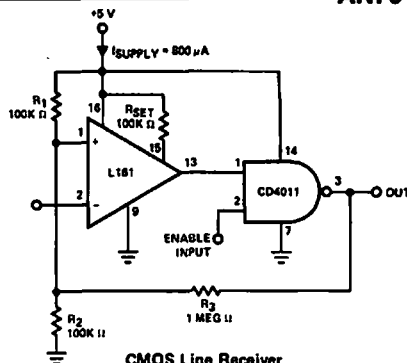
The L161 is especially suited for this application because of its wire OR capability; low output on either comparator will pull both outputs to ground. For this example a supply current of $90 \mu\text{A}$ was chosen to provide a slew rate of about $5 \text{ V}/\mu\text{s}$. If greater output drive current or decreased transition times are needed, lower R_{SET} .

The zero crossing detector shown in Figure 6 is useful in sine wave squaring circuits and A/D converters. This circuit also takes advantage of the L161's ability to detect signals below its negative rail, so only a positive supply is needed. The positive input may either be grounded or connected to a nulling voltage which cancels input offsets and enables accuracy to within microvolts of ground. The CMOS output will switch to within a few millivolts of either rail for an input voltage change of less than $200 \mu\text{V}$.

The circuit in Figure 6 may be modified to produce a line receiver (Figure 7). The trip point is set half way between the supplies by R_1 and R_2 ; R_3 provides over 200 mV of hysteresis to increase noise immunity. With $800 \mu\text{A}$ of quiescent supply current the maximum frequency of operation is about 300 kHz . If response to TTL levels is desired, change R_2 to 39 K . The trip point is now centered at 1.4 V .

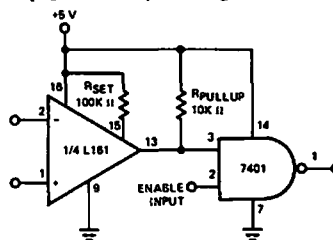


Zero Crossing Detector
Figure 6



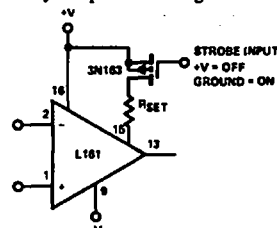
CMOS Line Receiver
Figure 7

Mating the L161 with CMOS logic is natural since the L161 draws microamps from a single 5 V supply. However, the L161 will also drive TTL when a suitable pull-up resistor is provided. Figure 8 shows this combination. Total power drain of the circuit is much heavier due to the presence of the 7401. Propagation delays through the circuit are about $1 \mu\text{sec}$.



Driving TTL
Figure 8

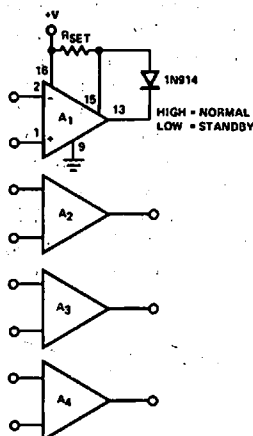
In many situations further power savings can be achieved by reducing or eliminating I_{SET} during part of the operating time. This is desirable. For example, when a system is multiplexed at a low duty cycle. The L161 may be strobed off completely by reducing I_{SET} to zero as shown in Figure 9. The 3N163 P-channel MOSFET is OFF when the strobe input is high so no set current flows into the L161. For a low strobe input, the 3N163 turns ON, pulling R_{SET} to the positive supply and turning on the comparator. The drain-source resistance of the 3N163 (3000Ω) is negligible compared to R_{SET} . If the negative supply terminal of the L161 is returned to ground, the 3N163 may be eliminated and R_{SET} connected directly to the output of a CMOS gate. The L161 will now be ON when the CMOS output is high. When the L161 is strobed OFF, its outputs assume a high-impedance state; this "three state" operation facilitates the connection of many outputs to a single bus.



Strobing the L161 ON and OFF
Figure 9

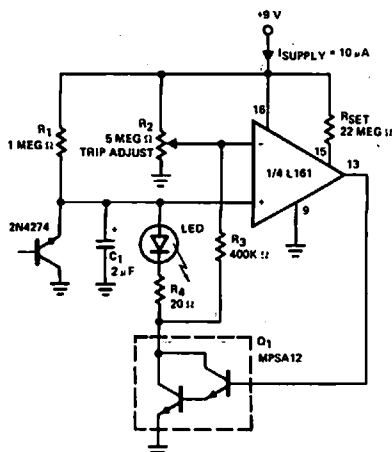
The L161 will switch itself into a standby mode if one of its outputs is connected to the I_{SET} terminal as illustrated in Figure 10. The diode blocks current when the output of A_1 is HIGH, and operation of the other three comparators is normal. When the output goes low, however, the 1N914 conducts most of I_{SET} to the negative supply. I_{OL} is therefore nearly equal to I_{RSET} , and (from Equations 2 and 4),

$$I_{SUPPLY} = 21 I_{SET}(\text{actual}) = \frac{21 I_{OL}}{2B} = \frac{I_{RSET}}{10} \quad (5)$$



Switching the L161 to a Low Current
"Standby" Mode
Figure 10

if a β of 105 is assumed. Equation 5 states that the supply current of the L161 is reduced from $21 \times I_{R1}$ (normal operation) to $I_{R1}/10$, a factor of 210 (or twice whatever β of Q_7 is). Total supply drain is simply the current through R_{SET} . This circuit has an important advantage over the previous strobe circuit—even though the L161 is operating at a greatly reduced supply current, it is still ON and continues to function. If a lesser reduction in supply current is desired, connect a resistor in series with the diode.

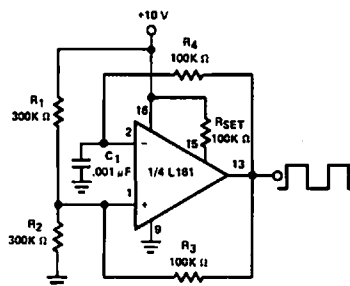


A Low Battery Indicator
Figure 11

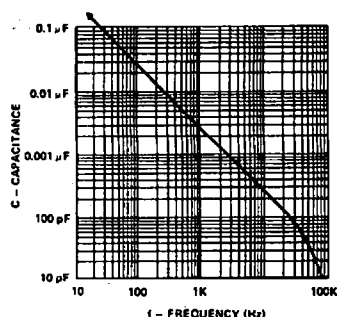
Figure 11 shows an L161 low battery indicator which flashes an LED when the battery voltage drops below a certain threshold. The 2N4274 emitter-base junction serves as a zener which establishes about 6 V on the L161's positive input. As the battery dies, the voltage at the negative input drops more quickly; when the low battery threshold (typically 7.5 V) is reached, the L161 output goes HIGH. This turns on the Darlington, which discharges C_1 through the LED. The interval between flashes is roughly equal to $R_1 C_1$, which in this case is 2 seconds. By flashing the LED at a very low duty cycle, this circuit gives a low battery warning with only 10 μ A average power drain.

Waveform Generators

Figure 12 is a square wave generator which is operable to over 100 kHz while Figure 13 depicts the typical frequency vs capacitance performance of the circuit. The low frequency limit is determined only by the size of C_1 . Frequency is constant for supply voltages down to +5 V; below that the charging rate of C_1 in the positive direction is determined by I_{OH} and not R_4 . For lower voltage operation, increase R_4 (and lower C accordingly) or decrease R_{SET} .



Squarewave Oscillator
Figure 12

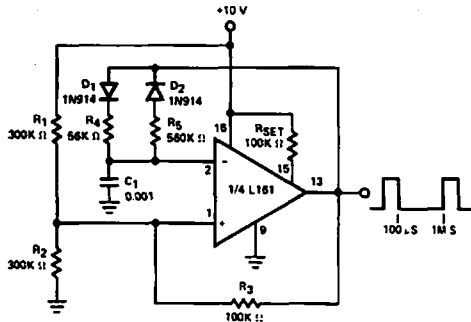


Frequency vs the Value of C_1
for the Squarewave Oscillator
Figure 13

To generate pulses the positive and negative charging rates of the capacitor must be unequal. Figure 14 illustrates a method using diodes and unequal resistors. The duty cycle of the output pulse is equal to $R_4/(R_4 + R_5) \times 100\%$. For duty cycles of less than 50%, D_1 can be eliminated and R_2 raised according to the formula,

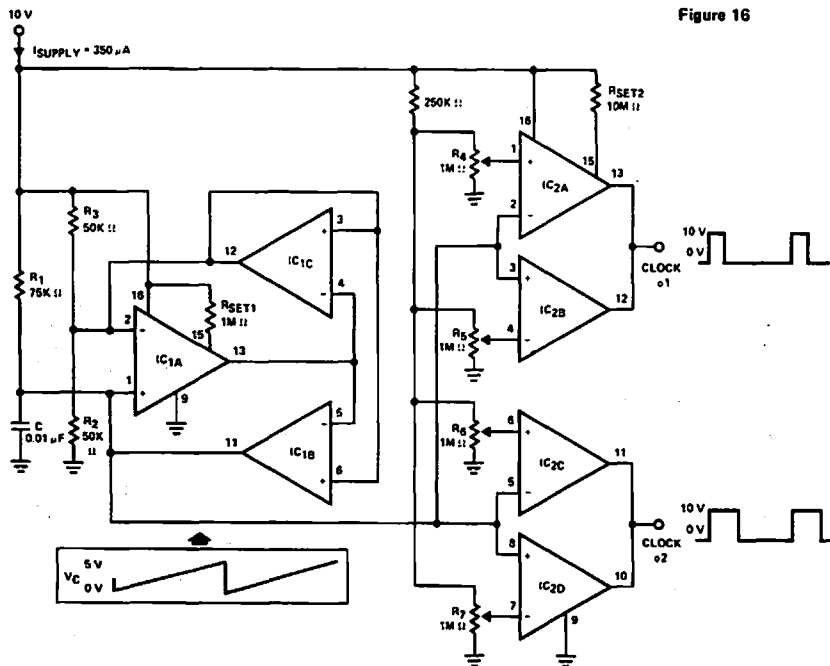
$$R_4(\text{actual}) = \frac{R_5 \times R_4(\text{eff})}{R_5 - R_4(\text{eff})} \quad (6)$$

where $R_4(\text{eff})$ is the effective value of R_2 in the circuit and $R_4(\text{actual})$ is the actual value used; $R_4(\text{actual})$ will always be larger than $R_4(\text{eff})$. A similar analysis could be made for eliminating D_2 when $t > 50\%$. Figure 13 may be used to determine frequency ($= 1/\text{period}$) if $1/2(R_4 + R_5) = 100K$.



Pulse Generator
Figure 14

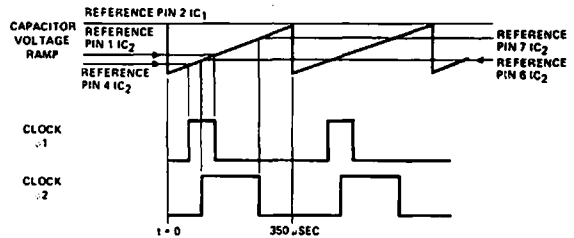
The versatile two phase clock generator of Figure 15 uses two L161's to generate pulses of adjustable widths and phase relationships. IC_1 is the heart of a ramp generator which



A Versatile 2φ Pulse Generator
Figure 15

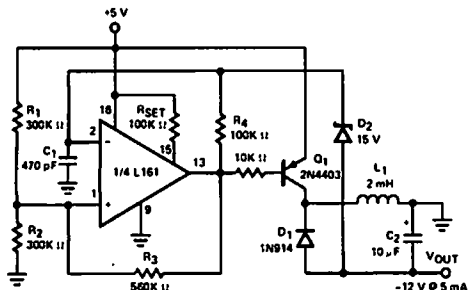
feeds two variable window comparators formed by $IC_{2A} - IC_{2B}$ and $IC_{2C} - IC_{2D}$ respectively. The voltage on pin 1 of IC_{1A} ramps up as C_1 charges through R_1 . When this voltage exceeds approximately 5 V (the potential on pin 2 of IC_{1A}), the output of IC_{1A} goes HIGH, forcing IC_{1B} and IC_{1C} LOW. C_1 is quickly discharged by I_{OL} of IC_{1B} , and the comparators reset to their normal state (IC_{1A} LOW, IC_{1B} and IC_{1C} HIGH).

As the ramp rises, its value passes through the two windows defined by the differences between the voltages on R_4 and R_5 in the case of ϕ_1 , and $R_6 - R_7$ for ϕ_2 . IC_2 is set for a supply current of 20 μA ; at this level its slow rate is too slow for the window comparators to respond to the fast negative transition of the ramp. By adjusting $R_4 - R_6$, ϕ_1 and ϕ_2 may be set for any width up to the period of the ramp (Figure 16 contains typical waveforms). If longer pulse lengths are needed, increase C_1 since $t(\text{ramp}) = 0.7 R_1 C_1$ (neglecting I_{OH} of IC_{1B} and IC_{1C}). A higher rep rate is obtained by lowering C_1 but R_{S1} and R_{S2} may also need to be lowered to insure IC_1 and IC_2 have adequate slew rates.



Typical Waveforms of the Two Phase
Pulse Generator
Figure 16

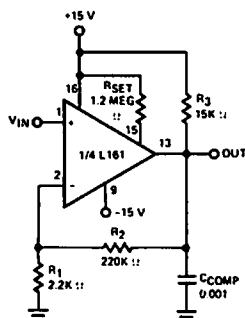
Figure 17 is a low power D.C. to D.C. converter obtained by adding a flyback circuit to the square wave oscillator. Operating frequency is 20 kHz to minimize the size of L_1 and C_2 . Regulation is achieved by zener diode D_2 ; when the output is less than -12 V, the zener breaks down and discharges C_1 slightly which reduces the duty cycle of the oscillator below 50%. Maximum current available before the converter drops out of regulation is 5.5 mA at an overall efficiency of 71%. With no load the converter draws 590 μ A.



A Regulated DC to DC Converter
Figure 17

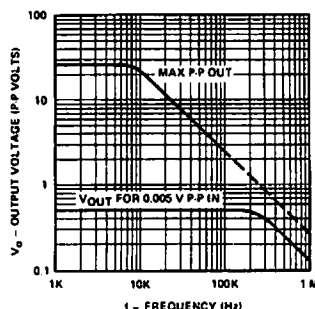
Operational Amplifiers

While designed primarily as a comparator, the L161 will perform as an op amp if proper compensation is applied. Figure 18 is a simple gain of 100 amplifier with a gain-bandwidth product of 20 MHz! The primary limitation in the



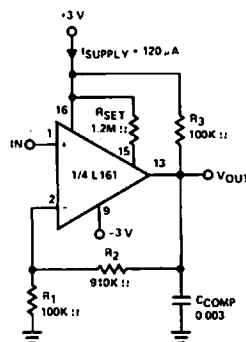
The L161 as a X100 Operational Amplifier
Figure 18

performance is the low slew rate (0.3 V/ μ sec) imposed by I_{OH} charging C_{comp} . The effects of slew rate and compensation are shown in Figure 19. A lower gain amplifier



Frequency Response and Maximum Output
for the X100 Op Amp
Figure 19

requires a larger C_{comp} , which in turn further reduces slew rate. For this reason it may actually be advantageous in certain cases to lower the gain by placing a resistive divider at the input rather than raising R_1 . Figure 20 shows a 700 μ watt X10 op amp whose slew rate is 0.02 V/ μ sec and is 3 dB down at 100 kHz.



A Micropower X10 Op Amp
Figure 20

BOOST OP-AMP OUTPUT POWER WITH COMPLEMENTARY POWER MOSFETS

Mark Alexander
September 1983

INTRODUCTION

Many high-quality, monolithic op-amps are available today at low cost. They offer low noise and distortion, high slew-rate and wide bandwidth. However, due to the limited chip-size, their small output transistors cannot deliver any appreciable power to a load.

Higher-power monolithic and hybrid op-amps are available, but their cost is inevitably much higher than their low-power counterparts. Also, their performance tends to be inferior in the categories of noise, distortion and slew-rate.

Clearly, a circuit topology that combines a low-power, high quality op-amp, a pair of inexpensive complementary power MOSFETs and a few additional components, is desirable. This combination should be expected to have very good performance, since power MOSFETs are inherently linear devices.

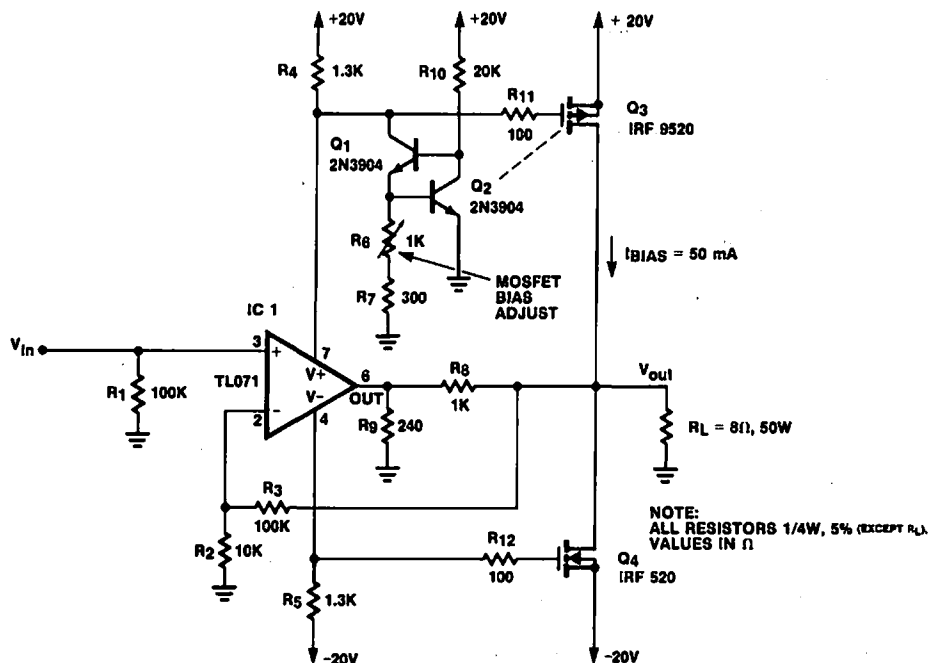
This Applications Note presents a power-booster op-amp circuit using Siliconix N and P channel power MOSFETs. It is configured as a current-booster DC amplifier operating from a standard op-amp power supply voltages. The design takes advantage of a new thermally-stable biasing technique for the MOSFETs. Emphasis is placed on the ease of interfacing complementary power MOSFETs to an op-amp, and the high performance obtainable.

A CURRENT-BOOSTED DC POWER-AMPLIFIER

Circuit Topology

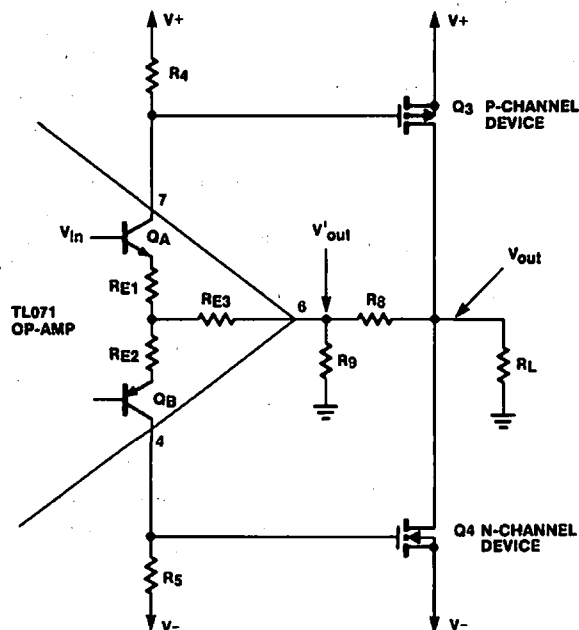
The schematic for this simple circuit is shown in Figure 1. It is configured as a non-inverting DC amplifier with a closed-loop gain of 11. Drive for the power MOSFET output stage is taken from the op-amp's power supply pins, rather than its output pin. This may seem somewhat unconventional, but there are very good reasons for doing this. The output pin could be used to drive a pair of MOSFETs configured as a complementary source-follower. However, the source-follower output-stage has two major disadvantages: a voltage gain of less than unity, and a substantial DC threshold offset-voltage. This results in peak gate-drive voltages, from the op-amp, several volts greater in magnitude than the output at the MOSFET sources. Also, the output of most op-amps can only swing to within about 2 volts of the supply rails. Thus, the peak voltage swing at the output of the source-follower is restricted to significantly less than the power-supply rail voltages.

The amplifier shown in Figure 1 does not have these limitations. Both the op-amp's output stage and the MOSFET current-booster stage provide voltage gain. The op-amp's output stage is used as an inverting common-emitter phase-splitter, while the MOSFETs are used as an inverting common-source output-stage. Since the collectors



A CURRENT BOOSTED DC POWER AMPLIFIER USING AN OP-AMP, A PAIR OF COMPLEMENTARY POWER MOSFETS AND A FEW ADDITIONAL COMPONENTS.

FIGURE 1



A SIMPLIFIED VIEW OF THE CURRENT BOOSTED AMPLIFIER, SHOWING THE SECONDARY FEED BACK LOOP. THIS IS FORMED BY THE OP-AMP'S OUTPUT STAGE, THE MOSFETS, AND THE FEEDBACK NETWORK R_9 AND R_8 .

FIGURE 2

of the output transistors in almost all monolithic op-amps are connected to their power supply pins, they can be used to drive the MOSFETs.

Load resistors R_4 and R_5 are connected from the op-amp's supply pins to the power supply rails. They generate the necessary bias and drive voltages that the MOSFETs require. Since these voltages are referenced to the power supply rails rather than the output voltage, a significantly larger peak output swing is possible. This circuit easily generates peak gate-to-source enhancement voltages for each MOSFET in excess of 10 volts. Thus, the output voltage swing is limited only by the peak output current multiplied by the $R_{DS(on)}$ of the MOSFETs.

Quiescent bias current for the op-amp also flows through resistors R_4 and R_5 . Since this current is regulated internally by the op-amp, it does not affect circuit performance. In fact, it proves beneficial because some DC bias voltage for the MOSFETs is generated across R_4 and R_5 . More will be said about DC biasing for the MOSFETs later.

It should be noted that small resistors (100 Ω) are included in series with the gates of each MOSFET. These are to suppress any potential parasitic oscillation that might occur in the circuit. The resistors should be placed as close to the MOSFET packages as possible, for maximum suppression. Care should be taken in the layout of the circuit to avoid excessively long lead lengths as well as any ground-loops.

Looking at Figure 2, it can be seen that a secondary feedback loop is formed by the op-amp's output stage, the power MOSFETs and the feedback network R_8 and R_9 . The effect of this feedback loop is to stabilize the voltage gain seen, going from V_{in} to V_{out} . It can be shown through linear circuit analysis, that at low frequencies:

$$\frac{V_{out}}{V_{in}} = \frac{g_{mA}g_{m3}R_4R_L}{1 + \beta g_{mA}g_{m3}R_4R_L} \left(\frac{r_{eA}}{r_{eA} + RE1 + RE3} \right) \quad (1)$$

$$\text{and } \beta = \frac{V'_{out}}{V_{out}} = \frac{R_9}{R_8 + R_9} + \frac{R_8R_9}{R_8 + R_9} \left(\frac{1}{g_{m3}R_4R_L} \right) \quad (2)$$

$$\text{where: } \begin{array}{lcl} g_{mA}(Q_A) & \approx & 40 \text{ mA/V} \\ r_{eA} & = & 1/g_{mA} = 26 \Omega \\ RE1 & = & 64 \Omega \\ RE2 & = & 128 \Omega \end{array}$$

$$\text{and } \begin{array}{lcl} g_{m3}(Q_3) & \approx & 2.5 \text{ A/V} \\ R_4 & = & 1.3 \text{ K}\Omega \\ R_8 & = & 1.0 \text{ K}\Omega \\ R_9 & = & 240 \Omega \\ R_L & = & 8 \Omega \end{array}$$

If, as in this case;

$$\frac{R_8R_9}{R_8 + R_9} \ll g_{m3}R_4R_L$$

$$\text{then, } \beta \approx \frac{R_9}{R_8 + R_9} \quad (3)$$

$$\text{Thus: } \frac{V_{out}}{V_{in}} = \frac{124.0}{1 + \beta(124.0)}$$

$$\text{and so, } \frac{V_{out}}{V_{in}} \approx 1/\beta = \frac{R_8 + R_9}{R_9} \quad (4)$$

This analysis has been done for the upper half of the output-stage only. Since the upper and lower halves are reasonably well-matched, this analysis will suffice for both.

Equation (4) shows that the low-frequency voltage-gain of the combined output-stage is set independently of the op-amp. This additional gain reduces the voltage swing at the output of the op-amp, and improves the bandwidth, slew-rate and distortion of the amplifier. Theoretically this improvement should be equal to $1/\beta$ or about a factor of 5 in this case. However, this value is only observed in the reduction of distortion over the source-follower output-stage. The rather large input capacitance of the MOSFETs (several hundred pF), degrades the frequency response somewhat and slows the amplifier down. The actual improvement in slew-rate was observed to be closer to a factor of 3, which is still more than acceptable. The full power bandwidth of this amplifier was well over 100KHz.

A detailed frequency response analysis of this amplifier has not been presented here, because it is somewhat lengthy. Suffice to say, however, that the additional gain provided by the combined output-stage increases the overall gain-bandwidth-product of the circuit. As well, the MOSFET stage adds an extra pole to the open-loop transfer function. Thus the amplifier is unstable for closed loop gains less than about $1/\beta$, or 5 in this case. If unity or very

low values of gain are desired, an externally compensated op-amp such as the TL080 should be used in place of the TL071. An external compensation capacitor can then be chosen so that the circuit will not oscillate at the particular closed-loop gain used.

Biasing The MOSFET Pair - A New Approach.

As mentioned previously, the op-amp's DC operating current generates some bias voltage for the MOSFETs, across R_4 and R_5 . This voltage is intentionally made less than either MOSFET's threshold voltage. Consequently the biasing circuitry comprised of Q_1 and Q_2 , has full control over the MOSFET idle current. The MOSFET threshold voltages are typically 3 volts for the N-channel device and 4 volts for the P-channel.

Texas Instruments' TL071 BIFET op-amp was chosen for its low supply current of 2.5mA (max) as well as its high speed and low noise.

The low supply current ensures that the voltage across R_4 and R_5 can be reduced to less than 3 volts. With the bias adjust trimpot (R_6) set for minimum bias, the MOSFETs should not conduct any current. In some cases though, the values of R_4 and R_5 may have to be changed to ensure that the MOSFETs do turn off with R_6 set for minimum bias. Q_1 and Q_2 form a variable, temperature-compensated

current-sink, connected to the positive supply pin of the op-amp. As trimpot R_6 is reduced from its maximum value, the additional current drawn by Q_1 , through R_4 , increases. At some point, the voltage across R_4 will reach the threshold voltage of the P-channel MOSFET and it will begin to conduct current.

This current will tend to force the output of the amplifier positive, if the N-channel device is conducting a lesser current. But the output of the amplifier is DC coupled back to the inverting terminal of the op-amp. Thus, the op-amp adjusts the voltage across R_5 to force the N-channel device to conduct the same current as the P-channel device. As trimpot R_6 is varied, the voltage at the op-amp's output pin can be seen to go more negative as the bias is increased. This makes sense because more current is then flowing out of the op-amp's negative supply pin, which increases the gate-to-source voltage of the N-channel MOSFET.

It can be seen that the op-amp is used not only as the main gain element in this amplifier, but also as the bias controller for the N-channel MOSFET. Any variations in the idle current of the P-channel MOSFET are mirrored, under control of the op-amp, by the N-channel device. This keeps the output centered at zero.

TABLE 1: CURRENT BOOSTED DC AMPLIFIER PERFORMANCE

Conditions:	$T_A = 25^\circ\text{C}$, SUPPLIES = $\pm 20\text{V}$, $R_L = 8\Omega$ MOSFET BIAS CURRENT = 50mA, CLOSED-LOOP GAIN (AV_{CL}) = 11
Output Voltage Swing:	+18.5V, -19.0V
Output Sink/Source Capability:	2.5A DC
Rise Time:	1 μS
Slew Rate:	35 V/ μS
Overshoot:	+ve: 15%, -ve: 20%
Output Offset: (Equal to $AV_{CL} \times V_{IO}$ (op-amp))	75mV
Noise Floor (at 10Hz bandwidth):	-90dB at 100mW into 8 Ω
THD:	0.0075% at 100Hz and 20W 0.0162% at 1KHz and 20W 0.1350% at 10KHz and 20W
Bias Stability:	After 20W output for 1/2 hour the bias decreased to 43mA.

Some provision must be made to compensate for the variation in MOSFET idle-current with temperature, at fixed gate-to-source voltages. The temperature coefficient of drain-current at low bias levels is positive, which is due to the decrease in threshold voltage with increasing temperature. This variation in threshold voltage is approximately $-5\text{mV}/^\circ\text{C}$. If the voltage across R_4 is changed by this amount as the output devices heat up, then the idle current will be thermally stable.

This is easily achieved by thermally bonding (i.e. glueing) Q_2 of the bias circuitry to the heatsink on which the MOSFETs are mounted. As Q_2 heats up its base-emitter voltage decreases by about $2.2\text{mV}/^\circ\text{C}$. The effective change in voltage across R_4 with temperature is thus:

$$\frac{dV(R_4)}{dT} = \frac{R_4}{R_6 + R_7} \times (-2.2\text{mV}/^\circ\text{C})$$

In this amplifier, the sum of $R_6 + R_7$ was set to about 420Ω for a MOSFET bias current of 50mA . From equation 5, this gives an effective decrease in voltage across R_4 of $-6.9\text{mV}/^\circ\text{C}$. This decrease is somewhat larger than that of

the threshold voltage with temperature. Consequently the MOSFET idle current will decrease slightly as the temperature increases. This is desirable because the output stage power dissipation at idle will then decrease as the MOSFETs heat up. In this amplifier, the idle current decreased by approximately 15% for a 60°C temperature rise at the heatsink surface.

Amplifier Performance

Table I lists the amplifier performance measured on a breadboard version. Of particular note is the large output voltage-swing possible, with a low impedance load. This makes it suitable for use in applications such as Winchester head-actuator drive amplifiers. Here, the larger the output voltage swing, the faster the head accelerates across the surface of the disc.

The excellent noise, distortion and slew-rate specifications make this amplifier suitable for audio use as well. Supplied by $\pm 20\text{V}$ generated from a 12V battery, through a DC-to-DC converter, two of these amplifiers would be more than adequate as a car-stereo booster-amplifier.

Small robots too, could benefit from servo power-amplifiers based on the design presented here.

APPLYING 240 VOLT MOSPOWER TRANSISTORS AND CURRENT LIMITING DIODES TO ELECTRONIC PULSE DIALER CIRCUITS

Gary Rothrock
September 1983

Siliconix MOSPOWER FETs and current-limiting diodes offer simple circuit solutions for operating in the transient-filled telephone environment.

Because of their high voltage rating and low ON resistance, MOSPOWER FETs are excellent devices for use as dial-pulse and muting switches in a dialer circuit. High-voltage current-limiting diodes with less than 1 mA forward current and high impedance work well in dialer circuits to protect low-voltage dialer chips and minimize circuit current requirements.

This application note discusses design considerations when using these devices and also describes device features, characteristics and advantages in dialer applications. An example application is included.

DESIGN REQUIREMENTS

The major design effort for dialer circuits using current-limiting diodes and MOSPOWER FETs focuses on meeting protection and operational requirements. Protection is needed for low-voltage semiconductor devices (such as dialer chips) that are subjected to high-voltage transients (surges) on the phone line. For example, Bell System publication PUB 48005, paragraph 5.2¹ specifies surge tests for telephone equipment. A portion of Table 5.1 of that document is reproduced here showing the surges applied between tip and ring.

Type	Peak Amplitude V	Peak Available Current A	Maximum Rise Time, μ Sec	Minimum Delay Time, μ Sec	Number of Surges of Each Polarity
M1 Normal	600	100	10	1000	4
M2 Normal (Part 68)	800	100	10	560	2
M3 Abnormal	600	100	10	2500	1
M4 Abnormal	1000	200	10	1000	1
L1 Normal	600	200	10	1000	4
L2 Normal	1000	200	10	360	2
L3 Normal (Part 68)	1500	200	20	160	2
L4 Abnormal	600	200	10	2500	1
L5 Abnormal	1500	400	10	1000	1

Figure 1

¹ References are tabulated at the end of the paper.

One source of transients is lightning surges. However, these transients rarely cause damage to the dialing circuitry since it is exposed only when the phone is off-hook (handset lifted from the cradle). For most phones, the off-hook condition occurs on average, a small percentage of the time. Of course, a direct or nearly direct hit may cause damage even if the phone is on-hook and regardless of the type of protective circuitry used.

Voltage transients also appear in the dialer circuit when the phone is answered while it is ringing. The PBX or central office switch can take 100ms or more to trip (disconnect) the ringing voltage after the phone is taken off-hook. During this time, the ring voltage is applied to the dialer circuit. This condition occurs about one-third of the time on incoming calls, with the normal 2-sec on, 4-sec off ringing cycle.

Paragraph 2.6.2 of PUB 48005 specifies ring voltages up to 130Vrms superimposed on a dc voltage of 0 to +105 V for bridged ringing. Connection of the ringer between tip and ring conductors is called bridged ringing. This ringer connection is normally used on single party lines. The magnitude of the voltage across the dialer circuit may be high or low, depending on the switch ring voltage, loop length, ringer impedance and number of ringers attached to the loop.

However, the major source of transients applied to the dialer circuitry is inductive spikes generated by dial pulsing into electromechanical switching equipment. The interruption of loop current flow during breaks in dialing causes large transient voltages produced by the collapsing magnetic field in the line-circuit relays of the telephone switching equipment. Since current flow cannot change instantaneously in an inductor, the voltage rises as high as necessary to maintain the current flow either by circuit components breaking down, contact arcing, or charging of circuit capacitances.

If this capacitance is low, the voltage rise can be substantial until breakdown or arcing occurs. For example, a capacitance of $0.005\mu\text{F}$ will allow transients of greater than 1500V. Each dial pulse causes a transient, and telephone dialing generates many such transients in rapid succession. On short low-resistance, high-current loops, high-energy pulses can be delivered to the dialer circuitry.

A standard approach for providing protection from inductive spikes is the use of a zener diode with high surge capability to limit the voltage impressed on the dialer circuit. Figure 2 shows allowable percent break and dial-pulse rate for dialers pulsing through a speech network with zener voltages below 300V. As the zener voltage is reduced, the percent break and dial pulse rate specs are tightened. It is desirable, therefore, to use the highest possible zener voltage consistent with protecting circuit components. Maximum zener voltage can now approach 240V for a corresponding

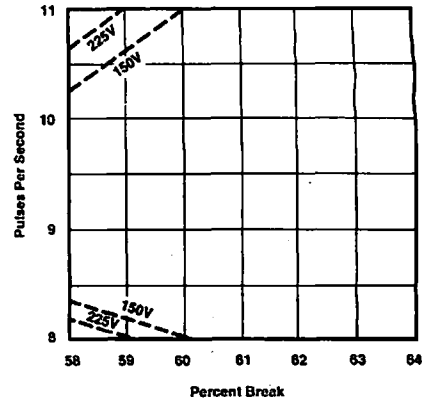


Figure 2 Percent break and pps limits as a function of zener voltage for devices which generate pulses. This diagram is used to determine the allowed area of operation of a dial for a given zener diode in the protective network. Thus, for the zener voltage of 225V the parameters of the dial pulses must lie in the hexagon bounded by the two sloping lines marked 225V, the 58 percent break line, the 8 pps line, the 11 pps line and the 64 percent break line.

increase in allowable operating area using high-voltage MOSPOWER FETs and current-limiting diodes.

Other important design considerations are loop current during breaks in dialing, dialer circuit current requirement and speech attenuation. Loop current must be below 1mA during the break period to maintain an acceptable break condition. Additionally the current requirement of the dialer circuit during talking periods must be low to prevent loss of efficiency of the carbon transmitter (if one is used) on long loops. A low supply current dialer circuit design is important for these reasons.

Speech attenuation is also important, especially for long loops. A dialer circuit operating in parallel with the speech circuitry should present a high shunt impedance to minimize speech level attenuation. A series dial-pulse or muting switch should exhibit low ON resistance for the same reason.

240-VOLT MOSPOWER DEVICE

Important attributes of MOSPOWER devices in dialer applications include high gate-input impedance, low ON resistance, high breakdown voltage, high current capability and low cost. The Siliconix VN2410M, for example, was designed for applications such as dialer circuits. As in all MOS devices, the gate requires only minute continuous drive current to hold it ON, unlike bipolar transistors. Gate current flows when the gate input capacitance charges during a change of state. The only other gate-current component is a few nanoamperes of input leakage current.

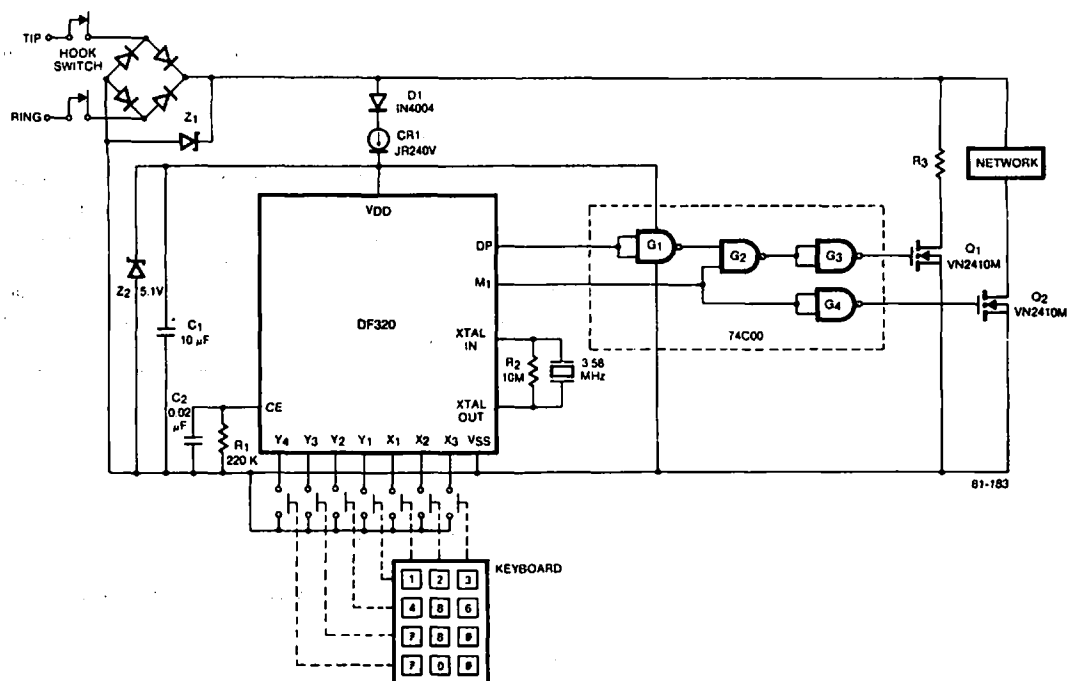


Figure 3 Dialer Circuit

Drain-to-source ON resistance for the VN2410M is specified as 10 ohms maximum. If the device is placed in series with a speech network, this low ON resistance contributes negligible speech-signal attenuation on long loops. The device breakdown voltage rating of 240V allows the use of protective clamping devices with voltage ratings approaching 240V. High voltage clamping allows a relaxation in percent break and dial-pulse rate limits relative to circuits using lower voltage clamping.

Other devices in the series have breakdown voltages of 170V (VN1710M) and 120V (VN1210M) for lower voltage requirements. The 0.25A continuous drain-current rating can handle full loop current on short loops. These devices are packaged in a TO-237 plastic package which is equipped with a power tab. The TO-92 package is available for lower power applications.

240-VOLT CURRENT-LIMITING DIODE

The JR240V current-limiting diode has a breakdown voltage rating of 240V. Other available breakdown voltage ratings are 220V (JR220V), 200V (JR200V), 170V (JR170V) and 135V (JR135V). These devices which are supplied in a 2-lead TO-92 plastic package feature a forward-current range of 200 to 770 μ A. Thus when used in series with a dialer circuit, they limit current to less than the required 1 mA during breaks. Since dynamic impedance is typically 2 megohms, there is no speech-signal attenuation.

DIALER CIRCUIT EXAMPLE

Figure 3 shows a dialer circuit using MOSPOWER devices for the dial-pulse switch and muting functions plus a current-limiting diode for dialer-circuit current regulation and protection. Dial-pulsing is performed through a resistor connected in shunt with the speech network. This circuit features a minimum number of components and low-current operation. The dialer chip is the Siliconix DF320, but other IC's can be used in similar designs.

Lifting the handset applies power through the diode bridge to the dialer circuit. Current flows through D1, CR1 and Z2, establishing Vdd for the DF320 and charging C1. When the minimum operating voltage (Vdd) is reached, power-on reset occurs via the CE network of C2 and R1. Initially, both DP and M1 are LOW, providing a LOW at the gate of Q1 to hold it off. A HIGH at the gate of Q2 turns it on, connecting the telephone network.

The current-limiting diode CR1 serves two purposes. First, it limits the total dialer-circuit current drawn from the loop to less than 1 mA, and second, it maintains a high dialer-circuit shunting impedance across the telephone set network. Z1 is a high-voltage zener diode with high surge capability that protects against loop transients and office inductance spikes. The device should limit all transients to less than the breakdown voltages of CR1, Q1 and Q2 (240V).

The DF320 clock starts upon recognition of the first keyed digit. M1 then goes HIGH, causing Q2 to turn off and Q1 to turn on. This change of states mutes the receiver connected to the network and maintains loop current flow through R3 and Q1. When dial pulse breaks occur, DP goes HIGH, causing the gate G3 output to go LOW and turn off Q1.

When dialing is complete, M1 goes LOW, causing Q1 to open and Q2 to close, reconnecting the telephone network. The DF320 then returns to the static standby condition and the oscillator turns off.

The diode bridge protects the dialer circuit from line polarity reversal. D1 prevents rapid discharge of C1 during makes in dialing if the voltage across R3 and Q1 is lower than the voltage across C1.

The MOSPOWER devices combine low ON resistance and high breakdown voltage with very high input impedance which allows direct drive from CMOS logic. This circuit configuration results in low dialer-circuit current as compared to bipolar devices. These features are ideal for accommodating wide variations in circuit operating conditions of both long and short loops.

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THEORY AND APPLICATIONS OF THE Si7660 AND Si7661 VOLTAGE CONVERTERS

Doyle L. Slack
April 1984

INTRODUCTION

Many times a simple digital circuit design can be greatly complicated by the needs of just one or two of the onboard devices. For example, analog devices often used along with digital circuits (such as op-amps and data acquisition systems) are notorious for negative voltage requirements of -5, -10, or -15 volts when everything else in the circuit needs only positive voltages. Until recently, the only answer was to either buy a DC-to-DC converter module (expensive) or redesign the power supply to generate the negative voltages (expensive and wasteful in parts count and space). This Application Note presents the newest alternative to this problem: the Si7660 and Si7661 monolithic voltage converters. With the Si7660 and Si7661, negative voltages from 1.5 to 20 volts can be generated from a positive supply with minimum parts count and minimum cost.

THEORY OF OPERATION

The basic theory behind the Si7660 and Si7661 is the same and is based on the ideal voltage doubler shown in Figure 1. Capacitor C_1 is the pump capacitor, and C_2 is the reservoir capacitor. The pairs of switches (S_1 with S_3 , and S_2 with S_4) are driven by an oscillator/toggle circuit, providing charge and transfer cycles of equal length.

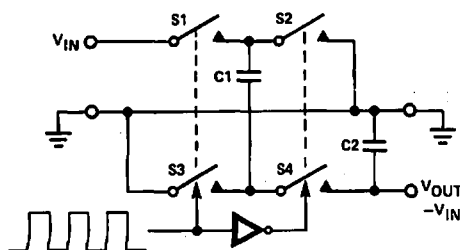


Figure 1. The Ideal Voltage Doubler.

During the charge cycle, S_1 and S_3 are closed, and current flows into C_1 , charging it to the value of V_{in} . The oscillator/toggle then changes state, and the transfer cycle begins. S_1 and S_3 are opened while S_2 and S_4 are closed, allowing C_1 to dump charge into C_2 until the potential across them has equalized. The oscillator/toggle then switches again, and the process starts over.

For no load conditions, the voltage inversion will be virtually perfect since the amount of charge that must be transferred from

C_1 to C_2 will be limited to losses due to leakage from C_2 and any parasitic capacitances. As the load increases, C_1 must transfer more and more charge to make up for the depletion of C_2 as it supplies current to the output during the charge cycle. This action causes the output voltage to drop, making the circuit appear to be a perfect inverter in series with an output resistor that varies in magnitude with the input voltage. Figure 2 shows this concept in a two port diagram of the device, and Figure 3 illustrates the typical output characteristics of both devices configured in the inverter mode.

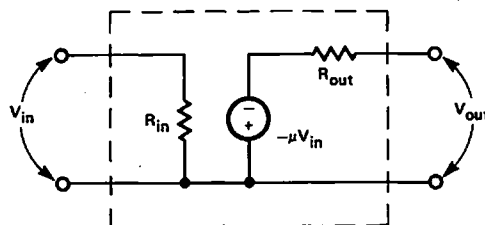


Figure 2. 2 Port Diagram of the Voltage Converter Circuit.

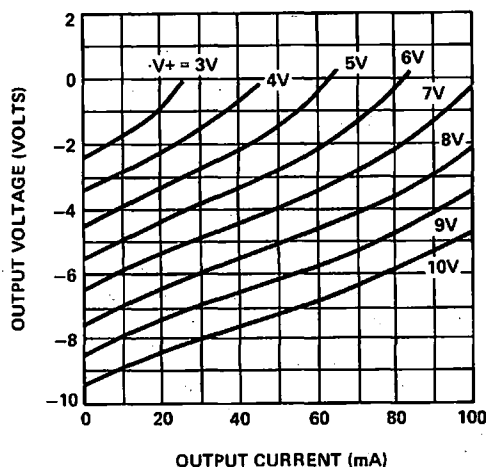


Figure 3(a). Output Characteristic of the Si7660 Voltage Converter. (D_x in Circuit)

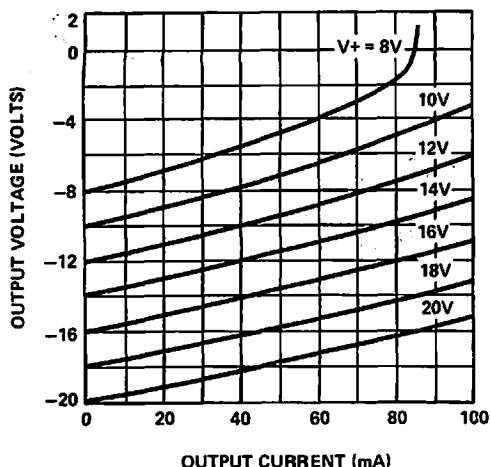


Figure 3(b). Output Characteristic of the Si7661 Voltage Converter.

CIRCUIT OPERATION

With the Si7660 and Si7661, the only parts of the doubler not included inside the package are the pump and reservoir capacitors. The internal switches are made with P-channel and N-channel MOSFETs. The main difference between the Si7660 and Si7661 is the breakdown voltage of the MOSFETs which in turn dictates the maximum input voltage. Also, the design of the Si7661 offers a much greater resistance to device latchup, which is discussed later. Since the internal sections of the two devices are very similar, description of the operation of the Si7660 and Si7661 is combined. The internal sections of the circuit are the oscillator, divider, regulator, level translator, and substrate logic. Figure 4 shows a block diagram of the internal sections of the inverter circuit.

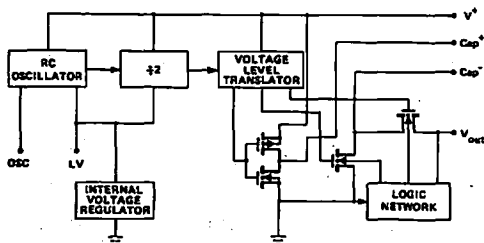


Figure 4. Block Diagram of the Voltage Converter Circuit.

The oscillator supplies the signal to the divider section which in turn drives the rest of the circuit. The OSC input has an input impedance of approximately 1 Megohm. This allows the internal oscillator to be overridden by an external clock or to be slowed down by the addition of an external capacitor.

The internal regulator is a series voltage regulator with a zener reference to insure that low voltage components of the circuit are provided with no more than 5 volts when the input voltage is greater than 5 volts. It also provides current limiting for the oscillator and divider circuits. The LV pin is provided to bypass the regulator when the input voltage is less than 3.5 volts for the Si7660 (less than 9.0 volts for the Si7661). However, when the

Si7660 is operated above 3.5 volts, the LV pin must be left open to provide latchup protection. This is not as critical for the Si7661, but it is still recommended to leave LV open above 9.0 volts for proper operation.

The divider is simply a divide-by-two counter that provides complementary outputs. Q and Q drive the inputs of the level translators, which in turn provide the necessary switching voltages to drive the MOSPOWER switches. The built-in delay of the translators guarantee that a break-before-make action occurs.

The substrate logic network insures that two things happen. First, it makes sure that the substrate-source/drain junctions of Q₃ and Q₄ are never forward biased, and that the on-resistance of each of the output transistors will be as low as possible for all operating conditions. Second, the network determines the most negative voltage in the device and uses it to supply power to the level translator.

Figure 5 gives the pin configuration of the Si7660 and Si7661. These devices are pin compatible to competitive products. Functionally, the Si7660 is an exact replacement for the competition while the Si7661 provides the advantage of greater voltage range at the expense of only slightly higher output resistance.

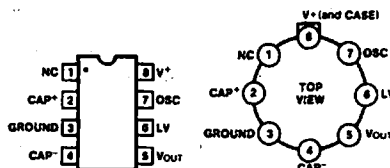


Figure 5. Pin Diagrams of the TO-99 and 8 Pin DIP Packages for the Si7660 and Si7661.

LATCHUP

Because of the basic internal four-layer geometry of CMOS devices, an SCR action can sometimes occur. Figure 6 depicts the SCR structure. This SCR action can, under certain conditions, cause the Si7660 device to latch up. As Figure 6 shows, the source of the N-channel device becomes the SCR cathode; the source of the P-channel is the anode; and either drain can act as a gate. Since an SCR does not trigger until certain conditions occur, it can sometimes cause no problems at all, yet sometimes it may be fatal to the CMOS device.

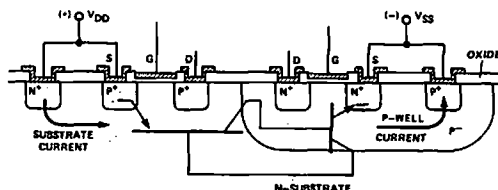


Figure 6. Intrinsic SCR Superimposed on a CMOS Gate Structure.

The intrinsic SCR needs three conditions to cause latchup. First, the current gain products (betas) of the two parasitic bipolar transistors must be greater than one. Second, the current flowing through the channels of the devices must be greater than the holding current of the SCR. Finally, some kind of pulse must be applied to one of the gates to trigger the SCR action.

The trigger pulse can come from several different sources. The power-up sequence of the CMOS device may cause problems if

the SCR gate receives power before the other terminals. Another possible trigger source is a high slew rate across the intrinsic SCR. When the SCR is triggered, the CMOS devices are suddenly shorted out by the SCR, and the output impedance of the device becomes very low.

Q_4 of the Si7660 can sometimes experience the conditions to cause SCR latchup when operating at the upper end of the input voltage range. The nearby P-channel substrate logic transistors form the complementary part of the intrinsic SCR. When the SCR action does occur, the circuit suddenly appears to be a short circuit between V_{in} and V_{out} . The reservoir capacitor (C_2) rapidly discharges through this path. After C_2 has discharged, the current through Q_4 drops below the SCR holding value, and the circuit resets. If the conditions that originally caused the SCR action remain present, the device will latch up repeatedly. If the circuit input is not current limited, this action can sometimes dissipate too much power through Q_4 and the substrate logic, resulting in damage to the device.

To prevent damage to the Si7660 when conditions for latchup occur, a diode must be placed in series with the V_{OUT} pin to block the discharge of C_2 and keep the current below the holding value of the SCR. This diode should be used whenever the input voltage could exceed 6.5 volts at room temperature. Figure 7 shows the derating curve for diode requirements over the entire temperature range.

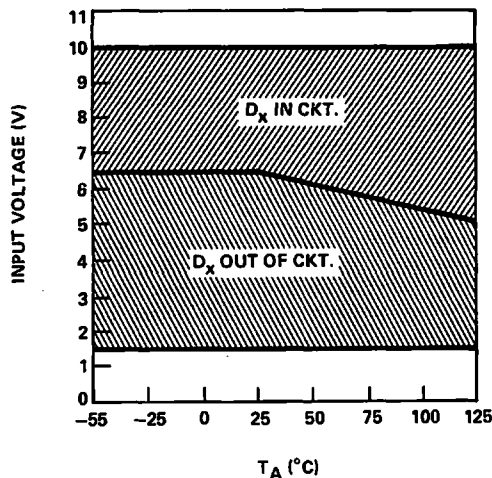


Figure 7. Range of Input Voltage and Operating Temperature for the Si7660.

The Si7661 is a higher voltage device than the Si7660, and is designed on a different process. This high voltage silicon gate process reduces the parasitic betas in Q_4 to a value that makes it extremely difficult to produce the conditions for latchup. Because of this, the series diode is not needed for operation anywhere in the specified voltage and temperature range of the Si7661.

GENERAL APPLICATIONS

The Si7660 and Si7661 are intended for use as voltage inverters. However, with a few added components, the inverter circuit can be rearranged to provide many different voltage levels. In some configurations, they can even provide more than one voltage output at the same time. The possibilities include voltage inversion, voltage multiplication, and even simultaneous inversion and multiplication.

BASIC VOLTAGE INVERSION

With no load, the output voltage magnitude of the basic voltage inverter circuit shown in Figure 8 will typically be within 0.1% of the V_+ (input voltage) magnitude for the Si7660 and within 0.3% of the input voltage magnitude for the Si7661. As the load current increases, the output will drop as shown in Figure 9(a). The effective output resistance will vary with input voltage as given in Figure 9(b). Once the load current reaches its limit (30–40 mA for the 5 volt case), the inverter can no longer regulate the voltage properly and shuts down to protect itself from extreme power dissipation.

CAUTION: At higher input voltages (for either device), the output maximum limit can cause the power dissipation to exceed the maximum rating of the package (especially plastic). Always calculate the maximum power dissipation for your design.

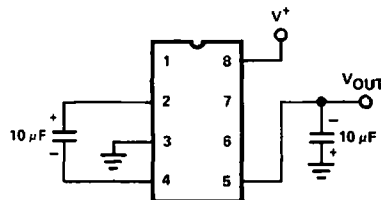


Figure 8. Schematic Diagram of the Basic Inverter Circuit.

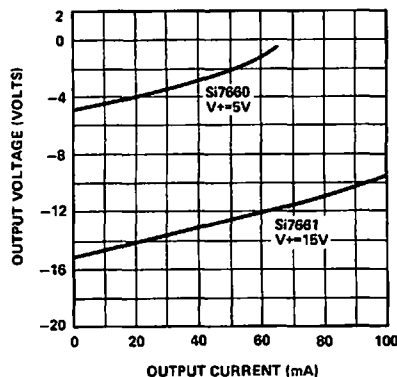


Figure 9(a). Variation of Output Voltage as a Function of Output Current.

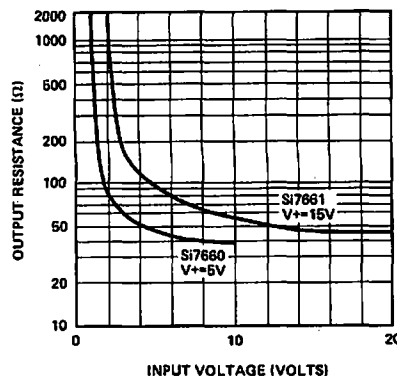


Figure 9(b). Variation of Output Resistance as a Function of Input Voltage.

The output ripple of the inverter is a function of the oscillator frequency as well as the size of the pump and reservoir capacitors. The nominal oscillator frequency is 12 kHz for the Si7660 and 10 kHz for the Si7661. Because the output ripple is important in some linear applications where supply noise is critical, Table 1 provides ripple values for different pump and reservoir capacitor values.

Table 1. Effect of Varying the Pump and Reservoir Capacitor Size on Output Ripple Noise.

	Capacitors (μF)	V_{OUT} (V)	V_R m($V_{\text{p-p}}$)
Si7660	10	-3.838	150
Inverter Mode	22	-3.862	75
(see Figure 8)	47	-3.873	30
$V_{\text{IN}} = +5\text{V}$	100	-3.874	26
$I_{\text{OUT}} = 10\text{mA}$	470	-3.879	10
	1000	-3.880	5
Si7661	10	-13.849	175
Inverter Mode	22	-13.872	80
(see Figure 8)	47	-13.882	38
$V_{\text{IN}} = +15\text{V}$	100	-13.883	29
$I_{\text{OUT}} = 10\text{mA}$	470	-13.885	10
	1000	-13.890	5

It is important to note that increasing the capacitor size can lead to other difficulties. The main problem is that the large capacitors may draw excessive amounts of current at turn-on. If the current is too great, the power dissipation of the device can be exceeded causing destruction of the converter. Even when the device is running, the charge transfer under heavy loads can push the switches to their limits.

The diode in the Si7660 output in Figure 10 is included to provide latchup protection (see LATCHUP). For operation above 6.5 volts at room temperature, the diode must be placed in the circuit to prevent the reservoir capacitor from discharging through the Si7660:

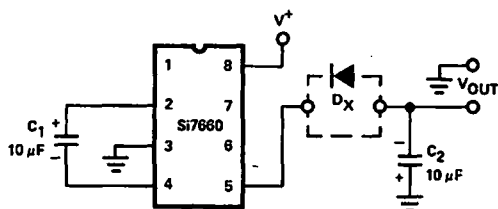


Figure 10. High Voltage (>6.5 V) Inverter Circuit for the Si7660.

Since the operating temperature is a factor in SCR latchup, it must be considered when deciding whether or not an output diode is required. Refer to Figure 7 when operating the Si7660 over the full temperature range. It is important to note that the output voltage of the circuit will be:

$$V_{\text{OUT}} = -(V^+) + V_{\text{diode}} \quad (1)$$

This shows that when the diode is in the circuit, the Si7660 can never achieve perfect inversion. An important advantage of the Si7661 is that the design allows operation over the full voltage and temperature range without the external diode. This does away with the output voltage drop, increasing the voltage inversion

efficiency of the circuit.

As stated before, the LV pin shorts out the internal regulator at low voltages when it is tied to ground. The LV pin should be grounded for operation below 3.5 volts for the Si7660 and 9.0 volts for the Si7661. However, it is necessary to leave the LV pin floating for high voltage operation. Failure to do so could permanently damage the device. Figure 11 shows the inverter configured for low voltage operations.

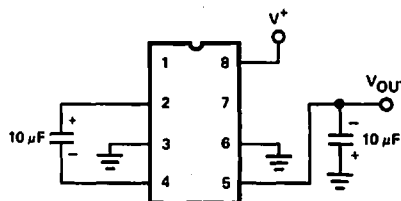


Figure 11. Inverter Circuit Connections for Low Voltage Operation.

VOLTAGE MULTIPLICATION

Since the inverter design is based on the ideal voltage doubler, it should be easy to convert the Si7660 and Si7661 devices to provide doubling of the input voltage. Figure 12 gives the schematic diagram of the voltage doubler. This circuit requires only one additional diode and will provide positive voltage multiplication at the expense of the voltage drops of the two diodes in series with the output. This means the positive multiplier will not be able to provide the near perfect output function like the basic inverter circuit does. The output voltage of the multiplier will be:

$$V_{\text{OUT}} = 2(V^+) - 2V_{\text{diode}} \quad (2)$$

However, another circuit can be built with the Si7661 that will eliminate the diode drops and give a much more efficient output voltage. Figure 13 illustrates this circuit which takes advantage of the bi-directionality of the CMOS output transistors. The 1 Megohm resistor injects a small current into the LV pin to insure that the oscillator starts. **NOTE:** This circuit cannot be used for the Si7660 due to oscillator protection circuitry inherent to the circuit.

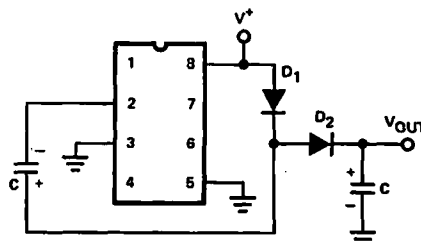


Figure 12. Voltage Doubler Schematic Diagram.

SIMULTANEOUS INVERSION AND MULTIPLICATION

The circuit shown in Figure 14 will provide both positive multiplication and inversion at the same time. The output voltages will be the same as those given in equations 1 and 2. This configuration is limited by the load current that can be drawn out of either output before the circuit becomes overloaded.

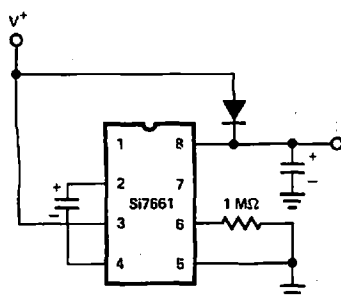


Figure 13. Schematic Diagram of the Alternate Voltage Multiplier (for use with the Si7661 only!)

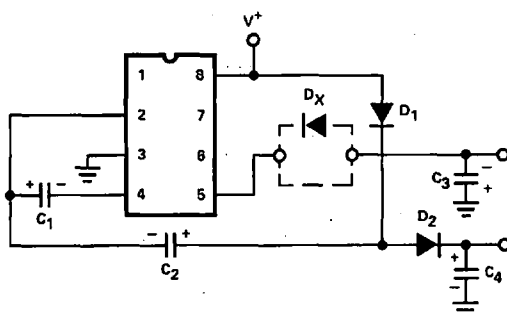


Figure 14. Combination Inverter/Multiplier Circuit.

PARALLEL CONNECTION

Although a single Si7660 and Si7661 cannot supply very large amounts of current, higher currents can be provided when several devices are connected in parallel. As shown in Figure 15, two or more inverter circuits can be paralleled to provide a lower output resistance, providing a smaller output voltage drop for a given current. This circuit will also expand the operating output current range slightly. Each device must have its own pump capacitor, but the reservoir capacitor is shared between all of the devices.

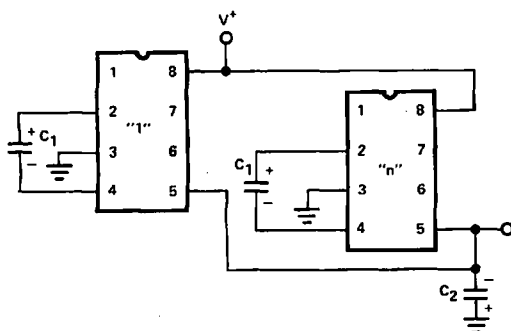


Figure 15. Paralleling Multiple Voltage Converters for Increased Current Capability.

When two or more devices are paralleled, the output noise (ripple) will contain not only components at frequencies of each of

the oscillators, but also at sum and difference frequencies due to a mixing action at the inverter outputs. If such noise cannot be tolerated, the OSC pin of one of the devices can be driven by an exclusive NOR gate that compares the oscillator frequencies of the two devices as shown in Figure 16. This forces the two devices to alternate their charge and transfer cycles, which will not only reduce output noise but also maximize efficiency.

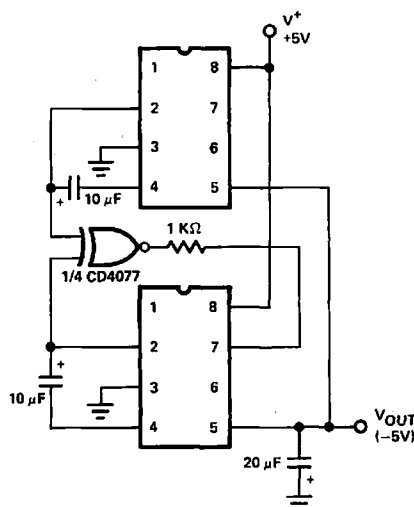
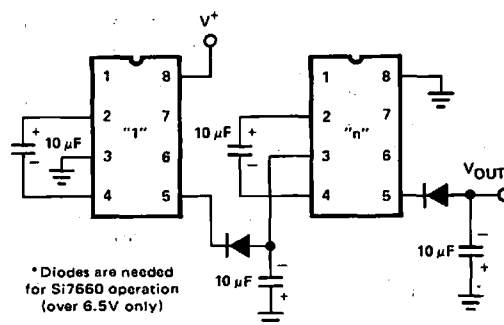


Figure 16. Synchronizing Two Si7660's or Si7661's with a Single Exclusive NOR Gate.

SERIES CONNECTION

When high voltage inversion is desired, inverter circuits can be placed in series to produce voltages outside of the operating range of a single Si7660 or Si7661. Figure 17 shows two inverters cascaded to double the input voltage magnitude while inverting the voltage at the same time.

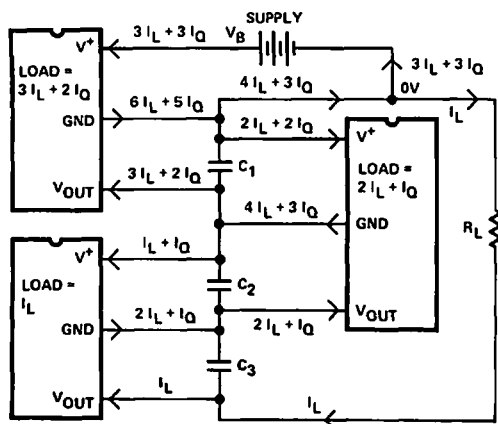


* Diodes are needed for Si7660 operation (over 6.5V only)

Figure 17. Cascading Devices for Greater Output Voltage Range.

When cascading devices, however, the power dissipation of each device must be considered. As each new stage is added, the previous stages will be subjected to more and more load current, from both the quiescent current of the new stage and the multiplying action of the load current through each of the stages, as shown

in Figure 18. As the number of cascaded devices increases, the effective output resistance also increases which will severely reduce the output voltage for a given current level when compared to a single inverter. This effect can be reduced by paralleling devices in the first stages, though the cost in parts increases twofold for every added stage.



$$\begin{aligned} V_{C1} &= V_B - R_O (3 I_L + 2 I_Q) & V_{OUT} &= -(3 V_B - R_O (14 I_L + 8 I_Q)) \\ V_{C2} &= V_B - R_O (5 I_L + 3 I_Q) \\ V_{C3} &= V_B - R_O (6 I_L + 3 I_Q) \end{aligned}$$

Figure 18. Current Model of Cascaded Voltage Converters.

CHANGING THE OSCILLATOR FREQUENCY

The typical oscillator frequencies were given in the description of the basic inverter circuit. However, Figure 19(a) shows that the maximum power efficiency is not achieved at the typical oscillator frequency. If maximum power efficiency is desired, an external capacitor can be connected between the OSC pin and ground. Figure 19(b) illustrates the effect of added capacitance on the oscillator frequency.

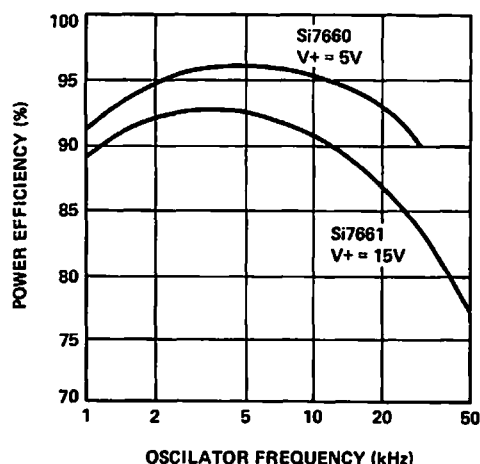


Figure 19(a). Graph of Efficiency Versus Oscillator Frequency.

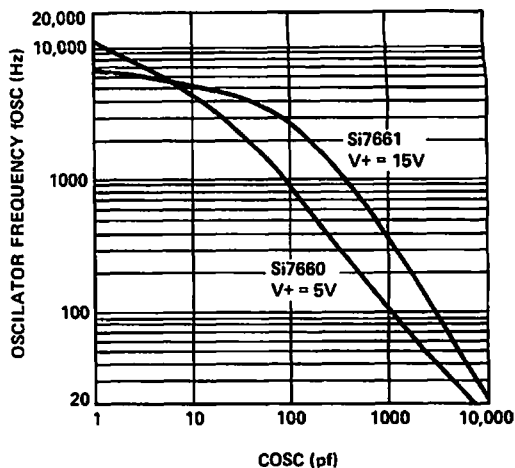


Figure 19(b). Graph of Oscillator Frequency Versus Added Capacitance.

If synchronization with an external driver or clock is needed, the OSC pin can be driven either by a TTL or CMOS logic gate. Figure 20 provides the proper circuits for interfacing to either logic standard. Note that the TTL interface can only be directly connected to the OSC pin if the circuit is using a 5 volt supply. If the input voltage is other than 5 volts, some type of buffer circuit will be required. The charge/transfer transitions will occur on each rising edge of the clock.

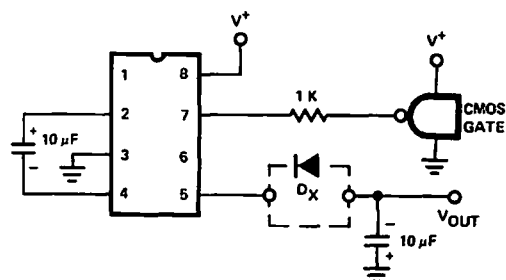


Figure 20(a). CMOS Drive Circuit for the Si7660 or Si7661.

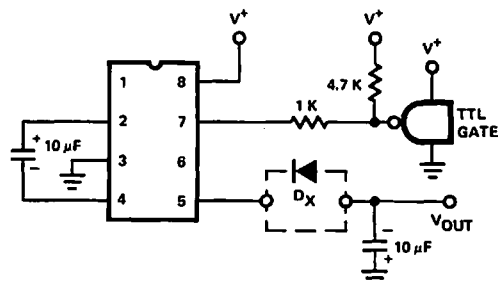


Figure 20(b). TTL Drive Circuit for the Si7660 or Si7661. (5 volt input only)

SPECIFIC APPLICATIONS

When looking at possible applications for the Si7660 and Si7661, it must be remembered that these devices are **VOLTAGE** sources, not **CURRENT** sources. Therefore, any heavy load will either greatly reduce the output voltage (possibly out of the desired range) or cause the device to go into power shutdown. If the concept of **VOLTAGE** conversion is kept in mind, many problems will be avoided.

There are many places where a low current negative supply made with an Si7660 or Si7661 would do just as well as a full conventional negative supply or DC-to-DC converter module. Some examples of possible uses are: power sources for operational amplifiers, dynamic RAM's, microprocessors, and data conversion products. Several examples of these systems are given below.

MEMORIES

Several different memory manufacturers produce 16K x 1 dynamic RAM's that have a need for a -5 volt low current supply to provide substrate biasing. The National MM5290, AMD MD9016, and MOSTEK MK4116 all use this type of arrangement. Table 2 gives the -5 volt supply current requirements for each of these devices.

Table 2. Current Requirements of Several Different Dynamic RAM's

Device	Operating Current	Standby Current	Refresh Current
MM5290 (0 to 70°C)	200 μ A	100 μ A	200 μ A
MD9016 (0 to 70°C)	200 μ A	100 μ A	200 μ A
(-55 to 85°C)	400 μ A	200 μ A	400 μ A
MK4116 (0 to 70°C)	200 μ A	100 μ A	200 μ A

The only constraint in using the Si7660 or Si7661 for this application is when calculating the voltage fluctuations that will occur when a location is read from or written to. Make sure that the **ABSOLUTE MAXIMUM** current is considered so that the negative supply for the dynamic RAM will not be pulled down more than 5% (below 4.75 volts) during a memory read or write. Even with the maximum current taken into account, the Si7660 or

Si7661 could easily provide the negative supply voltage supply for an entire 16K x 8 dynamic memory bank.

OP-AMPS

Operational amplifiers are one of the most commonly used integrated circuits and often use negative supply voltages. Although some op-amps can supply high current loads, more often the current requirements involved are well within the capabilities of the Si7661.

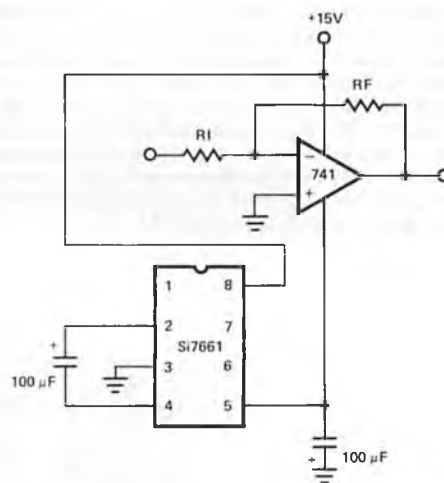


Figure 21. Using the Si7661 to Generate the Negative Rail for a 741 Op-amp.

Figure 21 shows the Si7661 supplying the negative voltage to a 741 op-amp configured as an inverting amplifier. As the current drain through the negative supply terminal of the op-amp increases, the output voltage of the Si7661 will decrease. However, this will not affect the output capability of the op-amp at its rated output current. Figure 22 illustrates this with a photograph of the input and output of the circuit in Figure 21 when a 1 kilohm load was placed on the amplifier output. The output was undistorted to 26 volts peak-to-peak.

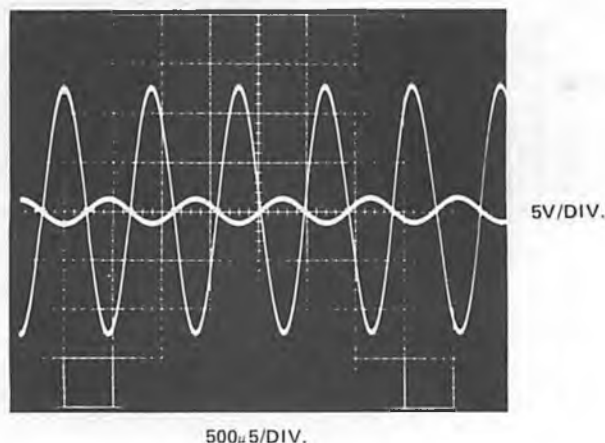


Figure 22. Output of the 741 Inverting Amplifier at Maximum Undistorted Output.

The output ripple of the Si7661 must be taken into consideration when using it as an op-amp supply. Some op-amps do not have adequate power supply rejection to withstand the ripple noise level of the Si7661. The pump and reservoir capacitors can be chosen to minimize this noise condition (see Table I). The ripple should be measured at the maximum negative supply current (i.e., rated load) to determine if the Si7661 can be used to supply the op-amp.

ANALOG SWITCHES

Although in most cases the Si7660 or Si7661 cannot supply sufficient current for analog switch applications, there are sometimes exceptions. For example, Figure 23 gives the schematic diagram of a circuit that was used to interface a Northern Telecom telephone set to an ICOM 2AT 2-meter amateur radio transceiver.

The analog switch provides isolation for the microphone and speaker connections of the transceiver since the telephone set uses a single path for the both transmission and reception. The telephone was operated at 12 volts for direct interface to the DG305A, and the supply current from the Si7661 was < 1 mA.

MICROPROCESSORS

Some of the older standard microprocessors need a negative supply for substrate biasing. The Intel 8080 microprocessor is a good example of this. It is an inexpensive 8-bit CPU that has many different available support chips. To provide the negative supply voltage (-5 volts), a basic inverter circuit (such as in Figure 8) using an Si7660 is connected to pin 11 of the microprocessor. The 8080 negative supply draws a maximum current of 1 mA which will not pull down the supply voltage to any great degree.

DATA CONVERSION

Data conversion and acquisition products often have the same problem as op-amps, in that noisy supply voltages can cause operational problems. However, the problems caused here can have a much greater impact on the operation of the A/D or D/A converter. Since power supply stability can be an important factor in specifying nonlinearity for data conversion products, it is easy to understand that slight fluctuations in supply voltage could be disastrous to a precision measurement system.

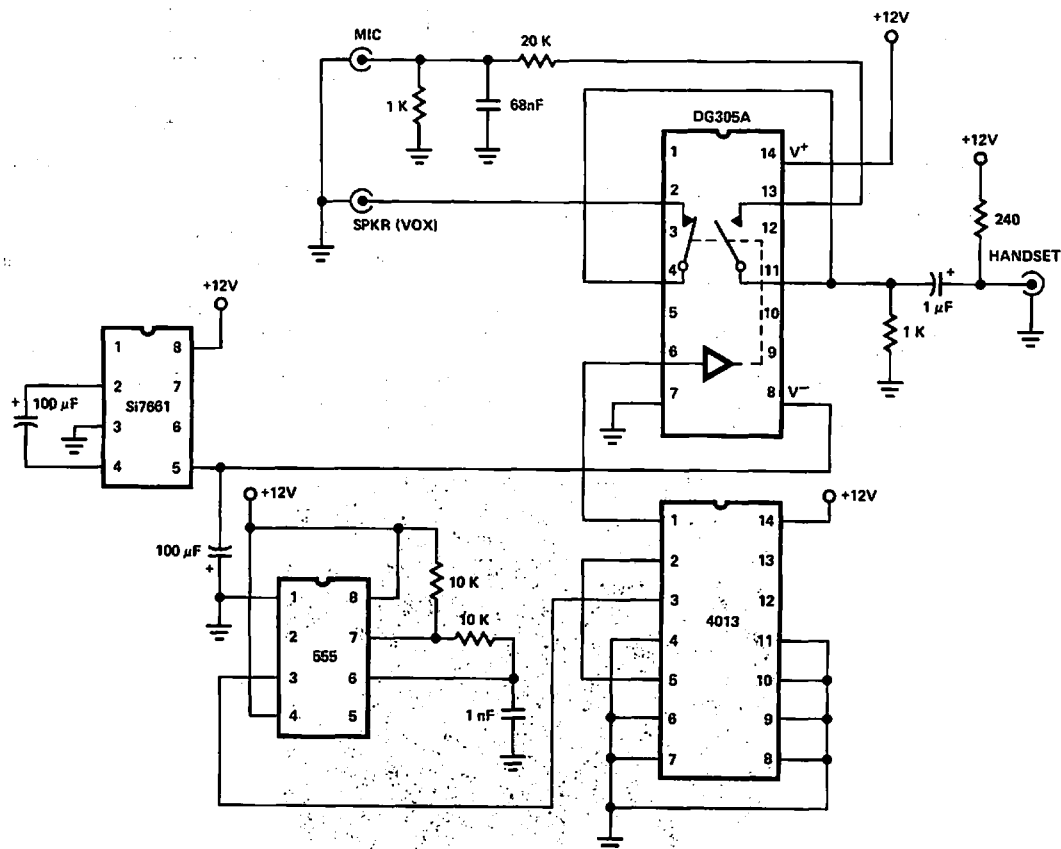


Figure 23. Using the Si7661 to Supply a Low-current Analog Switch Current.

The Siliconix Si7135 is a $4\frac{1}{2}$ digit integrating A/D converter that requires a negative supply when operating over a $\pm$ input voltage range. Figure 24 gives the schematic diagram of a DVM

circuit using the Si7661 to supply the negative voltage for the Si7135.

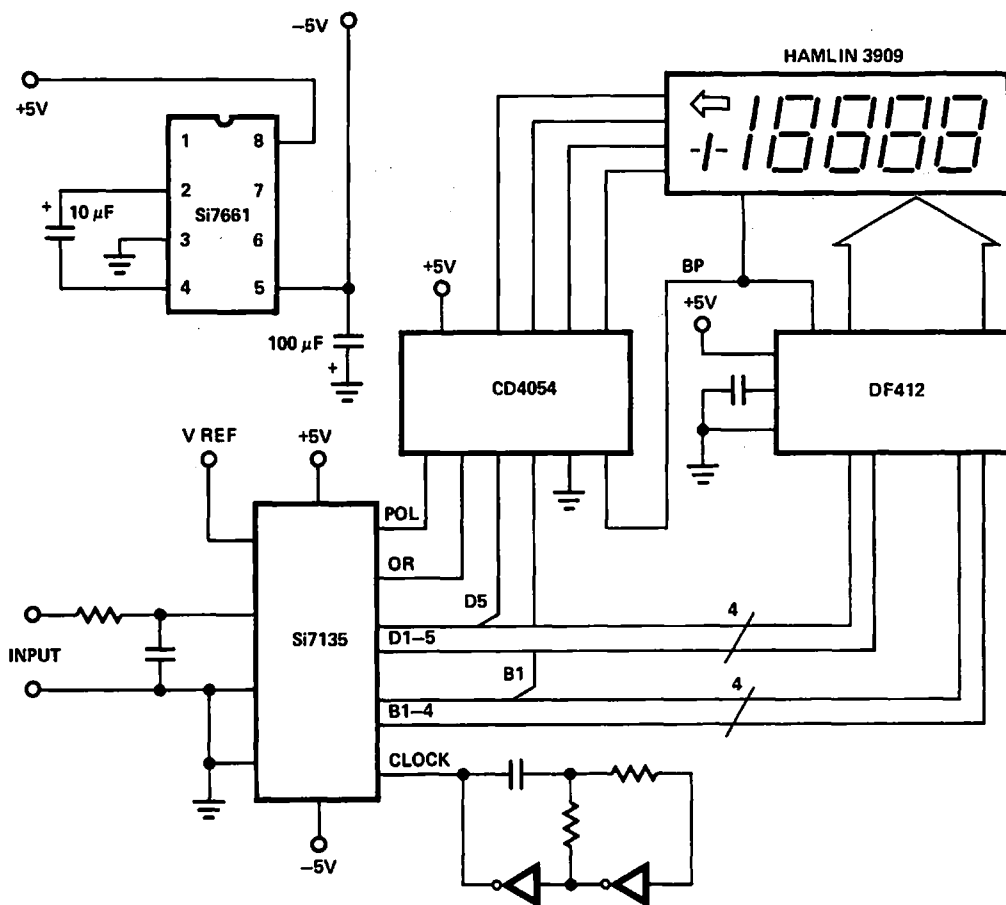


Figure 24. Si7661 Used in a DVM Circuit.

REGULATOR CIRCUITS

This section discusses some of the possible methods for using the Si7660 or Si7661 in constant-voltage output circuits over a given output current range. For low current inverter applications, the circuit shown in Figure 25 can be used. The output impedance of the circuit can be as low as 5 ohms with regulation up to approximately 20 mA. Note that if converters are paralleled on the output of this circuit, they should be synchronized to minimize output voltage fluctuations and output noise.

Another regulator circuit uses the Si7660 or Si7661 in a positive voltage regulator. Conventional three terminal voltage regulators have a voltage drop of greater than 1 volt between the input and output when operating at fairly heavy load currents. The circuit given in Figure 26 uses an Si7660 or Si7661 voltage converter to double the voltage which is then regulated by the op-amp and FET. This configuration allows regulation without the voltage drop as long as the input voltage does not drop below the zener voltage plus the product of I_D times $R_{DS(on)}$.

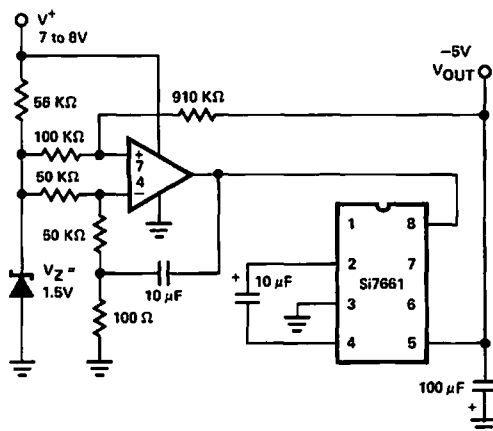


Figure 25. Low Current Inverting Regulator Circuit.

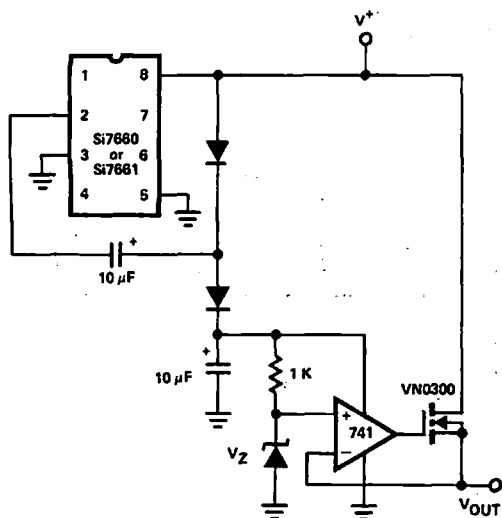


Figure 26. Schematic Diagram of the Positive Regulator Circuit.

For $I_D = 50 \text{ mA}$:

$$\begin{aligned} V_{in} &> V_Z + (I_D \times R_{DS(on)}) \\ V_{in} &> 5.2\text{V} + (50 \text{ mA} \times 1.2) \\ V_{in} &> 5.26 \text{ V} \end{aligned} \quad (3)$$

Therefore, as long as the input voltage does not drop below 5.26 volts, the input is guaranteed to be regulated as close to the zener voltage as can be attained by the common mode offset voltage of the op-amp. By selection of the zener diode, this circuit can supply more than 100 mA and can be adjusted for varying voltage outputs up to the input voltage limit of the voltage converter being used.

CONCLUSION

The Si7660 and Si7661 can be an inexpensive alternative to full negative supplies in many different low cost applications. Although they are designed for generation of negative voltages, many different voltage levels can be generated with a few additional parts. The Si7660 and Si7661 are pin compatible to competitive products and function as well or better than the competition in every operating specification. The examples given here are only a few of the many possible applications that could utilize the benefits of reduction in board space and cost that the Si7660 and Si7661 provide.

ACKNOWLEDGEMENTS

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UTILITY GATE ARRAY LOGIC SIMULATION WITH A PERSONAL COMPUTER

John Conover
November 1983

Introduction

Utility logic simulation programs are "indispensable" for gate array design in MSI/remedial logic conversion and test program generation. Although these are available through time-share services and as "canned programs" for mainframes and work stations, a personal computer is capable of executing a variety of simulations where "through put" and complexity are secondary to cost. The following program is written in simple Basic for the Timex/Sinclair 1000 and is, although a general simulation program, specifically tailored for gate array design.

Usually, a potential gate array design is "bread boarded" with standard LPS-MSI devices and converted to remedial logic functions for integration by a gate array manufacturer. Many of the major manufacturers will provide documentation, upon request, for the existing remedial logic cells that are available for use in their gate array products. The simulation program listing in the appendix includes the cells used by Siliconix, Universal Semiconductor and Nitron, etc. These are outlined in their respective design manuals.

The program requires at least a 16K memory module.

Unless hard copy documentation is desired, a printer is not necessary. Line 10 is a listing of the formats used to specify the different resident logic cells in the program net list. The program assigns the same unit time delay to all cells to conserve memory. All inverters (including I/O buffers, etc.) are specified by "in." The complex gate structures listed in the manufacturer's documentation may be implemented with the resident AND, OR and BUFF (i.e. buffer) cells. Multiple input combinational gates are expandable from two through six inputs by specifying the appropriate two through six input nodes in the "net list" data.

Lines 1030 to 1090 describe and initialize the circuit shown in Fig. 1 to illustrate program use. "Run" will result in Fig. 2 being displayed on the monitor. It represents 10 clock/bit times of the simulated timing diagram for Fig. 1. Zero clock number corresponds to the circuit states forced by the initializing conditions. If the initializing conditions are not valid, the program will alter the initial conditions so that a valid state exists prior to continuing execution. The circuit of Fig. 1. contains over 50 transistors. The time of execution to derive the timing diagram of Fig. 2. is just over 2 minutes.

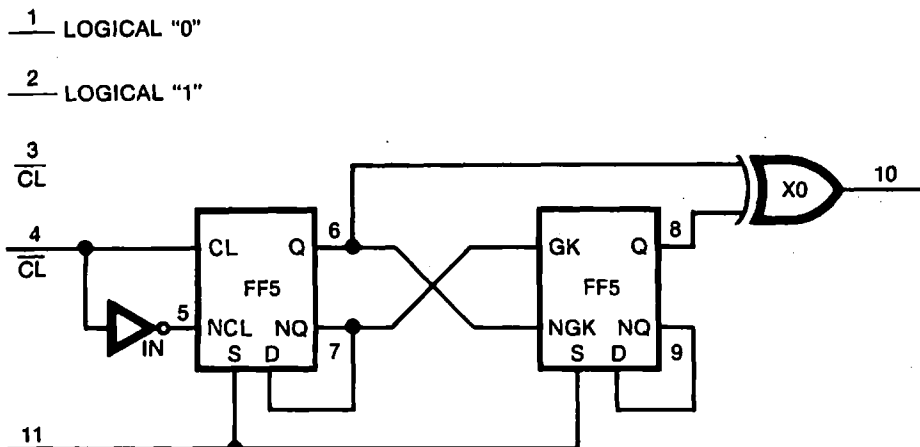


FIGURE 1
Illustrative Circuit

To use the program, purge the data for Fig. 1 (lines 1030 to 1090, 100, and 2040 - Fig. 1's net list/initializations, node format, and node 11's source generation, respectively.) Number the nodes of the circuit to be analyzed using consecutive numbers for multiple output gates. Using the formats outlined in lines 10, 20, and 30, input the circuit net list/initializations, node format, and source generation statements. The source generation statements, consisting of simple "basic statement" and complex patterns, can be derived with relatively few program lines. Lines 20 and 30 also contain information concerning the display initialization and format which can be modified if a printer is resident. They should be deleted to conserve memory space.

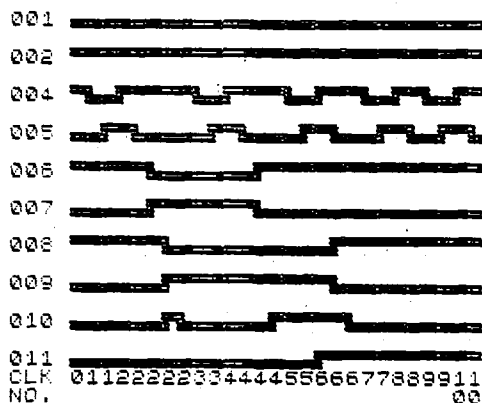


FIGURE 2
Simulated Timing Diagram for Figure 1.

The proceeding program may be applied to several gate array design methodologies. Generally, gate array manufacturers require that synchronous logic be utilized, with a maximum fan-out of five unit loads, depending on the gate geometry, throughout the design. (A unit load is defined as 1 minimum geometry inverter.) When fanning up, it is perfectly permissible to parallel gates to achieve this criterion. TTL suppliers give liberal information, including schematics, on many of the more frequently used 7400 series devices. These may be reconfigured, using the remedial cells in the program circuit function verification. Since the program is written in simple basic, entire "macro" algorithms may be derived as outlined in the program description.

The simulation program may also be used to verify the effectiveness of a testing format. An abbreviated test format that mimics the actual gate array system I/O requirements may be derived from the system architecture and evaluated by simulation. Most manufacturers require that a "device reset" function be incorporated for testability that sets all nodes in the gate array to a known state. The simulation program may then be used to verify that the subsequent outputs are valid for a specific input bit/clock pattern (i.e. test format). This information should be included in the design package that is submitted to the gate array vendor.

Fig. 3 is a flow diagram of the "state" algorithm. One loop pass constitutes a "unit time delay," during which, each gate is interrogated to determine its next output state. The collective states are maintained, to conserve memory, se-

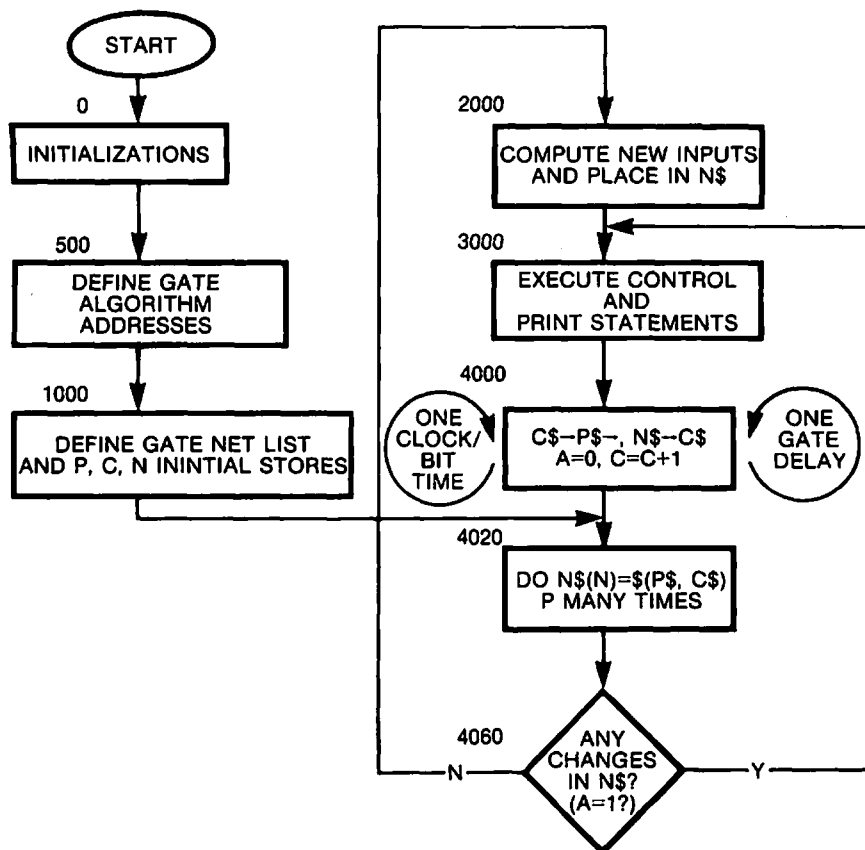


FIGURE 3
Flow Diagram of State Algorithm

quentially in three "string" registers, PS, CS, and NS. These registers represent the previous, (T-1), current, (T), and next, (T+1), collective states respectively. The variable N is the node (gate) pointer and always points to GS (N), the gate type, and interconnect net list for node N. Specifically, for the next state of node N:

$$NS(N) = f(PS, CS) \\ 1 \leq N \leq P$$

where f is the functional (logic) relationship of the Nth gate specified by GS (N). Again, "strings" are used, to conserve memory for GS. Each node is assigned the same number as the gate driving it excepting multiple output gates in which the output nodes are numbered sequentially, starting with N, for the Nth gate.

The program solves NS (N), sequentially for N = 1 to P.

If any character in NS is altered, the variable A is set, initiating another loop pass at the conclusion of the current pass. Additionally, at the conclusion of each pass, the previous state (PS) is replaced by the current circuit state (CS), and CS is replaced by the next circuit state (NS) which has just been altered in the last pass - i.e. one propagation delay or unit time delay has occurred for the circuit. This branching scheme ensues until a complete pass is achieved with no change in NS, (A = 0), signifying that a valid state for all nodes has been achieved with the current set of inputs. The program then diverts to a routine that places new inputs into NS, increments the clock bit time counter, C, and returns to the state algorithm to solve the circuit states for the next clock bit time. One major loop, from alter inputs - to alter inputs, constitutes one clock bit time. Referring to the appendix, the state algorithm occupies lines 4000 to 4070, inclusively.

Table 1 is a description of the system variables, and Table 2 is a listing of the variable dimensioning in memory. Each resident gate algorithm is treated as a variable with the algorithm address (argument) set equal to the variable name (gate name). Line 4040 executes a "go to (gate name)" and is vectored to the appropriate line number to execute a specific gate algorithm.

Table 3 is a list of the first and last line numbers for the various program functions. Table 4 is a list of the first and last line numbers of the resident gate algorithms. These algorithms may call one or both of the routines starting at 4080 and/or 4140. These routines are for "looking up" the current and previous states, respectively, of the inputs listed in GS (N). The current states are contained in AS and the previous states in BS. 4100 and 4160 detect if an input in GS (N) is "blank," and if it is, the input "look up" is terminated. This technique implements the "expandable" gate functions - NAND, NOR, AND and OR. The general format of all gate algorithms is of the form:

1. Set QS = (Default Value)
2. If Inputs = (True) Then Alter QS Accordingly

Combinational logic, of course, is dependent only on CS. Any edge triggered (memory) device is dependent on CS and PS - i.e. a DFF clock must be "O" previously and "1" currently, constituting a "rising edge," to clock D to Q. Several of the gate algorithms "call" (actually a "go to") other algorithms of a more general nature - i.e. a DFF with reset uses the RS DFF algorithm to conserve memory space. All gate algorithms exit with the gate state(s) in QS and vector to line 4200. Line 4200 increments N by the number of outputs contained in QS minus one, and 4210 compares QS with the corresponding values in NS. If the comparison is true, a "return" is executed. If not, QS is incorporated into NS and the variable A set to one, prior to "returning." The re-entry address is always line 4050 of the state algorithm.

Line 110 sets P equal to the number of nodes to be simulated, and line 120 sets the maximum number of inputs a gate may have to six. Lines 130 through 230 dimension the

TABLE 1
Program Variables

P = Number of Nodes to be Analyzed.	FF3 = Address of FF3 Algorithm
D = Number of Nodes to be Displayed	FF4 = Address of FF4 Algorithm
I = Utility Loop Counter	FF5 = Address of FF5 Algorithm
Q = Maximum Number of Inputs/Gate	FF6 = Address of FF6 Algorithm
R = $2 + 3 * Q$ = Length of GS + 4	T1 = Address of T1 Algorithm
C = Clock State Counter	T2 = Address of T2 Algorithm
A = State Resolved Flag	L1 = Address of L1 Algorithm
N = Node Pointer in Analysis Algorithm	L2 = Address of L2 Algorithm
NA = Address of NA Algorithm	L3 = Address of L3 Algorithm
NO = Address of NO Algorithm	T5 = Address of T5 Algorithm
IN = Address of IN Algorithm	E\$ = Number of Nodes + Node Numbers to be Displayed
FF7 = Address of FF7 Algorithm	G\$ = Net List Data
XN = Address of XN Algorithm	PS = Sequential List of Previous States
AND = Address of AND Algorithm	CS = Sequential List of Current States
ON = Address of ON Algorithm	NS = Sequential List of Next State
XO = Address of XO Algorithm	QS = Temporary Storage of Output States of a Particular Gate
BUF = Address of BUF Algorithm	AS = Utility String Storage
FF1 = Address of FF1 Algorithm	BS = Utility String Storage
FF2 = Address of FF2 Algorithm	D\$ = Display String

TABLE 2
Variable Dimensions

D\$ is dimensioned to D + 3, 32
 G\$ is dimensioned to P, 4 + 3 * Q
 PS is dimensioned to P
 CS is dimensioned to P
 NS is dimensioned to P

TABLE 3
Program Line Allocations

0 ↓ 30	Remarks	3000 ↓ 3980	Display/Print/Control Statements
100 ↓ 250	Initialization/Dimension of Memory	3990 ↓ 4070	State Analysis Algorithm
300 ↓ 370	Display Dimensioning & Initialization	4080 ↓ 4130	Fetch Current States Routine
500 ↓ 700	Definition of Gate Name/Algorithm Addresses	4140 ↓ 4190	Fetch Previous States Routine
1000 ↓ 1980	Definition of G\$, Initialization of P\$, C\$, N\$	4200 ↓ 4240	Alter N\$ Routine
2000 ↓ 2990	Clock/Source Algorithm(s)	5000 ↓ 9990	Gate Algorithms

memory as per table 2 setting all states to default "0" and all G\$ gates to "NOR." Lines 300 to 370 dimension D\$ to the number of nodes to be displayed and format the display screen. Lines 400 to 710 define the gate algorithm starting addresses. Line 710 is an "NOR" gate, and if encountered by the state algorithm, will result in N being incremented with no alterations to any state string.

Lines 1000 through 1980 are for G\$ (net list) and state initializations. Lines 2000 through 2990 are for clock and source statements. Lines 2000 through 2030 are the resident clock generations, with lines 2010 and 2030 determining the positive and negative clocks, respectively, depending on whether variable C is odd or even. Lines 3000 through 3980 are for control/print statements. Printing

"If A = 0" will result in only the final states being displayed and is useful for test program documentation. Other useful control statements are of the form; if C = (number) then STOP, SLOW, etc.

The program is memory efficient due to the utilization of string variables for all the major data manipulations. Although a program could be devised to input data into the dimensioned string variables, this data would be "invisible" and execution of "run" or "clear" would be catastrophic. Further, although machine code algorithms are an attractive alternative to speed up program execution, the inherent utility and simplicity of "Basic" would be destroyed. It is interesting to note that the algorithm that actually creates the simulation, lines 4000 to 4070, consists of only eight program lines.

TABLE 4
Gate Algorithm Line Numbers

5000 } No Op	5180 } FF7	5410 } Exclusive OR	5590 } FF3	5830 } T1
5010 }	5240 }	5440 }	5620 }	5860 }
5020 } Nand	5250 } Exclusive Nor	5450 } Buffer	5630 } FF4	5870 } T2
5070 }	5280 }	5480 }	5680 }	5920 }
5080 } Nor	5290 } AND	5490 }	5590 } FF5	5930 } L1
5130 }	5340 }	5520 } FF1	5740 }	5970 }
5140 } Inverter	5350 } OR	5530 } FF2	5750 }	
5170 }	5400 }	5580 }	5820 } FF6	

Appendix

```

00REM  GATE ARRAY
      LOGIC SIMULATION
      JOHN CONOVER-1983
10 REM  STATEMENT 100 OUTPUT (S)
NA  A  B  ...  0=>N
NO  A  B  ...  0=>N
IN  A  B  ...  0=>N
FF1 CK NCKD  0=>N,NQ=>N+1
FF2 CK NCKD  NR  0=>N,NQ=>N+1
FF3 CK NCKD  3  0=>N,NQ=>N+1
FF4 CK NCKD  N5  0=>N,NQ=>N+1
FF5 CK NCKD  5  0=>N,NQ=>N+1
FF6 CK NCKD  NR N5  0=>N,NQ=>N+1
FF7 CK NCKD  5  0=>N,NQ=>N+1
T1  CK NCK  0=>N,NQ=>N+1
T2  CK NCKNR  0=>N,NQ=>N+1
L1  CK NCKD  0=>N,NQ=>N+1
L2  CK NCKD  NR  0=>N,NQ=>N+1
L3  CK NCKD  5  0=>N,NQ=>N+1
XN  A  B  0=>N
XO  A  B  0=>N
TS  E  NE IN  0=>N
AND A  B  ...  0=>N
OR  A  B  ...  0=>N
BUF IN  0=>N

20 REM LINE 100 DEFINES E$, A
   STRING OF 3 DIGIT NUMBERS,
   BEGINNING WITH THE NUMBER OF
   NODES TO BE SIMULATED, AND THE
   NODE NUMBERS TO BE DISPLAYED.
   THERE ARE NO SEPARATOR SYMBOLS
   REQUIRED. LINES 1000-1980 ARE
   FOR G$(N) DATA. THE CIRCUIT NET
   LIST WHICH MUST BE COMPATABLE
   WITH LINE 10 AND STARTING
   STATE INITIALIZATIONS, P$,C$ AND
   N$. G$(N) MUST BE OF THE FORMAT:
1000 LET G$(1)="NA 002003004"
   WHICH SPECIFIES THAT NODE 1 IS
   THE OUTPUT OF AND GATE WITH
   INPUTS=NODES 2,3 AND 4. GATES
   EXIST THAT REQUIRE MORE THAN 1
   OUTPUT. THESE OUTPUT NODES MUST
   BE NUMBERED SEQUENTIALLY AS PER
   LINE 10. LINES 300-390 ARE FOR
   INITIALIZING THE DISPLAY
   ALGORITHM.
30 REM P$(3),C$(3) AND N$(3)
   ARE THE PREVIOUS, CURRENT AND
   NEXT STATES OF NODE 3. P$,C$ AND
   N$ INITIALIZATION IN LINES
1000-1980 IS OF THE FORMAT:
1010 LET P$(4 TO 5)="01", ECT.
   DEFAULT IS A LOGICAL "0". LINES
2000-2990 CONTROL SOURCES AND
   CLOCKS. THESE SET N$ ONLY AND
   ARE OF THE FORMAT (FOR C=31):
2000 IF C=30 THEN LET N$(5)="1",
   WHERE C IS THE CLOCK INTERVAL
   COUNT. THIS STATEMENT SETS NODE
   5 TO A LOGICAL "1" AT THE
   INITIATION OF THE 31ST CLOCK
   INTERVAL. NODE 5 WILL REMAIN IN
   THIS STATE UNTIL ALTERED. NODES
   1,2,3 AND 4 ARE COMMITTED TO
   LOGICAL "0", "1", POSITIVE AND
   NEGATIVE CLOCKS, RESPECTIVELY.
   LINES 3000-3980 ARE FOR THE
   DISPLAY ALGORITHM.
100 LET E$="0110010020040050060
07008009010011"
110 LET P=VAL E$(1 TO 3)
120 LET Q=6
130 LET R=2+3*Q
140 DIM G$(P,4+3*Q)
150 DIM P$(P)
160 DIM C$(P)
170 DIM N$(P)
180 FOR I=1 TO P
190 LET G$(I)="NOP"
200 LET C$(I)="0"
210 NEXT I
220 LET N$=C$
230 LET P$=C$
240 LET C=0
250 LET A=1
300 LET D=LEN E$/3-1
310 IF D>10 THEN LET D=10
320 DIM D$(D+3,32)
330 FOR I=1 TO D
340 LET D$(I+1 TO 3)=E$(3*I+1
   TO 3*I+3)
350 NEXT I
360 LET D$(D+1)(1 TO 3)="CLK"
370 LET D$(D+2)(1 TO 3)="NO,"
380 LET NA=5000
390 LET NO=5000
400 LET IN=5140
410 LET FF7=5180
420 LET XN=5250
430 LET AND=5290
440 LET OR=5350
450 LET XO=5410
460 LET BUF=5450
470 LET FF1=5490
480 LET FF2=5530
490 LET FF3=5570
500 LET FF4=5610
510 LET FF5=5650
520 LET FF6=5690
530 LET T1=5730
540 LET T2=5770
550 LET L1=5810
560 LET L2=5850
570 LET L3=5890
580 LET TS=5930
590 LET NOP=5970
1000 LET P$(1 TO 4)="0101"
1010 LET C$(1 TO 4)="0101"
1020 LET N$(1 TO 4)="0101"
1030 LET G$(5)="IN 004"
1040 LET G$(5)=FF5 004005007011
1050 LET G$(8)=FF5 007006009011
1060 LET G$(10)="XO 006008"
1070 LET P$(5 TO 10)="0101000"
1080 LET C$(5 TO 10)="0101000"
1090 LET N$(5 TO 10)="0101000"
1990 GOTO 4020
2000 LET N$(3)="1"
2010 IF C/2-INT (C/2)>=.25 THEN
   LET N$(3)="0"
2020 LET N$(4)="1"
2030 IF C/2-INT (C/2)<=.25 THEN
   LET N$(4)="0"
2040 IF C=5 THEN LET N$(11)="1"
3000 FOR I=1 TO D
3010 LET A$=P$(VAL D$(I)(1 TO 3))
3020 LET B$=C$(VAL D$(I)(1 TO 3))
3030 IF A$="0" AND B$="0" THEN L
   ET A$="1"
3040 IF A$="0" AND B$="1" THEN L
   ET A$="1"
3050 IF A$="1" AND B$="0" THEN L
   ET A$="1"
3060 IF A$="1" AND B$="1" THEN L
   ET A$="1"
3070 LET D$(I)=D$(I)(1 TO 3)+D$(
   I)(5 TO 31)+A$
3080 NEXT I
3090 LET A$=STR$ C+ " "

```

Appendix

```

3100 FOR I=1 TO 3
3110 LET D$(I+D)=D$(I+D) (1 TO 3)
+D$(I+D) (5 TO 31)+A$(I)
3120 NEXT I
3130 FOR I=1 TO D
3140 PRINT AT 2*(I-1),0;D$(I)
3150 NEXT I
3160 FOR I=1 TO 3
3170 PRINT AT 2*D-2+I,0;D$(D+I)
3180 NEXT I
3990 IF A=0 THEN LET C=C+1
4000 LET P=C#
4010 LET C=N#
4020 LET A=0
4030 FOR N=1 TO P
4040 GOTO VAL G$(N) (1 TO 4)
4050 NEXT N
4060 IF A=0 THEN GOTO 2000
4070 GOTO 3000
4080 LET A$=""
4090 FOR I=5 TO R STEP 3
4100 IF G$(N)(I)="" THEN RETURN

4110 LET A$=A$+C$(VAL G$(N) (I TO
I+2))
4120 NEXT I
4130 RETURN
4140 LET B$=""
4150 FOR I=5 TO R STEP 3
4160 IF G$(N)(I)="" THEN RETURN

4170 LET B$=B$+P$(VAL G$(N) (I TO
I+2))
4180 NEXT I
4190 RETURN
4200 LET N=N-1+LEN Q$
4210 IF N$(N+1-LEN Q$ TO N)=Q$ T
HEN GOTO 4050
4220 LET N$(N+1-LEN Q$ TO N)=Q$
4230 LET A=1
4240 GOTO 4050
5000 LET Q$=C$(N)
5010 GOTO 4200
5020 LET Q$="0"
5030 GOSUB 4030
5040 FOR I=1 TO LEN A$
5050 IF A$(I)="0" THEN LET Q$="1"

5060 NEXT I
5070 GOTO 4200
5080 LET Q$="1"
5090 GOSUB 4030
5100 FOR I=1 TO LEN A$
5110 IF A$(I)="1" THEN LET Q$="0"

5120 NEXT I
5130 GOTO 4200
5140 LET Q$="0"
5150 GOSUB 4030
5160 IF A$(1)="0" THEN LET Q$="1"

5170 GOTO 4200
5180 GOSUB 4030
5190 GOSUB 4140
5200 LET Q$=C$(N TO N+1)
5210 IF B$(1 TO 2)<>"10" AND A$(
1 TO 5)="10000" OR A$(4 TO 5)="1
0" THEN LET Q$="01"
5220 IF B$(1 TO 2)<>"10" AND A$(
1 TO 5)="10100" OR A$(4 TO 5)="0
1" THEN LET Q$="10"
5230 IF A$(4 TO 5)="11" THEN LET
Q$="11"
5240 GOTO 4200
5250 LET Q$="0"
5260 GOSUB 4030
5270 IF A$(1)="0" AND A$(2)="0"

OR A$(1)="1" AND A$(2)="1" THEN
LET Q$="1"
5280 GOTO 4200
5290 LET Q$="1"
5300 GOSUB 4030
5310 FOR I=1 TO LEN A$
5320 IF A$(I)="0" THEN LET Q$="0"

5330 NEXT I
5340 GOTO 4200
5350 LET Q$="0"
5360 GOSUB 4030
5370 FOR I=1 TO LEN A$
5380 IF A$(I)="1" THEN LET Q$="1"

5390 NEXT I
5400 GOTO 4200
5410 LET Q$="1"
5420 GOSUB 4030
5430 IF A$(1)="0" AND A$(2)="0"
OR A$(1)="1" AND A$(2)="1" THEN
LET Q$="0"
5440 GOTO 4200
5450 LET Q$="0"
5460 GOSUB 4030
5470 IF A$(1)="1" THEN LET Q$="1"

5480 GOTO 4200
5490 GOSUB 4030
5500 GOSUB 4140
5510 LET A$=A$+"00"
5520 GOTO 5200
5530 GOSUB 4030
5540 GOSUB 4140
5550 IF A$(4)="1" THEN LET A$=A$
+"00"
5560 IF A$(4)="0" THEN LET A$=A$
+"10"
5570 LET A$=A$(1 TO 3)+A$(5 TO 6)
5580 GOTO 5200
5590 GOSUB 4030
5600 GOSUB 4140
5610 LET A$=A$+"0"
5620 GOTO 5200
5630 GOSUB 4030
5640 GOSUB 4140
5650 IF A$(4)="1" THEN LET A$=A$
+"00"
5660 IF A$(4)="0" THEN LET A$=A$
+"01"
5670 LET A$=A$(1 TO 3)+A$(5 TO 6)
5680 GOTO 5200
5690 GOSUB 4030
5700 GOSUB 4140
5710 IF A$(4)="1" THEN LET A$=A$
+"01"
5720 IF A$(4)="0" THEN LET A$=A$
+"00"
5730 LET A$=A$(1 TO 3)+A$(5 TO 6)
5740 GOTO 5200
5750 GOSUB 4030
5760 GOSUB 4140
5770 IF A$(4 TO 5)="00" THEN LET
A$=A$+"11"
5780 IF A$(4 TO 5)="01" THEN LET
A$=A$+"10"
5790 IF A$(4 TO 5)="10" THEN LET
A$=A$+"01"
5800 IF A$(4 TO 5)="11" THEN LET
A$=A$+"00"
5810 LET A$=A$(1 TO 3)+A$(6 TO 7)
5820 GOTO 5200
5830 GOSUB 4030

```

Appendix

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5840 GOSUB 4140
5850 LET A$=A$+C$(N+1)+"00"
5860 GOTO 5200
5870 GOSUB 4080
5880 GOSUB 4140
5890 IF A$(3)="1" THEN LET A$=A$
+C$(N+1)+"00"
5900 IF A$(3)="0" THEN LET A$=A$
+C$(N+1)+"10"
5910 LET A$=A$(1 TO 2)+A$(4 TO 6
)
5920 GOTO 5200
5930 LET Q$=C$(N TO N+1)
5940 GOSUB 4080
5950 IF A$="100" THEN LET Q$="01"
"
5960 IF A$="101" THEN LET Q$="10"
"
5970 GOTO 4200
5980 LET Q$=C$(N TO N+1)
5990 GOSUB 4080
6000 IF A$="1001" OR A$(4)="0" T
HEN LET Q$="01"
6010 IF A$="1011" THEN LET Q$="1
0"
6020 GOTO 4200
6030 LET Q$=C$(N TO N+1)
6040 GOSUB 4080
6050 IF A$="1010" OR A$(4)="1" T
HEN LET Q$="10"
6060 IF A$="1000" THEN LET Q$="0
1"
6070 GOTO 4200
6080 LET Q$=C$(N)
6090 GOSUB 4080
6100 IF A$="101" THEN LET Q$="0"
6110 IF A$="100" THEN LET Q$="1"
6120 GOTO 4200

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Introduction

Siliconix is committed to your future system designs. As a multinational semiconductor manufacturer, we offer some of the industry's broadest product lines. No one gives you more analog switch ICs and MOSPOWER to choose from. Our multiple technologies include DMOS, VMOS, CMOS, PMOS, PMOS/bipolar and bipolar. And we are constantly advancing semi-custom state-of-the-art technology.

SMALL SIGNAL FETs

Siliconix is an industry leader in the manufacture of Small Signal FETs, offering a broad line of Junction Field Effect Transistors, MOS Field Effect Transistors, and DMOS Field Effect Transistors. Each line of transistors offers high-performance characteristics for such applications as low-noise, low-frequency amplifiers, low-drive DC amplifiers, high-frequency amplifiers on oscillators (to 1GHz), ultra-low operating gate currents (to 10^{-13} Amp), and high-speed analog switching (under 1ns).

Junction FETs are also used in N-channel monolithic and discrete pairs for a wide variety of use as high-performance amplifiers.

Siliconix offers a wide variety of package combinations, ranging from hermetic packaging to plastic packaging. The SOT package offers 100% testing capability and has reduced space requirements. Also offered are products in chip form to address hybrid requirements.

MOSPOWER

MOSPOWER identifies the "up front" technology that places Siliconix among the leaders in power device development for the 1980's, and has helped make Siliconix *the Discovery Company*.

MOSPOWER is a generic name coined by Siliconix to identify not only Siliconix's expanding family of medium and high power MOSFETs, but *all* power MOSFETs. The name also covers the many technologies used in the manufacture of these power MOSFETs which have been identified by various trade names. Vertical DMOS (double-diffused MOS); metal-gate V-groove MOS for high-frequency; lateral DMOS technology for arrays — all are covered by this generic name: MOSPOWER.

Analog Switch ICs

Siliconix JFET, MOSPOWER and Integrated Circuit (IC) technologies have been utilized to produce an extensive family of Analog Switch ICs. They are used in many high-reliability military and aerospace applications such as Mercury, Gemini, Apollo and Skylab manned space programs. The family of analog switch ICs includes monolithic multi-channel switches with integral drivers. Also high performance JFET switches packaged with IC drivers offering very low ON-resistance, fast switching, excellent frequency response (DG180 series); low spike feed-through, low leakage and high OFF-isolation (DG281); low cost, single or dual supply operation (DG308, DG211); low consumption CMOS switches (DG300 series) and multiplexers with up to 16 channels (DG506A). The recent addition to the range of analog switch ICs is the Plus-40 enhanced DG5040 series with guaranteed safe operation up to 44V, and DG243CJ, the dual make-before-break equivalent of the DG5043CJ.

LSI/Linear Circuits

Siliconix is an industry leader in telecommunications circuits, A/D conversion and micropower linears. The Company's LSI or linear ICs are incorporated in products ranging from sophisticated instrumentation to consumer smoke detectors. Advanced processing capabilities used in the manufacture of such ICs range from high and low voltage CMOS to bipolar-PMOS. High reliability processing procedures combined with volume production capabilities complement state-of-the-art products.

Telecommunications

Siliconix is a high-technology manufacturer of complex, highly specialized integrated circuits for the telecommunications industry. The current product lines use the CMOS process to satisfy the low power requirements of the telecom industry. Our Loop Disconnect Dialer Circuits offer subscribers push-button dialing privileges even with exchange systems presently tied to the rotary dial pulse timing.

High-Reliability Devices

Siliconix's capability in providing high-reliability devices to meet stringent military or aerospace applications is amply demonstrated by the Company's qualifications as a supplier for important European projects that include Ariane, Concorde, European Airbus, the Alpha Jet and Tornado Aircraft, also Apollo, Viking and Voyager space projects.

Siliconix has a number of standard Hi-Rel screening options that can be applied to standard products. These options include screening to BS9000 for analog switches and CECC standards for FETs, also MIL-STD-750 for discrete FETs. In addition, Siliconix offers certain JEDEC-registered FETs with JAN, JANTX and JANTXV processing, as well as an increasing number of QPL-listed analog switches. Special additional inspections and controls can be met and Siliconix can supply SEM-qualified products to meet individual customer requirements.

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FET Product Information

Siliconix FET products are divided into three basic categories:

- **Standard Products** All the part numbers described in this catalog are standard products. A summary list of the prefixes used is shown below in the Device Identification Table. Ordering any of the standard products is easily done by referring to the data sheet part number. For example, a 2N4391 is simply ordered by that number: "2N4391." It will also appear in that form on the price lists, published separately.
 - **Examples of Modified Standard Products are:**
 - Electrical Specials* Devices with either tightened, relaxed and/or special electrical specifications selected from a standard product.
 - Mechanical Specials* Devices with standard or modified electrical specifications mounted in non-standard packages or modified (lead formed) standard packages. Modifications and/or additions to standard marking are also considered mechanical specials.
 - High Reliability Specials* Siliconix has a number of standard High-Reliability screening options that can be ordered as standard products. These options include MIL-STD-750. High-Rel process option details will be found in the introductory section of this data book. In addition, Siliconix offers certain JEDEC-registered FETs with JAN, JANTX, or JANTXV processing. Refer to any current Siliconix OEM price list for details on specific part numbers. If existing screening processes do not meet individual customer requirements, Siliconix can provide special additional inspections and controls to meet the stringent demands.
- In all of the above cases (with the exception of JAN, JANTX, or JANTXV parts), a special part number is assigned which defines the part either by reference to customer's print(s) or by associated special requirements. Each special product is proprietary to the customer, and is *not* made available to other customers.
- **Custom Products** Are designed to meet customer requirements not realizable by selection from standard parts; usually, these products require special engineering development. The proprietary relationship described above also applies to custom products.

Inquiries for *SPECIAL DEVICES* may be directed to the nearest field sales office or to:

FET Marketing Department, Siliconix incorporated, 2201 Laurelwood Road, Santa Clara, California 95054, Telephone: (408) 988-8000.

FETs/Part Number Prefixes and Suffixes

Prefix	XXX	XXXX
BF	European Transistor Standard	
CR	SI Standard N-Channel Current Regulator	
CRR	SI Standard N-Channel Current Regulator	
DM		SI Special DMOS FET
DN		SI Dual N-Channel JFET
FN		SI N-Channel JFET
DPAD	SI Standard Dual JFET Diode	
J	SI Standard TO-92 Cased FET	Special TO-92 Cased FET
JR	SI Standard Current Limiter Diode TO-92 Cased FET	
JPAD	SI Standard JFET Diode	
PAD	SI Standard JFET Diode	
PN		SI Standard TO-92 Cased FET
SD		SI Standard DMOS FET
SI		N-Channel JFET Circuit
SST		JFET in SOT-23 Plastic Package
U	SI Standard FET	
VCR	SI Standard N- and P-Channel Voltage Controlled Resistors	
2N		JEDEC-Registered Device
3N	JEDEC-Registered Device	
Suffix		
-05	Std TO-92 Pkg. Lead Formed to TO-5 Pin Circle	
-18	Std TO-92 Pkg. with Center Lead Formed Toward Flat in TO-18 Pin Circle	
-TRF	Tape and Reel available on TO-92 FETs.	

PROCESS OPTION 750B-MIL-STD 750 - -2 Contact Factory
- -2A Contact Factory

SMALL SIGNAL FET Product Selector Guide

Application	Detail Application	Important FET Parameters Required	Major Tradeoffs	Unimportant FET Parameters	Preferred Parts
AMPLIFIER	Audio	Low noise (e_n), g_{fs}/g_{os}	Voltage amplification factor μ $= g_{fs}/g_{os}$ $= \Delta V_{DS}/\Delta V_{GS}$ $@ I_D = \text{const}$	$R_{DS(on)}$ $V_{DS(on)}$ $I_D(off)$ Switching Times	2N4339-40 2N4867-69 J230-32 J202-4 J308-10 U308-10 2N5911-12 2N4117A-19A U401-6 U421-6 2N6905-7 2N6908-11 S11000-20 S11100
	Buffer	Low I_G , high g_{fs}			
	Differential	Good matching V_{GS} , g_{fs} , I_{DSS} , I_G			
	High Input Impedance	Very low I_G (e.g., MOSFET)			
	High Frequency	High g_{fs}/C_{iss} ratio, NF, RF parameters			
	FET Input Op Amp	Good matching V_{GS} , g_{fs} , I_{DSS} , I_G			
	Low Distortion	High $V_{GS(off)}$ compared to signal amplitude			
	Low Supply Voltage	Low $V_{GS(off)}$			
	Low Noise	Low e_n , I_n , low 1/f noise, low NF			
	Preamplifier	Operate near I_{DQ} , high g_{fs}/I_D ratio			
	Video	High g_{fs}/C_{iss} ratio, NF			
SWITCHES	Analog Gates	Fast switching time	$R_{DS(on)}$ vs. Capacitance	g_{fs} g_{os} I_{DSS} max	SD210-15DE 2N4091-3 2N4391-3 PN4091-3 PN4391-3 J108-10 J105-7 U290-1 2N5432-4 2N4856-61 2N5114-16
	Choppers	$r_{DS}/I_D(off)$ switching efficiency			
	Commutators	Low C_{rss}			
	Digital	Fast switching time			
	Integrator Reset	Very low $R_{DS(on)}$, High I_{DSS}			
	Sample and Hold	Low C_{rss}			
CONSTANT CURRENT SOURCE	Current Limiting Reference Current Source Biasing	Low g_{oss} , low $V_{GS(off)}$, high BV_{GSS}	I_{DSS} vs. BV_{GSS}	g_{fs} , $R_{DS(on)}$, $I_D(off)$, $V_{DS(on)}$ switching times, RF parameters, capacitance	CRR Series J501-11 J552 Any J-FET
VOLTAGE CONTROLLED RESISTORS	Gain Control Amplitude Stability Attenuators	High $V_{GS(off)}$ for wide dynamic range and low distortion		g_{fs} , BV_{GSS} , I_{DSS}	VCR Series Any J-FET
MIXERS	VHF	RF parameters, NF, high g_{fs}/C_{iss} ratio, low C_{rss}		$r_{DS(on)}$ $V_{DS(on)}$ $I_D(off)$	U430-1 U440-1-3-4 2N5911-12 U308-10 J308-10 SD210-15DE
	UHF Double Balanced	Matching characteristics			
OSCILLATORS	Class A	Good g_{fs} at operating frequency	g_{fs} vs. Capacitance		2N4416 PN4418 U308-10 J308-10
	Class C	Low C_{iss} for VHF operation			

SMALL SIGNAL FET Application Selection Preferences

Additional Information

Popular Product Type	2N4112	2N4117A-19A	2N4130	2N4130A	2N4130B	2N4130C	2N4130D	2N4130E	2N4130F	2N4130G	2N4130H	2N4130I	2N4130J	2N4130K	2N4130L	2N4130M	2N4130N	2N4130P	2N4130Q	2N4130R	2N4130S	2N4130T	2N4130U	2N4130V	2N4130W	2N4130X	2N4130Y	2N4130Z	2N4130AA	2N4130AB	2N4130AC	2N4130AD	2N4130AE	2N4130AF	2N4130AG	2N4130AH	2N4130AI	2N4130AJ	2N4130AK	2N4130AL	2N4130AM	2N4130AN	2N4130AO	2N4130AP	2N4130AQ	2N4130AR	2N4130AS	2N4130AT	2N4130AU	2N4130AV	2N4130AW	2N4130AX	2N4130AY	2N4130AZ	2N4130BA	2N4130BB	2N4130BC	2N4130BD	2N4130BE	2N4130BF	2N4130BG	2N4130BH	2N4130BI	2N4130BJ	2N4130BK	2N4130BL	2N4130BM	2N4130BN	2N4130BO	2N4130BP	2N4130BQ	2N4130BR	2N4130BS	2N4130BT	2N4130BU	2N4130BV	2N4130BW	2N4130BX	2N4130BY	2N4130BZ	2N4130CA	2N4130CB	2N4130CC	2N4130CD	2N4130CE	2N4130CF	2N4130CG	2N4130CH	2N4130CI	2N4130CJ	2N4130CK	2N4130CL	2N4130CM	2N4130CN	2N4130CO	2N4130CP	2N4130CQ	2N4130CR	2N4130CS	2N4130CT	2N4130CU	2N4130CV	2N4130CW	2N4130CX	2N4130CY	2N4130CZ	2N4130DA	2N4130DB	2N4130DC	2N4130DD	2N4130DE	2N4130DF	2N4130DG	2N4130DH	2N4130DI	2N4130DJ	2N4130DK	2N4130DL	2N4130DM	2N4130DN	2N4130DO	2N4130DP	2N4130DQ	2N4130DR	2N4130DS	2N4130DT	2N4130DU	2N4130DV	2N4130DW	2N4130DX	2N4130DY	2N4130DZ	2N4130EA	2N4130EB	2N4130EC	2N4130ED	2N4130EE	2N4130EF	2N4130EG	2N4130EH	2N4130EI	2N4130EJ	2N4130EK	2N4130EL	2N4130EM	2N4130EN	2N4130EO	2N4130EP	2N4130EQ	2N4130ER	2N4130ES	2N4130ET	2N4130EU	2N4130EV	2N4130EW	2N4130EX	2N4130EY	2N4130EZ	2N4130FA	2N4130FB	2N4130FC	2N4130FD	2N4130FE	2N4130FF	2N4130FG	2N4130FH	2N4130FI	2N4130FJ	2N4130FK	2N4130FL	2N4130FM	2N4130FN	2N4130FO	2N4130FP	2N4130FQ	2N4130FR	2N4130FS	2N4130FT	2N4130FU	2N4130FV	2N4130FW	2N4130FX	2N4130FY	2N4130FZ	2N4130GA	2N4130GB	2N4130GC	2N4130GD	2N4130GE	2N4130GF	2N4130GG	2N4130GH	2N4130GI	2N4130GJ	2N4130GK	2N4130GL	2N4130GM	2N4130GN	2N4130GO	2N4130GP	2N4130GQ	2N4130GR	2N4130GS	2N4130GT	2N4130GU	2N4130GV	2N4130GW	2N4130GX	2N4130GY	2N4130GZ	2N4130HA	2N4130HB	2N4130HC	2N4130HD	2N4130HE	2N4130HF	2N4130HG	2N4130HH	2N4130HI	2N4130HJ	2N4130HK	2N4130HL	2N4130HM	2N4130HN	2N4130HO	2N4130HP	2N4130HQ	2N4130HR	2N4130HS	2N4130HT	2N4130HU	2N4130HV	2N4130HW	2N4130HX	2N4130HY	2N4130HZ	2N4130IA	2N4130IB	2N4130IC	2N4130ID	2N4130IE	2N4130IF	2N4130IG	2N4130IH	2N4130II	2N4130IJ	2N4130IK	2N4130IL	2N4130IM	2N4130IN	2N4130IO	2N4130IP	2N4130IQ	2N4130IR	2N4130IS	2N4130IT	2N4130IU	2N4130IV	2N4130IW	2N4130IX	2N4130IY	2N4130IZ	2N4130JA	2N4130JB	2N4130JC	2N4130JD	2N4130JE	2N4130JF	2N4130JG	2N4130JH	2N4130JI	2N4130JJ	2N4130JK	2N4130JL	2N4130JM	2N4130JN	2N4130JO	2N4130JP	2N4130JQ	2N4130JR	2N4130JS	2N4130JT	2N4130JU	2N4130JV	2N4130JW	2N4130JX	2N4130JY	2N4130JZ	2N4130KA	2N4130KB	2N4130KC	2N4130KD	2N4130KE	2N4130KF	2N4130KG	2N4130KH	2N4130KI	2N4130KJ	2N4130KK	2N4130KL	2N4130KM	2N4130KN	2N4130KO	2N4130KP	2N4130KQ	2N4130KR	2N4130KS	2N4130KT	2N4130KU	2N4130KV	2N4130KW	2N4130KX	2N4130KY	2N4130KZ	2N4130LA	2N4130LB	2N4130LC	2N4130LD	2N4130LE	2N4130LF	2N4130LG	2N4130LH	2N4130LI	2N4130LJ	2N4130LK	2N4130LL	2N4130LM	2N4130LN	2N4130LO	2N4130LP	2N4130LQ	2N4130LR	2N4130LS	2N4130LT	2N4130LU	2N4130LV	2N4130LW	2N4130LX	2N4130LY	2N4130LZ	2N4130MA	2N4130MB	2N4130MC	2N4130MD	2N4130ME	2N4130MF	2N4130MG	2N4130MH	2N4130MI	2N4130MJ	2N4130MK	2N4130ML	2N4130MM	2N4130MN	2N4130MO	2N4130MP	2N4130MQ	2N4130MR	2N4130MS	2N4130MT	2N4130MU	2N4130MV	2N4130MW	2N4130MX	2N4130MY	2N4130MZ	2N4130NA	2N4130NB	2N4130NC	2N4130ND	2N4130NE	2N4130NF	2N4130NG	2N4130NH	2N4130NI	2N4130NJ	2N4130NK	2N4130NL	2N4130NM	2N4130NN	2N4130NO	2N4130NP	2N4130NQ	2N4130NR	2N4130NS	2N4130NT	2N4130NU	2N4130NV	2N4130NW	2N4130NX	2N4130NY	2N4130NZ	2N4130OA	2N4130OB	2N4130OC	2N4130OD	2N4130OE	2N4130OF	2N4130OG	2N4130OH	2N4130OI	2N4130OJ	2N4130OK	2N4130OL	2N4130OM	2N4130ON	2N4130OO	2N4130OP	2N4130OQ	2N4130OR	2N4130OS	2N4130OT	2N4130OU	2N4130OV	2N4130OW	2N4130OX	2N4130OY	2N4130OZ	2N4130PA	2N4130PB	2N4130PC	2N4130PD	2N4130PE	2N4130PF	2N4130PG	2N4130PH	2N4130PI	2N4130PJ	2N4130PK	2N4130PL	2N4130PM	2N4130PN	2N4130PO	2N4130PP	2N4130PQ	2N4130PR	2N4130PS	2N4130PT	2N4130PU	2N4130PV	2N4130PW	2N4130PX	2N4130PY	2N4130PZ	2N4130QA	2N4130QB	2N4130QC	2N4130QD	2N4130QE	2N4130QF	2N4130QG	2N4130QH	2N4130QI	2N4130QJ	2N4130QK	2N4130QL	2N4130QM	2N4130QN	2N4130QO	2N4130QP	2N4130QQ	2N4130QR	2N4130QS	2N4130QT	2N4130QU	2N4130QV	2N4130QW	2N4130QX	2N4130QY	2N4130QZ	2N4130RA	2N4130RB	2N4130RC	2N4130RD	2N4130RE	2N4130RF	2N4130RG	2N4130RH	2N4130RI	2N4130RJ	2N4130RK	2N4130RL	2N4130RM	2N4130RN	2N4130RO	2N4130RP	2N4130RQ	2N4130RR	2N4130RS	2N4130RT	2N4130RU	2N4130RV	2N4130RW	2N4130RX	2N4130RY	2N4130RZ	2N4130SA	2N4130SB	2N4130SC	2N4130SD	2N4130SE	2N4130SF	2N4130SG	2N4130SH	2N4130SI	2N4130SJ	2N4130SK	2N4130SL	2N4130SM	2N4130SN	2N4130SO	2N4130SP	2N4130SQ	2N4130SR	2N4130SS	2N4130ST	2N4130SU	2N4130SV	2N4130SW	2N4130SX	2N4130SY	2N4130SZ	2N4130TA	2N4130TB	2N4130TC	2N4130TD	2N4130TE	2N4130TF	2N4130TG	2N4130TH	2N4130TI	2N4130TJ	2N4130TK	2N4130TL	2N4130TM	2N4130TN	2N4130TO	2N4130TP	2N4130TQ	2N4130TR	2N4130TS	2N4130TT	2N4130TU	2N4130TV	2N4130TW	2N4130TX	2N4130TY	2N4130TZ	2N4130UA	2N4130UB	2N4130UC	2N4130UD	2N4130UE	2N4130UF	2N4130UG	2N4130UH	2N4130UI	2N4130UJ	2N4130UK	2N4130UL	2N4130UM	2N4130UN	2N4130UO	2N4130UP	2N4130UQ	2N4130UR	2N4130US	2N4130UT	2N4130UU	2N4130UV	2N4130UW	2N4130UX	2N4130UY	2N4130UZ	2N4130VA	2N4130VB	2N4130VC	2N4130VD	2N4130VE	2N4130VF	2N4130VG	2N4130VH	2N4130VI	2N4130VJ	2N4130VK	2N4130VL	2N4130VM	2N4130VN	2N4130VO	2N4130VP	2N4130VQ	2N4130VR	2N4130VS	2N4130VT	2N4130VU	2N4130VV	2N4130VW	2N4130VX	2N4130VY	2N4130VZ	2N4130WA	2N4130WB	2N4130WC	2N4130WD	2N4130WE	2N4130WF	2N4130WG	2N4130WH	2N4130WI	2N4130WJ	2N4130WK	2N4130WL	2N4130WM	2N4130WN	2N4130WO	2N4130WP	2N4130WQ	2N4130WR	2N4130WS	2N4130WT	2N4130WU	2N4130WV	2N4130WW	2N4130WX	2N4130WY	2N4130WZ	2N4130XA	2N4130XB	2N4130XC	2N4130XD	2N4130XE	2N4130XF	2N4130XG	2N4130XH	2N4130XI	2N4130XJ	2N4130XK	2N4130XL	2N4130XM	2N4130XN	2N4130XO	2N4130XP	2N4130XQ	2N4130XR	2N4130XS	2N4130XT	2N4130XU	2N4130XV	2N4130XW	2N4130XX	2N4130XY	2N4130XZ	2N4130YA	2N4130YB	2N4130YC	2N4130YD	2N4130YE	2N4130YF	2N4130YG	2N4130YH	2N4130YI	2N4130YJ	2N4130YK	2N4130YL	2N4130YM	2N4130YN	2N4130YO	2N4130YP	2N4130YQ	2N4130YR	2N4130YS	2N4130YT	2N4130YU	2N4130YV	2N4130YW	2N4130YX	2N4130YY	2N4130YZ	2N4130ZA	2N4130ZB	2N4130ZC	2N4130ZD	2N4130ZE	2N4130ZF	2N4130ZG	2N4130ZH	2N4130ZI	2N4130ZJ	2N4130ZK	2N4130ZL	2N4130ZM	2N4130ZN	2N4130ZO	2N4130ZP	2N4130ZQ	2N4130ZR	2N4130ZS	2N4130ZT	2N4130ZU	2N4130ZV	2N4130ZW	2N4130ZX	2N4130ZY	2N4130ZZ				
Process Designation	NT	RPA	KH	KRL	MZA	MZF	NVA	NCP	KCB	MRA	KMT	KCP	KMR	MZF	MCS	PSB	NCL	KXL	KKM	NKO	CMC	YMA	NMZ	MKN	NBA																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																											

Military Application

As an option, Siliconix offers all hermetically packaged product processed to MIL-STD-750. For information, contact your local Siliconix Sales Office or Siliconix, Incorporated direct.

P = Prime Choice
S = Secondary, (alternative) Choice
LV = Limited Value

SMALL FET Product Specifications

N & P-Channel Single JFETs																
PART NUMBER	N or P	PACKAGE (TO-)	LEAKAGE (nA, MAX.)		THRESHOLD VOLTAGE (V, MAX.)	BREAKDOWN VOLTAGE (V, MAX.)	SATURATION CURRENT (mA)		TRANS- CONDUCTANCE gfs (umhos)		INPUT CAPACITANCE (pF, MAX.)	NOISE VOLTAGE (nV/√Hz, MAX.) or (NF, dB, MAX.)	RESISTANCE		GEOMETRY (Section 4)	DEVICE
			Gate	Chnl			Min.	Max.	Min.	Max.			Gate Ω	Chnl Ω, Max.		
2N4117	N	72	0.01	-	1.8	40	0.03	0.09	70	210	3	-	-	-	NT	LOW LEAKAGE
2N4117A	N	72	0.001	-	1.8	40	0.03	0.09	70	210	3	-	-	-	NT	
2N4118	N	72	0.01	-	3.0	40	0.08	0.24	80	250	3	-	-	-	NT	
2N4118A	N	72	0.001	-	3.0	40	0.08	0.24	90	250	3	-	-	-	NT	
2N4119	N	72	0.01	-	6.0	40	0.2	0.6	100	330	3	-	-	-	NT	
2N4119A	N	72	0.001	-	6.0	40	0.2	0.6	100	330	3	-	-	-	NT	
PN4117	N	92	0.01	-	4.0	-	0.03	0.09	70	210	-	-	-	3K	NT	
PN4117A	N	92	0.001	-	4.0	-	0.03	0.09	70	210	-	-	-	3K	NT	
PN4118	N	92	0.01	-	4.0	-	0.08	0.24	80	250	-	-	-	3K	NT	
PN4118A	N	92	0.001	-	4.0	-	0.08	0.24	80	250	-	-	-	3K	NT	
PN4119	N	92	0.01	-	4.0	-	0.2	0.6	100	330	-	-	-	3K	NT	
PN4119A	N	92	0.001	-	4.0	-	0.2	0.6	100	330	-	-	-	3K	NT	
PN4120	N	92	-	-	4.0	-	0.2	0.6	100	330	-	-	-	3K	NT	
FN4117	N	72	0.005	-	4.0	-	0.03	0.09	70	210	-	-	-	3K	NT	
FN4117A	N	72	0.001	-	2.0	40	0.03	0.2	70	210	3	-	-	-	NT	
FN4118	N	72	0.005	-	4.0	-	0.08	0.24	80	250	-	-	-	3K	NT	
FN4118A	N	72	0.001	-	2.0	40	0.08	0.4	80	250	3	-	-	-	NT	
FN4119	N	72	0.005	-	4.0	-	0.2	0.6	100	330	-	-	-	3K	NT	
FN4119A	N	72	0.001	-	6.0	40	0.2	1.2	100	330	3	-	-	-	NT	
FN4392	N	18	0.1	0.1	40	-	25	100	-	-	-	-	60	14	NCB	
FN4393	N	18	0.1	0.1	40	-	5.0	60	-	-	-	-	100	14	NCB	
2N4220A	N	72	0.1	-	4.0	30	0.5	3.0	1000	4000	6	2.5	1M	-	NRL	LOW NOISE
2N4221A	N	72	0.1	-	6.0	30	2.0	6.0	2000	5000	6	2.5	1M	-	NRL	
2N4222	N	72	0.1	-	8.0	30	5.0	15	2500	6000	6	2.5	1M	-	NRL	
2N4338	N	18	0.1	-	1.0	50	0.2	0.6	600	1800	7	1.0	1M	-	NPA	
2N4339	N	18	0.1	-	1.8	50	0.5	1.5	800	2400	7	1.0	1M	-	NPA	
2N4340	N	18	0.1	-	3.0	50	1.2	3.6	1300	3000	7	1.0	1M	-	NPA	
2N4341	N	18	0.1	-	6.0	50	3.0	9.0	2000	4000	7	1.0	1M	-	NPA	
2N4867	N	72	0.25	-	2.0	40	0.4	1.2	700	2000	25	20	-	-	NPA	
2N4867A	N	72	0.25	-	2.0	40	0.4	1.2	700	2000	25	10	-	-	NPA	
2N4868	N	72	0.25	-	3.0	40	1.0	3.0	1000	3000	25	20	-	-	NPA	
2N4868A	N	72	0.25	-	3.0	40	1.0	3.0	1000	3000	25	10	-	-	NPA	
2N4869	N	72	0.25	-	5.0	40	2.5	7.5	1300	4000	25	20	-	-	NPA	
2N4869A	N	72	0.25	-	5.0	40	2.5	7.5	1300	4000	25	10	-	-	NPA	
SI1000- (2N6908)	N	72	0.025	-	1.8	30	-	2.0	100	3000	5	25	-	-	NBA-A	
SI1010- (2N6909)	N	72	0.025	-	2.3	30	-	3.5	400	3500	5	25	-	-	NBA-A	
SI1020- (2N6910)	N	72	0.025	-	3.5	30	-	5.0	1200	4000	5	25	-	-	NBA-A	
SI1100- (2N6911)	N	72	0.025	-	2.8	30	-	-	-	-	-	25	-	-	NBA-B	
J230	N	92	0.25	-	3.0	40	0.7	3.0	1000	2500	-	30	-	-	NPA	
J230-18	N	92	0.25	-	3.0	40	0.7	3.0	1000	2500	-	30	-	-	NPA	
J231	N	92	0.25	-	5.0	40	2.0	6.0	1500	3000	-	30	-	-	NPA	
J231-18	N	92	0.25	-	5.0	40	2.0	6.0	1500	3000	-	30	-	-	NPA	
J232	N	92	0.25	-	6.0	40	5.0	10	2500	4000	-	30	-	-	NPA	

SMALL FET Product Specifications (Cont'd)

N&P-Channel Single JFETs																
PART NUMBER	N or P	PACKAGE (TO-)	LEAKAGE (nA, MAX.)		THRESHOLD VOLTAGE (V, MAX.)	BREAKDOWN VOLTAGE (V, MAX.)	SATURATION CURRENT (mA)		TRANS-CONDUCTANCE (µS (umhos))		INPUT CAPACITANCE (pF, MAX.)	NOISE VOLTAGE (nV/√Hz, MAX.) or (NF, dB, MAX.)	RESISTANCE		GEOMETRY (Section 4)	DEVICE
			Gate	Chnl			Min.	Max.	Min.	Max.			Gate Ω	Chnl Ω, Max.		
J232-18	N	92	0.25	-	6.0	40	5.0	10	2500	4000	-	30	-	-	NPA	RF AMPLIFIERS
J270-18	P	92	0.2	-	2.0	30	2.0	15	6000	15000	-	-	-	-	PA-A/B	
2N3819	N	92	2.0	-	8.0	25	2.0	20	2000	6500	8.0	-	-	-	NRL	
2N3823	N	72	0.5	-	8.0	30	4.0	20	3500	6500	6	2.5	1K	-	NRL	
2N4223	N	72	0.25	-	8.0	30	3.0	18	3000	7000	6	5.0	1K	-	NRL	
2N4224	N	72	0.5	-	8.0	30	2.0	20	2000	7500	6	-	-	-	NRL	
2N4416	N	72	0.1	-	6.0	30	5.0	15	4500	7500	4	2.0	1K	-	NH	
2N4416A	N	72	0.1	-	6.0	35	5.0	15	4500	7500	4	2.0	1K	-	NH	
2N5484	N	92	1.0	-	3.0	25	1.0	5.0	3000	6000	5	3.0	1K	-	NH	
2N5485	N	92	1.0	-	4.0	25	4.0	10	3500	7000	5	2.0	1K	-	NH	
2N5486	N	92	1.0	-	6.0	25	8.0	20	4000	8000	5	2.0	1K	-	NH	
2N5668	N	92	2.0	-	4.0	25	1.0	5.0	1500	6500	7	2.5	1K	-	NH	
2N5669	N	92	2.0	-	6.0	25	4.0	10	2000	6500	7	2.5	1K	-	NH	
2N5670	N	92	2.0	-	8.0	25	8.0	20	3000	7500	7.0	2.5	1K	-	NH	
J210	N	92	0.1	-	3.0	25	2.0	15	4000	12000	-	-	-	-	NZF	
J211	N	92	0.1	-	4.5	25	7.0	20	7000	12000	-	-	-	-	NZF	
J212	N	92	0.1	-	6.0	25	15	40	7000	12000	-	-	-	-	NZF	
J270	P	92	0.2	-	2.0	30	2.0	15	6000	15000	-	-	-	-	PS-A/B	
J271	P	92	0.2	-	4.5	30	6.0	50	8000	18000	-	-	-	-	PS-A/B	
J300	N	92	0.5	-	6.0	25	6.0	30	4500	9000	5.5	-	-	-	NZF	
J304	N	92	0.1	-	6.0	30	5.0	15	4500	7500	-	-	-	-	NH	
J305	N	92	0.1	-	3.0	30	1.0	8.0	3000	-	-	-	-	-	NH	
J308	N	92	1.0	-	6.5	25	12	60	8000	20000	7.5	-	-	-	NZA	
J309	N	92	1.0	-	4.0	25	12	30	10000	20000	7.5	-	-	-	NZA	
J310	N	92	1.0	-	6.5	25	24	60	8000	18000	7.5	-	-	-	NZA	
MPF102	N	92	2.0	-	7.5	25	2.0	20	2000	7500	7.0	-	-	-	NH	
MPF108	N	92	1.0	-	8.0	25	1.5	24	2000	7500	6.5	2.5	1M	-	NH	
MPF112	N	92	100	-	10	25	1.0	25	1000	7500	-	-	-	-	NH	
PN4416	N	92	1.0	-	6.0	30	5.0	15	4500	7500	4.0	2.0	1K	-	NH	
U308	N	52	0.15	-	6.0	25	12	60	10000	20000	7.5	-	-	-	NZA	
U309	N	52	0.15	-	4.0	25	12	30	10000	20000	7.5	-	-	-	NZA	
U310	N	52	0.15	-	6.0	25	24	60	10000	18000	7.5	-	-	-	NZA	
U311	N	72	0.15	-	6.0	25	20	60	10000	20000	7.5	-	-	-	NZA	
U312	N	52	0.1	-	6.0	25	10	30	6000	10000	5.0	-	-	-	NZF	

SMALL FET Product Specifications (Cont'd)

N & P-Channel Single JFETs																
PART NUMBER	N or P	PACKAGE (TO-)	LEAKAGE (nA, MAX.)		THRESHOLD VOLTAGE (V, MAX.)	BREAKDOWN VOLTAGE (V, MAX.)	SATURATION CURRENT (mA)		TRANS- CONDUCTANCE gfs (umhos)		INPUT CAPACITANCE (pF, MAX.)	NOISE VOLTAGE (nV/√Hz, MAX.) or (NF, dB, MAX.)	RESISTANCE		GEOMETRY (Section 4)	DEVICE
			Gate	Chnl			Min.	Max.	Min.	Max.			Gate Ω	Chnl Ω, Max.		
2N3824	N	72	0.1	0.1	8.0	50	-	-	-	-	6.0	-	-	250	NRL	SWITCHES & CHOPPERS
2N3970	N	18	0.25	0.25	10	40	50	150	-	-	25	-	-	30	NCB	
2N3971	N	18	0.25	0.25	5.0	40	25	75	-	-	25	-	-	60	NCB	
2N3972	N	18	0.25	0.25	3.0	40	5.0	30	-	-	25	-	-	100	NCB	
2N4091	N	18	0.2	0.2	10	40	30	-	-	-	16	-	-	30	NCB	
2N4092	N	18	0.2	0.2	7.0	40	15	-	-	-	16	-	-	50	NCB	
2N4093	N	18	0.2	0.2	5.0	40	8.0	-	-	-	16	-	-	80	NCB	
2N4391	N	18	0.1	0.1	10	40	50	150	-	-	14	-	-	30	NCB	
2N4392*	N	18	0.1	0.1	5.0	40	25	75	-	-	14	-	-	60	NCB	
2N4393*	N	18	0.1	0.1	3.0	40	5.0	30	-	-	14	-	-	100	NCB	
2N4856	N	18	0.25	0.25	10	40	50	-	-	-	18	-	-	25	NCB	
2N4856A	N	18	0.25	0.25	10	40	50	-	-	-	10	-	-	25	NCB	
2N4857	N	18	0.25	0.25	6.0	40	20	100	-	-	18	-	-	40	NCB	
2N4857A	N	18	0.25	0.25	6.0	40	20	100	-	-	10	-	-	40	NCB	
2N4858	N	18	0.25	0.25	4.0	40	8.0	80	-	-	18	-	-	60	NCB	
2N4858A	N	18	0.25	0.25	4.0	40	8.0	80	-	-	10	-	-	60	NCB	
2N4859	N	18	0.25	0.25	10	30	50	-	-	-	18	-	-	25	NCB	
2N4859A	N	18	0.25	0.25	10	30	50	-	-	-	10	-	-	25	NCB	
2N4860	N	18	0.25	0.25	6.0	30	20	100	-	-	18	-	-	40	NCB	
2N4860A	N	18	0.25	0.25	6.0	30	20	100	-	-	10	-	-	40	NCB	
2N4861	N	18	0.25	0.25	4.0	30	8.0	80	-	-	18	-	-	60	NCB	
2N4861A	N	18	0.25	0.25	4.0	30	8.0	80	-	-	10	-	-	80	NCB	
2N5018	P	18	2.0	10.0	10	30	10	-	-	-	45	-	-	75	PS-A/B	
2N5019	P	18	2.0	10.0	5.0	30	5.0	-	-	-	45	-	-	150	PS-A/B	
2N5114	P	18	0.5	0.5	10	30	30	90	-	-	25	-	-	75	PS-A/B	
2N5115	P	18	0.5	0.5	6.0	30	15	60	-	-	25	-	-	100	PS-A/B	
2N5116	P	18	0.5	0.5	4.0	30	5.0	25	-	-	27	-	-	150	PS-A/B	
2N5432	N	52	0.2	0.2	10	25	150	-	-	-	30	-	-	5.0	NIP	
2N5433	N	52	0.2	0.2	9.0	25	100	-	-	-	30	-	-	7.0	NIP	
2N5434	N	52	0.2	0.2	4.0	25	30	-	-	-	30	-	-	10	NIP	
2N5638	N	92	1.0	1.0	12	30	50	-	-	-	10	-	-	30	NCB	
2N5639	N	92	1.0	1.0	8.0	30	25	-	-	-	10	-	-	60	NCB	

*FN4392 and FN4393 available

*FN4392 and FN4393 available

SMALL SIGNAL FET Product Specifications (Cont'd)

N & P-Channel Single JFETs

DEVICE		SWITCHES & CHOPPERS															
GEOMETRY (Section 4)		NCB NVA NVA NVA NVA NVA NVA NIP NIP NIP NIP NIP NCB NCB NCB NCB NCB PS-A/B PS-A/B PS-A/B PS-A/B PS-A/B PS-A/B PS-A/B PS-A/B PS-A/B NCB NCB NCB NCB NCB															
RESISTANCE	Chnl Ω, Max.	100 3.0 3.0 6.0 8.0 8.0 8.0 12 18 18 18 30 30 50 50 100 100 85 85 125 125 250 300 300 75 75 150 150 30 60 60 100 100	Gate Ω														
NOISE VOLTAGE (nV/√Hz, MAX.) or (NF, dB, MAX.)																	
INPUT CAPACITANCE (pF, MAX.)		10															
TRANS- CONDUCTANCE gfs (μmhos)	Max.																
	Min.																
SATURATION CURRENT (mA)	Max.																
	Min.	5.0 500 500 200 200 100 100 100 80 40 40 10 20 35 5.0 5.0 2.0 2.0 20 20 7.0 7.0 25 20 20 1.5 20 10 10 5.0 5.0 50 50 25 25 5.0 5.0 3.0 3.0															
BREAKDOWN VOLTAGE (V, MAX.)		30 25 25 25 25 25 25 25 25 25 25 35 35 35 35 30 30 30 30 30 30 30 30 30 30 30 40 40 40 40 40															
THRESHOLD VOLTAGE (V, MAX.)		6.0 10.0 10 6.0 6.0 4.5 4.5 10 10 6.0 4.0 4.0 10 10 5.0 5.0 3.0 3.0 10 10 6.0 0.0 4.0 4.0 2.25 2.25 10 10 5.0 5.0 10 10 5.0 5.0 10 10 5.0 5.0 3.0 3.0															
LEAKAGE (nA, MAX.)	Chnl	1.0 3.0 3.0 3.0 3.0 3.0 3.0 3.0 3.0 3.0 3.0 1.0 1.0 1.0 1.0 1.0 1.0 1.0 1.0 1.0 1.0 1.0 1.0 1.0 1.0 1.0 1.0 1.0 1.0 1.0	Gate	1.0 3.0 3.0 3.0 3.0 3.0 3.0 3.0 3.0 3.0 3.0 1.0 1.0 1.0 1.0 1.0 1.0 1.0 1.0 1.0 1.0 1.0 1.0 1.0 1.0 1.0 1.0 1.0 1.0 1.0													
PACKAGE (TO- 1)		92 92															
N or P		N N N N N N N N N N N N N N N P P P P P P P P P P P P P P P P P P															
PART NUMBER		2N5640 J105 J105-18 J106 J106-18 J107 J107-18 J108 J108-18 J109 J109-18 J110 J110-18 J111 J111-18 J112 J112-18 J113 J113-18 J174 J174-18 J175 J175-18 J176 J176-18 J177 J177-18 P1086 P1086-18 P1087 P1087-18 PN4391 PN4391-18 PN4392 PN4392-18 PN4393 PN4393-18															

SMALL SIGNAL FET Product Specifications (Cont'd)

N & P-Channel Single JFETs

DEVICE	SWITCHES & CHOPPERS	
GEOMETRY (Section 4)		
RESISTANCE	Chnl Ω , Max.	Gate Ω
NOISE VOLTAGE (nV/ $\sqrt{\text{Hz}}$, MAX.) or (NF, dB, MAX.)		
INPUT CAPACITANCE (pF, MAX.)		
TRANS- CONDUCTANCE gfs (μmhos)	Max.	Min.
SATURATION CURRENT (mA)	Max.	Min.
BREAKDOWN VOLTAGE (V, MAX.)		
THRESHOLD VOLTAGE (V, MAX.)		
LEAKAGE (nA, MAX.)	Chnl	Gate
PACKAGE (TO-)		
N or P		
PART NUMBER		

SD210	DMCB-B	70	-	5.5	-	10	30	2.0	100	72	N	SD210
SD211	DMCB-A	70	-	5.5	-	10	30	2.0	100	72	N	SD211
SD212	DMCB-B	70	-	5.5	-	10	10	2.0	100	72	N	SD212
SD213	DMCB-A	70	-	5.5	-	10	10	2.0	100	72	N	SD213
SD214	DMCB-B	70	-	5.5	-	10	20	2.0	100	72	N	SD214
SD215	DMCB-A	70	-	5.5	-	10	20	2.0	100	72	N	SD215
U200	NCB	150	-	30	-	3.0	30	3.0	1.0	18	N	U200
U201	NCB	75	-	30	-	15	30	5.0	1.0	18	N	U201
U202	NCB	50	-	30	-	30	30	10	1.0	18	N	U202
U290	NVA	2.5	-	60	-	500	30	10	1.0	92	N	U290
U291	PS-A/B	85	-	27	-	200	30	4.5	0.5	52	N	U291
U304	PS-A/B	110	-	27	-	15	30	6.0	0.5	18	P	U304
U305	PS-A/B	175	-	27	-	30	30	4.0	0.5	18	P	U305
U306	NCB	30	-	16	-	5.0	30	10	0.4	18	N	U306
U1897	NCB	30	-	16	-	30	40	10	0.4	92	N	U1897
U1897-18	NCB	30	-	16	-	30	40	10	0.4	92	N	U1897-18
U1898	NCB	50	-	16	-	15	40	7.0	0.4	92	N	U1898
U1898-18	NCB	50	-	16	-	15	40	7.0	0.4	92	N	U1898-18
U1899	NCB	80	-	16	-	8.0	40	5.0	0.4	92	N	U1899
U1899-18	NCB	80	-	16	-	8.0	40	5.0	0.4	92	N	U1899-18

SMALL FET Product Specifications (Cont'd)

N & P-Channel Single JFETs																
PART NUMBER	N or P	PACKAGE (TO-)	LEAKAGE (nA, MAX.)		THRESHOLD VOLTAGE (V, MAX.)	BREAKDOWN VOLTAGE (V, MAX.)	SATURATION CURRENT (mA)		TRANS- CONDUCTANCE gfs (umhos)		INPUT CAPACITANCE (pF, MAX.)	NOISE VOLTAGE (nV/√Hz, MAX.) or (nF, dB, MAX.)	RESISTANCE		GEOMETRY (Section 4)	DEVICE
			Gate	Chnl			Min.	Max.	Min.	Max.			Gate Ω	Chnl Ω, Max.		
2N3821	N	72	0.1	-	4.0	50	0.5	2.5	1500	4500	6	200	-	-	NRL	GENERAL PURPOSE
2N3822	N	72	0.1	-	6.0	50	2.0	10	3000	6500	6	200	-	-	NRL	
2N4220	N	72	0.1	-	4.0	30	0.5	3.0	1000	4000	6	-	-	-	NRL	
2N4221	N	72	0.1	-	6.0	30	2.0	6.0	2000	5000	6	-	-	-	NRL	
2N4222	N	72	0.1	-	8.0	30	5.0	15	2500	6000	6	-	-	-	NRL	
2N5457	N	92	1.0	-	6.0	25	1.0	5.0	1000	5000	7	3.0	1M	-	NRL	
2N5458	N	92	1.0	-	7.0	25	2.0	9.0	1500	5500	7	3.0	1M	-	NRL	
2N5459	N	92	1.0	-	8.0	25	4.0	16	2000	6000	7	3.0	100M	-	NRL	
J201	N	92	0.1	-	1.5	40	0.2	1.0	500	-	5.0	-	-	-	NPA	
J201-18	N	92	0.1	-	1.5	40	0.2	1.00	500	-	5.0	-	-	-	NPA	
J202	N	92	0.1	-	4.0	40	0.9	4.5	1000	-	5.0	-	-	-	NPA	
J202-18	N	92	0.1	-	4.0	40	0.9	4.5	1000	-	5.0	-	-	-	NPA	
J203	N	92	0.1	-	10	40	4.0	20	1500	-	5.0	-	-	-	NPA	
J203-18	N	92	0.1	-	10	40	4.0	20	1500	-	5.0	-	-	-	NPA	
J204	N	92	0.1	-	2.0	25	1.2	3.0	-	-	5.0	-	-	-	NPA	
J204-18	N	92	0.1	-	2.0	25	1.2	3.0	-	-	5.0	-	-	-	NPA	
J270	P	92	0.2	-	4.5	30	6.0	50	8000	18000	-	-	-	-	PS-A/B	
J271-18	P	92	0.2	-	4.5	30	6.0	50	8000	18000	-	-	-	-	PS-A/B	
MPF109	N	92	1.0	-	8.0	25	0.5	24	800	6000	7.0	2.5	1M	-	NRL	
MPF111	N	92	100	-	10	20	0.5	20	500	-	-	-	-	-	NRL	
PN4302	N	92	1.0	-	4.0	30	0.5	5.0	1000	-	6	2.0	1M	-	NPA	
PN4302-18	N	92	1.0	-	4.0	30	0.5	5.0	1000	-	6.0	2.0	1M	-	NPA	
PN4303	N	92	1.0	-	6.0	30	4.0	10	2000	-	6	2.0	1M	-	NPA	
PN4303-18	N	92	1.0	-	6.0	30	4.0	10	2000	-	6.0	2.0	1M	-	NPA	
PN4304	N	92	1.0	-	10.0	30	0.5	15	1000	-	6	3.0	1M	-	NPA	
PN4304-18	N	92	1.0	-	10	30	0.5	15	1000	-	6.0	2.0	1M	-	NPA	
PN5163	N	92	10	-	8.0	25	1.0	40.0	2000	9000	20	50.0	-	-	-	

SMALL SIGNAL FET Product Specifications (Cont'd)

N-Channel Dual JFETs

PART NUMBER	N or P	PACKAGE (TO-)	LEAKAGE (nA, MAX.)	THRESHOLD VOLTAGE (V, MAX.)	BREAKDOWN VOLTAGE (V, MAX.)	SATURATION CURRENT (mA)		TRANS- CONDUCTANCE gfs (μmhos)		INPUT CAPACITANCE (pF, MAX.)	NOISE VOLTAGE (nV/√Hz, MAX.) or (NF, dB, MAX.)	THRESHOLD		OUTPUT CONDUCTANCE gfs (μmhos, MAX.)	GEOMETRY (Section 4)	DEVICE
			Gate			Min.	Max.	Min.	Max.			Static Match (mV, Max.)	Temp Tracking μV/°C			
2N5196	N	71	0.025	4.0	50	0.7	7.0	1000	—	6.0	20	5.0	5.0	50	NQP	
2N5197	N	71	0.025	4.0	50	0.7	7.0	1000	—	6.0	20	5.0	10	50	NQP	
2N5198	N	71	0.025	4.0	50	0.7	7.0	1000	—	6.0	20	10	20	50	NQP	
2N5199	N	71	0.025	4.0	50	0.7	7.0	1000	—	6.0	20	15	40	50	NQP	
2N5545	N	71	0.1	4.5	50	0.5	8.0	1500	—	6.0	200	5.0	10	25	NQP	
2N5546	N	71	0.1	4.5	50	0.5	8.0	1500	—	6.0	200	10	20	25	NQP	
2N5547	N	71	0.1	4.5	50	0.5	8.0	1500	—	6.0	200	15	40	25	NQP	
2N6905	N	71	0.015	2.5	35	0.5	10	2000	—	8.0	15	5	10	—	NNR	
2N6908	N	71	0.015	2.5	35	0.5	10	2000	—	8.0	15	15	25	—	NNR	
2N6907	N	71	0.015	2.5	35	0.5	10	2000	—	8.0	15	25	50	—	NNR	
U401	N	71	0.025	2.5	50	0.5	10	2000	—	8.0	20	10	10	2.0	NNR	
U402	N	71	0.025	2.5	50	0.5	10	2000	—	8.0	20	10	25	2.0	NNR	
U403	N	71	0.025	2.5	50	0.5	10	2000	—	8.0	20	15	25	2.0	NNR	
U404	N	71	0.025	2.5	50	0.5	10	2000	—	8.0	20	20	40	2.0	NNR	
U405	N	71	0.025	2.5	50	0.5	10	2000	—	8.0	20	20	80	2.0	NNR	
U406	N	71	0.025	2.5	50	0.5	10	2000	—	8.0	20	40	10	0.5	NNT	
U421	N	78	0.001	2.0	40	0.06	1.0	300	1500	3.0	10	15	25	0.5	NNT	
U422	N	78	0.001	2.0	40	0.06	1.0	300	1500	3.0	10	25	40	0.5	NNT	
U423	N	78	0.001	2.0	40	0.06	1.0	300	1500	3.0	10	15	10	1.0	NNT	
U424	N	78	0.003	3.0	40	0.06	1.8	300	1500	3.0	10	15	25	1.0	NNT	
U425	N	78	0.003	3.0	40	0.06	1.8	300	1500	3.0	10	25	40	1.0	NNT	
U426	N	78	0.003	3.0	40	0.06	1.8	300	1500	3.0	10	25	40	1.0	NNT	
U427	N	78	0.005	3.0	40	0.06	1.8	250	—	3.0	—	25	40	3.0	NNT	
U428	N	78	0.005	3.0	40	0.06	1.8	250	—	3.0	—	40	80	5.0	NNT	
2N5515	N	71	0.25	4.0	40	0.5	7.5	1000	—	25	30	5.0	5.0	1.0	NQP	
2N5516	N	71	0.25	4.0	40	0.5	7.5	1000	—	25	30	5.0	10	1.0	NQP	
2N5517	N	71	0.25	4.0	40	0.5	7.5	1000	—	25	30	10	20	1.0	NQP	
2N5518	N	71	0.25	4.0	40	0.5	7.5	1000	—	25	30	15	40	1.0	NQP	
2N5519	N	71	0.25	4.0	40	0.5	7.5	1000	—	25	30	15	80	1.0	NQP	
2N5520	N	71	0.25	4.0	40	0.5	7.5	1000	—	25	15	5.0	5.0	1.0	NQP	
2N5521	N	71	0.25	4.0	40	0.5	7.5	1000	—	25	15	5.0	10	1.0	NQP	
2N5522	N	71	0.25	4.0	40	0.5	7.5	1000	—	25	15	10	20	1.0	NQP	
2N5523	N	71	0.25	4.0	40	0.5	7.5	1000	—	25	15	15	40	1.0	NQP	
2N5524	N	71	0.25	4.0	40	0.5	7.5	1000	—	25	15	15	80	1.0	NQP	
2N6905	N	71	0.015	2.5	35	0.5	10	2000	—	8.0	15	5	10	—	NNR	
2N6906	N	71	0.015	2.5	35	0.5	10	2000	—	8.0	15	10	25	—	NNR	
2N6907	N	71	0.015	2.5	35	0.5	10	2000	—	8.0	15	25	50	—	NNR	
U401	N	71	0.025	2.5	50	0.5	10	2000	—	8.0	20	5.0	10	2.0	NNR	
U402	N	71	0.025	2.5	50	0.5	10	2000	—	8.0	20	10	10	2.0	NNR	

SMALL SIGNAL FET Product Specifications (Cont'd)

N-Channel Dual JFETs

PART NUMBER	N or P	PACKAGE (TO-)	LEAKAGE (nA, MAX.)	THRESHOLD VOLTAGE (V, MAX.)	BREAKDOWN VOLTAGE (V, MAX.)	SATURATION CURRENT (mA)		TRANS-CONDUCTANCE gfs (μmhos)		INPUT CAPACITANCE (pF, MAX.)	NOISE VOLTAGE (nV/√Hz, MAX.) or (NF, dB, MAX.)	THRESHOLD		OUTPUT CONDUCTANCE g _{os} (μmhos, MAX.)	GEOMETRY (Section 4)	DEVICE
						Min.	Max.	Min.	Max.			Static Match (mV, MAX.)	Temp Tracking μV/°C			
U404	N	71	0.025	2.5	50	0.5	10	2000	-	8.0	20	15	25	2.0	NNR	LOW NOISE
U405	N	71	0.025	2.5	50	0.5	10	2000	-	8.0	20	20	40	2.0	NNR	LOW NOISE
U406	N	71	0.025	2.5	50	0.5	10	2000	-	8.0	20	40	80	2.0	NNR	LOW NOISE
2N5564	N	71	0.1	3.0	40	5.0	30	7500	-	12	50	5.0	10	45	NCB	RF AMPLIFIER
2N5565	N	71	0.1	3.0	40	5.0	30	7500	-	12	50	10	25	45	NCB	RF AMPLIFIER
2N5566	N	71	0.1	3.0	40	5.0	30	7500	-	12	50	20	50	45	NCB	RF AMPLIFIER
2N5911	N	78	0.1	5.0	25	7.0	40	5000	-	3.0	20	10	20	100	NZF-D	RF AMPLIFIER
2N5912	N	78	0.1	5.0	25	7.0	40	5000	-	3.0	30	15	40	100	NZF-D	RF AMPLIFIER
U257	N	78	0.1	5.0	25	5.0	40	5000	-	5.0	30	100	-	150	NZF-D	RF AMPLIFIER
U430	N	99	0.15	4.0	25	12	30	10000	-	7.5	12	-	-	150	NZA-D	RF AMPLIFIER
U431	N	99	0.15	6.0	25	24	60	10000	-	7.5	10	-	-	150	NZA-D	RF AMPLIFIER
U440	N	71	0.50	6.0	25	6.0	30	4500	-	3.5	-	10	-	200	NZF-D	RF AMPLIFIER
U441	N	71	0.50	6.0	25	6.0	30	4500	-	3.5	-	20	-	200	NZF-D	RF AMPLIFIER
U443	N	78	.5	6	25	6.0	30	4500	9000	3.5	-	10	-	200	NZF-D	RF AMPLIFIER
U444	N	78	.5	6	25	6.0	30	4500	9000	3.5	-	20	-	200	NZF-D	RF AMPLIFIER
2N3921	N	71	1.0	3.0	50	1.0	10	1500	-	18	2.0	5.0	10	35	NNR	GENERAL PURPOSE
2N3922	N	71	1.0	3.0	50	1.0	10	1500	-	18	2.0	5.0	25	35	NNR	GENERAL PURPOSE
2N3954	N	71	0.1	4.5	50	0.5	5.0	1000	-	4.0	0.5	5.0	10	35	NQP	GENERAL PURPOSE
2N3954A	N	71	0.1	4.5	50	0.5	5.0	1000	-	4.0	0.5	5.0	5.0	35	NQP	GENERAL PURPOSE
2N3955	N	71	0.1	4.5	50	0.5	5.0	1000	-	4.0	0.5	10	25	35	NQP	GENERAL PURPOSE
2N3955A	N	71	0.1	4.5	50	0.5	5.0	1000	-	4.0	0.5	10	15	35	NQP	GENERAL PURPOSE
2N3956	N	71	0.1	4.5	50	0.5	5.0	1000	-	4.0	0.5	15	50	35	NQP	GENERAL PURPOSE
2N3957	N	71	0.1	4.5	50	0.5	5.0	1000	-	4.0	0.5	20	75	35	NQP	GENERAL PURPOSE
2N3958	N	71	0.1	4.5	50	0.5	5.0	1000	-	4.0	0.5	25	100	35	NQP	GENERAL PURPOSE
2N5045	N	71	0.25	4.5	50	0.5	8.0	1500	-	8.0	200	5.0	67	25	NQP	GENERAL PURPOSE
2N5046	N	71	0.25	4.5	50	0.5	8.0	1500	-	8.0	200	10	133	25	NQP	GENERAL PURPOSE
2N5047	N	71	0.25	4.5	50	0.5	8.0	1500	-	8.0	200	15	200	25	NQP	GENERAL PURPOSE
2N5452	N	71	0.1	4.5	50	0.5	5.0	1000	-	4.0	20	5.0	5.0	1.0	NQP	GENERAL PURPOSE
2N5453	N	71	0.1	4.5	50	0.5	5.0	1000	-	4.0	20	10	10	1.0	NQP	GENERAL PURPOSE
2N5454	N	71	0.1	4.5	50	0.5	5.0	1000	-	4.0	20	15	25	1.0	NQP	GENERAL PURPOSE
DN5564	N	71	.1	3.0	40	5	50	7500	12500	12	50	5	10	65	NCB-D	GENERAL PURPOSE
DN5565	N	71	.1	3.0	40	5	50	7500	12500	12	50	10	25	65	NCB-D	GENERAL PURPOSE
DN5566	N	71	.1	3.0	40	5	50	7500	12500	12	50	20	50	65	NCB-D	GENERAL PURPOSE
U231	N	71	0.1	4.5	50	0.5	5.0	1000	-	6.0	80	5.0	10	35	NQP	GENERAL PURPOSE
U232	N	71	0.1	4.5	50	0.5	5.0	1000	-	6.0	80	10	25	35	NQP	GENERAL PURPOSE
U233	N	71	0.1	4.5	50	0.5	5.0	1000	-	6.0	80	15	50	35	NQP	GENERAL PURPOSE
U234	N	71	0.1	4.5	50	0.5	5.0	1000	-	6.0	80	20	75	35	NQP	GENERAL PURPOSE
U235	N	71	0.1	4.5	50	0.5	5.0	1000	-	6.0	80	25	100	35	NQP	GENERAL PURPOSE
U410	N	71	0.2	3.5	40	0.5	6.0	1000	-	-	13	10	10	20	NQP	GENERAL PURPOSE
U411	N	71	0.2	3.5	40	0.5	6.0	1000	-	-	13	10	25	20	NQP	GENERAL PURPOSE
U412	N	71	0.2	3.5	40	0.5	6.0	1000	-	-	13	40	80	20	NQP	GENERAL PURPOSE
DN5567	N	71	0.1	3.0	-40	5	60	-	-	7.0	-	20	-	-	NCB-D	SWITCH

Product Specifications (Cont'd)

Low Leakage Diodes

Part Number	Package (TO-)	Diode	Reverse Current (pA, Max.)	Breakdown Voltage (Volts)		Forward Voltage Drop Volts (Max.)	Capacitance (pF, Max.)
				Min.	Max.		
DPAD1	78	Dual	1	45	120	1.5	0.8
DPAD2	71	Dual	2	45	120	1.5	0.8
DPAD5	71	Dual	5	45	120	1.5	0.8
DPAD10	71	Dual	10	35	—	1.5	2.0
DPAD20	71	Dual	20	35	—	1.5	2.0
DPAD50	71	Dual	50	35	—	1.5	2.0
DPAD100	71	Dual	100	35	—	1.5	2.0
JPAD5	92	Single	5	35	—	1.5	2.0
JPAD10	92	Single	10	35	—	1.5	2.0
JPAD20	92	Single	20	35	—	1.5	2.0
JPAD50	92	Single	20	35	—	1.5	2.0
JPAD100	92	Single	50	35	—	1.5	2.0
JPAD200	92	Single	100	35	—	1.5	2.0
JPAD500	92	Single	500	35	—	1.5	2.0
PAD1	18	Single	1	45	120	1.5	0.8
PAD2	18	Single	2	45	120	1.5	0.8
PAD5	18	Single	5	45	120	1.5	0.8
PAD10	18	Single	10	35	—	1.5	2.0
PAD20	18	Single	20	35	—	1.5	2.0
PAD50	18	Single	50	35	—	1.5	2.0
PAD100	18	Single	100	35	—	1.5	2.0

Voltage Controlled Resistors

Part Number	N or P	Package (TO-)	Breakdown Voltage (Volts, Min.)	Threshold Voltage (Volts)		Resistance (Channel Ω)		Geometry
				Min.	Max.	Min.	Max.	
VCR2N	N	18	15	5.5	7.0	20	60	NCB
VCR3P	P	72	15	3.5	7.0	70	200	PS-A/B
VCR4N	N	18	15	3.5	7.0	200	600	NPA
VCR5P	P	72	15	3.5	7.0	300	900	PS-A/B
VCR7N	N	72	15	2.5	5.0	4000	8000	NT

P-Channel MOSFETs

Part Number	Package (TO-)	Operating Mode	Threshold Voltage (Volts, Max.)	Resistance Channel (Ω , Max.)	Leakage Channel On (mA)		Leakage Channel Off (nA, Max.)	Breakdown Voltage (Volts, Max.)	Input Capacitance (pF, Max.)	Reverse Capacitance (pF, Max.)	Geometry
					Min.	Max.					
3N163	72	ENH	5.0	250	5.0	30	—	40	2.5	0.7	MRA
3N164	72	ENH	5.0	300	3.0	30	—	30	2.5	0.7	MRA
MF823	18	ENH	6.0	—	3.0	—	20	25	6.0	1.5	MRA

Product Specifications (Cont'd)

Current Regulator Diodes

Part Number	Package (TO-)	Forward Current (mA)	Forward Current Tolerance (%)	Limiting Voltage (Volts, Max.)	Peak Operating Voltage (Volts, Max.)	Dynamic Impedance (M Ω , Max.)	Forward Capacitance (pF, typ)	Geometry
CR022	18	0.22	10	1.00	100	13	—	NKL
CR024	18	0.24	10	1.00	100	10	—	NKL
CR027	18	0.27	10	1.00	100	9.0	—	NKL
CR030	18	0.30	10	1.00	100	8.0	—	NKL
CR033	18	0.33	10	1.00	100	6.6	—	NKL
CR039	18	0.39	10	1.05	100	4.1	—	NKL
CR043	18	0.43	10	1.05	100	3.3	—	NKL
CR047	18	0.47	10	1.10	100	2.7	—	NKL
CR056	18	0.56	10	1.20	100	1.9	—	NKL
CR062	18	0.62	10	1.30	100	1.55	—	NKL
CR068	18	0.68	10	1.15	100	1.35	—	NKM
CR075	18	0.75	10	1.20	100	1.15	—	NKM
CR082	18	0.82	10	1.25	100	1.00	—	NKM
CR091	18	0.91	10	1.29	100	0.88	—	NKM
CR100	18	1.00	10	1.35	100	0.80	—	NKM
CR110	18	1.10	10	1.40	100	0.70	—	NKM
CR120	18	1.20	10	1.45	100	0.64	—	NKM
CR130	18	1.30	10	1.50	100	0.58	—	NKM
CR140	18	1.40	10	1.55	100	0.54	—	NKM
CR150	18	1.50	10	1.60	100	0.51	—	NKM
CR160	18	1.60	10	1.65	100	0.475	—	NKO
CR180	18	1.80	10	1.75	100	0.42	—	NKO
CR200	18	2.00	10	1.85	100	0.395	—	NKO
CR220	18	2.20	10	1.95	100	0.37	—	NKO
CR240	18	2.40	10	2.00	100	0.345	—	NKO
CR270	18	2.70	10	2.15	100	0.32	—	NKO
CR300	18	3.00	10	2.25	100	0.30	—	NKO
CR330	18	3.30	10	2.35	100	0.28	—	NKO
CR360	18	3.60	10	2.50	100	0.265	—	NKO
CR390	18	3.90	10	2.60	100	0.255	—	NKO
CR430	18	4.30	10	2.75	100	0.245	—	NKO
CR470	18	4.70	10	2.90	100	0.235	—	NKO
CR530	18	5.30	10	3.10	100	0.20	—	NKO
CRR0240	18	.24	25	1.0	100	.9	—	NKL
CRR0360	18	.36	25	1.05	100	4.1	—	NKL
CRR0560	18	.56	25	1.30	100	1.15	—	NKL
CRR0800	18	.80	25	1.35	100	0.8	—	NKL
CRR1250	18	1.95	25	1.60	100	.54	—	NKM
CRR1950	18	1.95	25	1.95	100	.37	—	NKM
CRR2900	18	2.90	25	2.35	100	.28	—	NKO
CRR4300	18	4.30	25	3.00	100	0.5	—	NKO
J500	92	0.24	20	1.20	50	5.0	2	NCL
J501	92	0.33	20	1.30	50	3.0	2	NCL
J502	92	0.43	20	1.50	50	2.0	2	NCL
J503	92	0.56	20	1.70	50	1.4	2	NCL
J504	92	0.75	20	1.90	50	1.0	2	NCL
J505	92	1.00	20	2.10	50	0.6	2	NCL
J506	92	1.40	20	2.50	50	0.4	2	NCL
J507	92	1.80	20	2.80	50	0.25	2	NCL
J508	92	2.40	20	3.10	50	0.25	2	NCL
J509	92	3.00	20	3.50	50	0.20	2	NCL
J510	92	3.60	20	3.90	50	0.20	2	NCL
J511	92	4.70	20	4.20	50	0.15	2	NCL
J552	92	0.05	50	1.5	50	2.0	2	NKL
J553	92	(.18 - 0.75)	—	.75	50	10	—	NCL
J554	92	(.06 - 1.6)	—	.75	50	1.0	—	NCL
J555	92	(1.4 - 2.6)	—	.75	50	.88	—	NCL
J556	92	(2.4 - 3.8)	—	.75	50	.6	—	NCL
J557	92	(3.6 - 5.3)	—	1.5	50	.48	—	NCL
J9100	92	0.05	50	1.5	50	2.0	2	NCL
JR135V	92	0.200	—	0.9	135	2.0	—	VRMA
JR170V	92	0.200	—	0.9	170	2.0	—	VRMA
JR200V	92	0.200	—	0.9	200	2.0	—	VRMA
JR220V	92	0.200	—	0.9	220	2.0	—	VRMA
JR240V	92	0.200	—	0.9	240	2.0	—	VRMA

SMALL SIGNAL FETs Additional Product Options for European Customers

CECC 50 000

CECC 50 000 is a European system of continuous product assessment intended to produce electronic components of assessed quality to specifications and procedures which conform to internationally recognized standards. Components produced under the system are accepted by all participating countries without further testing being necessary.

At this time, member countries of the CECC are Belgium, Denmark, Germany, France, Ireland, Italy, the Netherlands, Norway, Sweden, Switzerland and the United Kingdom.

Under this assessment scheme, devices are manufactured on an approved line to nationally approved specifications written in accordance with CECC rules. The manufacturer must comply with defined standards relating to organization, facilities and quality control procedures.

Specific device types are individually qualified against a fixed detail specification which has been approved by the British Standards Institute acting as the national supervising agency on behalf of CECC.

The CECC 50 000 scheme is administered in the UK by the BSI, and UK generated specifications are prefixed with the letters BS.

A number of popular standard device types are now qualified and the following detail specifications are available:

Type Number	BS Specification
2N3970/1/2	BS CECC 50012-001
2N4091/2/3	BS CECC 50012-002
2N4391/2/3	BS CECC 50012-004
2N4856/7/8	BS CECC 50012-005
2N4859/60/61	BS CECC 50012-005
2N4856A/7A/8A	BS CECC 50012-006
2N4859A/60A/61A	BS CECC 50012-006
2N3821/2	BS CECC 50012-007
2N3824	BS CECC 50012-008
2N4220/1/2	BS CECC 50012-009
2N4220/1A/2A	BS CECC 50012-009

Each of the approved types is now available with additional screening options, including high temperature reverse bias burn-in, of either 48, 72 or 168 hours duration. Screening details are appended to the detail specification and conform to appendix VI of the European Standard CECC 50 0000 ISSUE 3.

Product is released with a BS CECC certificate of conformity and will have been submitted to:

1. Group A sample inspection (lot by lot)
quality assessment tests, assuring product conforms to electrical specification.
2. Group B sample inspection (lot by lot)
reliability tests, including package related tests and 168 hours electrical endurance, to identify potential early failures.
3. Group C sample inspection (periodic—3 monthly)
long term reliability tests including 1000 hours of high temperature storage and electrical endurance.

Data from the inspection tests is available to the customer in the form of CTRs (certified test records).

Manufacturing of BS CECC product is carried out at the Siliconix UK facility located in Morriston, Swansea SA6 6NE, South Wales

In addition to BS CECC approved product, the Siliconix UK facility can provide internationally recognized high-reliability screening options on standard products. These include Mil-750 and custom screening options.

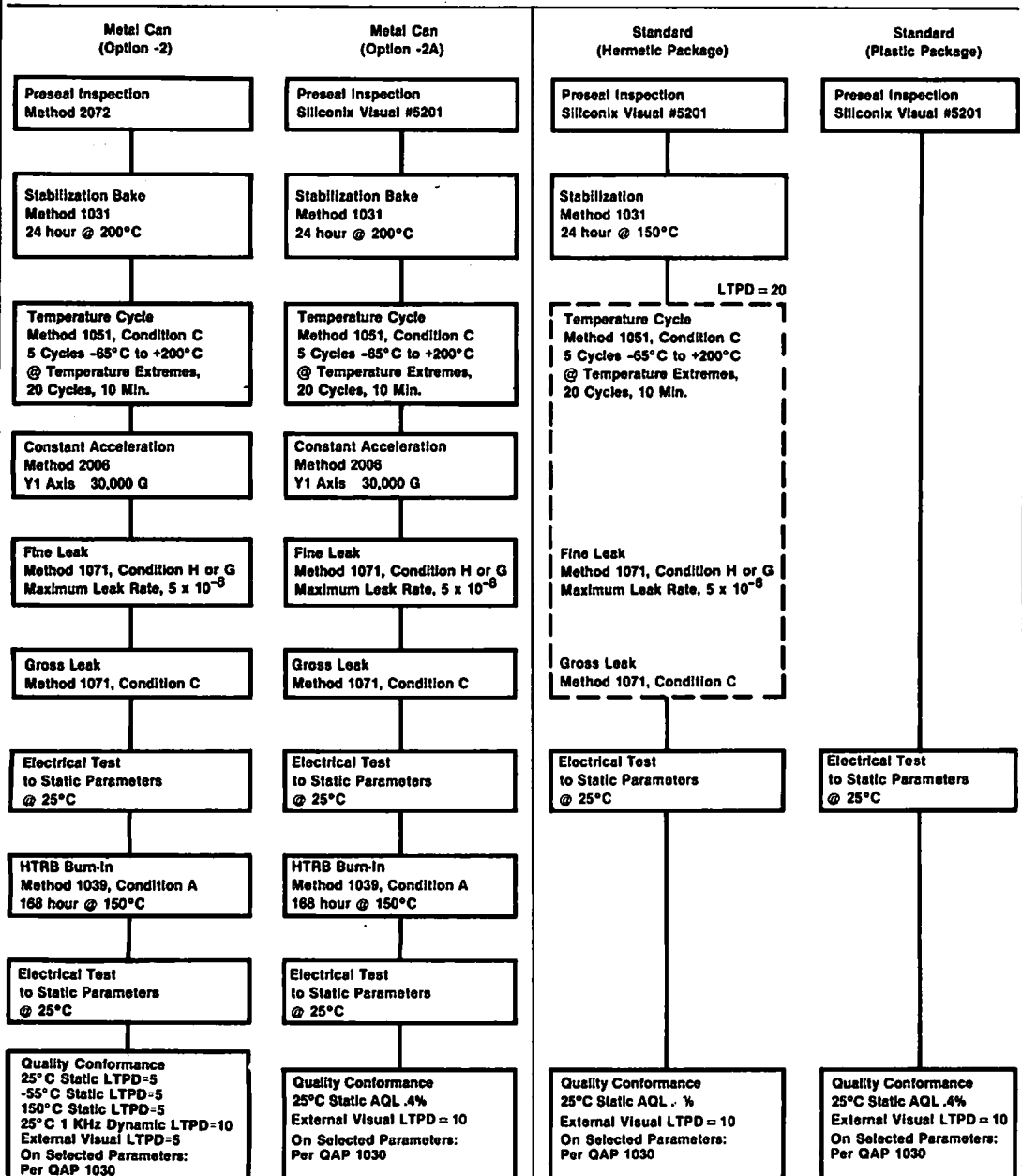
JAN, JANTX or JANTXV processing for certain JEDEC-registered FETs can also be supplied.

For additional information, enquiries may be directed to the nearest field sales office.

FET Process Option Flow Chart

Military Process

Industrial Process



NOTES: Processing and test methods are MIL-STD750 unless specified otherwise
-2A Significant savings.

How to Use the SMALL SIGNAL FET Cross Reference

The following examples illustrate how the FET Cross Reference and Index should be used:

Case (1) Recommended replacement offered by Siliconix is identical to Industry Part Number.

Industry Part Number	Type and Classification	Recommended Replacement
2N4391	N JFET	2N4391

Case (2) Recommended replacement offered by Siliconix is not identical to Industry Part Number.

Industry Part Number	Type and Classification	Recommended Replacement
2N3457	N JFET	2N4338

The recommended replacement may be exact, tighter or looser on electrical characteristics, and may be a different package or pin-out. Data sheets for both parts should, if possible, be reviewed for a complete comparison.

Type and classification abbreviations are described as follows:

BF (JFET Plastic)	ENH (Enhancement-Mode Normally-Off)
CR (Current Limited)	JPAD (Plastic Pico Ampere Diode)
CRR (Current Limiter)	JR (Plastic High Voltage Diode)
D (Dual)	N (N-Channel)
DM N-Channel DMOS	P (P-Channel)
DN (Dual N-Channel Metal Can)	PAD (Pico Ampere Diode)
DPAD (Dual Pico Ampere Diode)	SD (N-Channel DMOS)
FN (N-Channel Metal Can)	SI (N-Channel JFET Circuit)
	SST (JFET in SOT-23 Plastic Package)

SMALL FET Cross Reference

Industry Part Number	Type and Classification	Recommended Replacement	Date Sheet Page	Geometry Page	Industry Part Number	Type and Classification	Recommended Replacement	Date Sheet Page	Geometry Page
1N5283	CL N JFET	CR022			2N3437	N JFET	2N4341		
1N5284	CL N JFET	CR024			2N3438	N JFET	2N4341		
1N5285	CL N JFET	CR027			2N3452	N JFET	2N4340		
1N5286	CL N JFET	CR030			2N3453	N JFET	2N4338		
1N5287	CL N JFET	CR033			2N3454	N JFET	2N4338		
1N5288	CL N JFET	CR039			2N3455	N JFET	2N4340		
1N5289	CL N JFET	CR043			2N3456	N JFET	2N4338		
1N5290	CL N JFET	CR047			2N3457	N JFET	2N4338		
1N5291	CL N JFET	CR056			2N3458	N JFET	2N4341		
1N5292	CL N JFET	CR062			2N3459	N JFET	2N4341		
1N5293	CL N JFET	CR088			2N3460	N JFET	2N4340		
1N5294	CL N JFET	CR075			2N3608	P MCS ENH	3N163		
1N5295	CL N JFET	CR082			2N3684	N JFET	2N4339		
1N5296	CL N JFET	CR081			2N3685	N JFET	2N4339		
1N5297	CL N JFET	CR100			2N3686	N JFET	2N4340		
1N5298	CL N JFET	CR110			2N3687	N JFET	2N4341		
1N5299	CL N JFET	CR120			2N3819	N JFET	2N3819		
1N5300	CL N JFET	CR130			2N3820	P JFET	J270		
1N5301	CL N JFET	CR140			2N3821	N JFET	2N3821		
1N5302	CL N JFET	CR150			2N3822	N JFET	2N3822		
1N5303	CL N JFET	CR160			2N3823	N JFET	2N3823		
1N5304	CL N JFET	CR180			2N3824	N JFET	2N3824		
1N5305	CL N JFET	CR208			2N3921	D N JFET	2N3921		
1N5306	CL N JFET	CR220			2N3922	D N JFET	2N3922		
1N5307	CL N JFET	CR249			2N3954	D N JFET	2N3954		
1N5308	CL N JFET	CR270			2N3954A	O N JFET	2N3954A		
1N5309	CL N JFET	CR308			2N3955	O N JFET	2N3955		
1N5310	CL N JFET	CR330			2N3955A	D N JFET	2N3955A		
1N5311	CL N JFET	CR360			2N3956	D N JFET	2N3956		
1N5312	CL N JFET	CR390			2N3957	D N JFET	2N3957		
1N5313	CL N JFET	CR430			2N3958	D N JFET	2N3958		
1N5314	CL N JFET	CR470			2N3966	N JFET	2N3966		
2N2609	P JFET	2N2609			2N3967	N JFET	2N4221		
2N3066	N JFET	2N4340			2N3967A	N JFET	2N4221		
2N3067	N JFET	2N4338			2N3968	N JFET	2N4339		
2N3068	N JFET	2N4338			2N3968A	N JFET	2N4339		
2N3069	N JFET	2N4341			2N3969	N JFET	2N4339		
2N3070	N JFET	2N4339			2N3969A	N JFET	2N3970		
2N3071	N JFET	2N4338			2N3970	N JFET	2N3970		
2N3084	N JFET	2N4341			2N3971	N JFET	2N3971		
2N3085	N JFET	2N4341			2N3972	N JFET	2N3972		
2N3086	N JFET	2N4341			2N4084	O N JFET	2N4084		
2N3087	N JFET	2N4341			2N4085	D N JFET	2N4085		
2N3088	N JFET	2N4339			2N4091	N JFET	2N4091		
2N3088A	N JFET	2N4339			2N4091A	N JFET	2N4091		
2N3089	N JFET	2N4339			2N4092	N JFET	2N4092		
2N3089A	N JFET	2N4339			2N4092A	N JFET	2N4092		
2N3113	P JFET	2N3329			2N4093	N JFET	2N4093		
2N3365	N JFET	2N4340			2N4093A	N JFET	2N4093		
2N3366	N JFET	2N4338			2N4117	N JFET	2N4117		
2N3367	N JFET	2N4338			2N4117A	N JFET	2N4117A		
2N3368	N JFET	2N4341			2N4118	N JFET	2N4118		
2N3369	N JFET	2N4340			2N4118A	N JFET	2N4118A		
2N3370	N JFET	2N4339			2N4119	N JFET	2N4119		
2N3436	N JFET	2N4341			2N4119A	N JFET	2N4119A		

Refer to the Small Signal FET Design Catalog

Refer to the Small Signal FET Design Catalog

SMALL SIGNAL FET Cross Reference (Cont'd)

Industry Part Number	Type and Classification	Recommended Replacement	Data Sheet Page	Geometry Page	Industry Part Number	Type and Classification	Recommended Replacement	Data Sheet Page	Geometry Page
2N4120	P MOS ENH	3N163			2N4861	N JFET	2N4861		
2N4139	N JFET	2N3822			2N4861A	N JFET	2N4861A		
2N4220	N JFET	2N4220			2N4861JAN	N JFET	2N4861JAN		
2N4220A	N JFET	2N4220A			2N4861JANTX	N JFET	2N4861JANTX		
2N4221	N JFET	2N4221			2N4861JANTXV	N JFET	2N4861JANTXV		
2N4221A	N JFET	2N4221A			2N4867	N JFET	2N4867		
2N4222	N JFET	2N4222			2N4867A	N JFET	2N4867A		
2N4222A	N JFET	2N4222A			2N4868	N JFET	2N4868		
2N4223	N JFET	2N4223			2N4868A	N JFET	2N4868A		
2N4224	N JFET	2N4224			2N4869	N JFET	2N4869		
2N4267	P MOS ENH	3N163			2N4869A	N JFET	2N4869A		
2N4302	N JFET	PN4302-18			2N4977	N JFET	2N5432		
2N4303	N JFET	PN4303-18			2N4978	N JFET	2N5433		
2N4304	N JFET	PN4304-18			2N4979	N JFET	2N5434		
2N4338	N JFET	2N4338			2N5018	P JFET	2N5018		
2N4339	N JFET	2N4339			2N5019	P JFET	2N5019		
2N4340	N JFET	2N4340			2N5020	P JFET	2N3329		
2N4341	N JFET	2N4341			2N5045	D N JFET	2N5045		
2N4352	P MOS ENH	3N163			2N5046	D N JFET	2N5046		
2N4381	P JFET	2N2609			2N5047	D N JFET	2N5047		
2N4382	P JFET	2N5115			2N5103	N JFET	2N4416		
2N4391	N JFET	2N4391			2N5104	N JFET	2N4416		
2N4392	N JFET	2N4392			2N5105	N JFET	2N4416		
2N4393	N JFET	2N4393			2N5114	P JFET	2N5114		
2N4416	N JFET	2N4416			2N5115	P JFET	2N5115		
2N4416A	N JFET	2N4416A			2N5116	P JFET	2N5116		
2N4445	N JFET	2N5432			2N5158	N JFET	2N5434		
2N4446	N JFET	2N5433			2N5159	N JFET	2N5433		
2N4447	N JFET	2N5432			2N5196	D N JFET	2N5196		
2N4448	N JFET	2N5433			2N5197	D N JFET	2N5197		
2N4856	N JFET	2N4856			2N5198	D N JFET	2N5198		
2N4856A	N JFET	2N4856A			2N5199	D N JFET	2N5199		
2N4856JAN	N JFET	2N4856JAN			2N5245	N JFET	PN4416		
2N4856JANTX	N JFET	2N4856JANTX			2N5246	N JFET	J305-18		
2N4856JANTXV	N JFET	2N4856JANTXV			2N5247	N JFE	J304-18		
2N4857	N JFET	2N4857			2N5248	N JFET	2N5486		
2N4857A	N JFET	2N4857A			2N5257	N JFET	2N5457		
2N4857JAN	N JFET	2N4857JAN			2N5258	N JFET	2N5458		
2N4857JANTX	N JFET	2N4857JANTX			2N5259	N JFET	2N5459		
2N4857JANTXV	N JFET	2N4857JANTXV			2N5358	N JFET	2N4340		
2N4858	N JFET	2N4858			2N5359	N JFET	2N4340		
2N4858A	N JFET	2N4858A			2N5360	N JFET	2N4339		
2N4858JAN	N JFET	2N4858JAN			2N5361	N JFET	2N4339		
2N4858JANTX	N JFET	2N4858JANTX			2N5362	N JFET	2N4339		
2N4858JANTXV	N JFET	2N4858JANTXV			2N5363	N JFET	2N4222A		
2N4859	N JFET	2N4859			2N5364	N JFET	2N4224		
2N4859A	N JFET	2N4859A			2N5391	N JFET	2N4867A		
2N4859JAN	N JFET	2N4859JAN			2N5392	N JFET	2N4868A		
2N4859JANTX	N JFET	2N4859JANTX			2N5393	N JFET	2N4869A		
2N4859JANTXV	N JFET	2N4859JANTXV			2N5394	N JFET	2N4869A		
2N4860	N JFET	2N4860			2N5395	N JFET	2N4869A		
2N4860A	N JFET	2N4860A			2N5396	N JFET	2N4869A		
2N4860JAN	N JFET	2N4860JAN			2N5397	N JFET	U310		
2N4860JANTX	N JFET	2N4860JANTX			2N5398	N JFET	U312		
2N4860JANTXV	N JFET	2N4860JANTXV			2N5432	N JFET	2N5432		

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			Sheet Page	Geometry Page				Sheet Page	Geometry Page
2N5433	N JFET	2N5433			2N5951	N JFET	PM4416		
2N5434	N JFET	2N5434			2N5952	N JFET	1305		
2N5452	D N JFET	2N5452			2N5953	N JFET	1305		
2N5453	D N JFET	2N5453			2N6451	N JFET	2N4393		
2N5454	D N JFET	2N5454			2N6452	N JFET	2N4393		
2N5457	N JFET	2N5457			2N6453	N JFET	2N4393		
2N5458	N JFET	2N5458			2N6454	N JFET	2N4393		
2N5459	N JFET	2N5459			2N6483	D N JFET	U401		
2N5484	N JFET	2N5484			2N6484	D N JFET	U402		
2N5485	N JFET	2N5485			2N6585	D N JFET	U404		
2N5486	N JFET	2N5486			2N6588	N JFET	U290		
2N5515	D N JFET	2N5515			2N6556	V MOS N ENH	2N6556		
2N5516	D N JFET	2N5516			2N6557	V MOS N ENH	2N6557		
2N5517	D N JFET	2N5517			2N6558	V MOS N ENH	2N6558		
2N5518	D N JFET	2N5518			2N6559	V MOS N ENH	2N6559		
2N5519	D N JFET	2N5519			2N6660	V MOS N ENH	2N6660		
2N5520	D N JFET	2N5520			2N6661	P MOS ENH	2N6661		
2N5521	O N JFET	2N5521			3N145	P MOS ENH	3N163		
2N5522	D N JFET	2N5522			3N146	P MOS ENH	3N163		
2N5523	D N JFET	2N5523			3N155	P MOS ENH	3N163		
2N5524	D N JFET	2N5524			3N155A	P MOS ENH	3N163		
2N5545	D N JFET	2N5545			3N156	P MOS ENH	3N163		
2N5546	D N JFET	2N5546			3N156A	P MOS ENH	3N163		
2N5547	D N JFET	2N5547			3N157	P MOS ENH	3N163		
2N5549	N JFET	2N4392			3N157A	P MOS ENH	3N163		
2N5561	D N JFET	U401			3N158	P MOS ENH	3N163		
2N5562	D N JFET	U402			3N158A	P MOS ENH	3N163		
2N5563	D N JFET	U404			3N163	P MOS ENH	3N164		
2N5564	D N JFET	2N5564			3N164	P MOS ENH	3N164		
2N5565	D N JFET	2N5565			3N174	P MOS ENH	3N163		
2N5566	D N JFET	2N5566			14T	N JFET	2N3819		
2N5592	N JFET	2N3822			14T1	N JFET	PM4392		
2N5593	N JFET	2N3822			18T	N JFET	PM4302		
2N5594	N JFET	2N3822			19T	N JFET	PM4416		
2N5638	N JFET	2N5638			100S	N JFET	PM4304		
2N5639	N JFET	2N5639			100U	N JFET	2N3864		
2N5640	N JFET	2N5640			102M	N JFET	2N5486		
2N5647	N JFET	2N4117A			102S	N JFET	2N4302		
2N5648	N JFET	2N4117A			103M	N JFET	2N5457		
2N5649	N JFET	2N4117A			103S	N JFET	2N5459		
2N5801	N JFET	2N4393			104M	N JFET	2N5458		
2N5802	N JFET	2N4393			105M	N JFET	2N5459		
2N5803	N JFET	2N4392			105U	N JFET	2N4222		
2N5902	D N JFET	U421			106M	N JFET	2N5485		
2N5903	D N JFET	U422			107M	N JFET	2N5486		
2N5984	D N JFET	U423			110U	N JFET	2N4339		
2N5985	D N JFET	U421			115U	N JFET	2N4339		
2N5986	D N JFET	U422			120U	N JFET	2N4340		
2N5987	D N JFET	U423			125U	N JFET	2N4339		
2N5988	D N JFET	U423			130U	N JFET	2N4341		
2N5909	D N JFET	U423			135U	N JFET	2N4339		
2N5911	D N JFET	2N5911			155U	N JFET	2N4416		
2N5912	D N JFET	2N5912			182S	N JFET	2N4391		
2N5949	N JFET	PM4416			183S	N JFET	2N3823		
2N5950	N JFET	PM4416			197S	N JFET	2N4338		

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198S	N JFET	2N4340			2134U	D N JFET	2N3956		
199S	N JFET	2N4341			2136U	D N JFET	2N3957		
200S	N JFET	2N4392			2138U	D N JFET	2N3958		
200U	N JFET	2N3824			2139U	D N JFET	2N3958		
201S	N JFET	2N4391			2147U	D N JFET	2N3958		
202S	N JFET	2N4392			2148U	D N JFET	2N3958		
203S	N JFET	2N3821			2149U	D N JFET	2N3958		
204S	N JFET	2N3821			A513821	N JFET	J305		
210U	N JFET	2N4416			A513822	N JFET	J305		
231S	D N JFET	2N3954			A513823	N JFET	PN4416		
232S	D N JFET	2N3955			A513824	N JFET	J302-18		
233S	D N JFET	2N3956			A192	N JFET	2N4416		
234S	D N JFET	2N3957			A0830	D N JFET	U421		
235S	D N JFET	2N3958			A0831	D N JFET	U421		
241U	N JFET	2N4869			A0832	D N JFET	U422		
250U	N JFET	2N4091			A0833	D N JFET	U426		
251U	N JFET	2N4392			A0833A	D N JFET	U423		
703U	N JFET	2N4220			A0835	D N JFET	2N3921		
704U	N JFET	2N4220			A0836	D N JFET	2N3921		
705U	N JFET	2N4224			A0837	D N JFET	2N3922		
707U	N JFET	2N4860			A0838	D N JFET	2N4085		
714U	N JFET	2N3822			A0839	D N JFET	2N4085		
734U	N JFET	2N4416			A0840	D N JFET	2N5196		
734EU	N JFET	PN4416			A0841	D N JFET	2N5197		
751U	N JFET	2N4340			A0842	D N JFET	2N5199		
752U	N JFET	2N4340							
753U	N JFET	2N4341			AD3954	D N JFET	2N3954		
754U	N JFET	2N4340			AD3954A	D N JFET	2N3954A		
755U	N JFET	2N4341			AD3955	D N JFET	2N3955		
756U	N JFET	2N4340			AD3956	D N JFET	2N3956		
1277A	N JFET	2N3822			AD3957	D N JFET	2N3957		
1278A	N JFET	2N3821			AD3958	D N JFET	2N3958		
1279A	N JFET	2N3821			BC264	N JFET	PN4304		
1280A	N JFET	2N4224			BC264A	N JFET	PN4302		
1281A	N JFET	2N3822			BC264B	N JFET	PN4304		
1282A	N JFET	2N4341			BC264C	N JFET	PN4304		
1283A	N JFET	2N4340			BC264D	N JFET	PN4416		
1284A	N JFET	2N4222			BF244A/B/C*	N JFET	*Contact factory		
1285A	N JFET	2N3821			BF245A/B/C*	D N JFET	*Contact factory		
1286A	N JFET	2N4220			BF445	D N JFET	2N4416		
1325A	N JFET	2N4222			BF521	N JFET	2N5199		
1714A	N JFET	2N4340			BF521A	D N JFET	2N5199		
2000M	N JFET	2N3823			BF567	N JFET	2N3821		
2001M	N JFET	2N3823			BF567P	N JFET	2N4303		
2078A	D N JFET	2N3955			BF568	N JFET	2N3823		
2079A	D N JFET	2N3955			BF568P	N JFET	PN4416		
2080A	D N JFET	2N5546			BF570	N JFET	2N3821		
2081A	D N JFET	2N5546			BF571	N JFET	2N3822		
2083M	N JFET	2N3687			BF572	N JFET	2N3823		
2084M	N JFET	2N3686			BF573	N JFET	2N3821		
2093M	N JFET	2N3686			BF574	N JFET	2N4856		
2098A	D N JFET	2N5546			BF575	N JFET	2N4857		
2099A	D N JFET	2N5546			BF576	N JFET	2N4858		
2130U	D N JFET	2N5452			BF577	N JFET	2N4859		
2132U	D N JFET	2N3955			BF578	N JFET	2N4860		
					BF579	N JFET	2N4861		

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BF580	N JFET	2N4416A			C8022 Thru C8530 referenced Under 1N Series				
BFW10	N JFET	2N3923			CR8024D-4300	CL N FET	CR8024D-4300		
BFW11	N JFET	2N3922			DN5564-66	D N JFET	DN5564-66		
BFW54	N JFET	2N3922			DN5567	D N JFET	DN5567		
BFW55	N JFET	2N3922							
BFW56	N JFET	2N4689			DPAD1	D PAD N JFET	DPAD1		
BFW61	N JFET	2N4224			DPAD2	D PAD N JFET	DPAD2		
BSV22	N JFET	2N4416			DPAD5	D PAD N JFET	DPAD5		
BSV78	N JFET	2N4856A			DPAD10	D PAD N JFET	DPAD10		
BSV80	N JFET	2N4858A			DPAD20	D PAD N JFET	DPAD20		
C413N	N JFET	2N5434			DPAD50	D PAD N JFET	DPAD50		
C673	N JFET	2N4341			DPAD100	D PAD N JFET	DPAD100		
C674	N JFET	2N4341			DU4339	D N JFET	U235		
C680	N JFET	2N4338			DU4340	D N JFET	U235		
C680A	N JFET	2N4338			E100	N JFET	J203-18		
C681	N JFET	2N4338			E101	N JFET	J201-18		
C681A	N JFET	2N4338			E102	N JFET	J202-18		
C682	N JFET	2N4339			E103	N JFET	J105-18		
C682A	N JFET	2N4339			E105	N JFET	J105-18		
C683	N JFET	2N4339			E106	N JFET	J106-18		
C683A	N JFET	2N4339			E107	N JFET	J107-18		
C684	N JFET	2N4228			E108	N JFET	J108-18		
C684A	N JFET	2N4220			E109	N JFET	J109-18		
C685	N JFET	2N4220			E110	N JFET	J110-18		
C685A	N JFET	2N4220			E111	N JFET	J111-18		
C6690	N JFET	2N4341			E112	N JFET	J112-18		
C6691	N JFET	2N4341			E113	N JFET	J113-18		
C6692	N JFET	2N4340			E174	P JFET	J174-18		
C6693	N JFET	2N4092			E175	P JFET	J175-18		
C6694	N JFET	2N4091			E176	P JFET	J176-18		
C6695	N JFET	2N4091			E177	P JFET	J177-18		
C6696	N JFET	2N4091			E201	N JFET	J201-18		
C6697	N JFET	2N4093			E202	N JFET	J202-18		
C6698	N JFET	2N4093			E203	N JFET	J203-18		
C6699	N JFET	2N4093			E204	N JFET	J204-18		
C6699A	N JFET	2N4092			E210	N JFET	J210		
C6699B	N JFET	2N4092			E211	N JFET	J211		
C6699C	N JFET	2N4092			E212	N JFET	J212		
C6699D	N JFET	2N4092			E230	N JFET	J230-18		
C6699E	N JFET	2N4091			E231	N JFET	J231-18		
C6699F	N JFET	2N4091			E232	N JFET	J232-18		
C6699G	N JFET	2N4091			E270	P JFET	J270-18		
C6699H	N JFET	2N4091			E271	P JFET	J271-18		
C6699I	N JFET	2N4091			E300	N JFET	J300		
C6699J	N JFET	2N4091			E304	N JFET	J304		
C6699K	N JFET	2N4091			E305	N JFET	J305		
C6699L	N JFET	2N4091			E308	N JFET	J308		
C6699M	N JFET	2N4091			E309	N JFET	J309		
C6699N	N JFET	2N4091			E310	N JFET	J310		
C6699O	N JFET	2N4091			E400	D N JFET	U410		
C6699P	N JFET	2N4091			E401	D N JFET	U411		
C6699Q	N JFET	2N4091			E402	D N JFET	U410		
C6699R	N JFET	2N4091			E410	D N JFET	U410		
C6699S	N JFET	2N4091			E411	D N JFET	U411		
C6699T	N JFET	2N4091			E412	D N JFET	U412		

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E413	D N JFET	U410			FN4119	N J FET	FN4119		
E414	D N JFET	U411			FN4119A	N J FET	FN4119A		
E415	D N JFET	U412			FN4392	N J FET	FN4392		
E420	D N JFET	U440			FN4393	N J FET	FN4393		
E421	D N JFET	U441			FT0654A	N J FET	2N5486		
E430	D N JFET	U430			FT0654B	N J FET	2N5486		
E431	D N JFET	U431			FT0654C	N J FET	2N4221		
E500	CL N JFET	J500			FT0654D	N JFET	2N4221		
E501	CL N JFET	J501			FT704	P MOS ENH	3N163		
E502	CL N JFET	J502			GET5457	N JFET	2N5457		
E503	CL N JFET	J503			GET5458	N JFET	2N5458		
E504	CL N JFET	J504			GET5459	N JFET	2N5459		
E505	CL N JFET	J505			HDIG1030	P MOS ENH	3N163		
E506	CL N JFET	J506			ID100	D PAO N JFET	DP401		
E507	CL N JFET	J507			ID101	D PAO N JFET	DP4010		
E508	CL N JFET	J508			IMF3954	D N JFET	2N3954		
E509	CL N JFET	J509			IMF3954A	D N JFET	2N3954A		
E510	CL N JFET	J510			IMF3955	D N JFET	2N3955		
E511	CL N JFET	J511			IMF3955A	D N JFET	2N3955A		
EPAD50	DD N JFET	JPAD50			IMF3956	D N JFET	2N3956		
EPAD100	DD N JFET	JPAD100			IMF3957	D N JFET	2N3957		
EPAD200	DD N JFET	JPAD200			IMF3958	D N JFET	2N3958		
EPAD500	DD N JFET	JPAD500			IMF6485	D N JFET	U405		
FE100	N JFET	2N3821			IT100	P JFET	2N5116		
FE100A	N JFET	2N3821			IT101	P JFET	2N5114		
FE102	N JFET	2N4119			IT108	N JFET	2N5486		
FE102A	N JFET	2N4119			IT109	N JFET	U310		
FE104	N JFET	2N4118			IT1700	P MOS ENH	3N163		
FE104A	N JFET	2N4118			IT1702	P MOS ENH	3N163		
FE200	N JFET	2N3821			ITE500	CL N JFET	J500		
FE202	N JFET	2N3821			ITE501	CL N JFET	J501		
FE204	N JFET	2N3821			ITE502	CL N JFET	J502		
FE300	N JFET	2N3822			ITE503	CL N JFET	J503		
FE302	N JFET	2N3821			ITE504	CL N JFET	J504		
FE304	N JFET	2N3821			ITE505	CL N JFET	J505		
FE0654A	N JFET	2N5486			ITE506	CL N JFET	J506		
FE0654B	N JFET	2N5485			ITE507	CL N JFET	J507		
FE3819	N JFET	2N3819			ITE3066	N JFET	J202-18		
FE5457	N JFET	2N5458			ITE3067	N JFET	J201-18		
FE5458	N JFET	2N5458			ITE3068	N JFET	J201-18		
FE5459	N JFET	2N5459			ITE4117	N JFET	2N4117		
FE5484	N JFET	2N5484			ITE4118	N JFET	2N4118		
FE5485	N JFET	2N5485			ITE4119	N JFET	2N4119		
FE5486	N JFET	2N5486			ITE4338	N JFET	J201-18		
FM3954	D N JFET	2N3954			ITE4339	N JFET	J201-18		
FM3954A	D N JFET	2N3954A			ITE4340	N JFET	J202-18		
FM3955	D N JFET	2N3955			ITE4341	N JFET	J203-18		
FM3955A	D N JFET	2N3955A			ITE4391	N JFET	PN4391-18		
FM3956	D N JFET	2N3956			ITE4392	N JFET	PN4392-18		
FM3957	D N JFET	2N3957			ITE4393	N JFET	PN4393-18		
FM3958	D N JFET	2N3958			ITE4416	N JFET	PN4416		
FN4117	N JFET	FN4117			ITE4667	N JFET	J220-18		
FN4117A	N JFET	FN4117A			ITE4668	N JFET	J231-18		
FN4118	N JFET	FN4118			ITE4669	N JFET	J232-18		
FN4118A	N JFET	FN4118A			J105	N JFET	J106		

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Industry Part Number	Type and Classification	Recommended Replacement	Data Sheet Page	Geometry Page	Industry Part Number	Type and Classification	Recommended Replacement	Data Sheet Page	Geometry Page
J105-18	N JFET	J105-18			J403	D N JFET	U403		
J106	N JFET	J106			J404	D N JFET	U404		
J106-18	N JFET	J106-18			J405	D N JFET	U405		
J107	N JFET	J107			J410	D N JFET	U410		
J107-18	N JFET	J107-18							
J108	N JFET	J108			J411	D N JFET	U411		
J108-18	N JFET	J108-18			J412	D N JFET	U412		
J109	N JFET	J109			J500	CL N JFET	J500		
J109-18	N JFET	J109-18			J501	CL N JFET	J501		
J110	N JFET	J110			J502	CL N JFET	J502		
J110-18	N JFET	J110-18			J503	CL N JFET	J503		
J111	N JFET	J111			J504	CL N JFET	J504		
J111-18	N JFET	J111-18			J505	CL N JFET	J505		
J112	N JFET	J112			J506	CL N JFET	J506		
J112-18	N JFET	J112-18			J507	CL N JFET	J507		
J113	N JFET	J113			J508	CL N JFET	J508		
J113-18	N JFET	J113-18			J509	CL N JFET	J509		
J174	P JFET	J174			J510	CL N JFET	J510		
J174-18	P JFET	J174-18			J511	CL N JFET	J511		
J175	P JFET	J175			J552	CL N JFET	J552		
J175-18	P JFET	J175-18			J553	CL N JFET	J553		
J176	P JFET	J176			J554	CL N JFET	J554		
J176-18	P JFET	J176-18			J555	CL N JFET	J555		
J177	P JFET	J177			J556	CL N JFET	J556		
J177-18	P JFET	J177-18			J557	CL N JFET	J557		
J201	N JFET	J201			JPA05	PAD N JFET	JPA05		
J201-18	N JFET	J201-18			JPA010	PAD N JFET	JPA010		
J202	N JFET	J202			JPA020	PAD N JFET	JPA020		
J202-18	N JFET	J202-18			JPA050	PAD N JFET	JPA050		
J203	N JFET	J203			JPA0100	PAD N JFET	JPA0100		
J203-18	N JFET	J203-18							
J204	N JFET	J204			JPA0200	PAD N JFET	JPA0200		
J204-18	N JFET	J204-18			JPA0500	PAD N JFET	JPA0500		
J210	N JFET	J210			JR135V	CL N JFET	JR135V		
J211	N JFET	J211			JR170V	CL N JFET	JR170V		
J212	N JFET	J212			JR200V	CL N JFET	JR200V		
J230	N JFET	J230			JR220V	CL N JFET	JR220V		
J230-18	N JFET	J230-18			JR240V	CL N JFET	JR240V		
J231	N JFET	J231			J1401	D N JFET	U401		
J231-18	N JFET	J231-18			J1402	D N JFET	U402		
J232	N JFET	J232			J1403	D N JFET	U403		
J232-18	N JFET	J232-18			J1404	D N JFET	U404		
J270	P JFET	J270			J1405	D N JFET	U405		
J270-18	P JFET	J270-18			J1406	D N JFET	U406		
J271	P JFET	J271			J9100	CL N JFET	J9100		
J271-18	P JFET	J271-18							
J300	N JFET	J300			J211	N JFET	J211		
J300A/B/C/D	N JFET	J300A/B/C/D			J212	N JFET	J212		
J304	N JFET	J304			J300-18	N JFET	J300		
J305	N JFET	J305			J304-18	N JFET	J304		
J306	N JFET	J306			J305-18	N JFET	J305		
J308	N JFET	J308			K308-18	N JFET	J308		
J309	N JFET	J309			K309-18	N JFET	J309		
J310	N JFET	J310			K310-18	N JFET	J310		
J401	D N JFET	U401			KE3684	N JFET	2N4341		
J402	D N JFET	U402			KE3685	N JFET	2N4340		

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KE3686	N JFET	2N4339			MK10	N JFET	2N4416		
KE3687	N JFET	2N4338			MMBF4310	N JFET	SS1310		
KE3673	N JFET	J304-18			MMBF5484	N JFET	SS15484		
KE3970	N JFET	PM4391-18			MMBF5486	N JFET	SS15486		
KE3971	N JFET	PM4392-18			MMBF4416	N JFET	SS14416		
KE3972	N JFET	PM4393-18			MMBF5310	N JFET	SS1310		
KE4091	N JFET	PM4391-18			MMBF4391	N JFET	SS1113		
KE4092	N JFET	PM4392-18			MMBF4860	N JFET	SS1112		
KE4093	N JFET	PM4393-18			MMBF4392	N JFET	SS1112		
KE4220	N JFET	2N5457			MMBF4393	N JFET	SS1111		
KE4221	N JFET	2N5457			MMF1	D N JFET	2N3921		
KE4222	N JFET	2N5459			MMF2	D N JFET	2N3921		
KE4223	N JFET	J304-18			MMF3	D N JFET	2N3921		
KE4224	N JFET	J304-18			MMF4	D N JFET	2N3921		
KE4391	N JFET	PM4391-18			MMF5	D N JFET	2N3921		
KE4392	N JFET	PM4392-18			MMF6	D N JFET	2N3921		
KE4393	N JFET	PM4393-18			MMT3823	N JFET	2N3823		
KE4416	N JFET	PM4416			MPF102	N JFET	MPF102		
KE4886	N JFET	PM4391-18			MPF103	N JFET	2N5457		
KE4887	N JFET	PM4392-18			MPF104	N JFET	2N5458		
KE4888	N JFET	PM4393-18			MPF105	N JFET	2N5459		
KE4889	N JFET	PM4391-18			MPF106	N JFET	2N5485		
KE4890	N JFET	PM4392-18			MPF107	N JFET	2N5486		
KE4891	N JFET	PM4393-18			MPF108	N JFET	MPF108		
KE5103	N JFET	J305			MPF109	N JFET	MPF109		
KE5104	N JFET	J304			MPF111	N JFET	MPF111		
KE5105	N JFET	J306			MPF112	N JFET	MPF112		
KK4416-18	N JFET	PM4416			MPF256	N JFET	J309		
LD603	N JFET	2N4221A			MPF820	N JFET	U310		
LD604	N JFET	2N4221A			MPF970	P JFET	J174		
LD605	N JFET	2N4221A			MPF971	P JFET	J176		
M163	P MOS ENH	3N163			MPF4391	N JFET	PM4391-18		
M164	P MOS ENH	3N164			MPF4392	N JFET	PM4392-18		
MEM520	P MOS ENH	3N164			MPF4393	N JFET	PM4393-18		
MEM520C	P MOS ENH	3N164			MF500	N JFET	2N4416		
MEM561	P MOS ENH	3N163			MF501	N JFET	2N4416		
MEM561C	P MOS ENH	3N163			MF506	N JFET	2N4416		
MEM806	P MOS ENH	3N163			MF510	N JFET	2N4393		
MEM806A	P MOS ENH	3N163			MF511	N JFET	2N4393		
MEF823	P MOS ENH	MEF823			MF520	N JFET	2N4339		
MEF2000	N JFET	2N4416			MF521	N JFET	2N4339		
MEF2001	N JFET	2N4416			MF522	N JFET	2N4339		
MEF2004	N JFET	2N4093			MF523	N JFET	2N4340		
MEF2005	N JFET	2N4092			MF530	N JFET	2N4341		
MEF2006	N JFET	2N4091			MF531	N JFET	2N4339		
MEF2007	N JFET	2N4860			MF532	N JFET	2N4341		
MEF2008	N JFET	2N4859			MF533	N JFET	2N4339		
MEF2009	N JFET	2N4859			MF580	N JFET	2N5432		
MEF2010	N JFET	2N5434			MF581	N JFET	2N5432		
MEF2011	N JFET	2N5433			MF582	N JFET	2N5433		
MEF2012	N JFET	2N5432			MF583	N JFET	2N5434		
MEF2093	N JFET	2N4338			MF584	N JFET	2N5433		
MEF2094	N JFET	2N4339			MF585	N JFET	2N4859		
MEF2095	N JFET	2N4540			MF4302	N JFET	2N4302		
MEF4009	P JFET	2N3329			MF4303	N JFET	2N4303		

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NF4304	N JFET	2N4304			PF511	P JFET	2N5014		
NF4445	N JFET	2N5432			SD210DE	D N JFET	SD210DE		
NF4446	N JFET	2N5433			SD211DE	D N JFET	SD211DE		
NF4447	N JFET	2N5432			SD212DE	D N JFET	SD212DE		
NF4448	N JFET	2N5433			SD213DE	D N JFET	SD213DE		
NF5163	N JFET	2N5163			SD214DE	D N JFET	SD214DE		
NF5457	N JFET	2N5457			SD215DE	D N JFET	SD215DE		
NF5458	N JFET	2N5458			SU2078	D N JFET	U425		
NF5459	N JFET	2N5459			SU2079	D N JFET	U425		
NF5484	N JFET	2N5484			SU2098	D N JFET	2N5197		
NF5485	N JFET	2N5485			SU2098A	D N JFET	2N5197		
NF5486	N JFET	2N5486			SU2098B	D N JFET	2N5197		
NF5555	N JFET	2N5555			SU2099	D N JFET	2N5197		
NF5638	N JFET	2N5638			SU2099A	D N JFET	2N5197		
NF5639	N JFET	2N5639			SU2365	D N JFET	U401		
NF5640	N JFET	2N5640			SU2365A	D N JFET	U401		
NF5653	N JFET	2N5653			SU2366	D N JFET	U402		
NF5654	N JFET	2N5654			SU2366A	D N JFET	U402		
PA01	PAD N JFET	PA01			SU2367	D N JFET	U403		
PA02	PAD N JFET	PA02			SU2367A	D N JFET	U403		
PA05	PAD N JFET	PA05			SU2368	D N JFET	U404		
PA010	PAD N JFET	PA010			SU2368A	D N JFET	U404		
PA020	PAD N JFET	PA020			SU2369	D N JFET	U405		
PA050	PAD N JFET	PA050			SU2369A	D N JFET	U405		
PA0100	PAD N JFET	PA0100			SU2410	D N JFET	U424		
P1086	P JFET	P1086			SU2411	D N JFET	U425		
P1086-18	P JFET	P1086-18			SU2412	D N JFET	U426		
P1087	P JFET	P1087			T05802	D N JFET	U421		
P1087-18	P JFET	P1087-18			T05802A	D N JFET	U421		
PA4091	N JFET	PA4091							
PA4092	N JFET	PA4092			T05903	D N JFET	U422		
PA4093	N JFET	PA4093			T05903A	D N JFET	U422		
PA4117	N JFET	PA4117			T05904	D N JFET	U423		
PA4117A	N JFET	PA4117A			T05904A	D N JFET	U423		
PA4118	N JFET	PA4118			T05905	D N JFET	U424		
PA4118A	N JFET	PA4118A							
PA4119	N JFET	PA4119			T05905A	D N JFET	U424		
PA4119A	N JFET	PA4119A			T05906	D N JFET	U425		
PA4120	N JFET	PA4120			T05907	D N JFET	U422		
PA4120A	N JFET	PA4120A							
PA4302	N JFET	PA4302			T05908	D N JFET	U423		
PA4302-18	N JFET	PA4302-18			T05908A	D N JFET	U426		
PA4303	N JFET	PA4303			T05909	D N JFET	U428		
PA4303-18	N JFET	PA4303-18			T05909A	D N JFET	U426		
PA4304	N JFET	PA4304			T05911	D N JFET	2N5911		
PA4304-18	N JFET	PA4304-18							
PA4391	N JFET	PA4391			T05911A	D N JFET	2N5911		
PA4391-18	N JFET	PA4391-18			T05912	D N JFET	2N5912		
PA4392	N JFET	PA4392			T05912A	D N JFET	2N5912		
PA4392-18	N JFET	PA4392-18			TIS14	N JFET	2N4340		
					TIS25	D N JFET	U401		
PA4393	N JFET	PA4393							
PA4393-18	N JFET	PA4393-18			TIS26	D N JFET	U402		
PA4416	N JFET	PA4416			TIS27	D N JFET	U404		
PA5163	N JFET	PA5163			TIS41	N JFET	2N4859		
PF510	P JFET	2N5018			TIS58	N JFET	J305-18		
					TIS59	D N JFET	U1837		

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TI573	N JFET	PN4391-18			U275A	N JFET	2N4119A		
TI574	N JFET	PN4392-18			U280	D N JFET	U231		
TI575	N JFET	PN4393-18			U281	D N JFET	U231		
TI588	N JFET	2N5486			U282	D N JFET	U232		
TI541	N JFET	2N4859			U283	D N JFET	U232		
TI542	N JFET	PN4393-18			U284	D N JFET	U233		
TI417	N JFET	2N4117			U285	D N JFET	U234		
TI417A	N JFET	2N4117A			U290	N JFET	U290		
TI418	N JFET	2N4118			U291	N JFET	U281		
TI418A	N JFET	2N4118A			U295	N JFET	U295		
TI419	N JFET	2N4119			U296	N JFET	U296		
TI419A	N JFET	2N4119A			U300	P JFET	2N5114		
TI438	N JFET	2N4338			U301	P JFET	2N5115		
TI439	N JFET	2N4339			U304	P JFET	U304		
TI4340	N JFET	2N4340			U305	P JFET	U305		
TI4341	N JFET	2N4341			U306	P JFET	U306		
TP5114	P JFET	2N5114			U308	N JFET	U308		
TP5115	P JFET	2N5115			U309	N JFET	U309		
TP5116	P JFET	2N5116			U310	N JFET	U310		
U182	N JFET	2N4857			U311	N JFET	U311		
U183	N JFET	2N3824			U320	N JFET	U290		
U197	N JFET	2N4339			U321	N JFET	U291		
U198	N JFET	2N4340			U322	N JFET	U290		
U199	N JFET	2N4341			U401	D N JFET	U401		
U200	N JFET	U200			U402	D N JFET	U402		
U201	N JFET	U201			U403	D N JFET	U403		
U202	N JFET	U202			U404	D N JFET	U404		
U221	N JFET	2N4391			U405	D N JFET	U405		
U222	N JFET	2N4391			U406	D N JFET	U406		
U231	D N JFET	U231			U410	D N JFET	U410		
U232	D N JFET	U232			U411	D N JFET	U411		
U233	D N JFET	U233			U412	D N JFET	U412		
U234	D N JFET	U234			U421	D N JFET	U421		
U235	D N JFET	U235			U422	D N JFET	U422		
U240	N JFET	2N5432			U423	D N JFET	U423		
U241	N JFET	2N5433			U424	D N JFET	U424		
U242	N JFET	2N5432			U425	D N JFET	U425		
U243	N JFET	2N5433			U426	D N JFET	U426		
U248	D N JFET	U421			U427	D N JFET	U427		
U248A	D N JFET	U425			U428	D N JFET	U428		
U249	D N JFET	U422			U430	D N JFET	U430		
U249A	D N JFET	U422			U431	D N JFET	U431		
U258	D N JFET	U423			U440	D N JFET	U440		
U250A	D N JFET	U423			U441	D N JFET	U441		
U251	D N JFET	U424			U443	D N JFET	U443		
U251A	D N JFET	U426			U444	D N JFET	U444		
U254	N JFET	2N4859			U508	N JFET	CR030		
U255	N JFET	2N4860			U1177	N JFET	2N4280A		
U256	N JFET	2N4861			U1178	N JFET	2N3821		
U257	D N JFET	U257			U1179	N JFET	2N3821		
U273	N JFET	2N4118A			U1180	N JFET	2N4221A		
U273A	N JFET	2N4118A			U1181	N JFET	2N4220A		
U274	N JFET	2N4119A			U1182	N JFET	2N3821		
U274A	N JFET	2N4119A			U1277	N JFET	2N4339		
U275	N JFET	2N4119A			U1278	N JFET	2N4339		

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U1279	N JFET	2N4340			UC220	N JFET	2N3822		
U1280	N JFET	2N4339			UC240	N JFET	2N4869		
U1281	N JFET	2N3822			UC241	N JFET	2N4869		
U1282	N JFET	2N4341			UC250	N JFET	2N4091		
U1283	N JFET	2N4340			UC251	N JFET	2N4392		
U1284	N JFET	2N4341			UC401	P JFET	2N5116		
U1285	N JFET	2N4220			UC450	P JFET	2N5114		
U1288	N JFET	2N4341			UC451	P JFET	2N5116		
U1287	N JFET	2N4092			UC588	N JFET	2N4417		
U1322	N JFET	2N4221A			UC703	N JFET	2N4220		
U1323	N JFET	2N4221A			UC704	N JFET	2N4220		
U1324	N JFET	2N4220A			UC705	N JFET	2N4224		
U1325	N JFET	2N4222			UC707	N JFET	2N4860		
U1420	N JFET	2N3821			UC714	N JFET	2N3822		
U1421	N JFET	2N3822			UC714E	N JFET	J203-18		
U1422	N JFET	2N3822			UC734	N JFET	2N4416		
U1714	N JFET	2N4340			UC734E	N JFET	2N4416		
U1837E	N JFET	U1837			UC751	N JFET	2N4340		
U1897	N JFET	U1897			UC752	N JFET	2N4340		
U1897-18	N JFET	U1897-18			UC753	N JFET	2N4341		
U1897E	N JFET	U1897-18			UC754	N JFET	2N4340		
U1898	N JFET	U1898-18			UC755	N JFET	2N4341		
U1898E-18	N JFET	U1898-18			UC756	N JFET	2N4340		
U1898E	N JFET	U1898-18			UC805	P JFET	2N3331		
U1899	N JFET	U1899			UC807	N JFET	2N4860		
U1899-18	N JFET	U1899-18			UC814	P JFET	2N3331		
U1899E	N JFET	U1899-18			UC1700	P MOS ENH	3N163		
U1994E	N JFET	U1994			UC1764	P MOS ENH	3N163		
U2047E	N JFET	PN4416			UC2130	O N JFET	2N5452		
U3080	N JFET	2N4341			UC2132	O N JFET	2N3955		
U3001	N JFET	2N4339			UC2134	O N JFET	2N3956		
U3002	N JFET	2N4338			UC2136	D N JFET	2N3957		
U3010	N JFET	2N4341			UC2138	D N JFET	2N3958		
U3011	N JFET	2N4340			UC2139	D N JFET	2N3958		
U3012	N JFET	2N4338			UC2147	O N JFET	2N3956		
UC20	N JFET	2N4341			UC2148	O N JFET	2N3958		
UC100	N JFET	2N4339			UC2149	D N JFET	2N3958		
UC110	N JFET	2N4339			UCR2N	N JFET	VCRRN		
UC115	N JFET	2N4340			UCR3P	P JFET	VCRRP		
UC120	N JFET	2N3866			VCRAH	N JFET	VCRAH		
UC130	N JFET	2N4341			VCRRP	P JFET	VCRRP		
UC155	N JFET	2N4416			VCRRP	P JFET	2N5116		
UC280	N JFET	2N3824			VCRRN	N JFET	VCRRN		
UC201	N JFET	2N3824			VCRR11N	N JFET	VCRR11N		
UC210	N JFET	2N4416			WKS457	N JFET	2N5457		
					WKS458	N JFET	2N5458		
					WKS459	N JFET	2N5459		

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CMOS Gate Arrays

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Siliconix offers a wide selection of arrays ranging from 180 to 2400 gates, available in two different speed versions.

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Our CAD system was created to simplify the entering of schematic information. Moreover, special error checking routines help identify potential problems before any prototypes are generated.

Siliconix also offers a comprehensive design manual that leads you through the entire design process—from concept to prototype evaluation.

Each of the arrays is available in both ISO5 (five micron) and ISO3 (three micron) processes. The gate width is inversely proportional to the speed of the process.

The current family of arrays is shown in Table 1:

Table 2 lists typical gate delays for both processes with a fanout of two.

Designation	Total Cells	Gate Equivalent	I/O Buffers	Bonding Pads
ISO5I/ISO3I	120	180	30	40
ISO5A/ISO3A	240	360	36	46
ISO5B/ISO3B	360	540	48	58
ISO5C/ISO3C	480	720	54	64
ISO5D/ISO3D	640	960	62	72
ISO5E/ISO3E	800	1200	68	78
ISO5F/ISO3F	1000	1500	76	86
ISO5G/ISO3G	1200	1800	82	92
ISO5H/ISO3H	1600	2400	90	100

Table 1

Performance—ISO- 3, 5 Technology
Typical Gate Delays (ns) F.O.=2
(Room Temperature) ($V_{DD}=5V$)

Gate Type	ISO-3	ISO-5
Inverter	1.2	2.2
2-Input NAND	1.6	2.8
2-Input NOR	1.7	3.7
3-Input NAND	2.0	3.6
3-Input NOR	2.5	7.8
4-Input NAND	2.5	4.7

Table 2

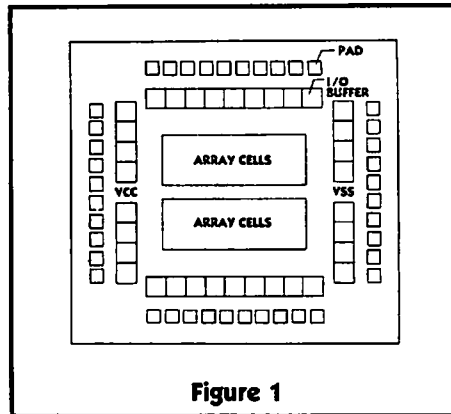


Figure 1

Designed For Maximum Flexibility.

The basic architecture of the arrays is shown in Figure 1. Bonding pads are located around the perimeter of the chip. Just inside the pads are the I/O buffer cells; in the center of the chip are the array cells. All the arrays are organized in the same manner and differ only by the amount of cells available.

These contact points or "windows" are programmable, allowing maximum routing flexibility. Individual N and P transistors may be configured into a variety of SSI and MSI logic elements. Pre-designed or characterized SSI and MSI functional building-blocks are called macrocells.

Easy-to-Use Cells.

Figure 2 illustrates the basic array cell which consists of three pairs of NMOS and PMOS transistors. The gate is common between adjacent N and P-channel devices. To simplify design and layout, each gate has four possible contact points; each source-and-drain has six contact points.

Macrocells.

The gate array design manual contains over 100 characterized macrocells. When used, all contact opening and metal routing within the macrocell is made automatically, eliminating the possibility of error when the function is selected.

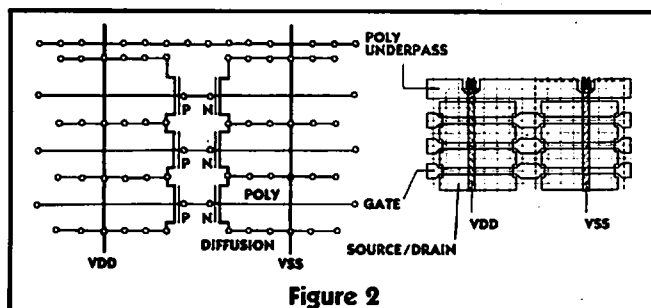
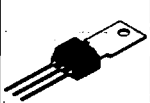


Figure 2

Introduction	0
Interface	1
Analog Switches/Multiplexers	2
A/D Converters	3
D/A Converters	4
Linear	5
Power Conversion	6
Telecommunications	7
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MOSPOWER Prime Product Selector Guide

 P-CHANNEL

Packages:								
BV_{DSS} (Volts)	TO-3	TO-220	TO-39	TO-237	TO-92	TO-202	Quad Side Braze	Quad Plastic
600-650	VNT013A 11.7A, 0.55 Ω , 650V	VNT008D 6A, 1.5 Ω , 650V						
	VNT008A 6A, 1.5 Ω , 650V							
450-500	VNP006A 20A, 0.3 Ω , 500V	IRF840 8A, 0.85 Ω , 500V	IRFF430 2.5A, 1.5 Ω , 400V					
	IRF450 13A, 0.4 Ω , 500V	VN5001D/IRF830 4.5A, 1.5 Ω , 500V						
	BUZ46 9.6A, 0.6 Ω , 500V	IRF820 2.5A, 3 Ω , 500V						
	IRF440 8A, 0.85 Ω , 500V							
	VNP002A† 6.5A, 1.5 Ω , 500V							
	VN5001A/IRF430 4.5A, 1.5 Ω , 500V							
	IRF420 2.5A, 3 Ω , 500V							
350-400	VNM005A 25A, 0.2 Ω , 400V	IRF740 10A, 0.55 Ω , 400V	IRFF330 3.4A, 1 Ω , 400V					
	IRF350 15A, 0.3 Ω , 400V	VN4000D/IRF730 5.5A, 1 Ω , 400V	IRFF320 2.1A, 1.8 Ω , 400V					
	BUZ84 10.5A, 0.4 Ω , 400V	IRF720 3A, 1.8 Ω , 400V	IRFF310 1.4A, 3.6 Ω , 400V					
	IRF340 10A, 0.55 Ω , 400V	IRF710 1.5A, 3.6 Ω , 400V						
	VNM001A† 8A, 1 Ω , 400V							
	BUZ69 8A, 1 Ω , 400V							
	VN4000A/IRF330 5.5A, 1 Ω , 400V							
	IRF320 3A, 1.8 Ω , 400V							

Packages:								
V_{DSS} (Volts)	TO-3	TO-220	TO-39	TO-237	TO-92	TO-202	Quad Side Braze	Quad Plastic
120-240	VN004A 45A, 0.06 Ω , 200V	VN2406D 1.4A, 6 Ω , 240V	VN2406B 0.8A, 6 Ω , 240V	VN2406M 0.3A, 6 Ω , 240V	VN2406L 0.21A, 6 Ω , 240V			
	IRF250 30A, 0.085 Ω , 200V	IRF640 18A, 0.18 Ω , 200V	IRFF230 5.5A, 0.4 Ω , 200V	VN2410M 0.25A, 10 Ω , 240V	VN2410L 0.16A, 10 Ω , 240V			
	BUZ36 22A, 0.12 Ω , 200V	IRF630 9A, 0.4 Ω , 200V	IRFF220 3.5A, 0.8 Ω , 200V	BSR72 0.25A, 10 Ω , 170V	BS107 0.1A, 28 Ω , 200V			
	IRF240 18A, 0.18 Ω , 200V	BUZ32 9.5A, 0.4 Ω , 200V	IRFF210 2.2A, 1.5 Ω , 200V	BSR76 0.25A, 10 Ω , 120V				
	BUZ35 9.9A, 0.4 Ω , 200V	IRF620 5A, 0.8 Ω , 200V						
	IRF230 9A, 0.4 Ω , 200V	IRF610 2.5A, 1.5 Ω , 200V						
	IRF220 5A, 0.8 Ω , 200V							
60-100	VNE003A 60A, 0.035 Ω , 100V	IRF540 27A, 0.085 Ω , 100V	IRFF130 8A, 0.18 Ω , 100V	VP1008M 0.37A, 5 Ω , -100V	VP1008L 0.23A, 5 Ω , -100V	VN88AF 1.5A, 4 Ω , 80V	VQ1006P 0.40A, 4.5 Ω , 90V	VQ1006J 0.40A, 4.5 Ω , 90V
	IRF150 40A, 0.055 Ω , 100V	VN1000D/IRF530 12A, 0.18 Ω , 100V	IRFF120 6A, 0.30 Ω , 100V	VN0808M 0.35A, 4 Ω , 80V	2N7000 0.20A, 5 Ω , 60V	VN80AF 1.3A, 5 Ω , 80V	VQ2006P 0.41A, 5 Ω , -90V	VQ2006J 0.41A, 5 Ω , -90V
	BUZ24 32A, 0.06 Ω , 100V	BUZ72A 9A, 0.25 Ω , 100V	IRFF110 3.7A, 0.6 Ω , 100V	VN0606M 0.4A, 3 Ω , 60V	VN0610L* 0.2A, 5 Ω , 60V	VN66AF 1.7A, 3 Ω , 60V	VQ1004P 0.46A, 3.5 Ω , 60V	VQ1004J 0.46A, 3.5 Ω , 60V
	IRF140 27A, 0.085 Ω , 100V	IRF520 8A, 0.30 Ω , 100V	VNE011B 4A, 0.5 Ω , 100V	VN10KM* 0.3A, 5 Ω , 60V	VN0610LL 0.2A, 5 Ω , 60V	VN67AF 1.6A, 3.5 Ω , 60V	VQ1000P 0.225A, 5.5 Ω , 60V	VQ1000J 0.225A, 5.5 Ω , 60V
	VN1000A/IRF130 12A, 0.18 Ω , 100V	IRF510 2.5A, 0.6 Ω , 100V	VP1008B 0.9A, 5 Ω , -100V	VN10LM 0.3A, 5 Ω , 60V	BS170 0.2A, 5 Ω , 60V		VQ2004P 0.41A, 5 Ω , -60V	VQ2004J 0.41A, 5 Ω , -60V
	IRF120 8A, 0.3 Ω , 100V	VN88AD 1.7A, 4 Ω , 80V	2N6661** 0.9A, 4 Ω , 90V	VN2222LM 0.25A, 7.5 Ω , 60V	VN2222L* 0.15A, 7.5 Ω , 60V			
	VN0600A 16A, 0.12 Ω , 60V	VN0600D 16A, 0.12 Ω , 60V	2N6660 1.1A, 3 Ω , 60V		VN2222LL 0.15A, 7.5 Ω , 60V			
		VN66AD 1.9A, 3 Ω , 60V						
30-50	VN0400A 16A, 0.12 Ω , 40V	VN0400D 16A, 0.12 Ω , 40V	2N6659 1.4A, 1.8 Ω , 35V	VN0300M 0.7A, 1.2 Ω , 30V	BS250 0.1A, 14 Ω , -45V	VN46AF 1.6A, 3 Ω , 40V	VQ1001P 0.85A, 1 Ω , 30V	VQ1001J 0.85A, 1 Ω , 30V
	2N6656 2A, 1.8 Ω , 35V	BUZ10/BUZ71 12A, 0.1 Ω , 50V	VP0300B 1.3A, 2.5 Ω , -30V	VP0300M 0.48A, 2.5 Ω , -30V	VP0300L 0.3A, 2.5 Ω , -30V	VN40AF 1.3A, 5 Ω , 40V	VQ2001P 0.60A, 2 Ω , -30V	VQ2001J 0.60A, 2 Ω , -30V
		VN0300D 2.5A, 1.5 Ω , 30V						
Specialty Products (N- and P-Channel Quad Arrays)							VQ3001P ±30V, 3 Ω Total	VQ3001J ±30V, 3 Ω Total
							VQ7254P ±20V, 3 Ω Total	VQ7254J ±20V, 3 Ω Total

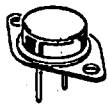
*Zener Protected Gate **JAN/JANTX/JANTXV QPL

† 200°C Operating Temperature Rating

MOSPOWER Selector Guide

N-Channel MOSPOWER

Device	Breakdown Voltage (Volts)	r _{DS} (on) (ohms)	I _D Continuous (Amps)	Power Dissipation (Watts)	Part Number
	650	0.550	11.700	176	VNT013A
	650	0.750	9.300	150	VNT012A
	650	1.500	5.700	125	VNT008A
	650	2.000	5.000	125	VNT009A
	600	0.550	11.700	176	VNS013A
	600	0.750	9.300	150	VNS012A
	600	1.500	5.700	125	VNS008A
	600	2.000	5.000	125	VNS009A
	500	0.300	20.000	250	VNP006A
	500	0.400	13.000	150	IRF450
	500	0.400	12.000	150	2N6770
	500	0.500	12.000	150	IRF452
	500	0.600	9.600	125	BUZ45
	500	0.850	8.000	125	IRF440
	500	1.100	7.000	125	IRF442
	500	1.500	6.500	175	BUP71
	500	1.500	6.500	75	IRF430
	500	1.500	4.500	75	2N6762
	500	1.500	4.500	100	BUP66
	500	1.500	4.500	100	VN5001A
	500	1.500	4.500	175	VNP002A
	500	2.000	4.200	78	BUZ46
	500	2.000	4.000	100	BUP67
	500	2.000	4.000	75	IRF432
	500	2.000	4.000	100	VN5002A
	500	3.000	2.500	40	IRF420
	500	4.000	2.000	40	IRF422
	450	0.300	20.000	250	VNN006A
	450	0.400	13.000	150	IRF451
	450	0.500	11.000	150	2N6769
	450	0.500	12.000	150	IRF453
	450	0.850	8.000	125	IRF441
	450	1.100	7.000	125	IRF443
	450	1.500	6.500	175	BUP70
	450	1.500	6.500	75	IRF431
	450	1.500	4.500	100	BUP64
	450	1.500	4.500	100	VN4501A
	450	1.500	4.500	175	VNN002A
	450	2.000	4.000	75	2N6761
	450	2.000	4.000	100	BUP65
	450	2.000	4.000	75	IRF433
	450	2.000	4.000	175	VN4502A
	450	3.000	2.500	40	IRF421
	450	4.000	2.000	40	IRF423
	400	0.200	25.000	250	VNM005A
	400	0.300	15.000	150	IRF350
	400	0.300	14.000	150	2N6768
	400	0.400	13.000	150	IRF352
	400	0.400	10.500	125	BUZ64
	400	0.550	10.000	125	IRF340
	400	0.800	8.000	125	IRF342
	400	1.000	8.000	175	BUP69
	400	1.000	8.000	75	IRF330
	400	1.000	6.000	125	BUP62
	400	1.000	6.000	125	VN4000A
	400	1.000	5.500	75	2N6760
	400	1.000	5.900	75	BUZ63
	400	1.000	5.500	175	VNM001A
	400	1.500	5.000	125	BUP63
	400	1.500	5.000	75	IRF332
	400	1.500	4.500	125	VN4001A
	400	1.800	3.000	40	IRF320
	400	2.500	2.500	40	IRF322
	350	0.200	25.000	250	VNL005A
	350	0.300	15.000	150	IRF351
	350	0.400	13.000	150	IRF353
	350	0.400	12.000	150	2N6767
	350	0.550	10.000	125	IRF341



TO-3

MOSPOWER Selector Guide (Cont'd)

N-Channel MOSPOWER (Cont'd)

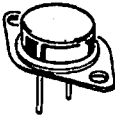
Device	Breakdown Voltage (Volts)	r _{DS(on)} (ohms)	I _D Continuous (Amps)	Power Dissipation (Watts)	Part Number
	350	0.800	8.000	125	IRF343
	350	1.000	8.000	175	BUP68
	350	1.000	8.000	75	IRF331
	350	1.000	6.000	125	BUP60
	350	1.000	6.000	125	VN3500A
	350	1.000	5.500	175	VNL001A
	350	1.500	5.000	125	BUP61
	350	1.500	5.000	75	IRF333
	350	1.500	4.500	75	2N6759
	350	1.500	4.500	125	VN3501A
	350	1.800	3.000	40	IRF321
	350	2.500	2.500	40	IRF323
	200	0.060	47.000	250	VN1004A
	200	0.085	30.000	150	2N6766
	200	0.085	30.000	150	IRF250
	200	0.120	25.000	150	IRF252
	200	0.120	22.000	125	BUZ36
	200	0.180	18.000	125	IRF240
	200	0.220	16.000	125	IRF242
	200	0.400	9.900	78	BUZ35
	200	0.400	9.000	75	2N6758
	200	0.400	9.000	75	IRF230
	200	0.600	8.000	75	IRF232
	200	0.800	5.000	40	IRF220
	200	1.200	4.000	40	IRF222
	150	0.060	47.000	250	VNG004A
	150	0.085	30.000	150	IRF251
	150	0.120	25.000	150	2N6765
	150	0.120	25.000	150	IRF253
	150	0.180	18.000	125	IRF241
	150	0.220	16.000	125	IRF243
	150	0.400	9.000	75	IRF231
	150	0.600	8.000	75	2N6757
	150	0.600	8.000	75	IRF233
	150	0.800	5.000	40	IRF221
	150	1.200	4.000	40	IRF223
	120	0.180	14.000	75	VN1200A
	120	0.250	12.000	100	VN1201A
	100	0.035	65.000	250	VNE003A
	100	0.055	40.000	150	IRF150
	100	0.055	38.000	150	2N6764
	100	0.080	32.000	125	BUZ24
	100	0.080	27.000	125	IRF140
	100	0.085	33.000	150	IRF152
	100	0.110	24.000	125	IRF142
	100	0.180	14.000	75	IRF130
	100	0.180	14.000	100	VN1000A
	100	0.180	14.000	75	2N6756
	100	0.200	10.000	78	BUZ23
	100	0.250	12.000	75	IRF132
	100	0.250	12.000	100	VN1001A
	100	0.300	8.000	40	IRF120
	100	0.400	7.000	40	IRF122
	90	4.000	1.900	25	2N6858
	90	4.500	1.800	25	VN99AA
	90	5.000	1.700	25	VN90AA
	80	0.180	14.000	100	VN0800A
	80	0.250	12.000	100	VN0801A
	60	0.035	60.000	250	VNC003A
	60	0.055	40.000	150	IRF151
	60	0.080	33.000	150	IRF153
	60	0.080	31.000	150	2N6763
	60	0.085	27.000	125	IRF141
	60	0.110	24.000	125	IRF143
	60	0.120	18.000	100	VN0600A
	60	0.150	16.000	100	VN0601A
	60	0.180	14.000	75	IRF131



TO-3

MOSPOWER Selector Guide (Cont'd)

N-Channel MOSPOWER (Cont'd)

Device	Breakdown Voltage (Volts)	r _{DS} (on) (ohms)	I _D Continuous (Amps)	Power Dissipation (Watts)	Part Number
 TO-3	60	0.250	12.000	75	2N6755
	60	0.250	12.000	75	IRF133
	60	0.300	8.000	40	IRF121
	60	0.400	10.000	80	VN64GA
	60	0.400	7.000	40	IRF123
	60	3.000	2.000	25	2N6657
	60	3.500	2.000	25	VN67AA
	40	0.120	18.000	100	VN0400A
	40	0.150	16.000	100	VN0401A
	35	1.800	2.000	25	2N6656
	35	2.500	2.000	25	VN35AA
 TO-220	650	1.500	6.000	125	VNT008D
	650	2.000	5.000	125	VNT009D
	600	1.500	5.700	125	VNS008D
	600	2.000	5.000	125	VNS009D
	500	0.850	8.000	125	IRF840
	500	1.100	7.000	125	IRF842
	500	1.500	4.500	75	IRF830
	500	1.500	4.500	75	VN5001D
	500	2.000	4.000	75	BUZ42
	500	2.000	4.000	75	IRF832
	500	2.000	4.000	75	VN5002D
	500	3.000	2.500	40	IRF820
	500	3.000	2.400	40	BUZ74
	500	4.000	2.000	40	IRF822
	450	0.850	8.000	125	IRF841
	450	1.100	7.000	125	IRF843
	450	1.500	4.500	75	IRF831
	450	1.500	4.500	75	VN4501D
	450	2.000	4.000	75	IRF833
	450	2.000	4.000	75	VN4502D
	450	3.000	2.500	40	IRF821
	450	4.000	2.000	40	IRF823
	400	0.550	10.000	125	IRF740
	400	0.800	8.000	125	IRF742
	400	1.000	6.000	75	VN4000D
	400	1.000	5.500	75	BUZ60
	400	1.000	5.500	75	IRF730
	400	1.500	5.000	75	VN4001D
	400	1.500	4.500	75	IRF732
	400	1.800	3.000	40	BUZ76
	400	1.800	3.000	40	IRF720
	400	2.500	2.500	40	IRF722
	400	3.600	1.500	20	IRF710
	400	5.000	1.300	20	IRF712
	350	0.550	10.000	125	IRF741
	350	0.800	8.000	125	IRF743
	350	1.000	6.000	75	VN3500D
	350	1.000	5.500	75	IRF731
	350	1.500	5.000	75	VN3501D
	350	1.500	4.500	75	IRF733
	350	1.800	3.000	40	IRF721
	350	2.500	2.500	40	IRF723
	350	3.600	1.500	20	IRF711
	350	5.000	1.300	20	IRF713
	240	6.000	1.400	20	VN2406D
	200	0.180	18.000	125	IRF640
	200	0.220	16.000	125	IRF642
	200	0.400	9.500	75	BUZ32
	200	0.400	9.000	75	IRF630
	200	0.600	8.000	75	IRF632
	200	0.800	5.000	40	IRF620
	200	1.200	4.000	40	IRF622
	200	1.500	2.500	20	IRF610
	200	2.400	2.000	20	IRF612

MOSPOWER Selector Guide (Cont'd)

N-Channel MOSPOWER (Cont'd)

Device	Breakdown Voltage (Volts)	r _{DS} (on) (ohms)	I _D Continuous (Amps)	Power Dissipation (Watts)	Part Number
 TO-220	170	6.000	1.400	20	VN1706D
	150	0.180	18.000	125	IRF641
	150	0.220	16.000	125	IRF643
	150	0.400	9.000	75	IRF631
	150	0.600	8.000	75	IRF633
	150	0.800	5.000	40	IRF621
	150	1.200	4.000	40	IRF623
	150	1.500	2.500	20	IRF611
	150	2.400	2.000	20	IRF613
	120	0.180	14.000	45	VN1200D
	120	0.250	12.000	75	VN1201D
	120	6.000	1.400	20	VN1206D
	100	0.085	27.000	125	IRF540
	100	0.110	24.000	125	IRF542
	100	0.180	14.000	75	IRF530
	100	0.180	14.000	75	VN1000D
	100	0.200	12.000	75	BUZ20
	100	0.250	12.000	75	IRF532
	100	0.250	12.000	75	VN1001D
	100	0.250	9.000	40	BUZ72A
	100	0.300	8.000	40	IRF520
	100	0.400	7.000	40	IRF522
	100	0.600	2.500	20	IRF510
	100	0.800	2.000	20	IRF512
	80	0.180	14.000	75	VN0800D
	80	0.250	12.000	75	VN0801D
	80	4.000	1.700	20	BSR82
	80	4.000	1.700	20	VN88AD
	80	4.500	1.600	20	VN89AD
	60	0.085	27.000	125	IRF541
	60	0.110	24.000	125	IRF543
	60	0.120	18.000	75	VN0600D
	60	0.150	16.000	75	VN0601D
	60	0.180	14.000	75	IRF531
	60	0.250	12.000	75	IRF533
	60	0.300	8.000	40	IRF521
	60	0.400	7.000	40	IRF523
	60	0.600	2.500	20	IRF511
	60	0.800	2.000	20	IRF513
	60	3.000	1.900	20	VN66AD
	60	3.500	1.800	20	VN67AD
	50	0.100	19.300	75	BUZ10
	50	0.100	12.000	40	BUZ71
	40	0.120	18.000	75	VN0400D
	40	0.150	16.000	75	VN0401D
	40	3.000	1.900	20	BSR80
	40	3.000	1.900	20	VN46AD
	40	5.000	1.500	20	VN40AD
	30	1.200	2.500	20	VN0300D
 TO-202	80	4.000	1.500	15	VN88AF
	80	4.500	1.400	15	VN89AF
	80	5.000	1.300	15	VN80AF
	60	3.000	1.700	15	VN66AF
	60	3.500	1.600	15	VN67AF
	40	3.000	1.600	15	VN48AF
	40	5.000	1.300	15	VN40AF

MOSPOWER Selector Guide (Cont'd)

N-Channel MOSPOWER (Cont'd)

Device	Breakdown Voltage (Volts)	r _{DS} (on) (ohms)	I _D Continuous (Amps)	Power Dissipation (Watts)	Part Number
 TO-52	60	5.000	0.200	0.315	VN10KE
	60	5.000	0.200	0.315	VN10LE
 TO-39	500	1.500	2.500	25	2N6802
	500	1.500	2.500	75	IRFF430
	500	2.000	2.230	75	IRFF432
	500	3.000	1.600	40	IRFF420
	500	3.000	1.500	20	2N6794
	500	4.000	1.400	40	IRFF422
	450	1.500	2.500	25	2N6801
	450	1.500	2.500	75	IRFF431
	450	2.000	2.230	75	IRFF433
	450	3.000	1.600	40	IRFF421
	450	3.000	1.500	20	2N6793
	450	4.000	1.400	40	IRFF423
	400	1.000	3.370	25	IRFF330
	400	1.000	3.000	25	2N6800
	400	1.500	2.750	25	IRFF332
	400	1.800	2.090	20	IRFF320
	400	1.800	2.000	20	2N6792
	400	2.500	1.770	20	IRFF322
	400	3.600	1.350	15	IRFF310
	400	3.600	1.250	15	2N6788
	400	5.000	1.150	15	IRFF312
	350	1.000	3.370	25	IRFF331
	350	1.000	3.000	25	2N6799
	350	1.500	2.750	25	IRFF333
	350	1.800	2.090	20	IRFF321
	350	1.800	2.000	20	2N6791
	350	2.500	1.770	20	IRFF323
	350	3.600	1.350	15	IRFF311
	350	3.600	1.250	15	2N6785
	350	5.000	1.150	15	IRFF313
	240	6.000	0.800	6.25	VN2406B
	200	0.400	5.500	25	2N6798
	200	0.400	5.500	25	IRFF230
	200	0.600	4.500	25	IRFF232
	200	0.800	3.500	20	2N6790
	200	0.800	3.500	20	IRFF220
	200	1.200	2.800	20	IRFF222
	200	1.500	2.250	15	2N6784
	200	1.500	2.200	15	IRFF210
	200	2.400	1.800	15	IRFF212
	170	6.000	0.800	6.25	VN1706B
	150	0.400	5.500	25	2N6797
	150	0.400	5.500	25	IRFF231
	150	0.600	4.500	25	IRFF233
	150	0.800	3.500	20	2N6789
	150	0.800	3.500	20	IRFF221
	150	1.200	2.800	20	IRFF223
	150	1.500	2.250	15	2N6783
	150	1.500	2.200	15	IRFF211
	150	2.400	1.800	15	IRFF213
	150	4.500	0.500	15	NOS100B
	120	4.500	0.500	15	NOS101B
	120	6.000	0.800	6.25	VN1206B
	100	0.180	8.000	25	2N6796
	100	0.180	8.000	25	IRFF130
	100	0.250	7.000	25	IRFF132
	100	0.300	6.000	20	2N6788

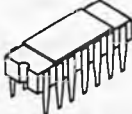
MOSPOWER Selector Guide (Cont'd)

N-Channel MOSPOWER (Cont'd)

Device	Breakdown Voltage (Volts)	r _{DS} (on) (ohms)	I _D Continuous (Amps)	Power Dissipation (Watts)	Part Number
 TO-39	100	0.300	6.000	20	IRFF120
	100	0.400	5.000	20	IRFF122
	100	0.500	4.000	15	VNE010B
	100	0.500	4.000	15	VNE011B
	100	0.600	3.680	15	IRFF110
	100	0.600	3.500	15	2N6782
	100	0.800	2.010	15	IRFF112
	90	4.000	0.900	75	2N6661
	90	4.500	0.900	6.25	VN99AB
	90	5.000	0.800	6.25	VN90AB
	80	0.500	4.000	15	VND010B
	80	0.500	4.000	15	VND011B
	80	4.500	0.800	15	NOS102B
	60	0.180	8.000	25	2N6795
	60	0.180	8.000	25	IRFF131
	60	0.250	7.000	25	IRFF133
	60	0.300	6.000	20	2N6787
	60	0.300	6.000	20	IRFF121
	60	0.400	5.000	20	IRFF123
	60	0.500	4.000	15	VNC010B
	60	0.500	4.000	15	VNC011B
	60	0.600	3.500	15	2N6781
	60	0.600	3.680	15	IRFF111
	60	0.800	2.010	15	IRFF113
	60	3.000	1.100	6.25	2N6660
	60	3.500	1.000	6.25	VN67AB
	35	1.800	1.400	6.25	2N6659
	35	2.500	1.200	6.25	VN35AB
	30	1.200	0.350	6.25	VN0300B
 TO-237	240	6.000	0.300	1.0	VN2406M
	240	10.000	0.250	1.0	BSR76
	240	10.000	0.250	1.0	VN2410M
	170	6.000	0.300	1.0	VN1706M
	170	10.000	0.250	1.0	BSR72
	170	10.000	0.250	1.0	VN1710M
	170	24.000	0.080	1.0	VN1720M
	120	6.000	0.300	1.0	VN1206M
	120	10.000	0.250	1.0	BSR70
	120	10.000	0.250	1.0	VN1210M
	80	4.000	0.350	1.0	BSR67
	80	4.000	0.350	1.0	VN0808M
	60	3.000	0.400	1.0	BSR66
	60	3.000	0.400	1.0	VN0606M
	60	5.000	0.300	1.0	VN10KM
	60	5.000	0.300	1.0	VN10LM
	60	7.500	0.300	1.0	BSR65
	60	7.500	0.250	1.0	BSR64
	60	7.500	0.250	1.0	VN2222KM
	60	7.500	0.250	1.0	VN2222LM
 TO-92	240	6.000	0.210	0.4	VN2406L
	240	10.000	0.160	0.4	VN2410L
	240	24.000	0.080	0.4	VN2420L
	200	24.000	0.080	0.4	VN2020L
	200	28.000	0.100	0.4	BS107
	170	6.000	0.210	0.4	VN1706L
	170	10.000	0.160	0.4	VN1710L
	120	5.000	0.230	0.4	VP1008L
	120	6.000	0.210	0.4	VN1206L
	120	10.000	0.160	0.4	VN1210L
	60	5.000	0.200	0.4	VN0610L
	60	5.000	0.200	0.4	VN0610LL
	60	5.000	0.179	0.4	BS170
	60	7.500	0.150	0.4	VN2222L

MOSPOWER Selector Guide (Cont'd)

N-Channel MOSPOWER (Cont'd)

Device	Breakdown Voltage (Volts)	$r_{DS(on)}$ (ohms)	I_D Continuous (Amps)	Power Dissipation (Watts)	Part Number
 TO-92	60 30	7.500 1.200	0.150 0.350	0.4 0.4	VN2222LL VN0300L
 14-Pin Dual-In-Line (Side Brazed)	90 60 60 30	4.500 3.500 5.500 1.000	0.400 0.460 0.225 0.850	1.3 1.3 1.3 1.3	VQ1006P VQ1004P VQ1000P VQ1001P
 14-Pin Dual-In-Line (Plastic)	90 60 60 30	4.500 3.500 5.500 1.000	0.400 0.460 0.225 0.850	1.3 1.3 1.3 1.3	VQ1006J VQ1004J VQ1000J VQ1001J

MOSPOWER Selector Guide (Cont'd)

P-Channel MOSPOWER

Device	Breakdown Voltage (Volts)	$r_{DS(on)}$ (ohms)	I_D Continuous (Amps)	Power Dissipation (Watts)	Part Number
 TO-38	-100	5.0	-0.90	6.25	VP1008B
	-80	5.0	-0.9	6.25	VP0808B
	-30	2.5	-1.3	6.25	VP0300B
 TO-237	-100	5.0	-0.37	1.0	VP1008M
	-80	5.0	-0.37	1.0	VP0808M
	-40	2.5	-0.48	1.0	VP0300M
	-30	2.5	-0.48	1.0	BSR78
 TO-92	-80	5.0	-0.23	0.4	VP0808L
	-45	14.0	-0.107	0.4	BS250
	-30	2.5	-0.30	0.4	VP0300L
 14-Pin Dual-In-Line (Side Brazed)	-90	5.0	-0.4	1.3	VQ2008P
	-60	5.0	-0.4	1.3	VQ2004P
	-40	2.0	-0.6	1.3	VQ2001P
 14-Pin Dual-In-Line (Plastic)	-90	5.0	-0.4	1.3	VQ2008J
	-60	5.0	-0.4	1.3	VQ2004J
	-40	2.0	-0.6	1.3	VQ2001J

N- and P-Channel Quad MOSPOWER

Device	Breakdown Voltage (Volts)	$r_{DS(on)}$ (ohms)	I_D Continuous (Amps)	Power Dissipation (Watts)	Part Number
 14-Pin Dual-In-Line (Side Brazed)	30	3.0**	N-0.85 P-0.60	1.3	VQ3001P
	20	3.0**	N-2.0 P-2.0	1.75	VQ7254P
 14-Pin Dual-In-Line (Plastic)	30	3.0**	N-0.85 P-0.60	1.3	VQ3001J
	20	3.0**	N-2.0 P-2.0	1.75	VQ7254J

**Total (N + P)

MOSPOWER Process Flows

LEVEL -1, -2, -3, -4, -5, -7 *

These optional flows include environmental and product conditioning which satisfy most Military/Hi-Rel requirements. Group B and Group C lot qualifications can also be performed at additional cost.

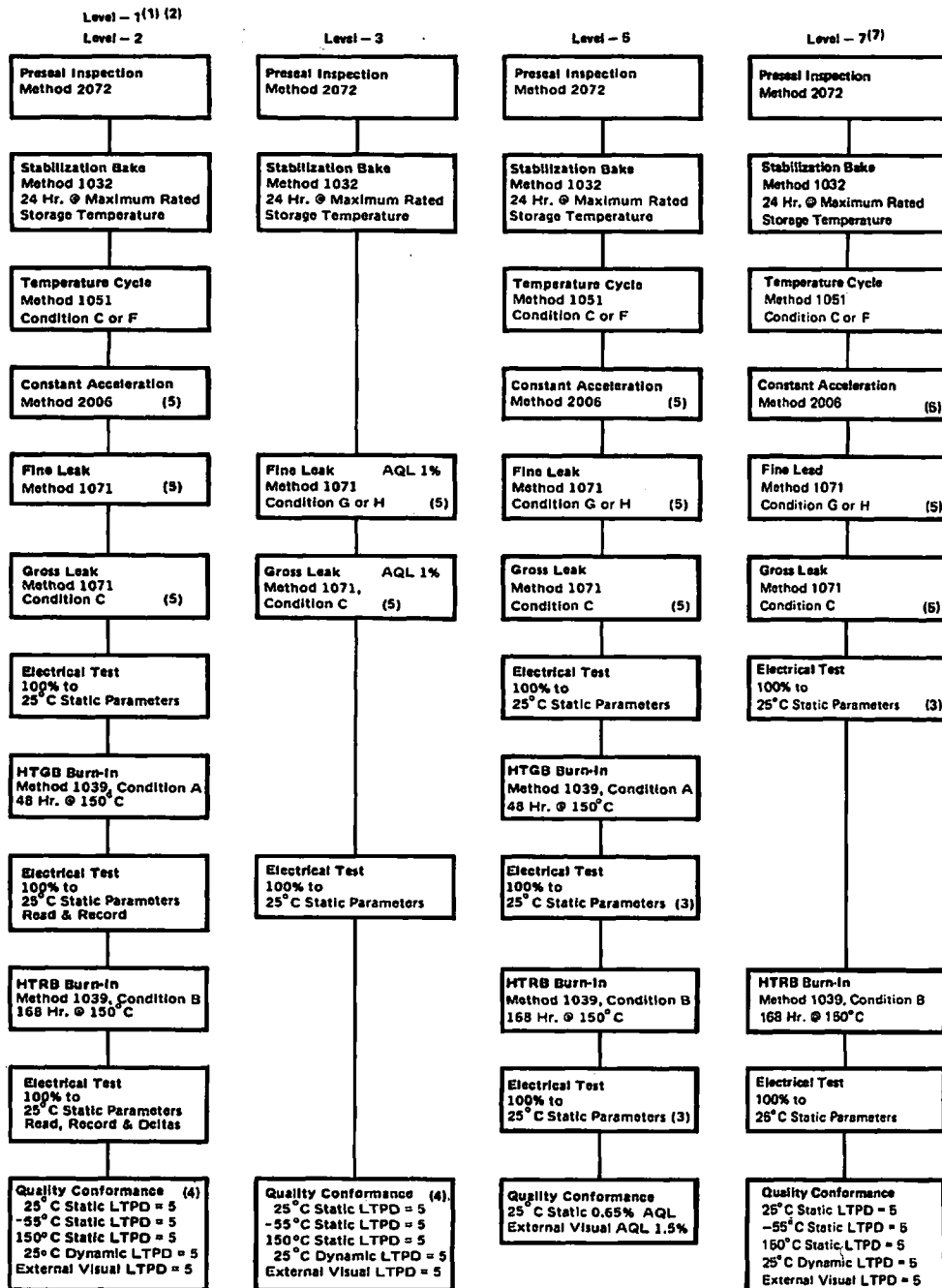
LEVEL -6

Siliconix's standard MOSPOWER flow which combines preseal visual with MIL-STD environmental procedures to assure the highest quality commercial grade products available.

- * For price, delivery and minimum quantity information on these optional process flows contact the local Siliconix Sales Representative.

MOSPOWER

Military/Hi-Rel Process Flow(4) (6) (7)



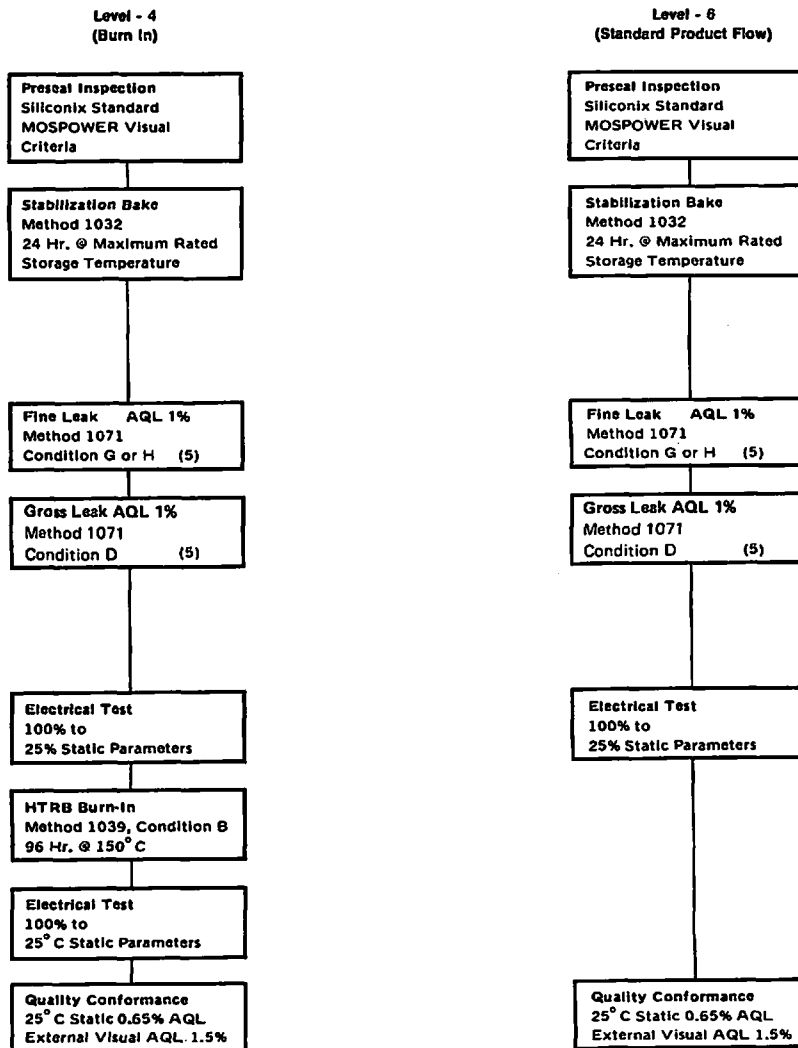
NOTES:

- (1) Level - 1: U.S. Build, U.S. Test.
- (2) Level - 2: Overseas Build, U.S. Test (Screening & OC).
- (3) No Read & Record, No Deltas.

- (4) Group B and C testing is additional.
- (5) Hermetic Only.
- (6) Levels 1 thru 6: Latest revision of MIL-STD-750 is applicable.
- (7) Level 7: Siliconix Flow for Hermetic Packages (optional).

MOSPOWER

Commercial/Industrial Process Flow(6)



NOTES: (1) Level - 1: U.S. Build, U.S. Test.
 (2) Level - 2: Overseas Build, U.S. Test (Screening & QC).
 (3) No Read & Record, No Deltas.
 (4) Group B and C testing is additional.

(5) Hermetic Only.
 (6) Physical Dimensions Excluded. The latest revision of MIL-STD-883 is applicable.
 (7) Levels 1 thru 6: Latest revision of MIL-STD-750 is applicable.
 (8) Level 7: Latest revision of MIL-STD-883 is applicable.

ADDITIONAL MOSPOWER

Generic-Quality Conformance Testing

For Levels 1, 2 and 3

Group B (1) (2) (4)

SUBGROUP 1 LTPD = 15
Solderability
Method 2026
Resistance to Solvents
Method 1022

SUBGROUP 2 LTPD = 10
Temp. Cycle Method 1051
Fine Leak Cond G
Gross Leak Cond C
Method 1071
Electrical Test
25°C End Points
Read and Record

SUBGROUP 3 LTPD = 5
Steady State OP Life
340 Hrs. Bias Cond
Method 1027
Electrical Test
25°C End Points
Read and Record

SUBGROUP 4 LTPD = 10
Decap Internal Visual
Method 2075
Bond Strength
Method 2037

SUBGROUP 5 LTPD = 15
High Temp Life
Method 4081

SUBGROUP 6 LTPD = 7
High Temp Life
340 Hrs. Method 1032
Electrical Test
25°C End Points
Read and Record

Group C (1) (2) (3) (4)

SUBGROUP 1 LTPD = 15
Physical Dimensions
Method 2066

SUBGROUP 2 LTPD = 10
Thermal Shock 25°C
Method 1056 Cond A or B
Terminal Strength
Method 2036
Fine Leak Cond G
Gross Leak Cond C
Method 1071
Moisture Resistance
Method 1021
External Visual
Method 2071
Electrical Test
25°C End Points
Read and Record

SUBGROUP 3 LTPD = 10
Shock Method 2016
Vibration Frequency
Method 2056
Constant Acceleration
Method 2006
Electrical Test
25°C End Points
Read and Record

SUBGROUP 4 LTPD = 15
Salt Atmosphere
Method 1041

SUBGROUP 5 LTPD = 15
Barometric Pressure (5)
Method 1001

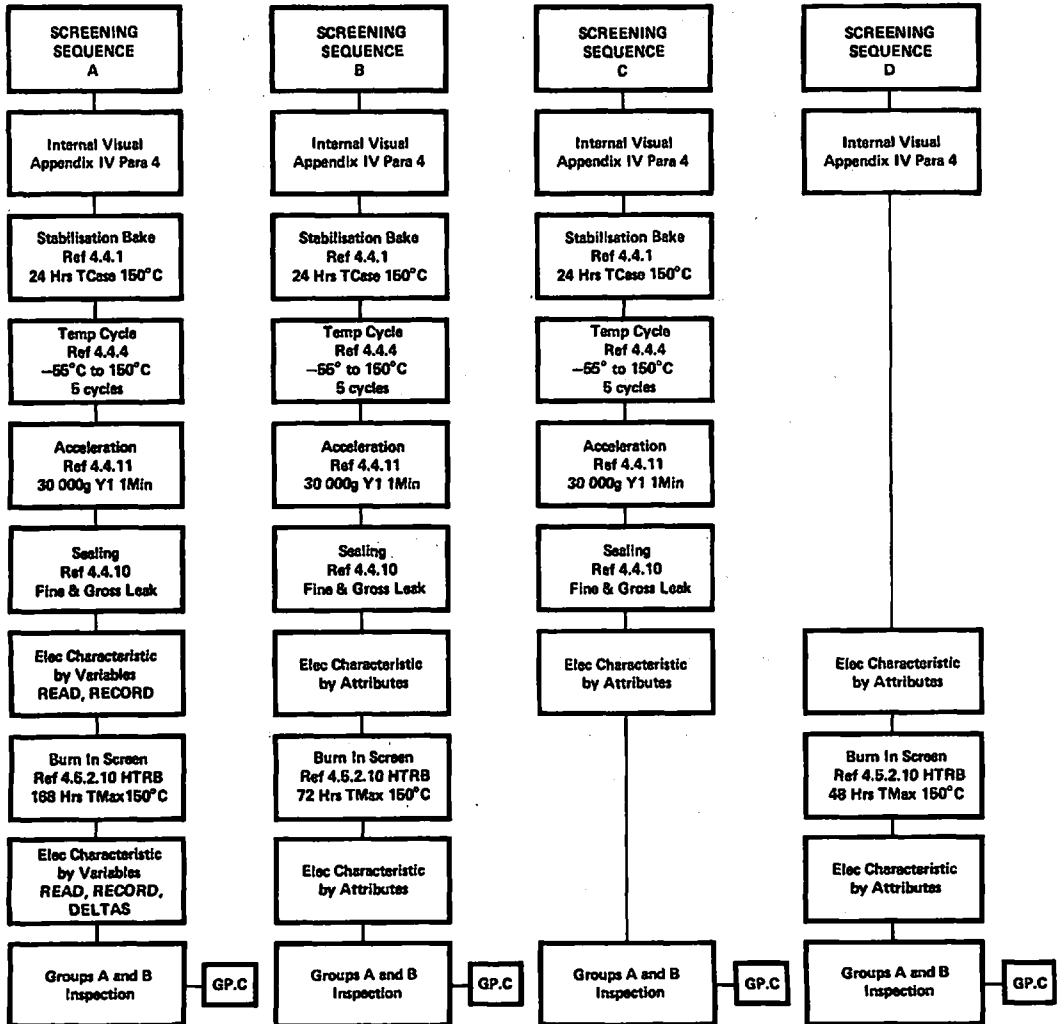
SUBGROUP 6 LTPD = 10
Steady State OP Life
Method 1026 1000 Hrs.
Max Rating Temp
Electrical Test
25°C End Points
Read and Record

NOTES:

- (1) Latest Revision of 19500 is Applicable
- (2) U.S. Test
- (3) Periodic Testing
- (4) Group B and C Testing Done at Additional Cost
- (5) For Devices > 200V

BS CECC 50 000 SERIES PROCESS OPTION FLOW CHART

ALL REFERENCES TO BS CECC 50 000



NOTES:

1. UK Build/Test
2. Delta values dependent upon device type.
3. All tests are per BS/CECC 50 000 Latest Revision.
4. For complete screening/inspection details refer to detail specification. Further information and detail specification available from your nearest field sales office.

ADDITIONAL PRODUCT OPTION FOR EUROPEAN CUSTOMERS

CECC 50000

CECC 50000 is a European system of continuous product assessment intended to produce electronic components of assessed quality to specifications and procedures which conform to internationally recognized standards. Components produced under the system are accepted by all participating countries without further testing being necessary.

At this time, member countries of the CECC are Belgium, Denmark, Germany, France, Ireland, Italy, the Netherlands, Norway, Sweden, Switzerland and the United Kingdom.

Under this assessment scheme, devices are manufactured on an approved line to nationally approved specifications written in accordance with CECC rules. The manufacturer must comply with defined standards relating to organization, facilities and quality control procedures.

The CECC scheme is administered by a committee of European representatives but individual countries have full capability for originating CECC 50000 specifications which are acceptable throughout the member countries. Specifications originating in the U.K. are prefixed with the letters BS.

Specific device types are individually qualified against a controlled detail specification which has been approved by the British Standards Institute acting as the national supervising agency on behalf of CECC.

The JEDEC registered 2N6659/60/61 series of device types are now qualified and available to the following detail specification.

<u>Type Number</u>	<u>Specification Number</u>
2N6659/60/61	BS CECC 50012-016

Screening options, including high temperature reverse bias burn-in are available. For details of screening options see flow chart.

Product is released with a BS CECC certificate of conformity and will have been submitted to:

1. Group A. Sample inspection (lot by lot)
Quality assessment tests, assuring product conforms to electrical spec.
2. Group B. Sample inspection (lot by lot)
Reliability tests, including package related tests and 168 hours electrical endurance, to identify potential early failures.
3. Group C. Sample inspection (periodic - 3 monthly)
Long term reliability tests including 1000 hours of high temperature storage and electrical endurance.

Data from the inspection tests is available to the customer in the form of CTR's (Certificate Test Records).

Manufacturing of BS CECC product is carried out at the Siliconix UK facility located in Morriston, Swansea SA6 6NE, South Wales.

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Publications Index

KEY

Catalogs

IC = Integrated
Circuit Data
Book

F = FET Design Catalog

AS = Analog Switches and
Their Applications

MAH = MOSPOWER Applications
Handbook

Catalog (See Key)	Document Number	Title Application Notes
	AN70-1	FET Cascode Circuits Reduce Feedback Capacitance
F	AN70-2	FETs for Video Amplifiers
	AN71-1	A High Resolution CMRR Test Method
F	AN72-1	FETs in Balanced Mixers
IC, AS	AN72-2	FETs as Analog Switches
F	AN73-1	FETs as Voltage-Controlled Resistors
IC, AS	AN73-2	IC Multiplexer Increases Analog Switching Speeds
IC, AS	AN73-3	Switching High-Frequency Signals with FET Integrated Circuits
	AN73-4	Junction FETs in Active Double-Balanced Mixers
IC, AS	AN73-5	Driver Circuits for the JFET Analog Switch
IC	AN73-6	Function/Application of the L144 Programmable Micro-Power Triple Op Amp
AS, F	AN73-7	An Introduction to FETs
IC	AN74-1	Function/Application of the LD110/LD111A 3½ Digit A/D Converter Set
IC, AS	AN74-2	Analog Switches in Sample and Hold Circuits
	AN74-3	Designing Junction FET Input Op Amps
F	AN74-4	Audio-Frequency Noise Characteristics of Junction FETs
IC, AS	AN75-1	CMOS Analog Switches—A Powerful Design Tool
	AN76-1	Measuring High Frequency S-Parameters on the Dual Gate MOSFET
	AN76-3	VMOS—A Breakthrough in Power MOSFET Technology
IC, AS	AN76-6	DG300A Series Analog Switch Applications
IC	AN76-7	Function/Application of the L161 Micropower Comparator
IC	AN77-1	Function/Application of the LD120/LD121A 4½ Digit A/D Converter Set in Measurement Systems
	AN77-2	Don't Trade Off Analog Switch Specs. VMOS—A Solution to High Speed, High Current, Low Resistance Analog Switches
MAH	AN79-1	A 500 KHz Switching Inverter for 12 V Systems
	AN79-3	Dynamic Input Characteristics of a VMOS Power Switch
	AN79-4	Driving VMOS Power FETs
	AN79-5	Using the VN64GA High Current, High Power VMOS Power FET
MAH	AN79-6	Using VMOS Transistors to Interface from IC Logic to High Power Loads
	AN79-7	Applications of the VN10KM VMOS Power FET
	AN80-1	A Key to the Advance of Switching Power Supplies
	AN80-2	Meet the VMOS FET Model
	AN80-3	Ultralinear Broadband Amplifier
	AN80-4	Enjoy VHF Power Amplifier Design
	AN80-5	An Alternative Power Amplifier Design
	AN80-6	AGC for the VMOS RF Power Amplifier

Catalog (See Key)	Document Number	Title
IC	AN80-8	Function/Application of the LD122/LD121A $\pm 4\frac{1}{2}$ Digit A/D Converter Set in Measurement Systems
IC	AN81-1	Microprocessor Interface Techniques As Applied to the Siliconix A/D Converter Family
IC	AN81-2	Introduction to Quantized Feedback
F	AN81-3	Composite Op Amp for High Performance
MAH	AN82-1	Solving the Stepper Motor Interface Problems
IC	AN83-1	The DG308A Digitally Switches Analog Signals
MAH, IC	AN83-2	Applying 240 Volt MOSPOWER Transistors and Current Limiting Diodes to Electronic Pulse Dialer Circuits
IC	AN83-3	A Microprocessor Compatible Analog Switch Makes Interfacing Easy
IC	AN83-4	Improved System Performance Using Microprocessor Compatible Multiplexers
MAH, IC	AN83-5	Boost OP-AMP Output Power with Complimentary Power MOSFETS
IC	AN83-6	A System Solution to HP-IL Equipment Interface
IC	AN83-7	A High-Quality Audio Crosspoint Switch
MAH	AN83-8	Frequency Response Analysis of the MOSFET Source-follower
	AN83-9	A New Current Limiter Extends Protection to 240 Volts
MAH	AN83-10	Safe Operating Area and Thermal Design for MOSPOWER Transistors
MAH, IC	AN83-11	The D469: An Optimized CMOS Quad Driver for MOSPOWER FET Switches
IC	AN83-12	Utility Gate Array Logic Simulation with a Personal Computer
IC	AN83-13	Si520 Data Acquisition System Interfaces for I/O or Memory Mapped Operation
IC	AN83-14	A Simple Approach to Si7135/8085 Interface
IC	AN83-15	A High Performance Video Switch Using the SD5002
IC	AN83-16	Si8020/21 Digital-to-Analog Converter Interface for Microprocessor Systems
	AN84-1	Applications for Si1000 Series JFET Amplifier
IC	AN84-2	Theory and Applications of the Si7660 and Si7661 Voltage Converters
Design Aids		
IC	DA74-1	Design Aid of the LD110/111A $3\frac{1}{2}$ Digit DVM
	DA76-1	VMOS Power FET Audio Amplifier
IC	DA77-2	Design Aid of the LD120/LD121A $4\frac{1}{2}$ Digit DVM
	DA78-4	Build a Smoke Detector With the SM110 IC
MAH	DA80-1	A Low Cost Regulator for Microprocessor Applications
	DA81-2	Logic Interfacing Made Easy with the DG308
Design Ideas		
F	DI71-1	The FET Constant Current Source
	DI71-4	Wideband Mixer-Preamplifier Using FETs
	DI71-5	A FET Frequency Doubler
	DI71-6	Using FETs in Selective VHF Amplifiers
	DI71-8	Using JFETs in Ultra-Wideband UHF Amplifiers
F	DI71-9	Wideband UHF Amplifier with High Performance FETs
F	DI73-2	High Performance FETs in Low-Noise VHF Oscillators
	DI80-1	A 5 Watt, Parallel-Mode Crystal Oscillator
	DI83-1	Differential JFET Amplifier
	DI83-2	Build a Precision Constant Current Source
Technical Articles		
	TA70-1	High Frequency Junction FET Characterization and Application

Catalog (See Key)	Document Number	Title
F	TA70-2	FET Biasing
IC, AS	TA73-1	Multiplexer Adds Efficiency to 32-Channel Telephone System
IC, AS	TA73-2	Designing with Monolithic FET Switches
	TA76-1	VMOS Power FETs in Your Next Broadband Driver
	TA76-2	A New Technology: Application of VMOS Power FETs for High Frequency Communications
	TA78-2	Designing a VMOS 250 Watt Off-Line Inverter
MAH	TA83-1	Using Power MOSFETs as High-Efficiency Synchronous and Bridge Rectifiers in Switch-Mode Power Supplies
	TA83-2	Controlling Oscillation in Parallel Power MOSFETS
	TA83-3	Correlating the Charge-Transfer Characteristics of Power MOSFETS with Switching Speed
MAH	TA84-1	Understand MOSPOWER Transistor Characteristics Minimizes Incoming Testing Requirements
MAH	TA84-2	MOSFETs Move in on Low Voltage Rectification
MAH	TA84-3	Power MOSFETs and Radiation Environments
MAH	TA84-4	dV _{ds} /dt Turn-on in MOSFETs
MAH	TA84-5	Parallel Operation of Power MOSFETs

Catalogs

Integrated Circuit Data Book

Analog Switches and Their Applications

FET Design Catalog

MOSPOWER Applications Handbook

MOSPOWER Data Book

OEM Pricing with Cross Reference

Siliconix Short Form Selector Guide

Reprints & Reports

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Bellevue (98005)
Wyle Distribution Group
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(206) 453-8300
Twx: 910-443-2526

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Hamilton/Avnet, #57
2975 Moorland Road
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Mississauga (L4V 1M5)

Hamilton/Avnet, #59
6845 Redwood Drive
(416) 677-7432
Twx: 610-492-8887

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Hamilton/Avnet, #60
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Future Elec.
Baxter Centre
1050 Baxter Rd.
(613) 820-8313

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Calgary (T2E 6Z2)
Hamilton/Avnet
2816 21st Street N.E.
(403) 230-3586

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Pointe Claire (H9R 4C7)
Future Elec.
237 Humus Blvd.
(514) 694-7710
Twx: 610-421-3251

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B-1810 Wemmel
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Tlx: 24610

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DK-2600 Glostrup
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Tlx: 33257

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SF 02631 Espoo 63
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Tlx: 124426 HAVUL SF

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92164 Anthony Cedex
Tel: (1) 666-21-12
Tlx: 250067

Alrodis
40 Rue Villon
69008 Lyon
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Tlx: 380636

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Tlx: 870952F

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Avenue Gustave Eiffel
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33605 Pessac Cedex
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Tlx: 550696F

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31400 Toulouse
Tel: (61) 20-82-38
Tlx: 530957

Composants S.A.
183 Route de Paris
86000 Poitiers
Tel: (49) 88-60-50
Tlx: 591525

Composants S.A.
57 Rue Manoir de Servigne
ZI, Route de Lorient
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35013 Rennes Cedex
Tel: (99) 54-01-53
Tlx: 740311

I.T.T. Multicomposant
38 Avenue Henri Barbusse
92220 Bagneux
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Tlx: 270763

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7 Rue de la Couture
ZI, de la Platerie
59700 Marqu'en-Baroeuil
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Tlx: 160-143F

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80 Rue d'Arcueil
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Tlx: 204-674F

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Julius-Hoelder Str. 42
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Tel: (0711) 720010
Tlx: 7255638

EBV Elektronik GmbH
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D-8025 Unterhaching
Tel: 089-61105-1
Tlx: 524535

EBV Elektronik GmbH
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7000 Stuttgart 1
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4000 Ousseldorf
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EBV Elektronik GmbH
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6000 Frankfurt M.90
Tel: 069/785037
Tlx: 413590

Ing. Büro Rainer König
Königsbergerstrasse 16A
1000 Berlin 45
Tel: 030-772-8009
Tlx: 184-707

Ing. Büro K.H. Dreyer
Albert Schweitzer-Ring 36
2000 Hamburg 70
Tel: (040) 669027
Tlx: 2164484

Ing. Büro K.H. Dreyer
Flensburger Strasse 3
2380 Schleswig
Tel: (04621) 24055
Tlx: 02-21334

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Münchner Strasse 6
8031 Seefeld
Tel: (08152) 7090
Tlx: 05-26459

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Nikaia, Piraeus GR-184 54
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Elektrotechniek BV
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Tlx: 31528

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Bucks HP19 3RG
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Tlx: 83518

Farnell Electronic
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Tel: 0532-636311
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Semiconductor Specialists (UK)
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Carroll House
159 High Street
West Drayton
Middlesex UB7 7X8
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Tlx: 21958

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Coselo Comercio e Servicos
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01310 Sao Paulo
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Tlx: 910-338-0227

NOTES

1. The first part of the notes is a list of the names of the people who were present at the meeting.

2. The second part of the notes is a list of the topics that were discussed during the meeting.

3. The third part of the notes is a list of the actions that were taken during the meeting.

4. The fourth part of the notes is a list of the conclusions that were reached during the meeting.

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